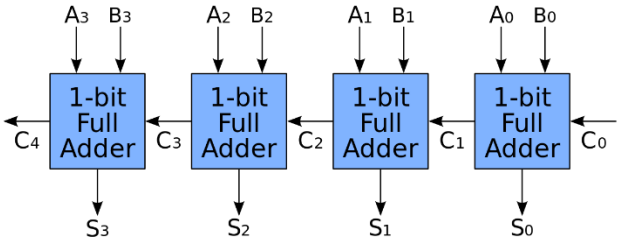
In this Project you will perform layout design with Magic and simulations with Spice. Write an comprehensive report for your homework. Submit the magic and spice files with the report.

Carry Ripple Adder

Carry Ripple Adder is the simplest adder that is perfect for small number additions as it consumes a very small area and it is also power efficient.

However, it results in higher delays because of its carry propagation nature. Its critical path starts with A0 and propagates to S3 passing through all the carries.

In this assignment you will design this 4-bit adder using as few transistors and occupying as few area as possible. There is also a competition for smallest area. The one coming up with the smallest design will win the competition. Of course, the design must be working accurately.



Magic Layout

- First, you have to design a minimal **sum** circuit that is responsible for computing the sum result of 3 bits.
- Theni you should design the **carry** computation circuit using as few transistors as possible.
- Combining those two circuits, i.e. sum and carry circuits, you should construct the **full adder**.
- Using 4 full adders you should construct the 4-bit adder.
- Use as few transistors as possible at each stage.
- Your PMOS transistors must be sized so that low to high and high to low delays are equal. You should know that ratio from your first homework.
- You should compute the total area of your circuit.

Spice Simulations

- You will extract your magic layout as explained in the first homework.
- You will insert the necessary lines to the extracted spice deck for simulations.
- You should show the functional correctness of your design, therefore show an accurate output for 16 additions of different numbers.
- You should compute the critical path delay for your circuit.