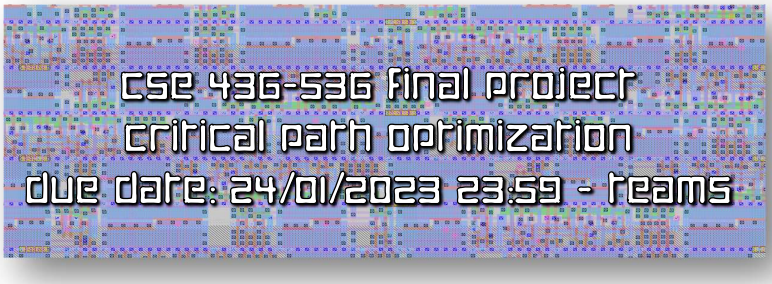

In this Project, you will try to optimize a critical path using logical effort formalism.

Gate Characterization

- ✓ First design a min-sized inverter in Magic Layout Tool. This will be your reference inverter.
- ✓ Size the transistors so that H2L and L2H delays are equal.
- ✓ Extract the inverter to Spice.
- ✓ Design the characterization circuit in Fig. 1 for that inverter.
- ✓ Change h (fanout) from 1 to 4 and plot delay vs fanout.
- ✓ The slope (g.τ) gives you τ as g of inverter is 1 by definition.
- ✓ The point where the fitted line crosses the y-axis is p.τ
- ✓ After finding p and τ of the inverter, design a 2-input NAND gate in Magic.
- ✓ Repeat the same procedures you did for the inverter to find p and g of NAND.
- ✓ Repeat the very same procedure with NAND for 2-input NOR to find p and g of NOR.

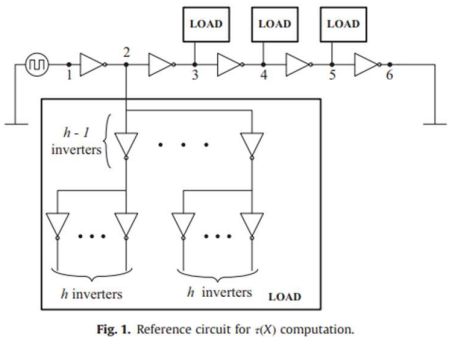

Fig. 1. Reference circuit for $\tau(X)$ computation.

Figure 1 τ and p Characterization Circuit for the inverter

Critical Path Construction

The critical path that you will design in Magic is shown next.

- ✓ First of all, compute Path Effort F using the g values you compute in previous part.
- ✓ Using F compute the optimum stage effort f.
- ✓ According to that size the logic cells for that optimum delay.
- ✓ Compute that optimum delay using logical effort.
- ✓ Design the optimum path in Magic.
- ✓ Extract that Magic Layout to Spice.
- ✓ Compute the actual delay of the path by simulation, while inputs are as shown in the figure.
- ✓ What is the difference between Logical Effort Delay and the actual delay. Justify your result.
- ✓ **BONUS** (25pts): Construct the same path in Magic with min sized NAND, NOR and inverters. Again, compare the logical effort result with the Spice result. How does the delay change?