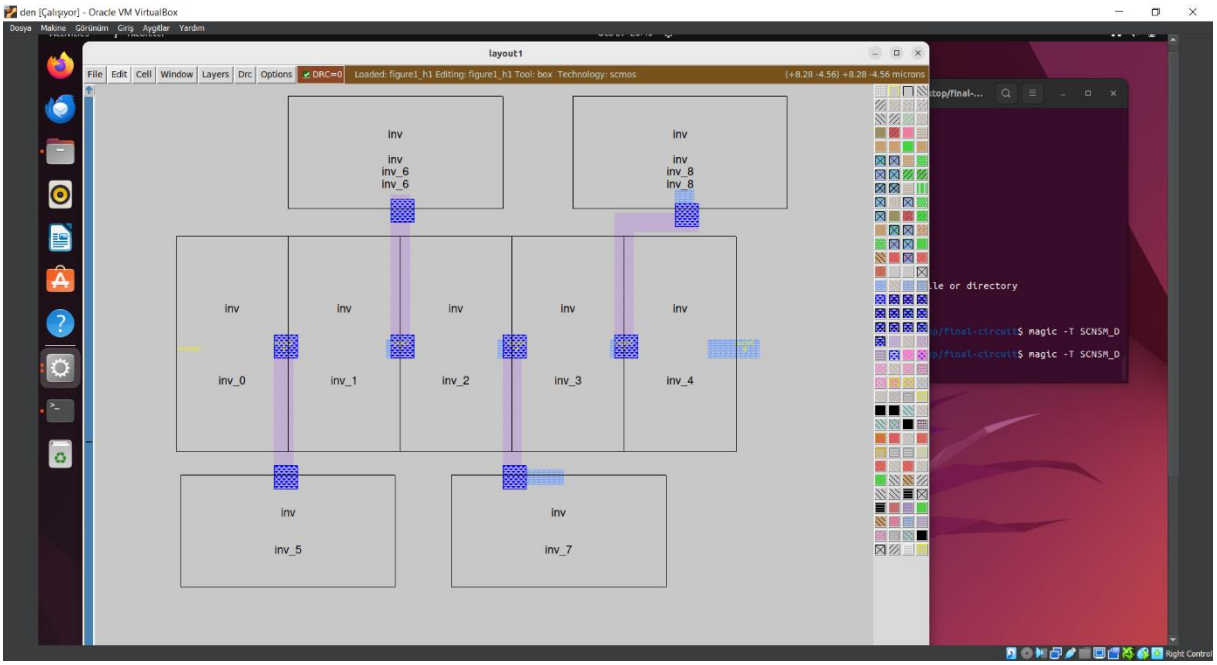
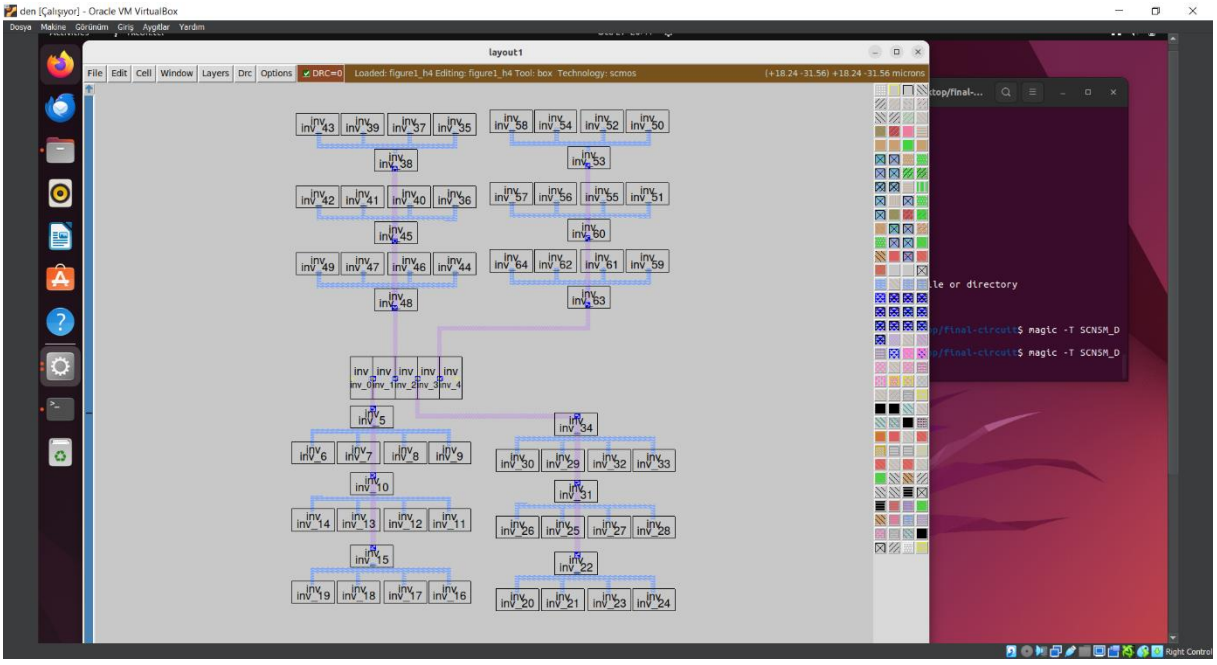
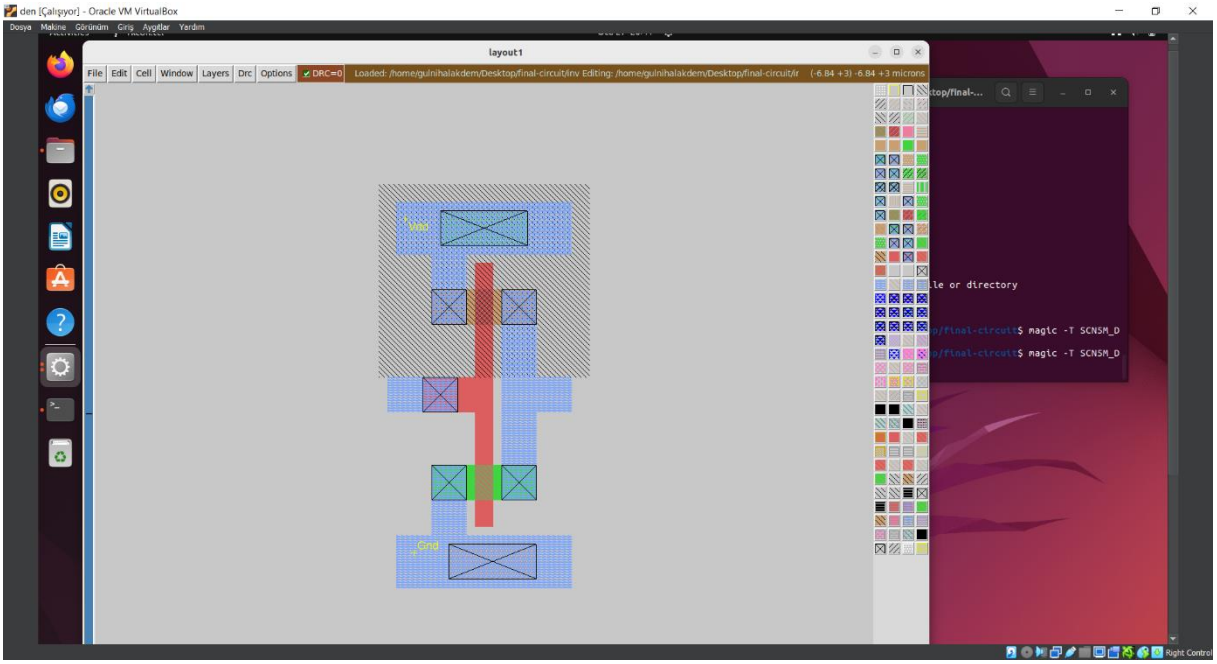
The layout of figure1 when h=1



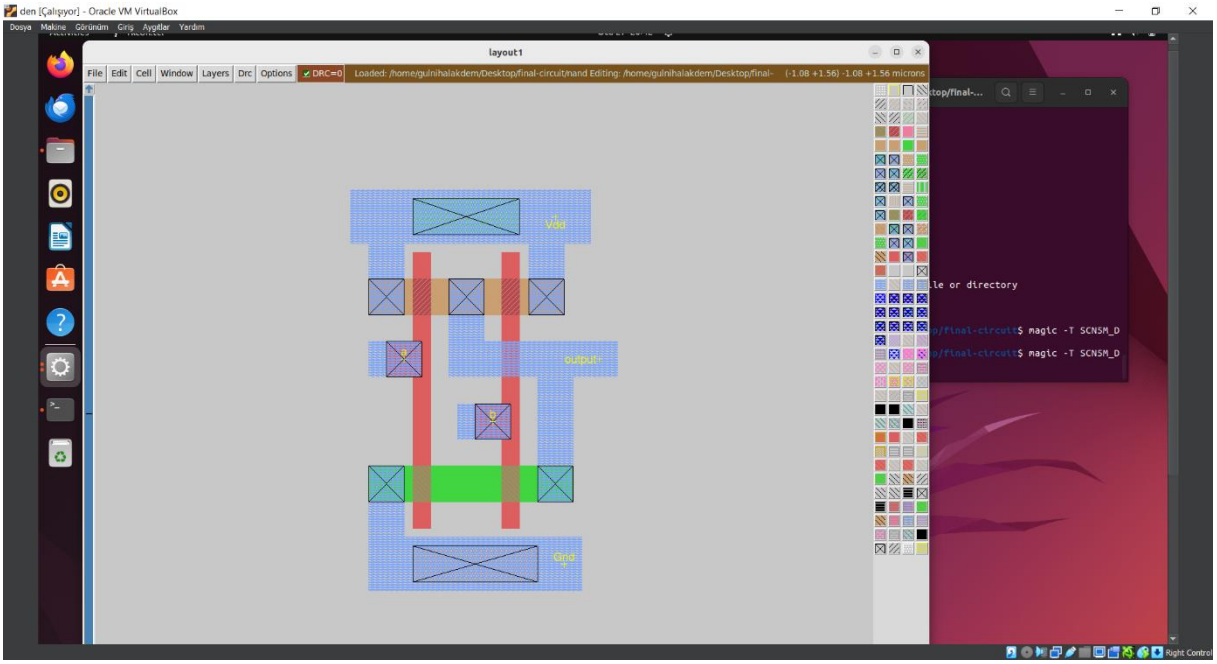
The layout of figure1 when h=4



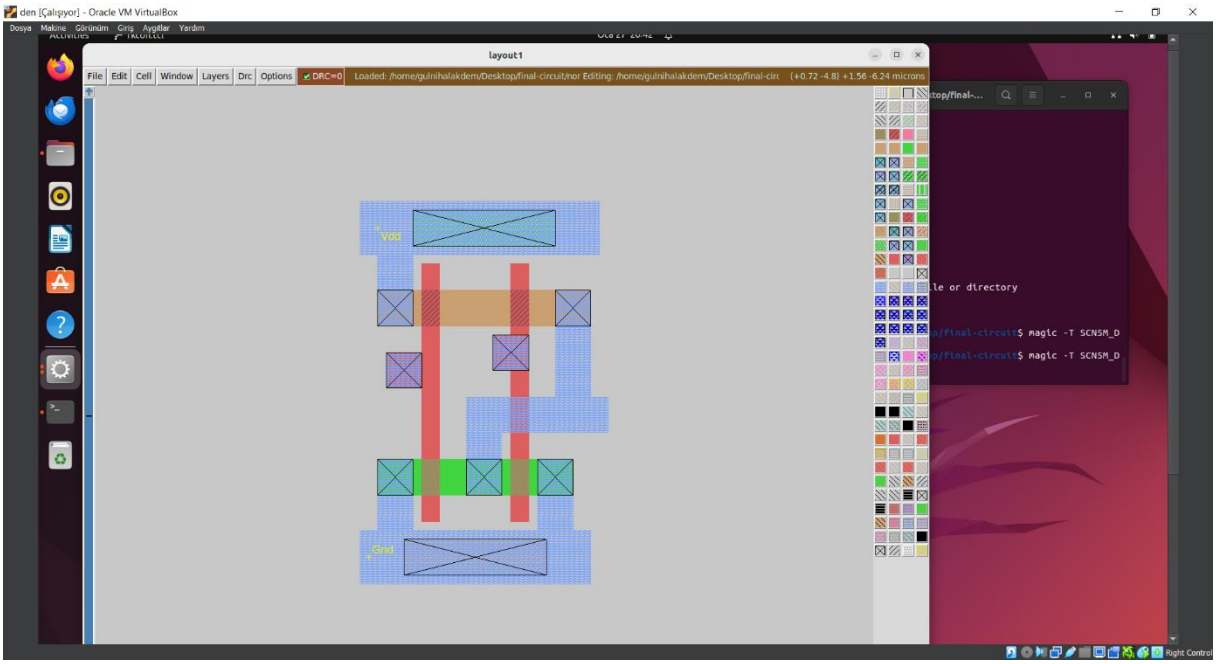
The layout of Inverter



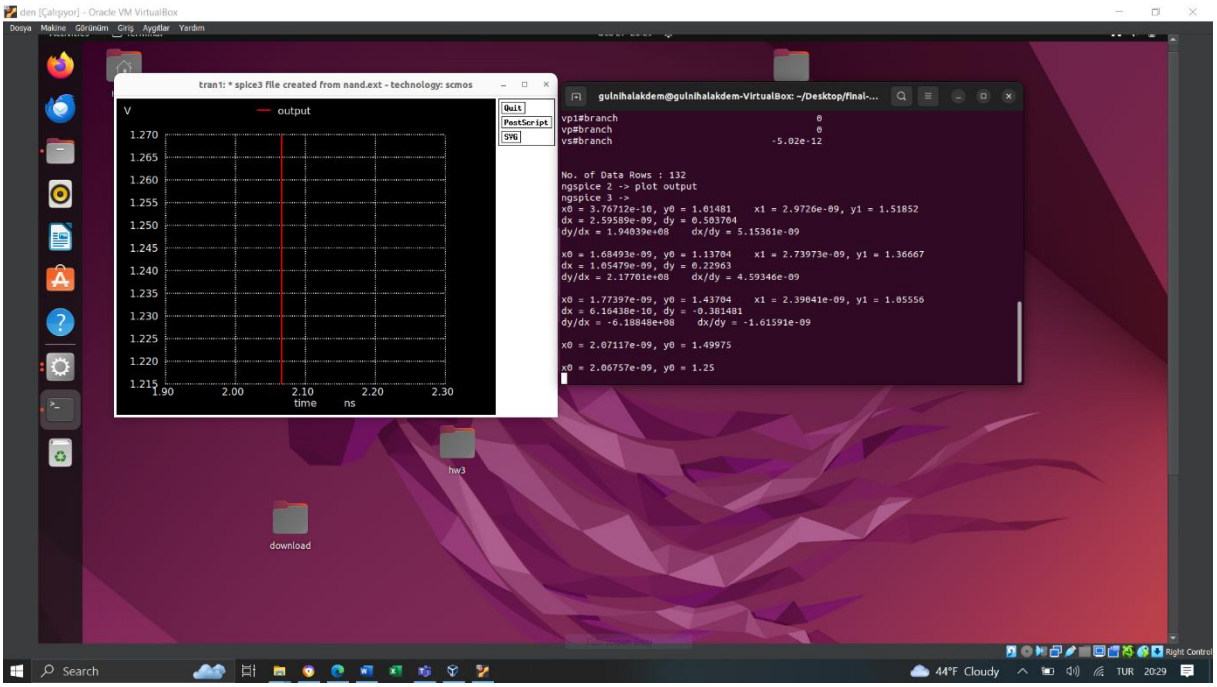
The layout of NAND



The layout of NOR

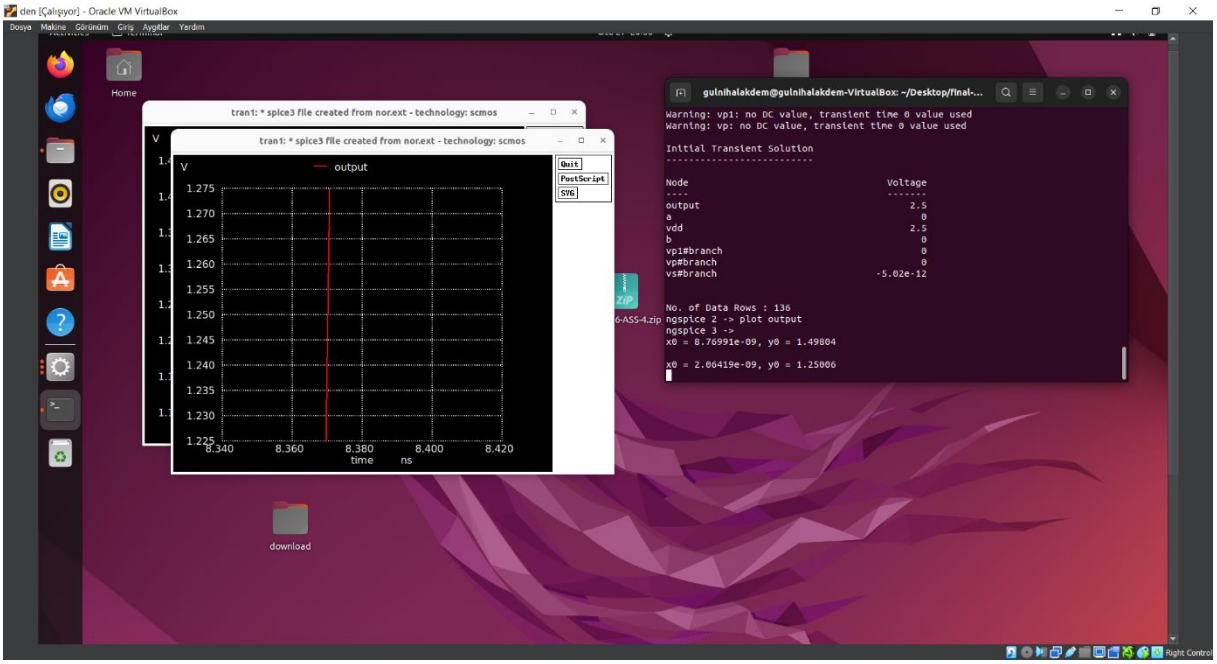


NAND H2L delay is 2.06757e-9 when y0 = 1.25(Vdd/2)

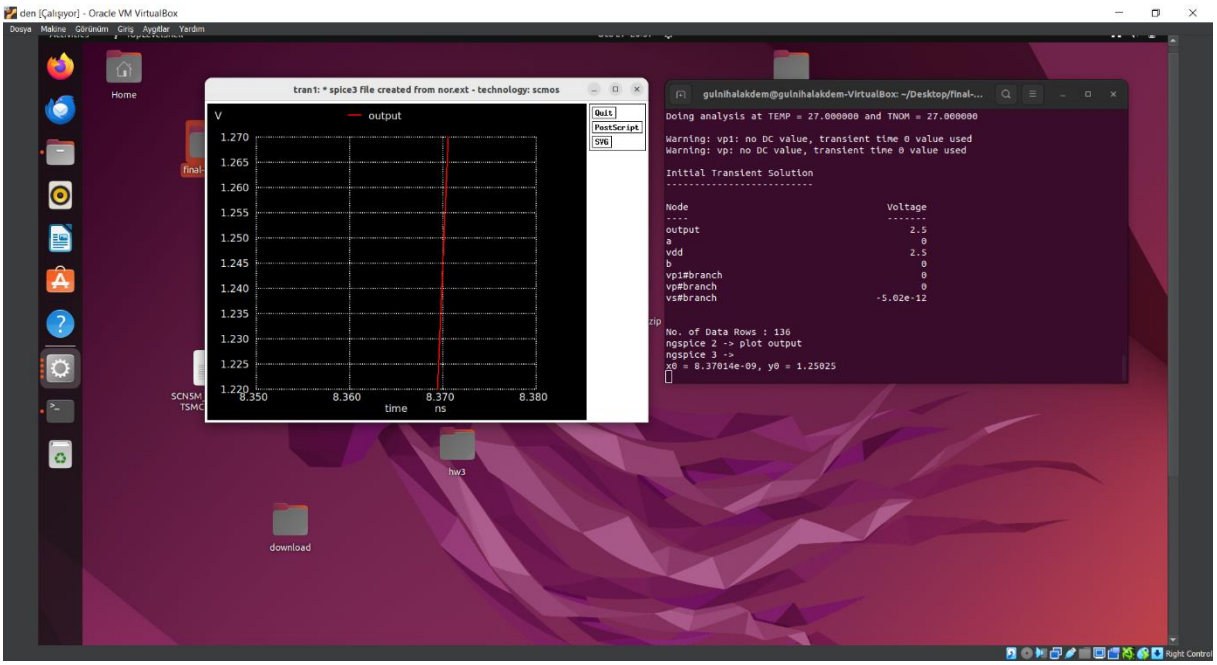


NAND L2H delay is 8.37315e-09 – 6 = 2.37315e-09 .(when y0 = 1.25(Vdd/2))

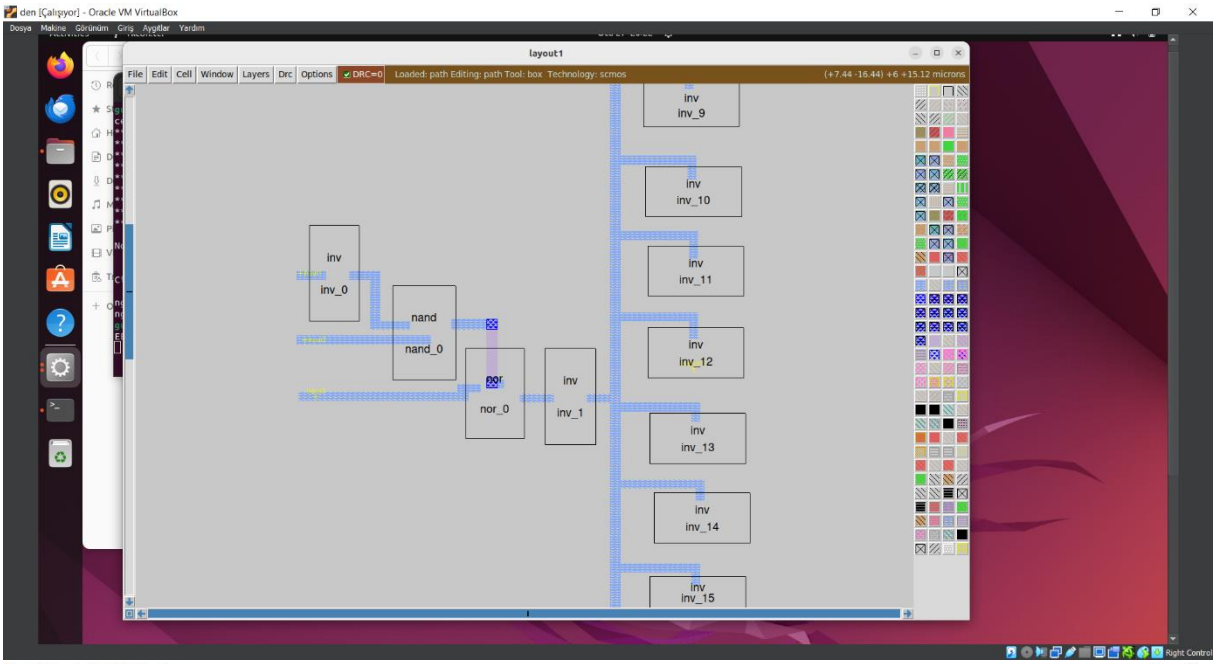
NOR H2L delay is 2.06419e-09 when y0 = 1.25006

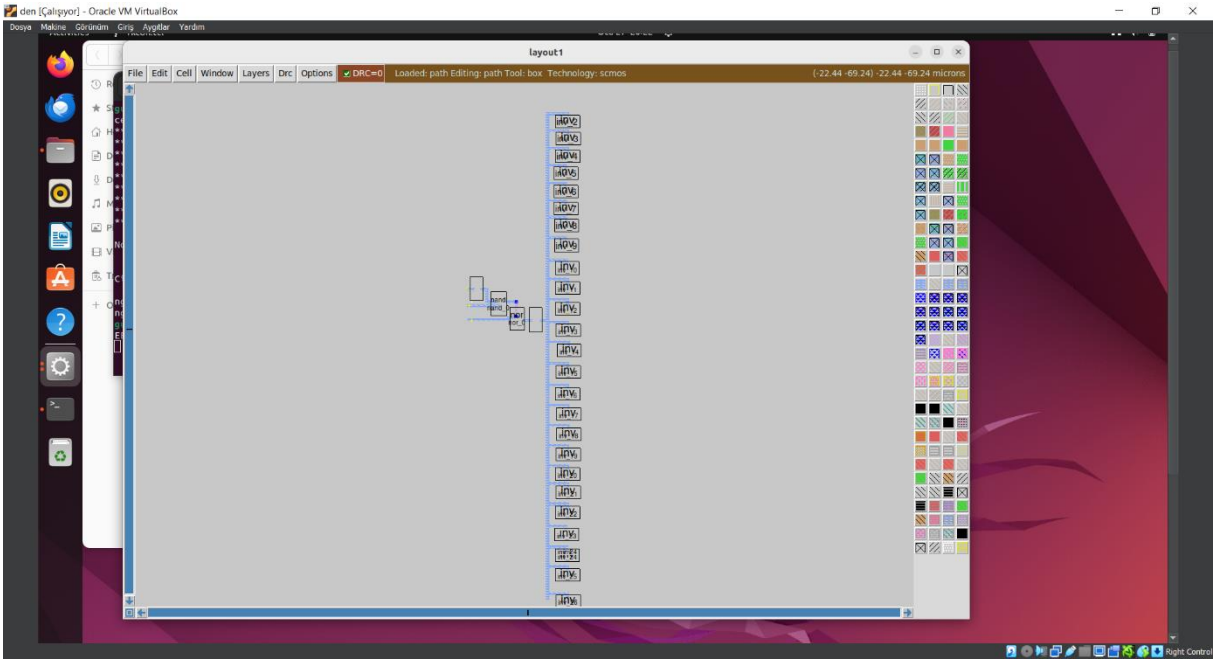


NOR L2H delay is 8.37014e-09-6 = 2.37014e-09 when y0 ? 1.25025



The layout of path





Path

$G_2(1)\left(\frac{4}{5}\right)\left(\frac{5}{5}\right)(1.)\ (1) = 20/9$

$B = 1.\ 1.\ 1.1\ 25 = 25$

$H = c_{out}/c_{in} = h$

$F = GBH = \frac{20}{9}\ 25.h = \frac{500}{9}h$

$P = 1+2+2+1+1 = 7$

$D = \frac{500}{9}h + 7$

The stick diagram for NAND and NOR respectively