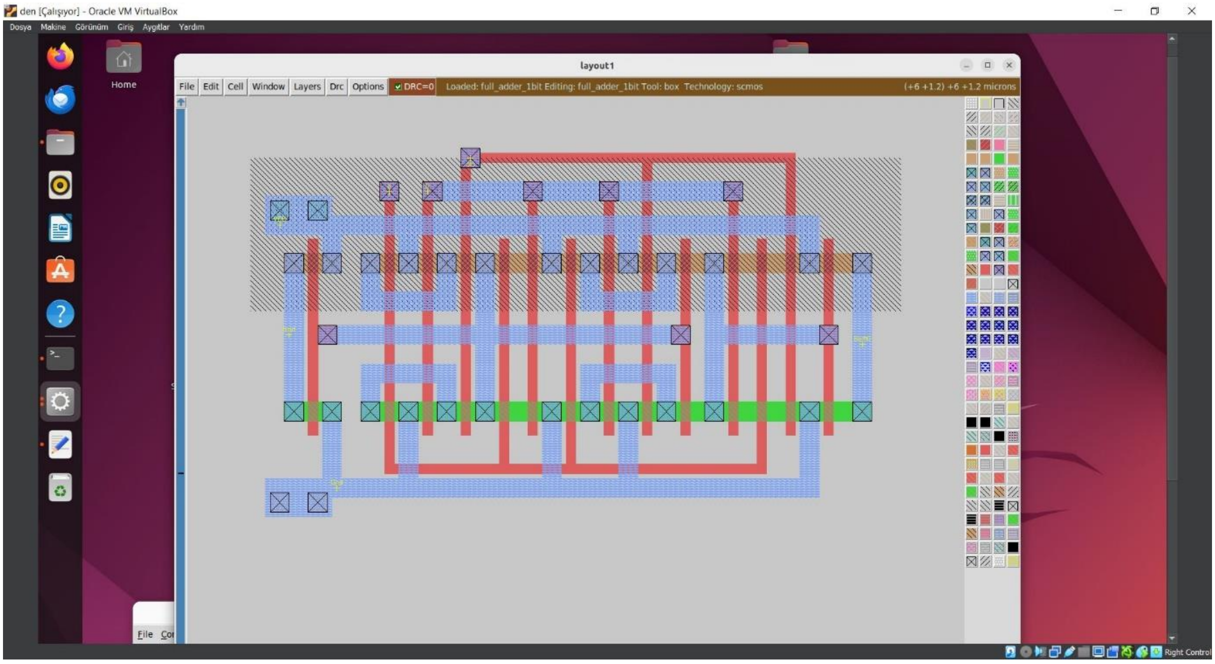
First of all, The 1 bit full adder is designed.


den [Çalışıyor] - Oracle VM VirtualBox
Dosya Makine Görünüm Giriş Aygıtlar Yardım
Home
layout1
File Edit Cell Window Layers Drc Options
DRC=0
Right Control

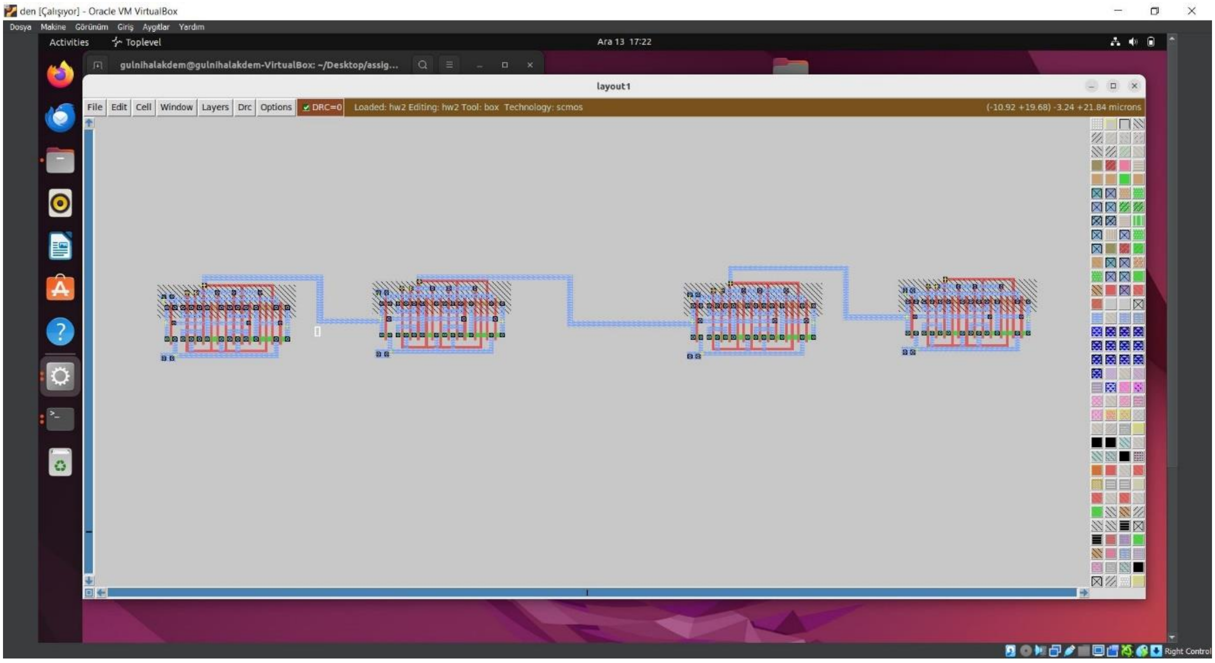
Loaded: full_adder_1bit Editing: full_adder_1bit Tool: box Technology: scmos (+6 +1.2) +6 +1.2 microns

The full adder is checked whether Works correctly or not.

In the ss folder, you can see the values correctness.

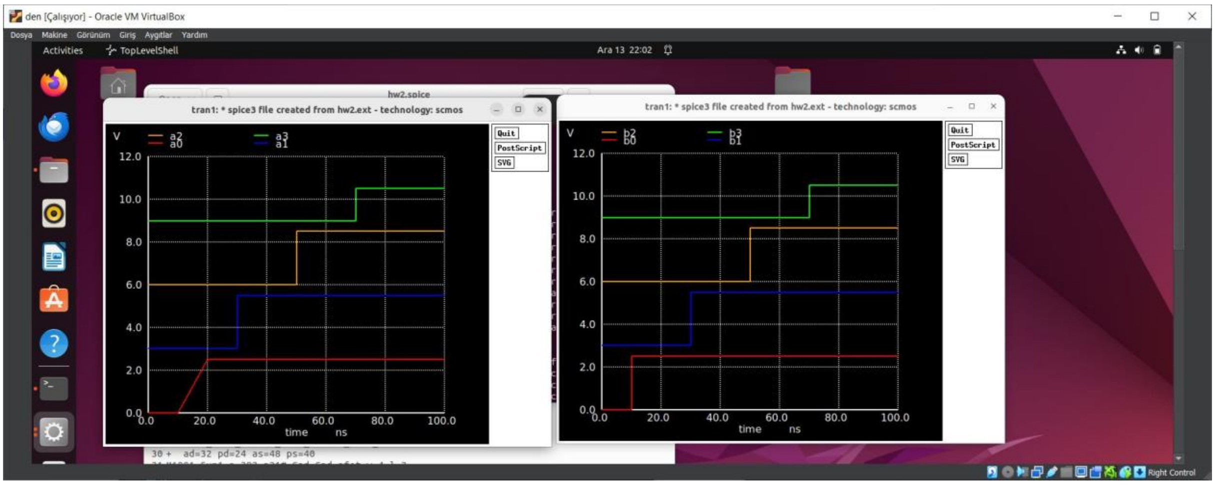
Then, 4 full adders(1 bit) are merged to create 4 bit Carry Riple Adder.

4 bit Carry Riple Adder

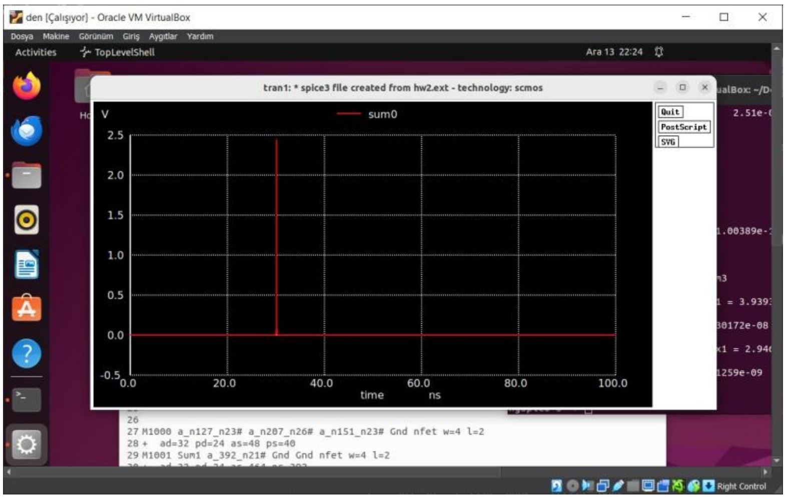

den [Çalışıyor] - Oracle VM VirtualBox
Dosya Makine Görünüm Giriş Aygıtlar Yardım
Activities
Toplevel
Ara 13 17:22
gulnihalakdem@gulnihalakdem-VirtualBox: ~/Desktop/assig...
layout1
File Edit Cell Window Layers Drc Options
DRC=0
Right Control

Loaded: hw2 Editing: hw2 Tool: box Technology: scmos (-10.92 +19.68) -3.24 +21.84 microns

This image show a and b inputs.


den [Çalışıyor] - Oracle VM VirtualBox
Dosya Makine Görünüm Giriş Aygıtlar Yardım
Activities
TopLevelShell
Ara 13 22:02
hw2.spice
tran1: * spice3 file created from hw2.ext - technology: scmos
V
a2
a0
a3
a1
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time ns
Quit
PostScript
SVG
tran1: * spice3 file created from hw2.ext - technology: scmos
V
b2
b0
b3
b1
Right Control

```
+ ad=32 pd=24 as=48 ps=40
```

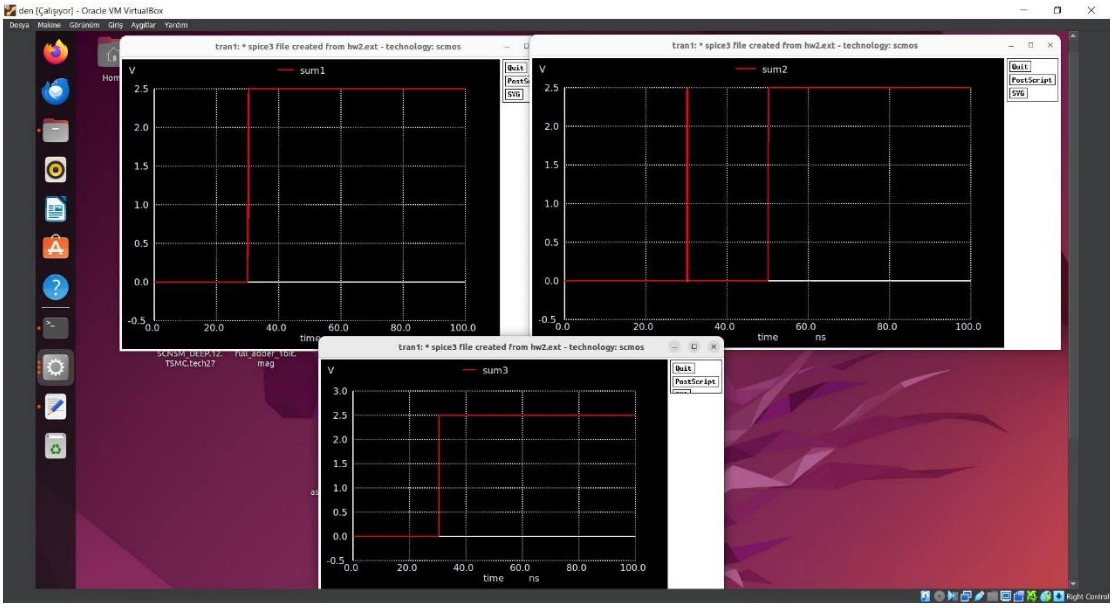

den [Çalışıyor] - Oracle VM VirtualBox
Dosya Makine Görünüm Giriş Aygıtlar Yardım
Activities
TopLevelShell
Ara 13 22:24
tran1: * spice3 file created from hw2.ext - technology: scmos
V
sum0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
20.0
40.0
60.0
80.0
100.0
time ns
Quit
PostScript
SVG
Right Control

```
2.51e-
1.00389e-
1 = 3.939
30172e-08
x1 = 2.94
1259e-09
```

```
M1000 a_n127_n23# a_n207_n26# a_n151_n23# Gnd nfet w=4 l=2
+  ad=32 pd=24 as=48 ps=40
M1001 Sum1 a_392_n21# Gnd Gnd nfet w=4 l=2
```

This shows sum0.

This Shows sum1,sum2 and sum3.


den [Çalışıyor] - Oracle VM VirtualBox
Dosya Makine Görünüm Giriş Aygıtlar Yardım
tran1: * spice3 file created from hw2.ext - technology: scmos
V
sum1
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
20.0
40.0
60.0
80.0
100.0
time ns
Quit
PostScript
SVG
sum2
sum3
3.0
SCN3M_DEEP.12.TSMC.tech27
full_adder_1bit.mag
Right Control

From 0 to 10ns => a[3:0] is 0000 and b[3:0] is 0000. The result should be 0000. The last cout is 0.

From 20 to 30ns => a[3:0] is 0001 and b[3:0] is 0001. The result should be 0010. The last cout is 0.

From 30 to 50ns => a[3:0] is 0011 and b[3:0] is 0011. The result should be 0110. The last cout is 0.

From 50 to 70ns => a[3:0] is 0111 and b[3:0] is 0111. The result should be 1110. The last cout is 0.

From 70 to 90ns => a[3:0] is 1111 and b[3:0] is 1111. The result should be 1110. The last cout is 1.

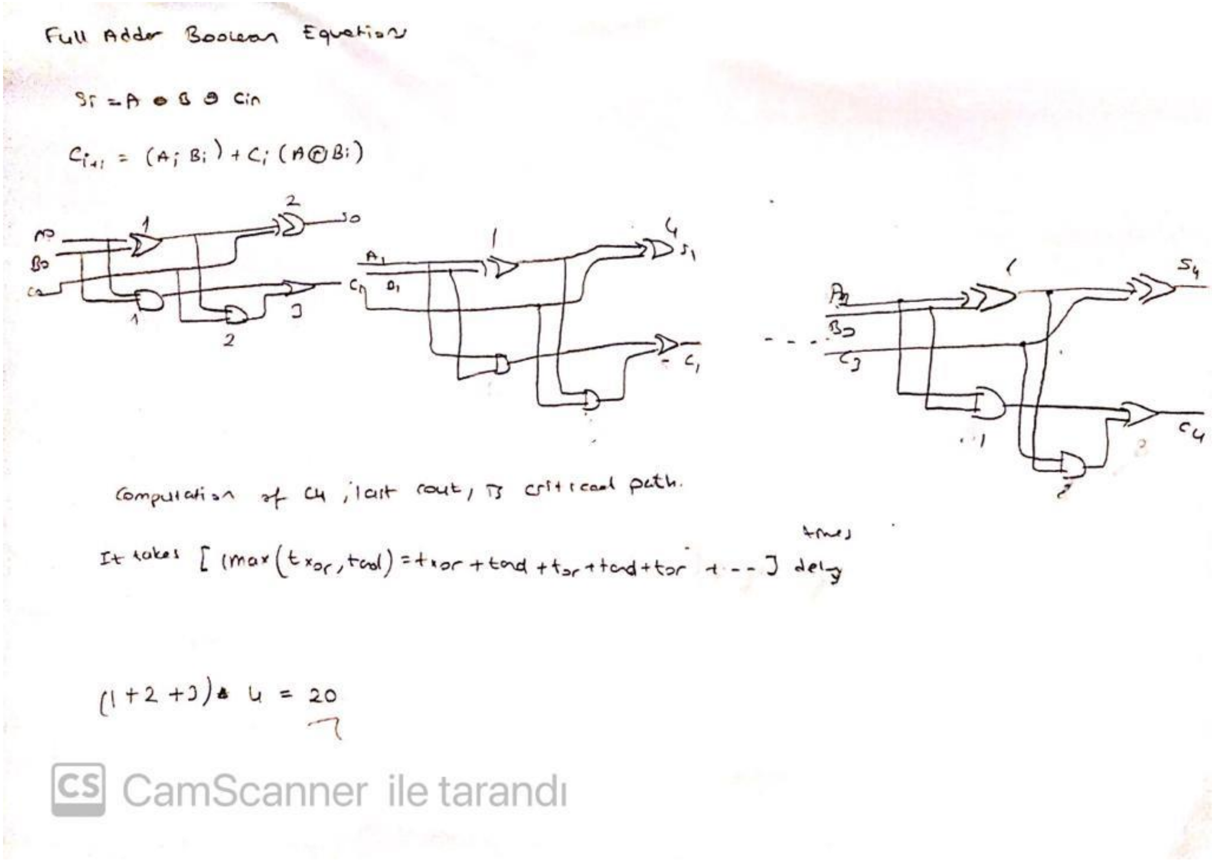
According to these information sum0 should be 0 from 0 to 90 ns. And the garph is 0 ,but suddenly goes up 1 to 0. I thought that when adding the signal goes to 1 ,then change to 0.

When range is 20ns to 30ns sum 1 is become 1.The remaing ones are same.

When range is 30ns to 50ns sum 2 is become 1. The remaing ones are same.

When range is 50ns to 70ns sum 3 is become 1. The remaing ones are same.

When range is 70ns to 90ns ,the sum values same but last cout becomes 1.



Full Adder Boolean Equation

$S_i = A \oplus B \oplus C_{in}$

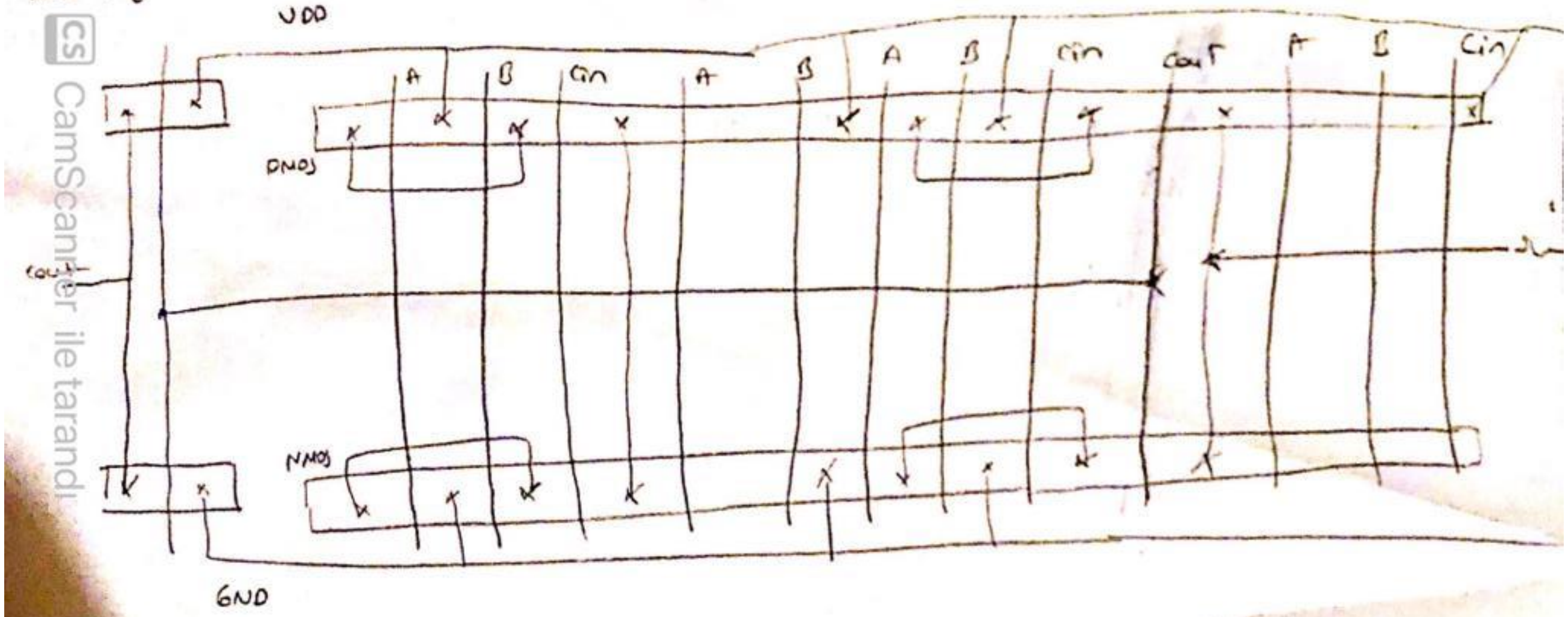
$C_{i+1} = (A_i B_i) + C_i (A \oplus B_i)$

Computation of C4 ,last cout, is critical path.

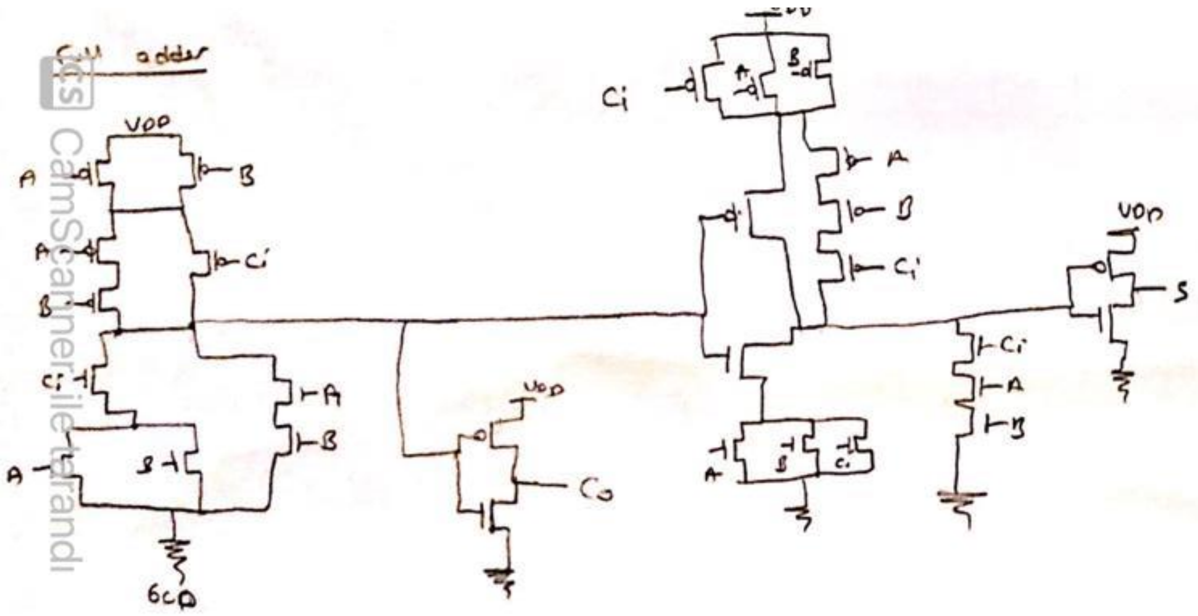
It takes [(max(t_{xor}, t_{and}) = t_{xor} + t_{and} + t_{or} + t_{and} + t_{or} + - -] delay times

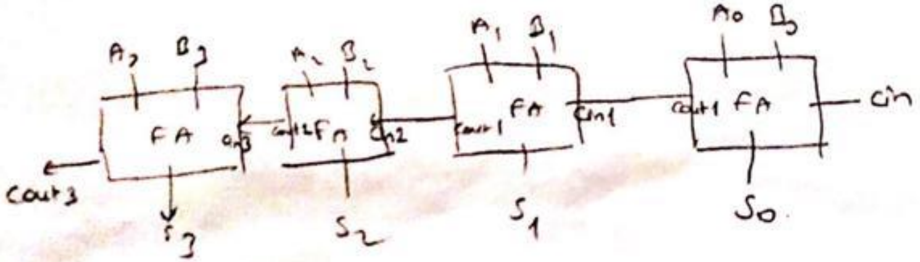
$(1+2+3) * 4 = 20$

Stick Diagram



Full adder





carry riple Adder

9*8=72 lambda width, 14*8=112 lambda height for full adder

Between two full adder ,at least 9 lmabda space should be because of metal.

So height becomes 112+9+9+9=139 lambda

The ares is 72*139= 10.008 lambda.