Final Coursework Report

Imperial College London

ELEC96021 - Instrumentation

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1 Introduction

This document is the final deliverable report of the subject *Instrumentation*. The purpose of this Coursework is to design a Vector Network Analyser (VNA).

2 Theoretical Analysis

From this point on, it is assumed that the Device Under Test (DUT) will be a two port device. Therefore, the goal of this report is to present an instrument that measures all four parameters that fully characterise the two port network.

2.1 Admittance Parameters

Firstly, a two port network can be fully characterised by using the admittance matrix of eq. 2. Y_{11} variable is called input admittance, Y_{12} is called reverse admittance gain, Y_{21} is called trans-admittance (gain) and variable Y_{22} is called output admittance.

$$\mathbf{I} = \mathbf{Y} * \mathbf{V} \tag{1}$$

or

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2}$$

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \quad Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0}$$
$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \quad Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0}$$

Therefore, the circuits that will be used, they have to be able to apply a voltage signal on the one port and ground the other. These kind of circuits can be implemented by using Op Amps in feedback mode. Before, presenting the proposed circuits, a brief analysis on feedback systems will be conducted.

2.2 Stability Analysis on Feedback Systems

Any feedback system can be represented by the block diagram shown on fig. 1[1]. The transfer function that describes the system is shown on eq. 3. This equation is called the *closed loop gain* and its symbol is A_{cl}. The A function is called the *open loop gain* and it is often represented by A_{ol}. Function β is called the feedback factor. By inspecting this equation, the stability of the system is not dependent on the closed loop gain but in the *loop gain* product $A*\beta$. If the loop gain $A*\beta \rightarrow -1$ or $A*\beta \rightarrow 1\underline{/180^\circ}$ then $A_{cl} = \frac{1}{0}$. At this case there are two possible outcomes, the system either constantly rises and settles at the highest possible value (for example power supply for electronic systems) or it oscillates[1].

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A * \beta} \tag{3}$$

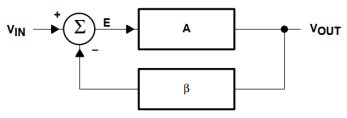


Figure 1: Feedback System Block Diagram

A method to calculate the loop gain is to ground the input, break the feedback loop, apply a test signal at the input and measure the response of the feedback factor. This method is show on fig. 2. The transfer function is provided on eq. 4 [1].

$$\frac{V_{return}}{V_{test}} = A * \beta \tag{4}$$

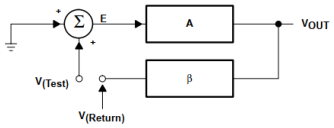


Figure 2: Calculation Method of Loop Gain

From the analysis made above, it is clear that the phase margin of loop gain has to be at least positive in order for the system to be stable. Ideally, the phase margin has to be greater than 45°, otherwise, ringing artifacts and overshooting may affect the closed loop response[2].
Analysis of loop gain is made by finding poles and zeros of the transfer function. The visual representation in a dB scale may be difficult to be interpreted. Therefore, an alternative method is proposed based on the closure rate of A and $1/\beta$. If the closure rate is $40dB/dec$, it means that phase margin is between $[0°, 45°]$ and the systems tends to be unstable. If the closure rate is less than or equal to $20dB/dec$, it means that the system is stable and the phase margin is greater than 45°. Essentially, this analysis provides a powerful tool that allows to define the stability of the system by plotting the open loop A, the reciprocal of the feedback factor $1/\beta$ and checking the closure rate[2].

$$
\begin{aligned}
&|20log(A * \beta)| = |20log(A) + 20log(\beta)| \Rightarrow \\
&|20log(A * \beta)| = |20log(A) - 20log(\frac{1}{\beta})| \Rightarrow \\
&\text{Closure Rate} = |\text{Slope}(A) - \text{Slope}(\frac{1}{\beta})|
\end{aligned}
$$

2.3 Non Inverting Op Amp Configuration

The Non Inverting Op Amp Configuration is a feedback system that can be analysed using the methods described above. The schematic of this circuit is shown on fig. 3. The transfer function of this system is described in eq. 5. This is the closed loop gain equation. The loop gain is equal to $\frac{a(s)Z_G}{Z_G+Z_F}$, where $a(s)$ is the Op Amp response and $\beta = \frac{Z_G}{Z_G+Z_F}$. From this point on, all Z impedances are considered as complex impedances, unless otherwise stated.

$$
\frac{V_{OUT}}{V_{IN}} = \frac{a(s)}{1 + \frac{a(s)Z_G}{Z_G+Z_F}} \tag{5}
$$

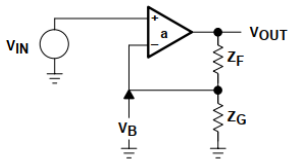


Figure 3: Non Inverting Op Amp

The above circuit can be modified in a Voltage buffer configuration. In this way, it can provide the desired input voltage signal to the one port of the Device Under Test of the author's design, as it will be shown subsequently in the following paragraphs.

2.4 Inverting Op Amp Configuration

The Inverting Op Amp Configuration is also a feedback system that can be analysed in the same way as above and it will be the core of the proposed instrument. The inverting Op Amp is essentially the Auto-Balancing Bridge Configuration which is used for impedance measurement. The schematic is presented on fig. 4. Its transfer function is shown on eq. 6[1]. On the nominator there is a gain factor and a negative sign, however the loop gain is equal to that of the non inverting Op Amp configuration[1]. This observation is important for the SPICE simulations provided in the following paragraphs. The open loop gain is equal to $a(s)$. It can be proven by using figure 1. The forward gain will be a block before the summing input node. By following the proposed

methodology and grounding the input in order to break the loop, the forward gain block will be removed as it will be multiplied with zero input. The proof was not included to save space.

$$\frac{V_{OUT}}{V_{IN}} = \frac{-a(s)\frac{Z_F}{Z_G+Z_F}}{1+\frac{a(s)Z_G}{Z_G+Z_F}} \tag{6}$$

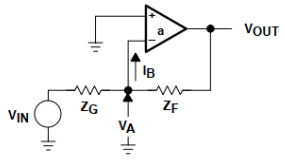


Figure 4: Inverting Op Amp

This circuit is the well known, from the previous coursework, as the Auto-Balancing Bridge. If the circuit is stable and no phase shift is induced by the feedback, then the Impedance of Z_G can be calculated. Additionally, the current can also be calculated.

2.5 Auto Balancing Bridge Compensation

From the first Coursework, it was shown that the auto balancing bridge cannot be used for higher frequencies because of its instability.Assuming Z_F is resistive, when Z_G is capacitive, then $1/\beta = 1+R_F*C_G*s$. Assuming, that $Aol = a(s)$ has a pole close to DC, it is expected that the rate of closure will be $40dB/dec$ and the circuit will be unstable. This allegation is shown on fig. 5[3].

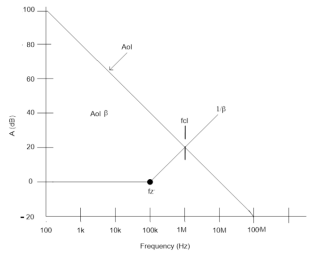


Figure 5: Stability Analysis of Auto Balancing Bridge for Capacitive Z_G.

A potential solution would be to add a parallel capacitor to Z_F, but this is not a general solution, because for every DUT, a different value of Capacitor is needed for compensation[3].
A generic solution that can solve the problem is to add a resistor on the left side of the DUT. The proposed solution is presented on fig. 6. The transfer function remains the same as it was in the inverting Op Amp configuration. However, now $\beta = \frac{1+R_F*C_X*s}{1+(R_F+R_G)C_X*s}$. For the stability analysis, $1/\beta$ has to be examined. There is a zero $\omega_z = \frac{1}{(R_F+R_G)C_X}$ and a pole $\omega_p = \frac{1}{R_G C_X}$. By choosing, $R_F = R_G$, the following relationship applies $\omega_p = 2\omega_z$. In this way, if the zero occurs, before $1/\beta$ crosses A_{ol}, the rate of closure is $20db/dec$ and the system is stable, as it is shown on fig. 7. The system is not stable only when Aol gets through f_p' and f_z.

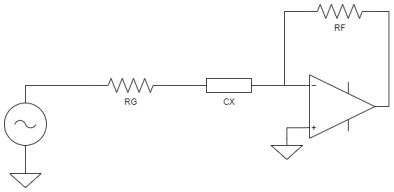


Figure 6: Compensated Auto Balancing Bridge for Capacitive Loads.

In case the DUT is an inductor then $1/\beta = \frac{sL+2R}{sL+R}$, therefore, there is a zero $\omega_z = 2R/L$ and a pole $\omega_p = R/L$. The relationship between zero and pole is $\omega_z = 2\omega_p$. If the Aol curve crosses $1/\beta$ later than ω_z, then the rate of closure is $20dB/dec$ and the system is stable. If the Aol curve crosses $1/\beta$ between ω_z or ω_p, the rate of closure is $0dB/dec$ and the system is also stable. In any case, the system is stable when the DUT is inductive.

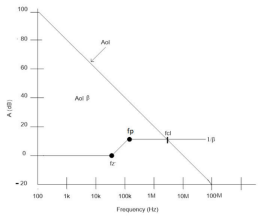


Figure 7: Stability Analysis of Modified Auto Balancing Bridge for Capacitive DUT.

2.6 Proposed Vector Network Analyser

Based on the circuits described above and their stability, the circuit of fig. 8 is a symmetrical modified Auto Balancing Bridge. This topology allows to apply on the one side a voltage signal and to ground the other side by using the suitable switches and the signal sources. The configuration in the image shows an non-inverting Op Amp, which applies a Signal Voltage at $V1O = V1$ node (short circuit through $S2$). The rest of the circuit is the modified Auto balancing Bridge proposed previously for compensation and stability. The Resistors can be assigned different values to achieve better performance for different DUTs. During the measurement all Resistors have the same value as explained before.
In this Configuration, by measuring V_1, V_2, V_{1PORT} through an ADC, Y_{11} and Y_{21} parameters can be obtained, since V_{20} is grounded, which means that V applied on the right side of DUT V_{2PORT} is grounded. Therefore, $I_{1PORT} = \frac{V_1 - V_{1PORT}}{R}$ and $I_{2PORT} = -V_2/R$.
In order to calculate Y_{12} and Y_{22}, all switches must be reversed in respect to the configuration shown on the image. Additionally, Voltage Signal Source on the left has to be grounded and a Voltage Signal has to be applied on the right side. The procedure to calculate the corresponding Y parameters is the same.
All measurements are conducted with respect to the ground through an Instrumentation Amplifier, in order for the signals to have the same voltage reference. At first glance, $V1O$ and $V2O$ may seem useless, however, it is important to track their value and ensure that they remain grounded, otherwise there is a phase shift in the closed loop and the measured values are wrong.
At this point, it is clear that the stability of the Non-Inverting Op Amp and the Inverting Op Amp has to be simulated and examined. Furthermore, it is important to simulate and examine the closed loop gain and phase shift of the proposed Auto-Balancing bridge. In this way, the operating range of the instrument can be obtained.
This instrument has another drawback besides the closed loop phase shift and this is the ADC. The target of this device is to measure frequencies up to $100MHz$. The ADC has to sample 4 different signals in order to complete a measurement. The sampling frequency has to be at least two times the frequency of operation, therefore, the minimum specification for an ADC to be used is $800MSamples/sec$. Cheapest ADC found to outperform this sampling rate costed 36$. It is noted here that the part of the circuit including MUXes, switches and ADC has not been included in simulations.

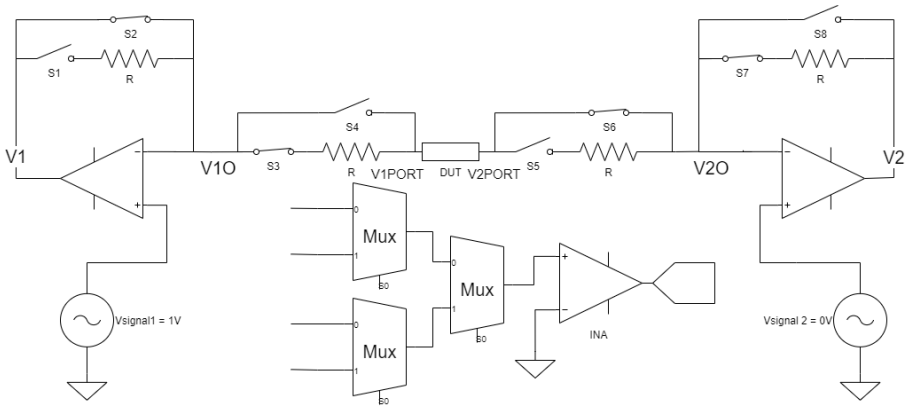


Figure 8: Proposed Vector Network Analyser

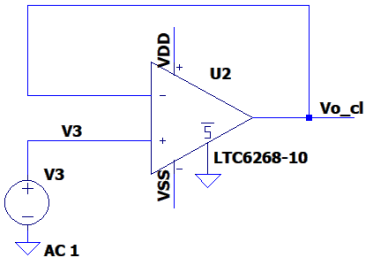
3 Results and Methods

This section discusses the obtained results of the proposed device and the methods used to characterise it.

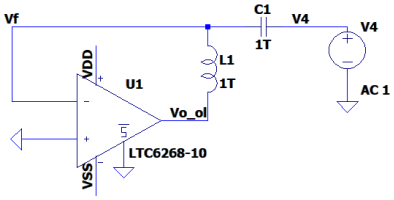
3.1 Stability Analysis of LTC6268-10 without passive components on the loop.

The circuit shown on fig. 9a is a voltage buffer. Assuming that $a(s)$ is the Op Amp transfer function, the closed loop gain is equal to eq. 7. Therefore, the feedback factor β is equal to 1 and the loop gain $Aol * \beta = a(s)$. By using the circuit shown on figure 9b, the open loop gain and the feedback factor can be calculated, therefore, the loop gain can also be calculated. The capacitor and the inductor are used in order for the circuit to maintain its DC characteristics during the AC analysis. This method is officially proposed by Texas Instruments in [2]. The open loop response and the reciprocal of the feedback factor are shown on fig. 10a. The closure rate between the open loop gain and the $1/\beta$ is $40db/dec$, therefore, this Op Amp is marginally stable and can cause overshooting and ringing. Additionally, it is expected to cause ringing when driving capacitive loads. However, for lower frequencies $< 100MHz$, the circuit remains stable, since the phase shift is only 90°. On the fig. 10b, the Closed Loop AC response is presented. It is shown that the output suffers only 1° phase shift at $100MHz$. Taking the above statement into consideration, the circuit is stable for $f < 100MHz$ and it has only 1° phase shift, therefore it can be used to generate the input voltage signal.

$$A_{cl} = \frac{a(s)}{1 + a(s)} \tag{7}$$

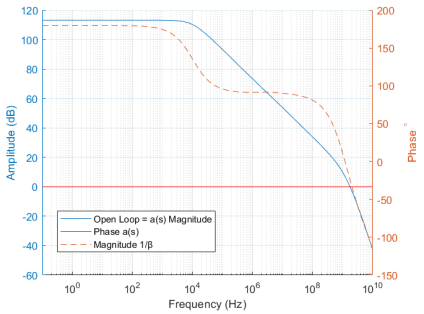


(a) LT6268-10 used in Voltage Buffer Configuration to Generate desired signal on V_{out} node.

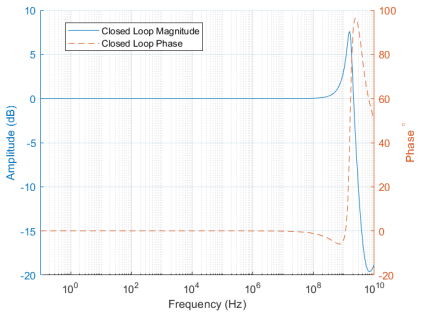


(b) LT6268-10 Testbench to calculate $a(s)$, loop gain $Aol * \beta = a(s) * 1 = a(s)$.

Figure 9: LT6268-10 Voltage Buffer



(a) LT6268-10 Open Loop and $1/\beta$ response.



(b) LT6268-10 in Voltage Buffer Configuration Closed Loop.

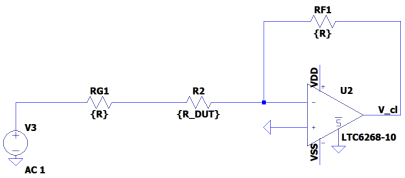
Figure 10: LT6268-10 Open loop gain, $1/\beta$ and Closed Loop Gain response.

3.2 Stability Analysis of the proposed Vector Network Analyser

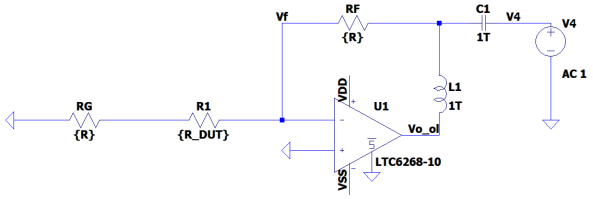
The ideal VNA proposed instrument, can be shown in fig. 11a and the proposed one on fig. 11c. It is assumed that switches are closed/open in a similar manner as it is in fig. 8. These circuits were simulated simultaneously to ensure they produce similar results.

As it was explained in previous section, the stability of the circuit is analysed by plotting the loop gain and the reciprocal of the feedback factor. Assuming, $Z_{DUT} = R$ and $R_G = R_F = 100\Omega$, a parametric sweep is executed for $R \in [1\Omega, 10M\Omega]$. The result is shown in fig. 12a. The system is marginally stable for $1GHz$, but it is stable for $f < 100MHz$.

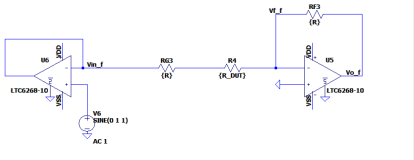
In a similar manner, the stability of the system is investigated for all possible combinations where $R_F = R_G \in 100\Omega, 1k, 10k, 100k, 1M\Omega, 10M\Omega$ and $Z_{DUT} = R, L, C$. The stability ranges for various configuration are shown



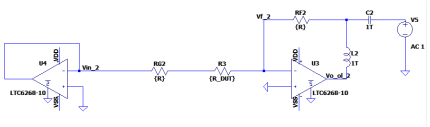
(a) LT6268-10 used in the proposed Auto-Balancing Bridge Configuration.



(b) LT6268-10 proposed Auto-Balancing Bridge Testbench to calculate open loop, loop gain and feedback.



(c) LT6268-10 used in the proposed Architecture to measure Y parameters.



(d) LT6268-10 proposed Instrument Testbench to calculate open loop, loop gain and feedback.

Figure 11: LT6268-10 Instrument Stability Analysis

on table 1. This table sets the first restriction of the operating points of the instrument. The next restrictions to be set will be extracted by the closed loop system response and the phase shift induced in the virtual ground. An important conclusion that can be derived by table 1 is that the stability of the proposed system does not depend on the DUT but on the configuration settings.

$R_F = R_G$	$R \in [1\Omega, 10M\Omega]$	$C \in [1pF, 1F]$	$L \in [1mH, 1kH]$
100	0-100MHz	0-100MHz	0-100MHz
$1k$	0-100MHz	0-100MHz	0-100MHz
$10k$	0-50MHz	0-50MHz	0-100MHz
$100k$	0-5MHz	0-8MHz	0-100MHz
$1M$	0-600kHz	0-591kHz	0-100MHz
$10M$	0-76kHz	0-75kHz	0-100MHz

Table 1: Stability Ranges for different $R_F = R_G$ configurations.

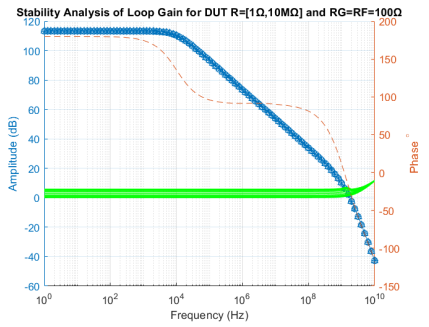
3.3 Closed Loop and Virtual Ground Analysis of the proposed Vector Network Analyser.

The Closed Loop Response of the System is described by eq. 8. Assuming an ideal operation where $a(s) \to \infty$, the transfer function will be defined by eq. 9. In order for the eq. 9 to be true, the AC closed loop response and the AC response of the feedback node have to be examined. It is expected that, even if the closed loop has no shift, the feedback node will show small oscillations that will deteriorate the accuracy of the measurement. Additionally, an acceptable range of error has to be defined. The input offset voltage of the Op Amp according to the data sheet is $3mV$[4]. Therefore, the author decided that the minimum voltage to be measured on the output of the Auto Balancing bridge to be $100mV$. The maximum error will be 3%.

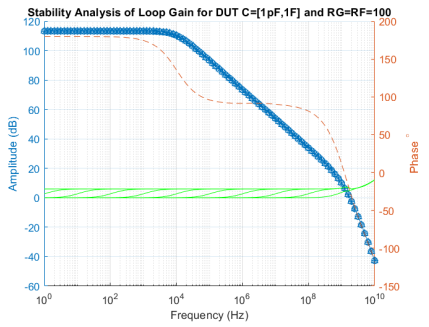
$$\frac{V_{OUT}}{V_{IN}} = \frac{-a(s)\frac{Z_F}{Z_G+Z_F}}{1+\frac{a(s)Z_G}{Z_G+Z_F}} \tag{8}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_G} = -\frac{R_F}{R_G + Z_{DUT}} \tag{9}$$

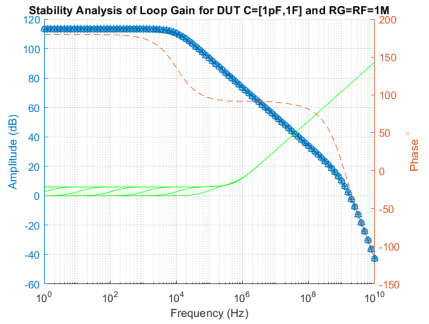
Firstly, a Resistive DUT will be examined. Given that the Input Signal is $1V$ and $R = 100\Omega$. In order for the minimum output to be $100mV$ and based on the eq. 9, the greatest R_{DUT} to be measured will be 900Ω, or $20log(100/(100+900)) = -20dB$. Additionally, in order for the instrument to have good sensitivity, the Resistance Under Test has to be at least equal to $2 * R_F = 2 * R_G$. If the resistance is smaller than this, then the accuracy will not lead to clear results. Therefore, the output value has to be equal to maximum $500mV$ or in logarithmic scale it should be no greater than $-6dB$ with respect to the input.
The closed loop AC analysis is shown on fig. 13a. The acceptable range of R_{DUT} is $[100\Omega, 900\Omega]$. The phase shift is $1°$ at $100MHz$.



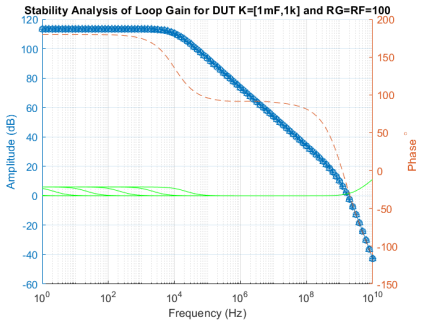
(a) Stability Analysis of Instrument for $R_F = R_G = 100$ and $Z_{DUT} = R \in [1\Omega, 10M\Omega]$. Blue lines are Open Loop Gain Aol and orange lines are its phase shift. Green lines are $1/\beta$. The system is marginally stable for $10GHz$. However, for the operation frequency $< 100MHz$, the system remains stable.



(b) Stability Analysis of Instrument for $R_F = R_G = 100$ and $Z_{DUT} = C \in [1pF, 1F]$. Blue lines are Open Loop Gain Aol and orange lines are its phase shift. Green lines are $1/\beta$. The system is marginally stable for $10GHz$. However, in the range of operation frequency $< 100MHz$, the system remains stable. Note the compensation of the $1/\beta$ as it was explained in fig. 7. The zero is cancelled by the pole and the system remains stable.



(c) Stability Analysis of Instrument for $R_F = R_G = 1M\Omega$ and $Z_{DUT} = C \in [1pF, 1F]$. Blue lines are Open Loop Gain Aol and orange lines are its phase shift. Green lines are $1/\beta$. The system is marginally stable for $10GHz$. However, in the range of operation frequency $< 100MHz$, the system remains stable only for $f \in [0Hz, 591kHz]$. Note the compensation of the $1/\beta$ as it was explained in fig. 7 still applies. However, for values greater than $591kHz$, the rate of closure increases and the phase shift of the loop gain tends to 180° leading to instability.



(d) Stability Analysis of Instrument for $R_F = R_G = 100$ and $Z_{DUT} = L \in [1mH, 1kH]$. Blue lines are Open Loop Gain Aol and orange lines are its phase shift. Green lines are $1/\beta$. The system is marginally stable for $10GHz$. Note the compensation of the $1/\beta$ and the fact that due to the inductor a pole is induced before the zero and the system is always stable for $f < 100MHz$.

Figure 12: Instrument Stability Analysis

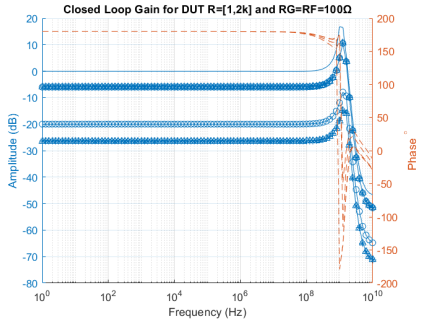
As explained earlier, the feedback node is expected not to be grounded, but it will have a small voltage for higher frequencies. The author defined that, if the measured voltage of the Output is 100 times greater than the voltage of the feedback node, then the error percentage will be maximum 1%. Which means that:

$$V_2 = 100 * V_f \Rightarrow \frac{V_2}{V_f} = 100$$

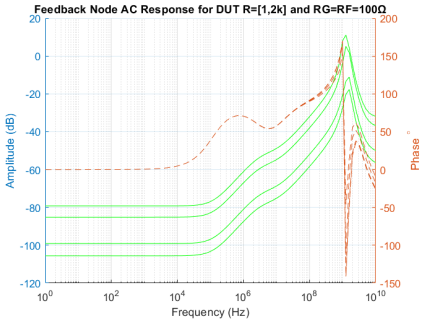
$$log\left(\frac{V_2}{V_f}\right) = log(100) \Rightarrow$$

$$20log\left(\frac{V_2}{V_{in}}\right) - 20log\left(\frac{V_f}{V_{in}}\right) = 40dB$$

Given that the phase shift of the feedback node remains close to 0° and the difference is greater than $40dB$, the voltage at virtual ground can be ignored. By inspecting fig. 13b, the feedback node can be assumed as a ground point for measurements below $100kHz$. After this point, the instrument is potentially going to produce ringing around this node.
A transient analysis is executed with $R_F = R_G = R = 100$ and $R_{DUT} = 100\Omega$. If V_1 frequency is $100kHz$, the system behaves normally, as it is shown on fig. 14a. The Input Voltage is $1V$, the V_2 is equal to $0.5V$ as expected since $R_F/(R_G + R_{DUT}) = 100/200$. Additionally, V_2 has reverse polarity as expected. Feedback voltage is approximately zero as it is shown on the plot and therefore, it is negligible.



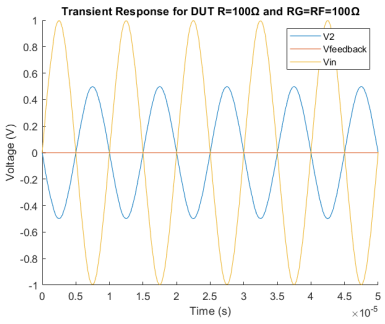
(a) Closed Loop AC Analysis of V_2, output of Op Amp. It is shown that for $R = 1\Omega$, V_2 is $0dB$, which means that the signal level is not enough to define whether the R_DUT is $1\Omega, 2\Omega$ or 0Ω. On the other hand if $R_DUT = 2k$, then V_2 is equal to $-27dB$ and a real time measurement will lead to an error of approximately 6% if the input offset voltage is $3mV$. Therefore, when $R_F = R_G = 100\Omega$, $R_{DUT} \in [100\Omega, 900\Omega]$.



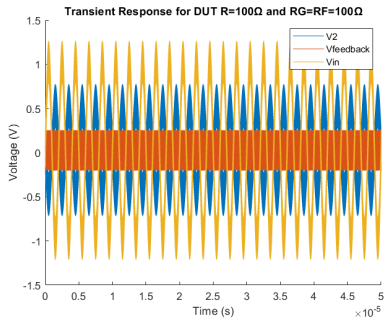
(b) Feedback Node AC Analysis of V_2, output of Op Amp. It is shown that for values approximately below $100kHz$ the feedback node gets a value which will be significantly small enough compared to V_{in} value. The $40dB$ limit is well maintained. However, for higher values there is a phase shift and a rise in the voltage of that node. This means that this node will most probably produce ringing artifacts.

Figure 13: Closed Loop and Feedback Node AC Analysis

On the contrary, for a frequency equal to $500kHz$, ringing artifacts occur and the Voltage on the feedback node oscillates. This is presented on fig. 14b.



(a) Transient Analysis for $R = 100\Omega$ at $100kHz$.



(b) Transient Analysis for $R = 100\Omega$ at $500kHz$.

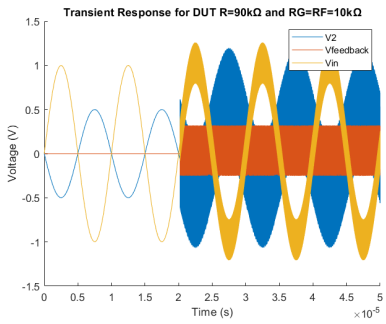
Figure 14: Transient Analysis for $R_{DUT} = 100\Omega$ and $R_F = R_G = 100\Omega$.

Considering, the ringing artifacts, one could attempt to measure the current across the left resistor and across the feedback resistor. In this way, the current of port 1 and the current going to feedback node could be found. At first glance, someone would thought that in this way the difference can be found and it can be compensated. However, the DUT is a black box and in case where there is a 3rd port to ground then the current from port 2 to ground would be different and not equal to the current entering port 1. Therefore, this method cannot be used.

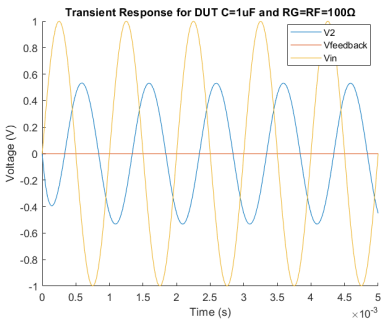
As the Magnitude of the Resistance increases the performance deteriorates. The transient Analysis in fig. 15a shows that for a $500kHz$ signal, the system produces ringing artifacts after a while. The Op Amp was chosen to be a low input bias current in order to accommodate as large resistors as possible, however, it is tested in a few $k\Omega$ resistors[4]. The greater the Resistor, the smaller the current driving the feedback node. There is a certain point where, the input bias current is of the same order of magnitude as the feedback and the port 2 current. This situation deteriorates the oscillating problem and decreases the measurement range of the instrument.

For the capacitive and the inductive DUT, the ranges of operation of the instrument are calculated in a similar manner. The only difference this time is that depending on the frequency of operation, the DUT range changes. Once again, the aim of the author is to achieve gains at V_2 in the range of $[-6dB, -20dB]$. As previously, the system produces ringing artifacts for frequencies above $100kHz$.

The following table, summarises all possible configurations. These results were extracted from the simulations performed in LTSPICE.



(a) Transient Analysis for $R_F = R_G = 10k\Omega$ and $R_{DUT} = 90k\Omega$ at $100kHz$. After a while ringing occurs.



(b) Transient Analysis for $R_F = R_G = 100\Omega$ and $C_{DUT} = 1u$ at $1kHz$. Notice that, if $V2$ is altered polarity, then there is $-\pi/2$ phase difference. A capacitive component has $-\pi/2$ phase different compared to a real one.

Figure 15: Transient Analysis for various configurations.

Frequency	Component	R=100	R=1k	R=10k	R=100k	R=1M	R=10M
1	R	[100,900]	[1k,9k]	[10k,90k]	[100k,900k]	[1M,9M]	10M
	L	[20,200]	[200,2k]	[2k,20k]	[20k,200k]	[200k,2M]	-
	C	[200u,2m]	[20u,200u]	[2u,20u]	[0.2u,2u]	[20n,200n]	[2n,20n]
100	R	[100,900]	[1k,9k]	[10k,90k]	[100k,900k]	[1M,9M]	-
	L	[0.2,2]	[2,20]	[20,200]	[200,2k]	[2k,20k]	[20k,200k]
	C	[2u,20u]	[0.2u,20u]	[20n,0.2u]	[2n,20n]	[0.2n,2n]	[20p,200p]
1k	R	[100,900]	[1k,9k]	[10k,90k]	[100k,900k]	[1M,9M]	-
	L	[20m,0.2]	[0.2,2]	[2,20]	[20,200]	[200,2k]	-
	C	[0.2u,20u]	[20n,0.2u]	[2n,20n]	[0.2n,2n]	[20p,200p]	[2,20p]
10k	R	[100,900]	[1k,9k]	[10k,90k]	[100k,900k]	[1M,9M]	-
	L	-	-	-	-	-	-
	C	[20n,0.2u]	[2n,20n]	[200p,2n]	-	-	-
100k	R	[100,900]	[1k,9k]	-	-	-	-
	L	-	-	-	-	-	-
	C	[2n,20n]	-	-	-	-	-

Table 2: Range of Operation.

3.4 Measurements of 3 Port Networks.

In order to save space, only Y_{11} and Y_{21} calculations are shown. The following circuits are symmetrical and the simulations on both sides have no meaning. The author acknowledges that this fact does not apply in reality. This first 3-port network is a T network of equal resistances $R = 1k\Omega$. For this measurement, $R_G = R_F = R = 10k\Omega$ and the operation for $100kHz$ will be shown. Based on hand calculations and voltages shown on fig. 16, $Y_{11} = 0.666mS$

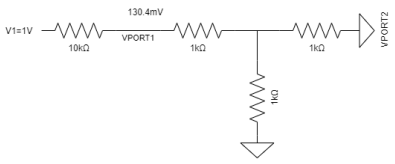
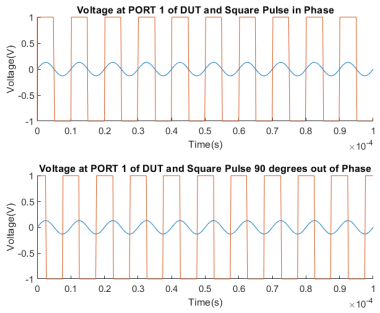


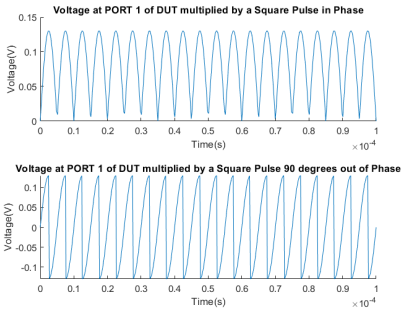
Figure 16: Resistive 3-port Tee Network with V_{2PORT} grounded. Equivalent Configuration to measure Y_{11} and Y_{21}.

In order to calculate Y_{11} from the testbench, the signals V_1,V_{1PORT} and $V_{2O} = V_{2PORT}$(short circuit) and V_2 are extracted. Four signals in total, as explained earlier. V_{2O} remains grounded and its effect is negligible. By using these signals in MATLAB, complex numbers of V_{1PORT} and I_{1PORT} will be extracted.
The signal V_{1PORT} is multiplied by an in phase square pulse and an 90° out of phase square pulse as shown on fig. 17. The multiplication products are shown in fig. 17b. By calculating the average of the product signals, V_I and V_Q are obtained[3]. These Values are *average* values of a sinusoidal wave. The relationship between average and peak values is $V_p = V_{AVE}/0.637$. Therefore, the complex value of the signal can be extracted as $V = V_I/0.637 + i * V_Q/0.637$. In this way, $V_{PORT1} = 0.1261 + i * 0.0027$.

By using the same procedure, V_1 is calculated and V_2 as well. Then $Y_{11} = 6.6666 * 10^{-4} - i * 2.3741 * 10^{-8}$. Compared to the hand calculations, the proposed method calculated correctly the real part of Y_{11}, however, there is additionally a small imaginary part that is an error. The error is four orders of magnitude smaller than the expected result and therefore can be neglected for this measurement. The error in magnitude is equal to $(130.4mV - 126.1mV)/130.4mV = 0.0331$ or 3% and the error in phase is equal to 1.29°.
Similarly, Y_{21} was calculated by hand equal to -0.3332, while in MATLAB, by using signal V_2, it was calculated equal to $-3.3332 * 10^{-4} + 5.5216e * 10^{-8}$. The magnitude error was equal to $3.66 * 10^{-4}$ and the phase error was equal to 0.0095°.
Resistive Tee Network is a symmetric device, therefore, Y_{12}, Y_{22} can be calculated by $Y_{11} = Y_{22}$ and $Y_{12} = Y_{21}$. In order to calculate them through the proposed circuit, closed switches should be opened, and opened switches should be closed. In this way, through the symmetrical instrument the unknown Y-Parameters can be extracted. This procedure is not presented on this document to save space.



(a) Transient Analysis V_{PORT1} for $R_F = R_G = 10k\Omega$ $100kHz$ and an in phase Square Wave.



(b) Multiplication Products.

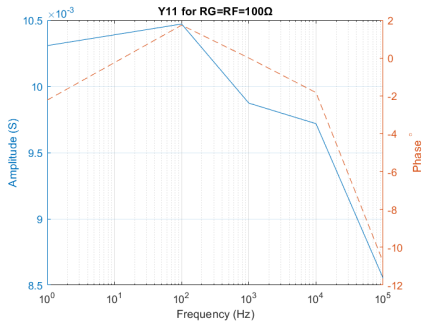
Figure 17: Transient Analysis V_{PORT1} for $R_F = R_G = 10k\Omega$ $100kHz$. The sampled signal is multiplied by an in phase and a 90° out of phase square wave.

RLC	R	f	Y11	Y21	Phase Error	Mag Error
Resistive T						
10k	10k	100kHz	6.6667e-05 - 4.0170e-11i	-3.3333e-05 + 2.3013e-10i	0.343	-
100k	100k	10kHz	6.6667e-05 - 3.9140e-11i	-3.3333e-05 + 2.5799e-10i	0.343	-
1M	1M	10kHz	6.6667e-05 - 3.9185e-11i	-3.3333e-05 + 2.0182e-10i	0.343	-
Resistive Pi						
10k	10k	10kHz	2.0000e-04 - 3.6372e-11i	-9.9999e-05 + 1.0915e-10i	0.343	-
100k	100k	10kHz	2.0000e-04 - 3.4489e-11i	-9.9999e-05 + 1.0267e-10i	0.343	-
1M	1M	1kHz	2.0000e-04 - 3.4145e-11i	-9.9999e-05 + 1.1392e-10i	0.343	-
Capacitive T						
10p	1M	10kHz	1.1789e-07 + 3.3324e-07i	-5.8946e-08 - 1.6662e-07i	19.4828	18.50%
10n	10k	1kHz	-5.3785e-06 + 4.1748e-05i	2.6893e-06 - 2.0874e-05i	7.3412	0.49%
1n	100	1kHz	-0.0005 + 0.0040i	0.0002 - 0.0020i	6.42	2.79%
Capacitive Pi						
10p	1M	1kHz	-9.8141e-09 + 1.3016e-07i	4.9076e-09 - 6.5079e-08i	4.3119	4%
10n	1k	1kHz	-1.0162e-05 + 1.2507e-04i	5.0813e-06 - 6.2535e-05i	4.645	1.40%
1n	1k	100kHz	0.0001 + 0.0012i	-3.6888e-05 - 6.1484e-04i	3.1944	2.48%
Inductive T						
1m	100	10kHz	-0.0010 - 0.0112i	0.0005 + 0.0056i	5.3067	5.41%
1	10k	10kHz	6.1672e-07 - 9.5869e-06i	-1.5180e-07 + 5.4057e-06i	3.6807	10.45%
1k	1k	1kHz	1.0327e-08 - 1.2970e-07i	-3.7294e-09 + 5.7279e-08i	4.5523	18.45%
Inductive Pi						
1	10k	1kHz	-8.2976e-06 - 3.5494e-04i	4.6599e-06 + 1.7795e-04i	1.3392	10.34%
1k	1MEG	10kHz	9.2577e-11 - 2.4502e-08i	1.9798e-09 + 1.1168e-08i	10.0527	29.90%

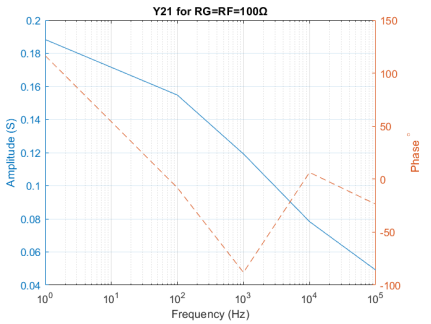
Table 3: Y_{11} and Y_{21} measurements for various operating points.

3.5 Measurement of Op Amp Gain

Since the Instrument Calculates Y Parameters, Y_{11} (input admittance) and Y_{21} (trans-admittance gain) will be calculated. The Op Amp to be examined is the *RH101A*. By placing the inverting Op Amp in the DUT position and doing an AC Analysis, it is expected to start ringing below $10kHz$, therefore all results above $10kHz$ cannot be taken into consideration as valid results.
Furthermore, the Output of the DUT will have to remain grounded as the input will have to remain grounded because it is in inverting mode. For the inverting Op Amp, Resistances of 100Ω have been chosen, to facilitate as large operation range as possible. The $R_F = R_G = R$ were chosen equal to 100Ω, as it was explained previously on how to choose range.
The Y_{11}, Y_{21} are shown on fig. 18. The input admittance remains around zero. This can be explained as the admittance, the DUT Op Amp sees at the input which is 100Ω. Therefore, Y_{11} is expected to be equal to $1/100S$. The value measured on the figure at $1Hz$ is pretty close equal to $1.5 * 10^(-3)S$. On the other hand regarding Y_{21}, even though, small currents get through the feedback loop, since both input and output are virtually grounded, there is a phase shift. Initially, the trans-admittance (gain) seems to be inductive ($Y_L = 1/j\omega L$). After $1kHz$, it becomes capacitive, reaching probably to a resonance at $10kHz$ as explained by AC analysis. The Op Amp in general behaves capacitively, since its $a(s)$ open loop transfer function is like a low pass filter/Capacitor response.



(a) Input Admittance of Inverting Op Amp DUT.



(b) Trans-admittance Gain of Op Amp DUT.

Figure 18: Transient Analysis V_{PORT1} for $R_F = R_G = 10k\Omega$ $100kHz$. The sampled signal is multiplied by an in phase and a $90°$ out of phase square wave.

3.6 Measurement of RLC

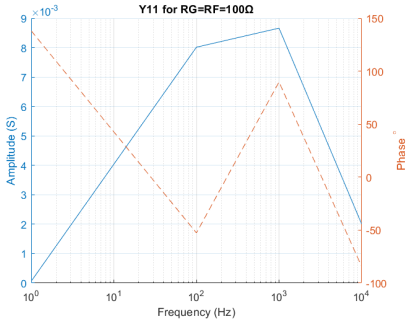
The same LCR circuit was designed as Report 1. Values chosen are $L = 0.008H$, $C = 3.18uF$ and $R = 50\Omega$. For these values $\zeta = 0.5$(underdamped), resonance frequency $f_o = 1kHz$ and $Q = 1$. Y_{11}, Y_{21} is defined by equation eq. 10. However, in our case, the virtual ground is not grounded for higher frequencies and it is expected to have variations. By inspecting the AC response, V_{PORT2} has unity gain at resonance frequency and it is suppressed for the rest of the frequencies. In order to calculate Y_{11}, port 2 is supposed to be grounded, therefore, it is expected to have complex values. It is chosen to use $R_F = R_G = R = 100\Omega$. Results are shown on fig. 19.It is clear that Y_{12} is much alike Y_{21} and have opposite phase from Y_{11} as expected. For Y_{11}, Y_{12}, Y_{21} there are abrupt changes on phase on both $100Hz$ and $1kHz$, which is a typical AC behaviour of current around oscillation frequency for an LCR circuit. While Y_{22} shows a similar pattern but in smaller extend.
From simulations, at $10kHz$ ringing artifacts were encountered, which means that from that point on, system is not robust.

$$Y_{11} = \frac{j\omega C}{-\omega^2 LC + 1} = -Y_{21} = -Y_{12} \tag{10}$$

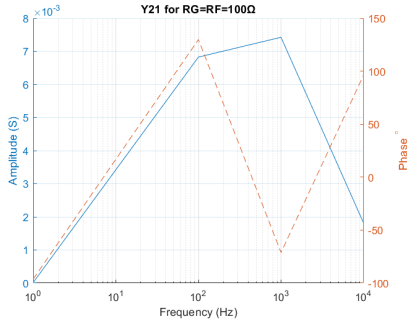
$$Y_{22} = \frac{-\omega^2 LC + 1 + Rj\omega}{R(-\omega^2 LC + 1)} \tag{11}$$

3.7 Calibration Method.

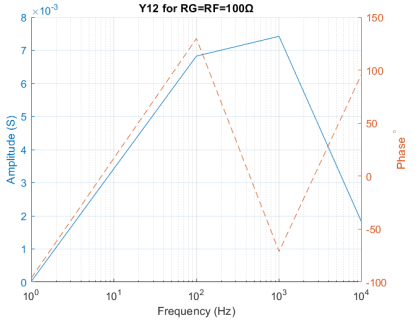
In order to calibrate the instrument, R_F, R_G have to be defined. For every frequency, the following procedure can be used. Firstly, by short circuiting DUT ports, an expression can be obtained $V_2/V_1 = -R_F/R_G$. Then by placing a known Resistance as a DUT, another expression can be obtained $V_2/V_1 = -R_F/(R_G + R_{DUT})$. Therefore, there are 2 equations with two unknown values. In this way, and by doing it for various frequencies,



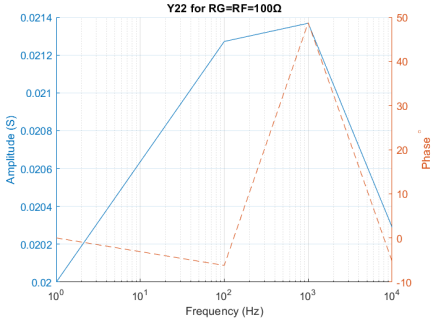
(a) Input Admittance of LCR.



(b) Trans-admittance Gain of LCR.



(c) Reverse Admittance Gain of LCR.



(d) Output Admittance of LCR.

Figure 19: Y Parameters for LCR with respect to frequency.

the resistors of the device can be calculated for more accurate results. This should be done for both sides. Therefore, at least 4 measurements are needed for every spot frequency.
Potential errors that can alter performance is the Capacitive input of the Op Amp, the oscillations in the feedback path and the inductive behaviour of the Settings Resistors.

4 Discussion and Conclusion

This document presented a modified Auto Balancing Bridge in a symmetric configuration, employing switches, able to calculate *Y-Parameters* of DUT. The system operates under condition for $1Hz$ to $100kHz$. Furthermore, it is able to measure DUTs with impedances ranging from 1Ω to $10M\Omega$, capacitances from pF to mF and inductances from uH to kH.
The proposed instrument, behaves relatively well, The phase error is relatively low for small values and low frequencies and increases for greater values up to $20°$. The magnitude error is also low for low magnitudes and small frequencies and increases up to 30% for higher frequencies and values that require $10M\Omega$ configuration
It should be noted that, the circuit is stable for up to $100MHz$. Therefore, the ringing artifacts can be removed through digital processing and extend its range. The range presented in this reports accounts only for pure measurements without further noise/ringing rejection.
The proposed architecture achieves this range without need to change many configuration but one value of a set of resistors. This makes this application extremely simple.
The proposed method of ADC sampling and Digital Signal Processing was chosen because it was easier to be conducted during simulation procedures. Otherwise, for a real application, the Digital Signal Processing could be replaced by Analogue Blocks as it was explained in Report 1. In phase and out of Phase bistable square signals could be implemented with a PLL, a schmitt trigger, 2 flip-flops(Digital phase shift) and 2 comparators extending the range of square wave to $[-1, 1]V$. Then the average value could be calculated by low pass filter. However, the low pass filters. require long simulation times due to their time constant integration. Therefore, a simulation in which clock was $10kHz$ and the time constant was a few seconds would require ages to finish. The equivalent analogue circuit is shown on fig. 20. The schematic shown on this figure is a simplified schematic. Potentially, more mixers and low pass filters would be used and less multiplexers.

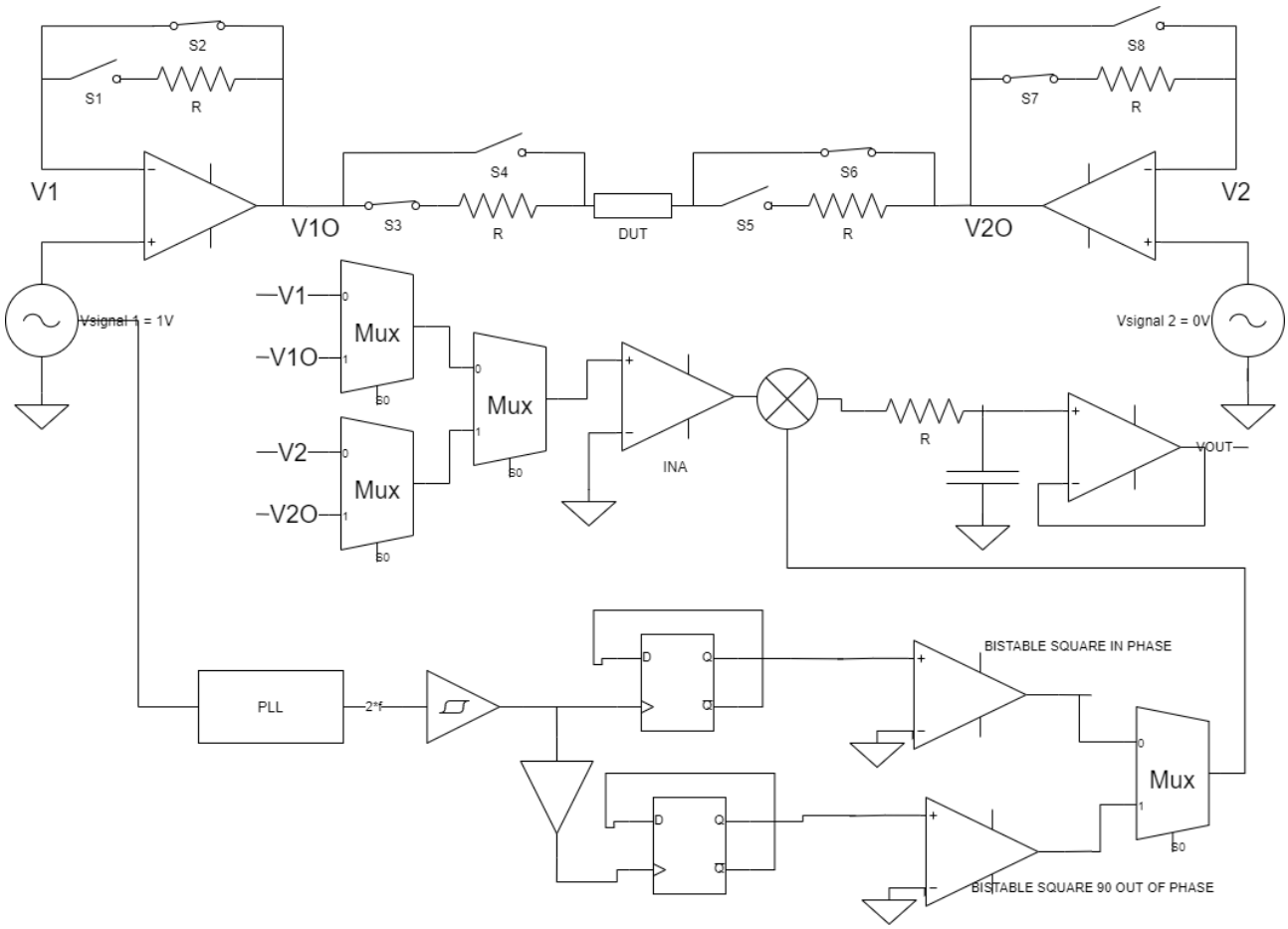


Figure 20: Equivalent Analogue Circuit

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[4] Linear Technology, *LTC6268-10/LTC6269-10 – 4GHz Ultra-Low Bias Current FET Input Op Amp*. Linear Technology Analog Devices, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, 2015.