1. Description

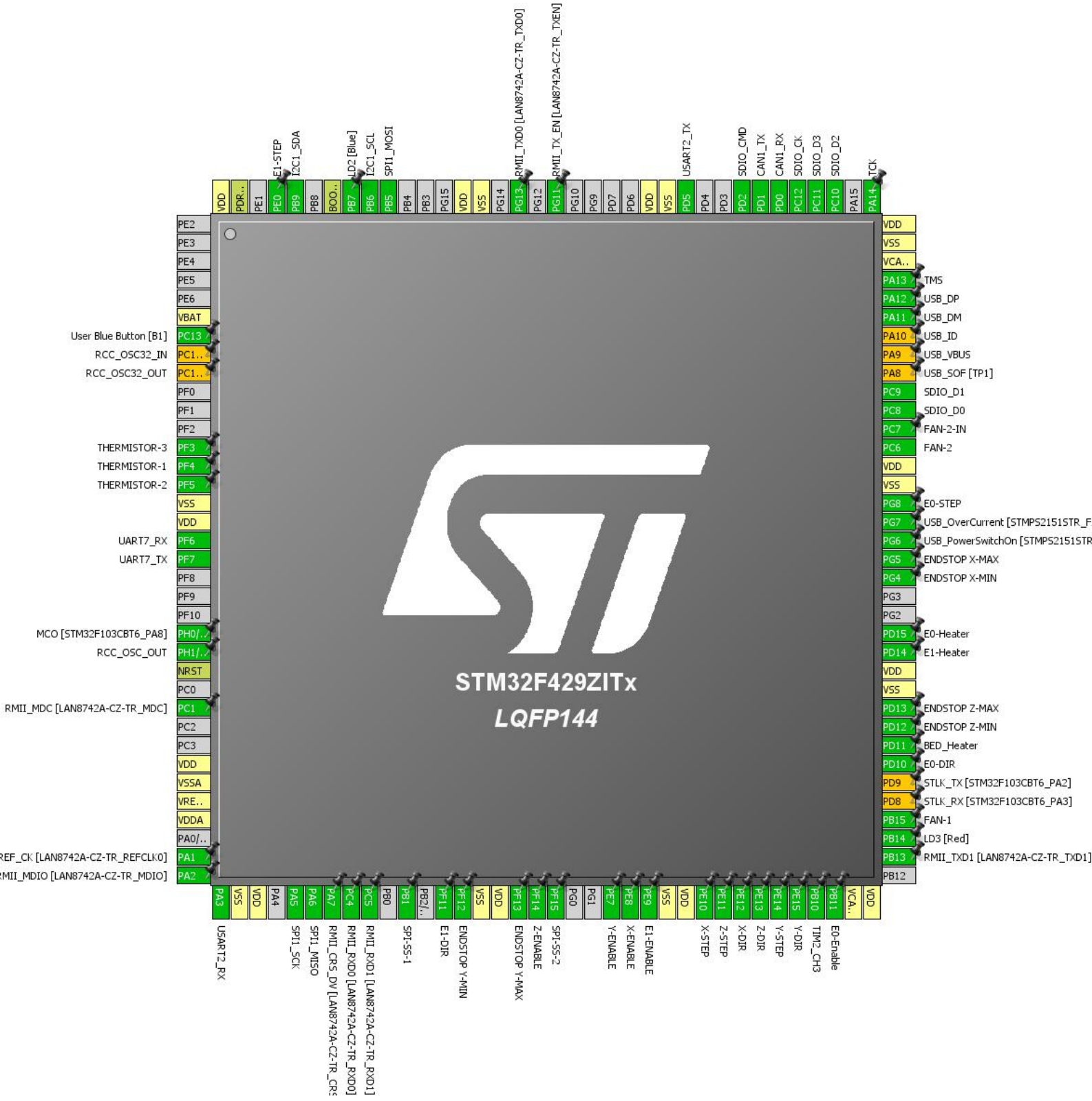
1.1. Project

Project Name	Salamander
Board Name	NUCLEO-F429ZI
Generated with:	STM32CubeMX 4.16.1
Date	10/29/2016

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	User Blue Button [B1]
8	PC14/OSC32_IN **	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT **	I/O	RCC_OSC32_OUT	
13	PF3	I/O	ADC3_IN9	THERMISTOR-3
14	PF4	I/O	ADC3_IN14	THERMISTOR-1
15	PF5	I/O	ADC3_IN15	THERMISTOR-2
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	UART7_RX	
19	PF7	I/O	UART7_TX	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ-TR_MDC]
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CK [LAN8742A-CZ-TR_REFCLK0]
36	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
37	PA3	I/O	USART2_RX	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
44	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
45	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
47	PB1 *	I/O	GPIO_Output	SPI-SS-1

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	PF11 *	I/O	GPIO_Output	E1-DIR
50	PF12 *	I/O	GPIO_Input	ENDSTOP Y-MIN
51	VSS	Power		
52	VDD	Power		
53	PF13 *	I/O	GPIO_Input	ENDSTOP Y-MAX
54	PF14 *	I/O	GPIO_Output	Z-ENABLE
55	PF15 *	I/O	GPIO_Output	SPI-SS-2
58	PE7 *	I/O	GPIO_Output	Y-ENABLE
59	PE8 *	I/O	GPIO_Output	X-ENABLE
60	PE9 *	I/O	GPIO_Output	E1-ENABLE
61	VSS	Power		
62	VDD	Power		
63	PE10 *	I/O	GPIO_Output	X-STEP
64	PE11 *	I/O	GPIO_Output	Z-STEP
65	PE12 *	I/O	GPIO_Output	X-DIR
66	PE13 *	I/O	GPIO_Output	Z-DIR
67	PE14 *	I/O	GPIO_Output	Y-STEP
68	PE15 *	I/O	GPIO_Output	Y-DIR
69	PB10	I/O	TIM2_CH3	
70	PB11 *	I/O	GPIO_Output	E0-Enable
71	VCAP_1	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
76	PB15	I/O	TIM8_CH3N	FAN-1
77	PD8 **	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9 **	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
79	PD10 *	I/O	GPIO_Output	E0-DIR
80	PD11 *	I/O	GPIO_Output	BED_Heater
81	PD12 *	I/O	GPIO_Input	ENDSTOP Z-MIN
82	PD13 *	I/O	GPIO_Input	ENDSTOP Z-MAX
83	VSS	Power		
84	VDD	Power		
85	PD14 *	I/O	GPIO_Output	E1-Heater
86	PD15 *	I/O	GPIO_Output	E0-Heater
89	PG4 *	I/O	GPIO_Input	ENDSTOP X-MIN
90	PG5 *	I/O	GPIO_Input	ENDSTOP X-MAX

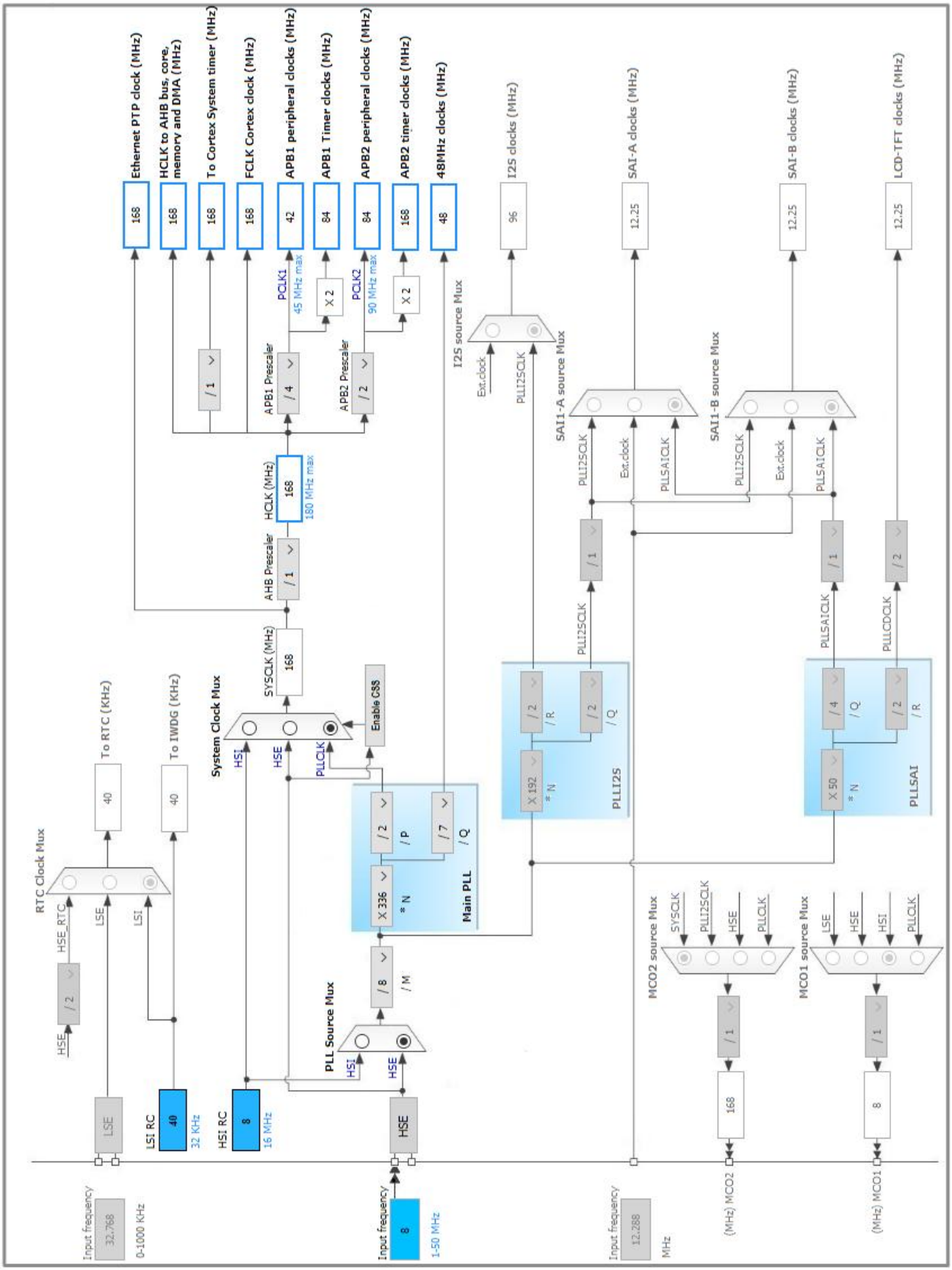
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
93	PG8 *	I/O	GPIO_Output	E0-STEP
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	TIM8_CH1	FAN-2
97	PC7	I/O	TIM3_CH2	FAN-2-IN
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	SDIO_D1	
100	PA8 **	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9 **	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 **	I/O	USB_OTG_FS_ID	USB_ID
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
111	PC10	I/O	SDIO_D2	
112	PC11	I/O	SDIO_D3	
113	PC12	I/O	SDIO_CK	
114	PD0	I/O	CAN1_RX	
115	PD1	I/O	CAN1_TX	
116	PD2	I/O	SDIO_CMD	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDD	Power		
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
128	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
130	VSS	Power		
131	VDD	Power		
135	PB5	I/O	SPI1_MOSI	
136	PB6	I/O	I2C1_SCL	
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
140	PB9	I/O	I2C1_SDA	
141	PE0 *	I/O	GPIO_Output	E1-STEP
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC3

mode: IN9

mode: IN14

mode: IN15

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 14 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. CAN1

mode: Mode

5.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**380.95238095238096 ***
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	**1142 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.3. CRC

mode: Activated

5.4. ETH

Mode: RMII

5.4.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

5.4.2. Advanced Parameters:

External PHY Configuration:

PHY Address Name	DP83848_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY status register Offset	**0x10 ***
MII Interrupt Control Register	**0x11 ***
MII Interrupt Status and Misc. Control Register	**0x12 ***
PHY Link mask	**0x0001 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***
PHY Enable interrupts	**0x0002 ***
PHY Enable output interrupt events	**0x0001 ***
Enable Interrupt on change of link status	**0x0020 ***
HY link status interrupt mask	**0x2000 ***

5.5. I2C1

I2C: I2C

5.5.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

5.7. RNG

mode: Activated

5.8. SDIO

Mode: SD 4 bits Wide bus

5.8.1. Parameter Settings:

SDIO parameters:	
SDIOCLK clock divide factor	0

5.9. SPI1

Mode: Full-Duplex Master

5.9.1. Parameter Settings:

Basic Parameters:	
Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	2
Baud Rate	**42.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSS Signal Type	Software

5.10. SYS

Debug: Serial Wire

Timebase Source: TIM1

5.11. TIM2

Clock Source : Internal Clock

Channel3: Input Capture direct mode

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.12. TIM3

Clock Source : Internal Clock

Channel2: Input Capture direct mode

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 2:

Polarity Selection	Rising Edge

IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.13. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel3: PWM Generation CH3N

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CHN Polarity	High

CHN Idle State	Reset

5.14. UART7

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.15. USART2

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.16. USB_OTG_FS

Mode: Device_Only

5.16.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

5.17. FATFS

mode: SD Card

5.17.1. Set Defines:

Version:

FATFS version	R0.11

Function Parameters:

FS_TINY (Tiny mode)	Disabled
FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FORWARD (Forward function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FASTSEEK (Fast seek function)	Enabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1 (Windows)
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled

USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.17.2. IPs instances:

SDIO/SDMMC:

SDIO instance	SDIO

5.18. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

5.18.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	**3: All messages and internal debug messages are shown ***

Class Parameters:

USBD_CDC_INTERVAL (Number of micro-frames interval)	1000

5.18.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155

LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC3	PF3	ADC3_IN9	Analog mode	No pull-up and no pull-down	n/a	THERMISTOR-3
	PF4	ADC3_IN14	Analog mode	No pull-up and no pull-down	n/a	THERMISTOR-1
	PF5	ADC3_IN15	Analog mode	No pull-up and no pull-down	n/a	THERMISTOR-2
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_REF_CK [LAN8742A-CZ-TR_REFCLK0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	FAN-2-IN
TIM8	PB15	TIM8_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	FAN-1
	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	FAN-2
UART7	PF6	UART7_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PF7	UART7_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART2	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD5	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
Single Mapped Signals	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	STLK_RX [STM32F103CBT6_PA3]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_ID
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	User Blue Button [B1]
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI-SS-1
	PF11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1-DIR
	PF12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENDSTOP Y-MIN
	PF13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENDSTOP Y-MAX
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Z-ENABLE
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI-SS-2
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Y-ENABLE
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	X-ENABLE
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1-ENABLE
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	X-STEP
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Z-STEP
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	X-DIR
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Z-DIR
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Y-STEP
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Y-DIR
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0-Enable
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0-DIR
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BED_Heater
	PD12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENDSTOP Z-MIN
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENDSTOP Z-MAX
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1-Heater
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0-Heater
	PG4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENDSTOP X-MIN
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ENDSTOP X-MAX
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E0-STEP

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	E1-STEP

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
USB On The Go FS global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
CAN1 TX interrupts	unused		
CAN1 RX0 interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
SDIO global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
HASH and RNG global interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	024030_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Salamander
Project Folder	F:\git_repositories\myrepos\Salamander\firmware\Salamander
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.13.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes