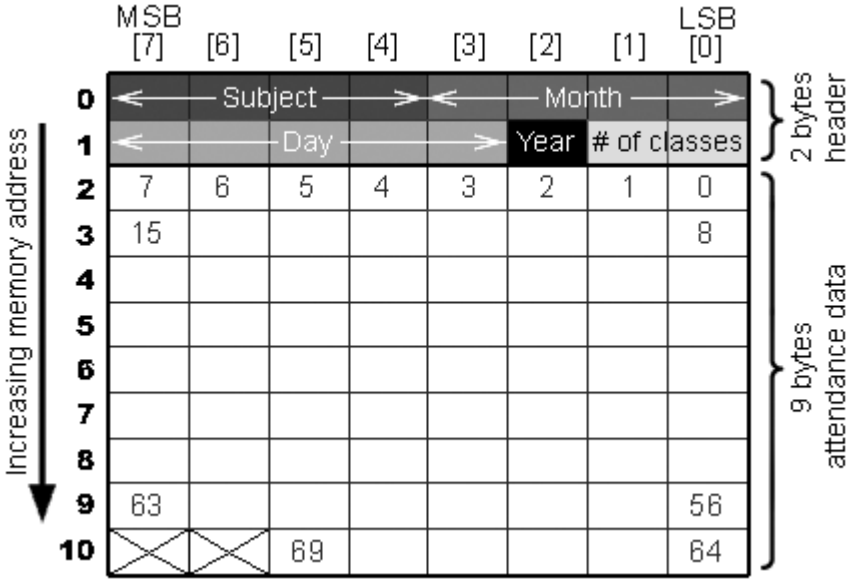
Digital Attendance Recorder (D.A.R)

Memory and Protocol Specifications

Memory map

- 512-bytes of EEPROM is available on chip
- Every class requires 11-bytes
- 512 / 11 = **46 classes** + 6-bytes to spare
- 46 classes are more than two weeks
- Every field has MSB on the left side
- Field values correspond to original values according to an index starting from 0 (see table 1)
- Note carefully the orientation of attendance bits.
- 1 last byte in EEPROM keeps track of number of classes currently stored in the memory



Serial Port data communication protocol b/w DAR and PC

Settings:

Baud rate	9600 bps
Start bit	1
Data bits	8
Parity	none
Stop bit	1

Steps:

1. [PC] "SEND" → [DAR]
   PC requests DAR to send the stored data.
2. [DAR] "YES" or "NO" → [PC]
3. If "NO" then PC program terminates.
4. If "YES" then PC waits for DAR to send the complete burst of data.
5. DAR first sends a byte which contains the "number of classes" currently stored in it. It means ("number of classes" x 11) bytes will be sent towards PC.
6. DAR then sends the bytes in the order of increasing addresses as shown in fig.1
7. After every 11th byte, data for a new class begins.
8. [DAR] "FINISH" → PC
   After all the classes, DAR signals PC to terminate the connection.
9. PC software must then manipulate these bytes to retrieve human readable information from it and then save it to a file or database for permanent storage.

2-Byte Header										9-Byte Attendance	
Subject		Month		Day		Year		# of Classes		Attendance	
											Bit number
SSD	0000	Jan	0000	1	00000	2007	0	1	00	Roll#01	0
Opto	0001	Feb	0001	2	00001	2008	1	2	01	Roll#02	1
VLSI	0010	Mar	0010	3	00010			3	10	Roll#03	2
LCS	0011	Apr	0011	4	00011			4	11	Roll#04	3
CS-2	0100	May	0100	5	00100					Roll#05	4
DSP	0101	Jun	0101	6	00101					……	……
MPAL	0110	July	0110	7	00110					……	……
CCN	0111	Aug	0111	……	……					……	……
NM	1000	Sep	1000	……	……					Roll#69	68
		Oct	1001	……	……					Roll#70	69
		Nov	1010	30	11101					*Not used*	*70*
		Dec	1011	31	11110					*Not used*	*71*

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