Study on 32 bit RISC-V CPU core using Open ROAD Flow Scripts

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***Abstract*— This works presents the theoretical study experience of 32-bit RISC-V CPU core design using Open road flow. Two stage pipeline design considered for analysis purpose. In Open ROAD Flow Scripts (ORFS) is an automated digital design allows the designer to work from Register Transfer Level(RTL) to GDSII flow using open-source tools. Discussed the advantages and challenges of OFRS during my study.**

Keywords—RISC-V Core, ORFS, RTL-GDS-II.

I. INTRODUCTION

Open-source software was used to build the entire RTL-to-GDS flow known as open ROAD Flow[1]. The goal of the ORFS is to develop digital circuits in 24 hours using automated processes without a person in the loop. The main aim of OpenROAD is democratization of hardware design", by reducing cost, expertise, schedule and risk barriers that confront system designers today. These include (i) enabling pervasive machine learning within and around design tools and flows, (ii) parallel search and optimization to take advantage of cloud resources, (iii) problem partitioning and decomposition to decrease solution latency, and (iv) layout generation methodologies that offer "freedoms from choice" without disproportionately sacrificing design quality.

II. OFRS DESIGN FLOW

The OpenROAD ("Foundations and Realization of Open, Accessible Design") project [2] was launched in June 2018 as part of the DARPA IDEA program The main objective of OpenROAD is to lower the financial, technical, and unpredictable hurdles that prevent system designers from implementing hardware in cutting-edge technologies.

To setup the OpenROAD Flow the system must consists 1 CPU core and 4GB RAM as minimum requirement. Installation steps are mentioned for different operating systems. The layout generation tool chain for Open ROAD consists of a collection of open-source programme that attempt to produce tape out-ready GDSII[3] files from RTL Verilog, constraints (.sdc), liberty (.lib), and technology (.lef) files. The GUI of OpenROAD is is a powerful visualization, analysis, and debugging tool with a customizable Tcl interface. GUI views for various flow stages including post-routed timing, placement congestion, and CTS.

The OpenROAD application is PDK independent. However, it has been tested and validated with specific PDKs likes of skywater130nm, GF180, ASAP7,Nandgate45nm.

III. ANAYZING RISC-V USING OFRS

To understand the overall flow of OFRS, A 32-bit RISC-V CPU considered which is a design example provided in OpenROAD flow. The installation of OpenROAD in UBUNTU is required different packages which encounters lot of challenges for the designer especially non Linux users.The next step in to configure the core design file for specific PDK followed by constraints file(.sdc) for specific for technology is typical task then the running the Automated RTL-to-GDS Flow. The entire autonomous flow, from synthesis to the generation of the final.gds file, is carried out by the OpenROAD programme without the need for human involvement utilizing Tcl scripts that use open-sourced tools. In my future work i will try to evaluate the tool compatibility also its stability and its optimization capability.Also at finally i need to check how design files are compatible with actual fabrication process.

IV. CONCLUSIONS AND RECOMMENDATIONS

Overall, the idea of promoting the Opensource tool to design design circuits using OpenROAD Flow Scripts will boost the Academics who cannot invest huge amount money in commercial tools as well as its fabrication. It allows the academics and digital designer to explore different architectures in real silicon. However we need to explore more on stability and its design results of opensource tools compared with commercial tools in the market.

not label axes with a ratio of quantities and units. For example, write "Temperature (K)", not "Temperature/K".

ACKNOWLEDGMENT

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