RTL Design to Synthesis 130nm Process

**ASIC Design Flow - An Overview**

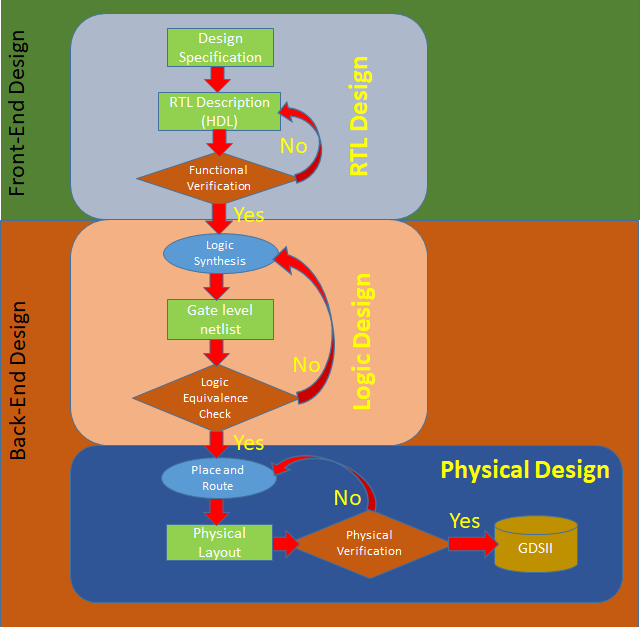
In this post, ASIC (Application Specific Integrated Circuit) Design flow has been explained. The very first step of ASIC flow is design specification, which comes from the customer end. Where customer writes down the specification of the chip basically the functionality which he wants to develop in a chip.  The whole design process is going through various design cycles and it generally takes 6 to 24 months to complete the design depending on the complexity inside the chip.

The complete ASIC design process can be divided into two parts.

1. ***Front End Design***
2. ***Back End Design***

**Front End Design:**

Front end design process starts with the specification received from the customer end. RTL (Register Transfer Level) design engineer converts the specification into an RTL code using the HDL (Hardware Description Language) generally either in Verilog or VHDL. Once the RTL code is written, RTL designer simulates the code in RTL Simulator and check the functionality of the design. Once the functionality of code is correct and verified by the verification engineers and if there is no bug found, This RTL code is taking to the next stage which is logic synthesis. This flow starts with RTL coding and ends with GDS (Graphic Data Stream) file which is the final output of back end design, so this complete flow is also known as RTL to GDS (RTL2GDS) flow. A Simple flow diagram has been described here.



**Back End Design:**

RTL code received from the front end engineer is technology independent, now the next step is Logic synthesis.

***Logic Synthesis:***  In logic synthesis, a high-level description of the design (RTL Code) is converted into an optimized gate-level representation of a given standard cell library and certain design constraints. Now the code is in the form of a gate-level netlist of a particular standard cell library. LEC (Logic Equivalence Check is must in this stage to make sure that there are not logical changes occurred during the synthesis. During logical Synthesis, we also get various reports on timing power and area of design. We also get an SDC (Synopsys Design Constraint) file in this stage which is used in the next stage. DFT (Design For Testability) Insertion is also done in this stage to verify the chip after fabrication is done.

***Place and Route (PnR):***Gate level netlist after DFT Insertion and SDC file is taken as input for the PnR and based on standard cells library, PnR starts. The goal of PnR stage is to place all the standard cells, Macros and I/O pads with minimal area, with minimal delay and Route them together in such a way that there is no DRC (Design Rule Check) error. The final output of this stage is the layout of design in the form of GDSII file which is defacto standard of layout file in the industry.

PnR stage is a very challenging stage with large design cycle time depending on the complexity of a chip. This stage is further divided into various sub-stages. The main stages are starting from Design Import, followed by FloorPlan, Power Plan, Placement, CTS (Clock Tree Synthesis), and Routing.

After routing we expect the design has met the timing and all DRC, But in the modern chip, it's not easy to close the design in this stage. So Further we go to Signoff stage.

***Signoff:*** If there are some timing violations in the post route design, we have a further stage called ECO (Engineering Change Order) where we can fix the timing violations. Apart from timing violation, there may be issues like IR Drop, DRC Violations all these are fixed in this stage and a final layout file free from all the violation is streamed out in GDSII format. This process is known as tapeout in ASIC flow. This is the final design stage and the gdsII file is sent to fabrication lab for the fabrication of chip.

