Active-Matrix GaN Micro Light-Emitting Diode Display With Unprecedented Brightness

Johannes Herrnsdorf, Jonathan J. D. McKendry, *Member, IEEE*, Shuailong Zhang, Enyuan Xie, Ricardo Ferreira, David Massoubre, Ahmad Mahmood Zuhdi, Robert K. Henderson, Ian Underwood, Scott Watson, Anthony E. Kelly, Erdan Gu, and Martin D. Dawson, *Fellow, IEEE*

***Abstract*— Displays based on microsized gallium nitride light-emitting diodes possess extraordinary brightness. It is demonstrated here both theoretically and experimentally that the layout of the n-contact in these devices is important for the best device performance. We highlight, in particular, the significance of a nonthermal increase of differential resistance upon multipixel operation. These findings underpin the realization of a blue microdisplay with a luminance of 10^6 cd/m^2.**

***Index Terms*— CMOS integrated circuits, displays, flip-chip devices, integrated optoelectronics, light-emitting diodes (LEDs).**

I. Introduction

GALLIUM nitride-based light-emitting diodes (GaN LEDs) not only hold great promise for lighting but also can be fabricated into arrays of microscale LEDs integrated with CMOS control electronics [1], [2]. Such devices can serve as miniature displays [3], multisite excitation sources [4], and manipulation tools [5], [6] in the life sciences. LEDs with a size of 100×100 μm^2 or less (here referred to as micro-LEDs) can be driven at significantly higher current and optical power density than conventional large-area LEDs [7]. Consequently, they are promising for applications requiring, or benefitting from, high intensity, e.g., displays in high brightness environments (sunlight), projection [8], optoelectronic tweezers [5], [6], or pumping of organic lasers [9]. A further consequence of high current density operation is a reduction of the carrier lifetime [10], making micro-LEDs attractive candidates for high-speed data transmission using visible light [11]. CMOS control of multiple micro-LEDs has the potential to enhance the capabilities of such a communications system [12].

In recent years, matrix-addressed and individually addressed CMOS-controlled GaN microdisplays with a luminance on the order of 10^4 cd/m^2 have been demonstrated [3], [13]. This is already one order of magnitude higher than alternative technologies, such as organic LED displays [3]. A single micropixel can provide an optical power density >150 W/cm^2 yielding luminance in excess of 10^7 cd/m^2. However, scaling this single-pixel performance up to an entire high-brightness display is very challenging. The work reported here is based on CMOS driver electronics and LED arrays specifically designed to tackle this challenge.

We investigate the limitations and issues in high current density operation of flip-chip micro-LED arrays bump-bonded to a CMOS driver chip where several pixels are switched ON at the same time. It is found that in arrays with high LED fill-factor (i.e., the ratio of light-emitting area to total pixel area) a brightness drop occurs which we refer to as the multipixel droop. In the previous study, high current density operation in micro-LEDs was linked to improved thermal management of the small pixels [7]. Therefore, a drop in brightness due to device heating is expected when operating high fill-factor arrays. Interestingly, it is found here that, while thermal issues play a role, a severe limitation for multipixel operation is a nonthermal increase of differential resistance, which may be linked to current crowding. Current crowding will always cause additional device heating, but we demonstrate that the multipixel droop occurs in pulsed and moderate current continuous wave operating regimes where such heating is insignificant. It is, therefore, an electrical crosstalk that occurs in both pulsed and dc operation. This effect can be mitigated by careful layout of the n-contact, possibly sacrificing LED fill-factor. The importance of the n-contact layout has recently been highlighted in [14]

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J. Herrnsdorf, J. J. D. McKendry, E. Xie, R. Ferreira, E. Gu, and M. D. Dawson are with the Institute of Photonics, University of Strathclyde, Glasgow G4 0NW, U.K. (e-mail: johannes.herrnsdorf@strath.ac.uk; jonathan.mckendry@strath.ac.uk; enyuan.xie@strath.ac.uk; ricardo.ferreira@strath.ac.uk; erdan.gu@strath.ac.uk; m.dawson@strath.ac.uk).

S. Zhang is with the Institute of Photonics, University of Strathclyde, Glasgow G4 0NW, U.K., and also with the School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K. (e-mail: shuailong.zhang@strath.ac.uk).

D. Massoubre was with the Institute of Photonics, University of Strathclyde, Glasgow G4 0NW, U.K. He is now with the Queensland Micro- and Nanotechnology Centre, Griffith University, Nathan QLD 4111, Australia (e-mail: d.massoubre@griffith.edu.au).

A. M. Zuhdi, R. K. Henderson, and I. Underwood are with the Joint Research Institute for Integrated Systems, Institute for Micro and Nano Systems, School of Engineering, University of Edinburgh, Edinburgh EH93JL, U.K. (e-mail: a.w.mahmood-zuhdi@ed.ac.uk; robert.henderson@ed.ac.uk; ian.underwood@ed.ac.uk).

S. Watson and A. E. Kelly are with the School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K. (e-mail: s.watson.2@research.gla.ac.uk; anthony.kelly@glasgow.ac.uk).

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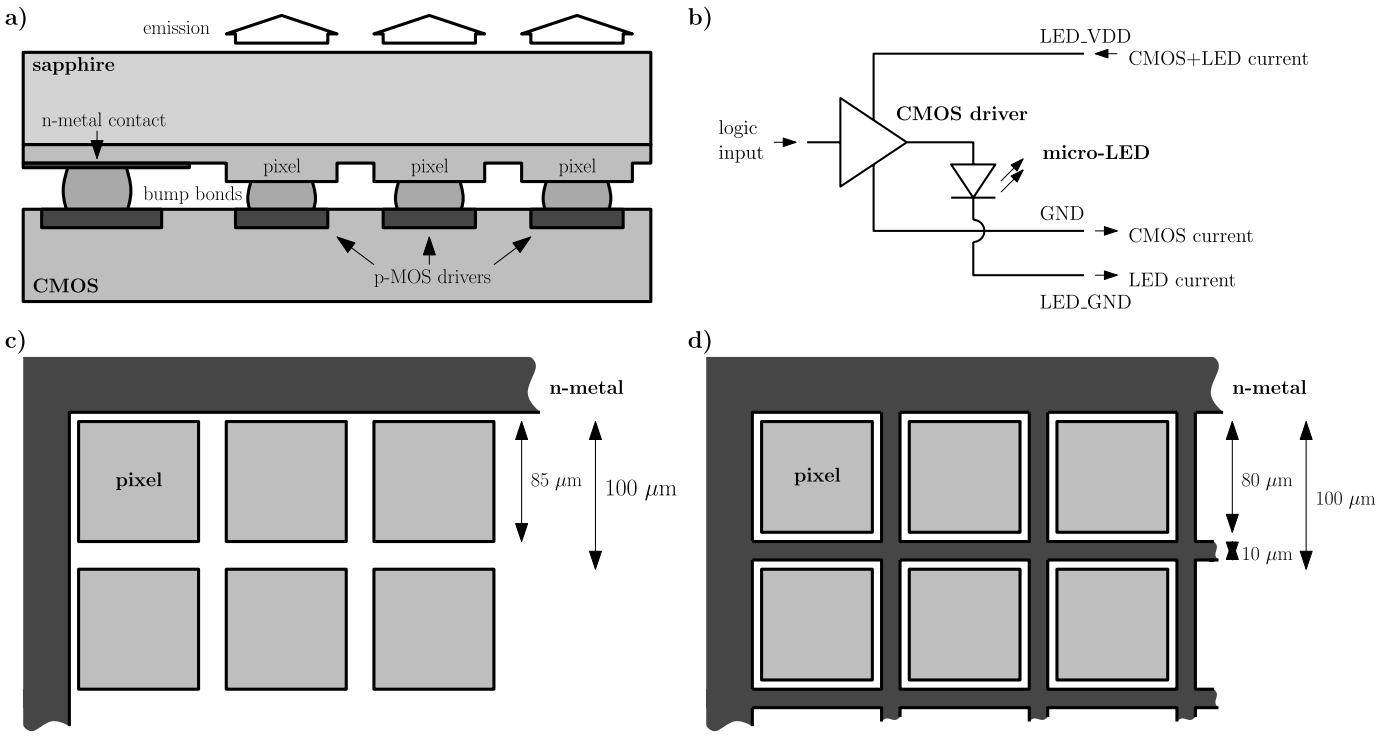

Fig. 1. Schematic of the devices for experimental investigation. (a) Cross section showing the integration of the LED arrays with the CMOS-chip. (b) Electric circuit. (c) Layout A. (d) Layout B.

and here we present a more in-depth study of the underlying physics and performance limitations. As a result of these investigations, we demonstrate a CMOS-integrated blue microdisplay with a display luminance of 10^6 cd/m^2 (12 W/cm^2), exceeding current commercial displays by a factor of 10^3.

II. Experimental Results

A range of factors influences the brightness achievable with micro-LED displays, including the quality of the epitaxial material, the layout of LEDs and CMOS, as well as thermal management. In this paper, we focus on the LED and CMOS layout. The epitaxial structures used are commercial sapphire-grown InGaN/GaN multiquantum-well structures emitting at 450 nm. The LEDs were fabricated as reported earlier [1] using Pd as the p-contact metal [15]. To the best of our knowledge, the epitaxial layer thicknesses and electrical properties are similar to those in Section III. All results reported here were obtained from a single wafer (and, where possible, from the same die) in order to allow the best comparison.

A. CMOS Layout

Each micro-LED array was bump-bonded directly on top of a CMOS driver chip fabricated in a 0.35-μm process containing a pitch-matched array of drive circuits [Fig. 1(a)]. These were designed with the aim of driving the highest possible current per pixel while also allowing switching on a nanosecond timescale. To enable LED drive voltages beyond the operating voltage of the CMOS, the driver chip was implemented with three voltage terminals, LED_VDD, GND, and LED_GND, which are shown in Fig. 1(b). LED operating voltages up to 8.3 V are possible by supplying a CMOS compatible voltage of 3.3 V (with respect to GND) on the LED_VDD terminal and -5 V on the LED_GND terminal. Note that the CMOS driver reported here is the latest development in a series of driver chips specifically designed for driving micro-LED pixel arrays [1], [10], [16]–[18]. In this section, we compare the present driver (generation 2) to the previous one (generation 1) [10], [18]. We highlight the changes that were made to enable high-power display operation. A synopsis of both generations is given in Table I.

TABLE I
Comparison of the Generation 1 and Generation 2 CMOS Driver

	Generation 1	Generation 2
Array dimensions	16×16	10×40
Pixel pitch	100 μm	100 μm
Bond pad size	50×50 μm^2	100×100 μm^2
Number of power rails connected to one pixel	2	4
Power rail width LED_VDD	5.6 μm	40 μm 33 μm
Power rail width GND	4 μm	25 μm 17 μm
Power rail resistance LED_VDD	0.71 Ω	0.21 Ω 0.17 Ω
Power rail resistance GND	1 Ω	0.40 Ω 0.28 Ω
DC Driving current per pixel	200 mA	400 mA
Electronics underneath bond pad	No	Yes
Fraction of pixel area used by drive transistors	36 %	90 %

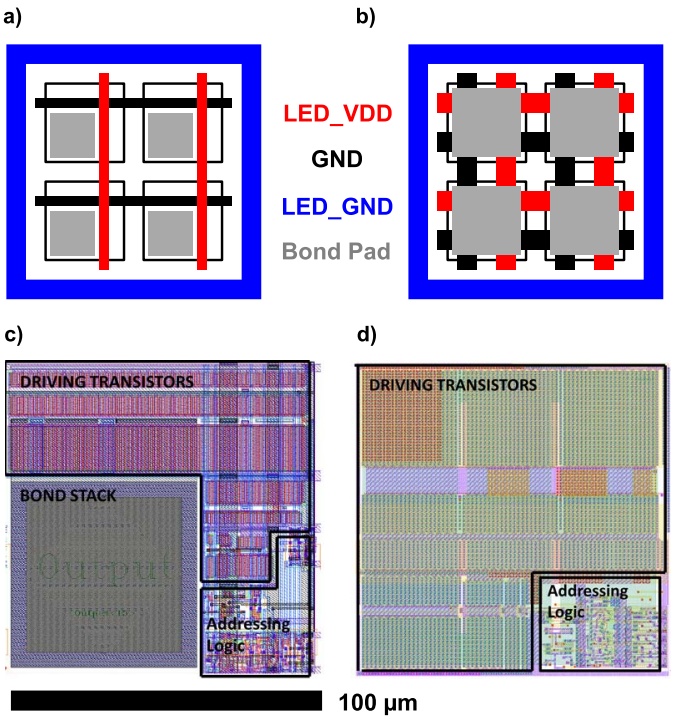

Fig. 2. Schematic of the design changes between (a) and (c) generation 1 CMOS driver and (b) and (d) generation 2 CMOS driver. (a) and (b) Power rail configuration. (c) and (d) Layout of an individual pixel. Note that in (d), the bond stack covers the entire pixel.

The voltage uniformity across the pixel array was improved by reducing the voltage drop along the power rails of the chip due to their resistance. This was minimized by making the power rails supplying each pixel as wide as possible. Furthermore, they were laid out in a grid arrangement, which compares with a linear arrangement in generation 1 [Fig. 2(a) and (b)]. Values for the rail width and resistance in both generations are given in Table I. Both the LED_VDD and the GND rails have a factor 3 and 4 lower rail resistance in generation 2 compared with generation 1. Furthermore, the power rails are each routed through ten dedicated bonding pads.

The integration by bump-bonding requires each pixel to have a bond pad. An important difference between the two CMOS driver generations is that in generation 1, the bond pad area was prohibited to active circuitry in order to avoid fusion with the lower level metals during the bump-bonding process, thus short-circuiting the circuitry underneath [16]. In generation 2, the bond pad was placed on top of the drive circuit so that both could utilize the full pixel area, as shown in Fig. 2(d). This was enabled by making the top metal layer thick and mechanically strong so that it can withstand the forces applied during bonding. The resulting area increase of the driving transistors is clearly visible in Fig. 2(c) and (d). In generation 2, 90% of the pixel area was occupied by the driving transistors, which compares with 36% for generation 1. This increase of transistor size enhances the current handling capability of each driver element.

As a result of these improvements, the generation 2 driver can handle up to 400-mA dc per pixel, which is twice the value of the generation 1 device. A single pixel current of ~300 mA (limited by the LED) has been realized, and a 10×10 section of the array (1×1 mm^2 area) has been operated at a total current of 900 mA.

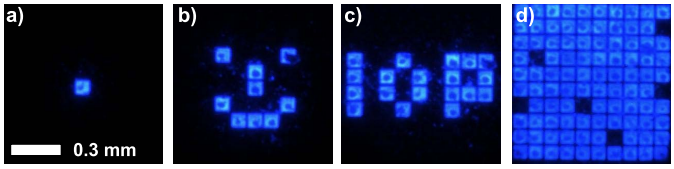

Fig. 3. Patterns displayed on device B at 10^6 cd/m^2 (~7.7 mA/pixel). (a) Single pixel. (b) Smiley. (c) Letters IOP. (d) Full array with a few defects. The voltage was 3.6 V and the camera settings were kept identical for all micrographs.

B. LED Layout

We illustrate the multipixel droop on the basis of two 10×10 LED arrays, labeled A and B. These correspond to Fig. 1(c) and (d), respectively. Both were implemented in flip-chip format on the same wafer die and bonded to the same CMOS chip allowing optimal comparison. Note that six other layouts have been fabricated as well and confirm the trends outlined here. These further results are not shown here for brevity and clarity.

Array A is similar to previously reported micro-displays [3], [18] and serves as a reference. It consists of 85×85 μm^2 mesas at 100-μm pitch, forming a 10×10 array. The n-contact metal surrounds the array and there is no n-metal between the mesas. It is, therefore, similar to devices A1 and A2 in Section III.

Array B is a 10×10 array of 80×80 μm^2 mesas at 100-μm pitch. In this case, the surrounding n-metal contact is supplemented by 10-μm wide n-metal tracks running through the gaps between each mesa. It is, therefore, similar to device B in Section III.

Both array types are part of a larger 10×40 array on a single die, which was bump-bonded to a CMOS chip, as shown in Fig. 1(a). Therefore, both device types have undergone exactly the same fabrication steps at the same time. Fig. 3 shows micrographs of representative displayed patterns. Even though the bump-bonding causes a dark region in the center of the pixels, the optical output power of the individual pixels differs minimally from that prior to bonding the device measured by needle probing. At an operating voltage of 3.3 V, the individual pixels draw a uniform current with <10% pixel-to-pixel variation. This is particularly relevant because in Section II-C it will be shown that the multipixel droop manifests in the current–voltage (I–V) characteristics.

C. Limitation of Display Luminance

At a given LED voltage and resulting LED current, the optical power was measured using a silicon photodetector, which was placed at 3-cm distance from the device. The collection efficiency in this configuration was estimated by assuming a Lambertian emission pattern [9] and the conversion of optical power to luminous intensity was also based on the assumption of a Lambertian emission pattern. Note that the optical power

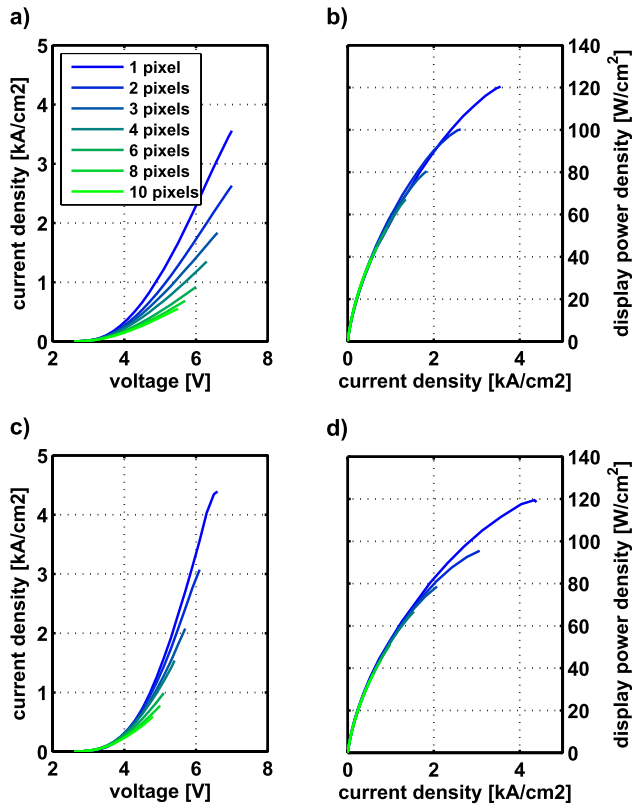

Fig. 4. (a) I–V and (b) L–I of layout A. (c) I–V and (d) L–I of layout B.

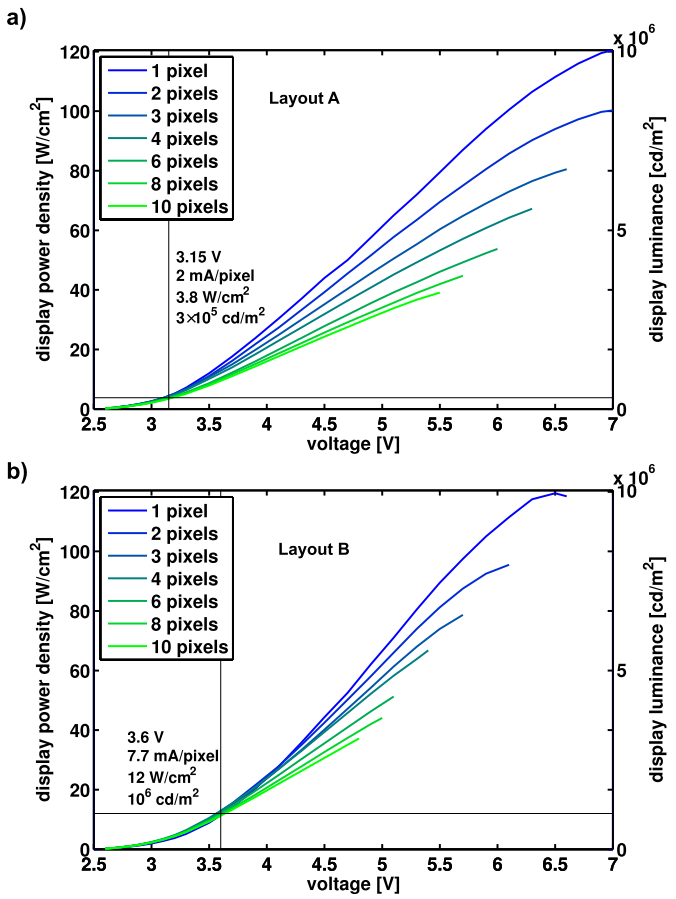

Fig. 5. L–V characteristics of (a) layout A and (b) layout B. Left y-axis: optical output power density normalized to the pixel area ($100 \times 100\ \mu\text{m}^2$). Right y-axis: equivalent display luminance for an emission wavelength of 450 nm and a Lambertian emission profile.

and luminous intensity are normalized to the pixel area as a direct measure of display brightness. The current, on the other hand, is normalized to the active area because in the light of earlier investigations [7], [10], [19] this allows the best comparison between the slightly differently sized mesas of layouts A and B.

Earlier studies investigated the dependence of the (I–V) and luminance–current (L–I) characteristics of GaN LEDs as a function of LED size [7] and showed significant variation. Similarly, the I–V and L–I characteristics of a densely packed LED array both vary with the number of pixels that are switched ON, as shown in Fig. 4. Interestingly, the L–I curves are almost identical and the major difference is due to the slightly different LED fill-factor of the two devices. This is discussed in Section II-D. However, clear differences can be seen in the I–V curves.

In both layouts, the I–V shows a higher resistance per pixel the more pixels are switched ON. This multipixel droop depends on both the pixel number and the operating voltage. Close to turn ON, the I–V is independent of the pixel number. However, at voltages that significantly exceed turn ON, a large number of pixels will draw a smaller current density than a small number of pixels, i.e., there is a crosstalk between the pixels that reduces the current per pixel.

By comparing Fig. 4(a) and (c), we see that the multipixel droop is less severe in layout B, indicating that a suitable layout of the n-contact can alleviate the multipixel droop. This finding is well-aligned with an observation in [20] that the n-contact layout is generally important for high performance of lateral-injection LEDs.

The impact of this phenomenon on the display performance shows up in the luminance–voltage (L–V) characteristics shown in Fig. 5. At low voltages, the L–V curves overlap but at higher values they fan-out significantly. This means that above a certain drive voltage the brightness changes upon switching ON and OFF pixels are too large for useful display operation. As indicated in Fig. 5, this operating point for maximal brightness has approximately three times higher optical output power in device B than in device A despite the slightly lower LED fill-factor.

Patterns with larger pixel numbers are compared in Fig. 6 at a constant operating voltage, showing clear multipixel droop. Layout B has generally higher brightness and the relative droop is less severe (54% for layout A and 45% for layout B when switching on a 10×10 array). When the full array is switched ON, the power density has dropped to 8.8 W/cm^2. Notably, by raising the voltage from 3.6 to 3.8 V, the brightness of the full array was raised to 11.5 W/cm^2, i.e., only moderate adjustments to the operating voltage are needed to maintain good uniformity.

D. Thermal Effects

The influence of device heating on the multipixel droop can be assessed indirectly from the L–I characteristics and

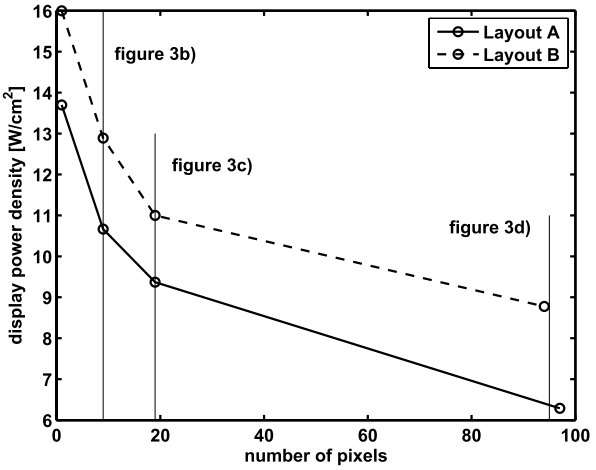

Fig. 6. Optical output power of the display at a constant drive voltage of 3.6 V as a function of pixel number up to a large scale. Note that the power is normalized to the pixel area (100 × 100 μm^2) and not to the active area (85 × 85 μm^2 for device A and 80 × 80 μm^2 for device B). Vertical lines: pixel numbers corresponding to the patterns are shown in Fig. 3.

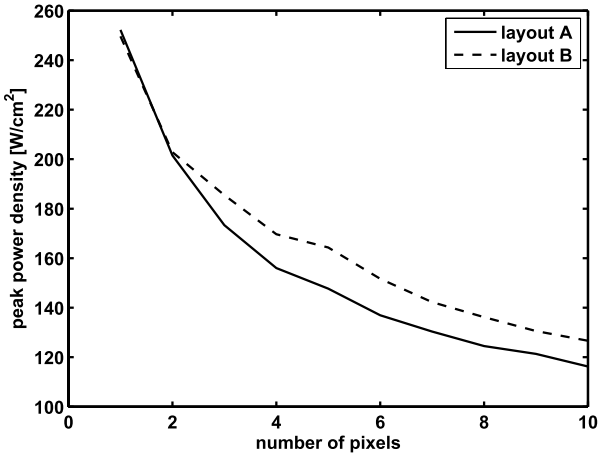

Fig. 7. Peak optical power normalized to pixel area of 10-ns pulses at 8.3 V and 100-Hz repetition rate as a function of pixel number.

directly by thermal imaging. At high currents, heating causes thermal rollover of the optical output power. It can be noted though that rollover occurs at lower current densities, the more pixels are switched ON. This means that cumulative heating has an impact on the device performance and will need to be addressed when pushing display brightness toward and beyond the 10^7 cd/m^2 mark.

Interestingly though, we find that the observed multipixel droop is not entirely of a thermal nature. A first evidence for this is given by nanosecond pulsed operation at low duty cycle, where virtually no cumulative heating occurs. Fig. 7 shows the optical output power when operating with pulses of 10-ns duration (achieved by switching the CMOS transistors with an external clock signal) at a duty cycle of 10^{-6}. In this configuration, no device heating will occur, yet a significant (factor 2) multipixel droop is observed. Note that layout B performs slightly better in pulsed operation, which is remarkable considering the different LED fill-factor.

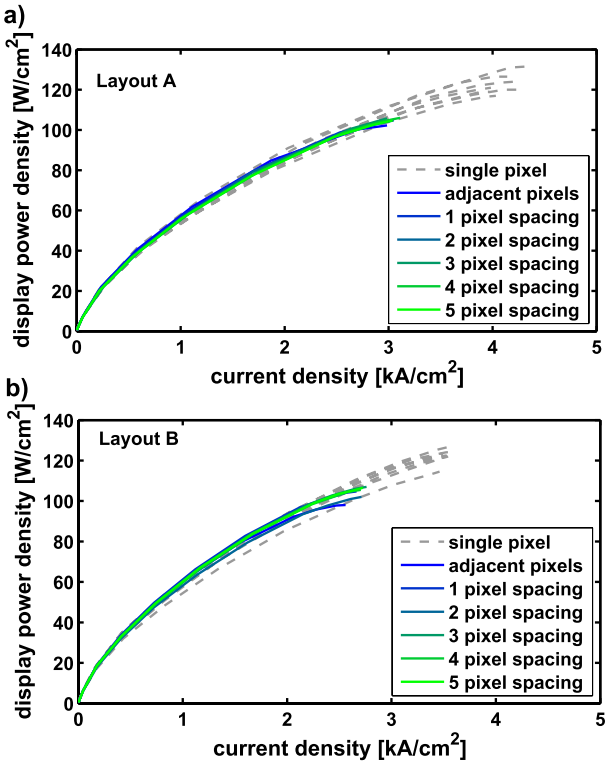

Fig. 8. L–I characteristics of two pixels at different relative position in (a) layout A and (b) layout B. Dashed gray curves: single pixel L–I characteristics of all the individual pixels involved in this measurement.

Further evidence is obtained in dc operation. Fig. 8 compares the L–I characteristics of two pixels switched ON simultaneously and the two pixels are either adjacent to each other or separated by some distance. When the two pixels are adjacent to each other, thermal rollover occurs at ∼75% of the current density at which the single pixels rollover. However, when the two operated pixels are several hundred micrometers apart, the thermal rollover is not changed. First of all, this indicates that heat is efficiently spread across the die. Notably though, this behavior is identical for both layouts. This indicates that the thermal property is not responsible for the different multipixel-droop behavior of the two layouts.

To gain better insight into the temperature distribution in the device, we used a thermal infrared camera. Fig. 9(a) presents the junction temperature of a single pixel as a function of current density (kept below rollover). There is no significant difference between layouts A and B. Device B has marginally lower temperatures due to the lower LED fill-factor. Note that the observed junction temperatures are lower than usually reported for GaN-based LEDs under similar driving conditions [21]. We attribute this to improved heat sinking via the bump bonds to the CMOS chip and the small size of the LED pixels.

An example of a thermal image of the device with two pixels switched ON is given in Fig. 9(b). In this case, the pixels have a temperature of ∼35 °C and the whole die is heated up to 32 °C. Here, the device was operated at a voltage

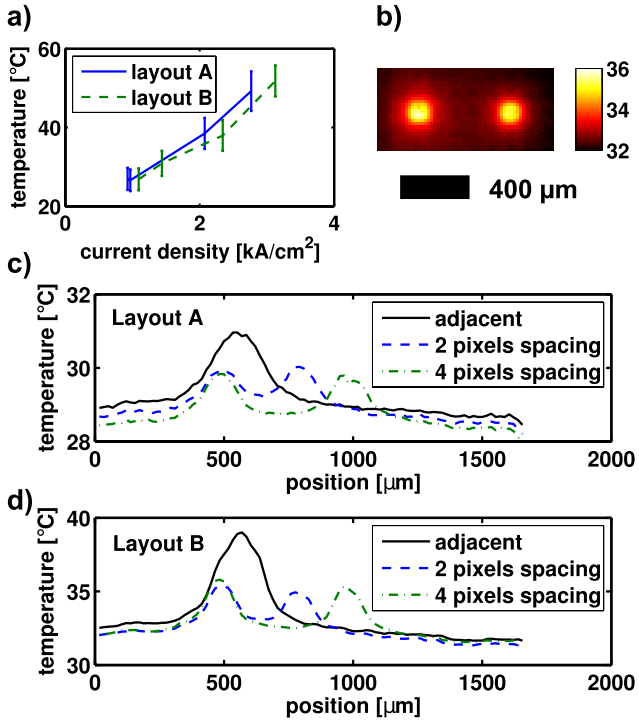

Fig. 9. Thermal performance analyzed by IR imaging. (a) Junction temperature for a single pixel. (b) Image of two pixels switched ON simultaneously (layout B, four pixels spacing). (c) and (d) Temperature profiles of two pixels with different spacing operated at 4.8 V for (c) layout A at 0.78 kA/cm^2 and (d) layout B at 1.28 kA/cm^2.

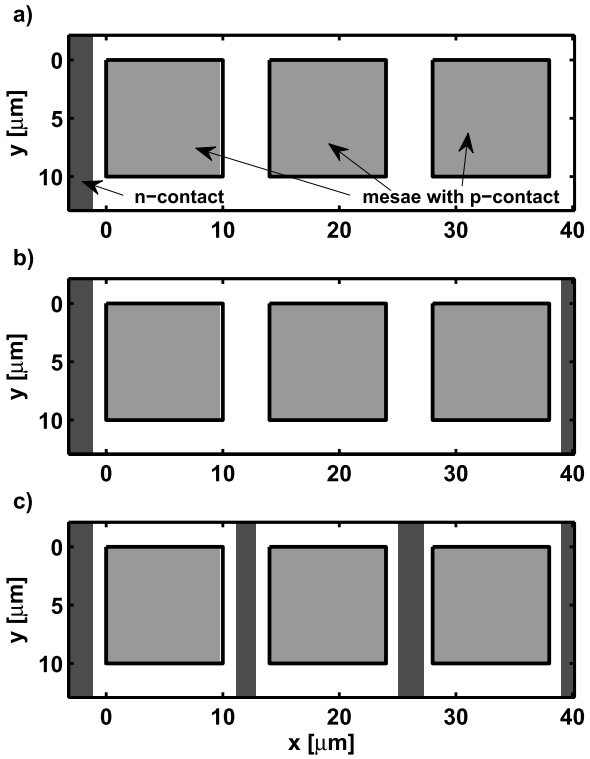

Fig. 10. Schematic of the modeled devices. (a) Layout A1. (b) Layout A2. (c) Layout B. Light gray: mesa area. Dark gray: area covered by n-metal.

of 4.8 V and a current density of 1.28 kA/cm^2, which is well below thermal rollover. For a better quantitative comparison, Fig. 9(c) and (d) shows the temperature profile along a cross section through the centers of both pixels for different pixel spacing. The voltage was kept constant at 4.8 V and, therefore, layout A operated at 60% of the current density of layout B and consequently it had a lower temperature. If the pixels are spaced apart by 100-μm separation or more, their temperature is independent of the pixel spacing. In this case, the mutual heating of the pixels is enabled by the uniform widespread heating across the whole die. Only for directly adjacent pixels, a rise in junction temperature can be seen by thermal imaging. Even then, the temperature of the whole die is the same as for any other pixel spacing.

III. Theoretical Investigation of the Current Distribution

The experimental results indicate that the current distribution within the n-layer of the devices is important. Therefore, the current density was calculated from a finite-difference model implemented in MATLAB [22], [23]. Here, thermal effects are neglected, highlighting the impact of the n-contact layout on the current distribution in the structure. The following material parameters were used:

$$n_n = 5 \times 10^{18}\ \text{cm}^{-3} \quad n_p = 10^{17}\ \text{cm}^{-3} \tag{1a}$$

$$\mu_n = 200\ \text{cm}^2/\text{Vs} \quad \mu_p = 1\ \text{cm}^2/\text{Vs} \tag{1b}$$

$$\rho_{c,n} = 10^{-5}\ \Omega\text{cm}^2 \quad \rho_{c,p} = 10^{-5}\ \Omega\text{cm}^2 \tag{1c}$$

where n_n and n_p are the electron and hole concentrations in the n- and p-doped regions, μ_n and μ_p are the corresponding carrier mobilities, and $\rho_{c,n}$ and $\rho_{c,p}$ are the contact resistivities of the metal contacts to the n- and p-doped semiconductor regions. The junction was described as an ideal diode with saturation current $j_{\text{sat}} = 10^{-9}$ A/cm^2, ideality factor $n = 5$, and room temperature Boltzmann factor $kT = 27$ meV.

Fig. 10 shows the schematic of the three modeled devices, labeled A1, A2, and B for easy comparison with the devices in Section II. All of them consist of three 10×10 μm^2 mesas with a mesa height of 1 μm and a total semiconductor thickness of 3 μm, of which 200 nm are p-doped and the rest n-doped GaN. These devices are smaller than the LEDs in the experimental section in order to reduce the computational effort. The difference between the devices is the layout of the n-contact. Layouts A1 and A2 have no n-contact in between the mesas, whereas layout B has a metal stripe between each mesa. Design A1 has a single n-contact on one side of the device. This is known to cause current crowding effects at high current densities [24], [25]. In layout A2, the pixel group has n-metal contacts on both sides, which is typical for high LED fill-factor arrays and provides good uniformity at low current densities [3]. Finally, design B has n-contacts surrounding each mesa individually.

We look first at the operation of a single pixel at a bias voltage of 4.5 V. Under these conditions, a relatively uniform (<10% variation) current density of ~700 A/cm^2 passes through the junction of the biased pixel. Fig. 11 maps the current density distribution along a cross section through

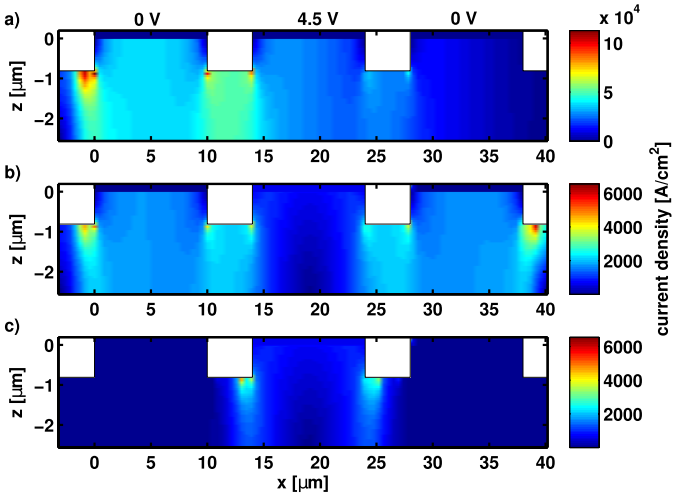

Fig. 11. Current density distribution in the devices shown in Fig. 10 when a voltage of 4.5 V is applied to the center pixel and the side pixels are left at 0 V. (a) Cross-sectional view at $y = 5$ μm through the device A1 shown in Fig. 10(a). (b) and (c) Correspond to layouts A2 [Fig. 10(b)] and B [Fig. 10(c)], respectively.

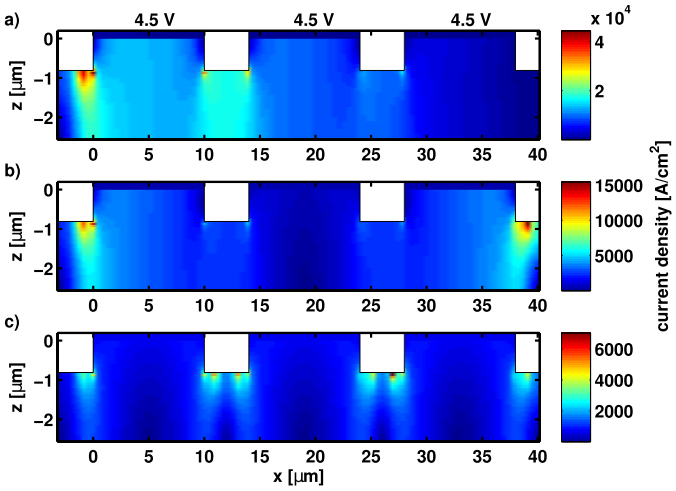

Fig. 12. Similar to Fig. 11, current density cross sections through the devices in Fig. 10. A bias voltage of 4.5 V is applied to all three pixels.

the device. It can be seen that the asymmetric n-layout (device A1) suffers from significant current crowding toward the single n-contact. In the symmetric layouts, the current injected into the center pixel is evenly distributed to the two closest n-contacts, giving similar peak current densities. Note also that in layouts A1 and A2 high lateral currents flow underneath pixels with 0 V bias. Even though there is no vertically injected current in these pixels, the current density in the n-layer is still large due to the current injected at adjacent pixels.

Fig. 12 shows the current density distribution when all pixels are operated simultaneously. It can be seen that current crowding effects at the mesa edges and n-contact edges are only minimized when each mesa is surrounded by its own n-contact regions [layout B, Figs. 10(c) and 12(c)]. Furthermore, the asymmetric n-contact [Fig. 12(a)] leads to current crowding toward the n-contact [24].

Section II-C demonstrates that the multipixel droop is an effect of increased parasitic differential resistance upon switching ON several pixels. It was shown in Section II-D that this differential resistance cannot solely be attributed to device heating and that the n-contact layout has an influence on this effect. The simulation confirms that a major difference between the layouts is the current density distribution. This suggests that there may be a link between current crowding and the multipixel droop. For example, the n-GaN conductivity may change nonthermally as a function of current density. This interpretation is in line with earlier observations that the drift velocity of electrons in semiconductors rolls over at high electric field strength [26], i.e., effectively the electron mobility μ_n decreases at high current density.

IV. Conclusion

High brightness CMOS-controlled microdisplays can be made on the basis of GaN flip-chip micro-LEDs. Limiting factors to the achievable luminance include the current handling capability of the control electronics, the current distribution within the LED structure and thermal management. In particular, it is demonstrated that careful LED design toward optimal current distribution in the n-GaN layer is crucial for obtaining the highest possible display luminance. These design considerations may have impact on the fill-factor, pixel size, and resolution. Furthermore, we show that in high-brightness dc and pulsed operation an electrical crosstalk occurs, which is caused by a nonthermal increase of differential resistance and may be linked to current crowding.

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Johannes Herrnsdorf received the Ph.D. degree in physics from the University of Strathclyde, Glasgow, U.K., in 2012.

He is involved in GaN micro-LEDs.

Jonathan J. D. McKendry (M'13) received the Ph.D. degree in physics from the University of Strathclyde, Glasgow, U.K., in 2011.

He is involved in GaN micro-LEDs.

Shuailong Zhang received the Ph.D. degree in physics from the University of Strathclyde, Glasgow, U.K., in 2015.

He is currently with the University of Glasgow, Glasgow.

Enyuan Xie received the Ph.D. degree in physics from the University of Strathclyde, Glasgow, U.K., in 2013.

He is involved in fabrication of GaN LEDs.

Ricardo Ferreira received the M.Sc. degree in engineering physics from the University of Aveiro, Aveiro, Portugal. He is currently pursuing the Ph.D. degree in visible light communications with the University of Strathclyde, Glasgow, U.K.

David Massoubre received the Ph.D. degree in physics from the University of Paris-Sud, Orsay, France, in 2006.

He was with the University of Strathclyde, Glasgow, U.K. He is currently with Griffith University, Nathan, QLD, Australia, where he is involved in SiC/Si for photonics and GaN devices.

Ahmad Mahmood Zuhdi received the M.Eng. degree in electrical and electronics engineering from the University of Edinburgh, Edinburgh, U.K., in 2008, where he is currently pursuing the Ph.D. degree in displays and sensors with feedback.

Robert K. Henderson received the Ph.D. degree from the University of Glasgow, Glasgow, U.K., in 1990.

He was with the Swiss Centre for Microelectronics, Neuchatel, U.K., VLSI Vision Ltd., Edinburgh, U.K., and the University of Edinburgh, Edinburgh. His current research interests include CMOS electronics.

Ian Underwood received the Ph.D. degree in physics from the University of Edinburgh, Edinburgh, U.K., in 1987.

He was involved in the development of liquid crystal on Si technology with the University of Edinburgh, and the University of Colorado, Boulder, CO, USA. He has been a Professor since 2004, and currently leads the Institute for Integrated Micro and Nano Systems.

Scott Watson received the B.Eng. degree in electronics with music from the University of Glasgow, Glasgow, U.K., where he is currently pursuing the Ph.D. degree in visible light communications.

Anthony E. Kelly received the Ph.D. degree from the University of Strathclyde, Glasgow, U.K., in 1999.

He was with the Corning Research Centre, U.K., and Amphotonix Ltd., U.K. He is currently a Senior Lecturer with the University of Glasgow, Glasgow. His current research interests include optical communications.

Erdan Gu received the Ph.D. degree in physics from the University of Aberdeen, Aberdeen, U.K., in 1992.

He was with the Cavendish Laboratory, Cambridge, U.K., Oxford Instruments plc, Abingdon, U.K., and the University of Strathclyde, Glasgow, U.K. He is currently an Associate Director with the Institute of Photonics.

Martin D. Dawson (M'85–SM'98–F'09) received the Ph.D. degree in physics from Imperial College London, London, U.K., in 1985.

He was with the University of North Texas, Denton, TX, USA, the University of Iowa City, Iowa, IA, USA, SLE Oxford, and the University of Strathclyde, Glasgow, where he is currently a Professor. He is also the Director of Research with the Institute of Photonics and the Fraunhofer Center for Applied Photonics.