

# Two input XOR gate using CMOS in 28nm

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**Abstract:** The purpose of article is to design and implement two input XOR gate in 28nm CMOS technology. Design implementation is performed by using Synopsys Custom tool. I have to analyse the behaviour of XOR gate using CMOS by generating output waveform.

## I. Introduction [2]

An XOR gate is a digital logic gate that gives a true (i.e. a HIGH or 1) output when the number of true inputs is odd. An XOR gate implements an exclusive OR, i.e., a true output result occurs if one – and only one – of the gate's inputs is true. If both inputs are false (i.e. LOW or 0) or both inputs are true, the output is false.

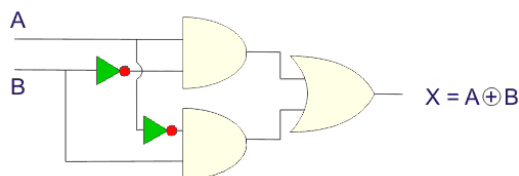
XOR represents the inequality function, i.e. the output is true if the inputs are not alike; otherwise, the output is false. A common way to remember the XOR is “must have one or the other, but not both”.

The logic gate performs this modulo sum operation without including carry is known as XOR gate. An XOR gate is normally two inputs logic gate where the output is only logical 1 when only one input is logical 1. When both inputs are equal, either are 1 or both are 0, the output will be logical 0.

This is the reason an XOR gate is also called an anti-coincidence gate or inequality detector. This gate is called XOR or exclusive OR gate because its output is only 1 when its input is exclusively 1.

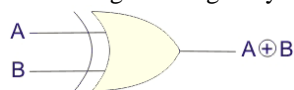
## II. Reference Circuit Details [2]

From this Boolean expression, one can easily realize the logical circuit of an XOR gate, and this will be as shown,



Logical Symbol of XOR Gate

An XOR gate is logically represented as,



Input A	Input B	Output X
0	0	0
0	1	1
1	0	1
1	1	0

## III. Reference Circuit Design [1]

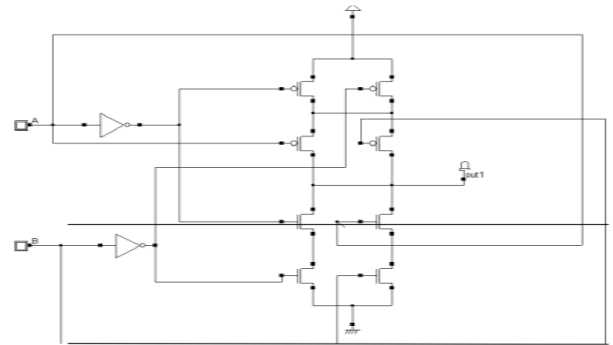
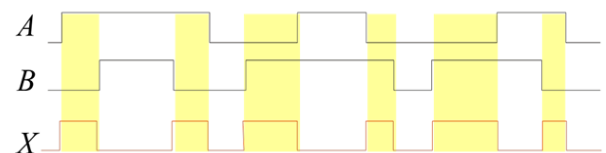


Figure1: XOR using CMOS

## IV. Reference Waveform & Area Estimate

Output Waveform [3]:



Notice that the XOR gate will produce a HIGH only when exactly one input is HIGH.

Figure2: XOR Output Waveform

Area Estimate [1]: less than  $18.8\mu\text{m}^2$

## V. References

1. Pooja Singh, Rajesh Mehra, Design Analysis of XOR Gates Using CMOS & Pass Transistor Logic”; International Journal of Engineering Science Invention Research & Development; Vol. I Issue I July 2014
2. <https://www.electrical4u.com/exclusive-or-gate/>
3. [https://grace.bluegrass.kctcs.edu/~kdunn0001/files/Exclusive\\_OR\\_Gate/5\\_Exclusive\\_OR\\_Gate2.html](https://grace.bluegrass.kctcs.edu/~kdunn0001/files/Exclusive_OR_Gate/5_Exclusive_OR_Gate2.html)