# EE-254 Final Project

# Team

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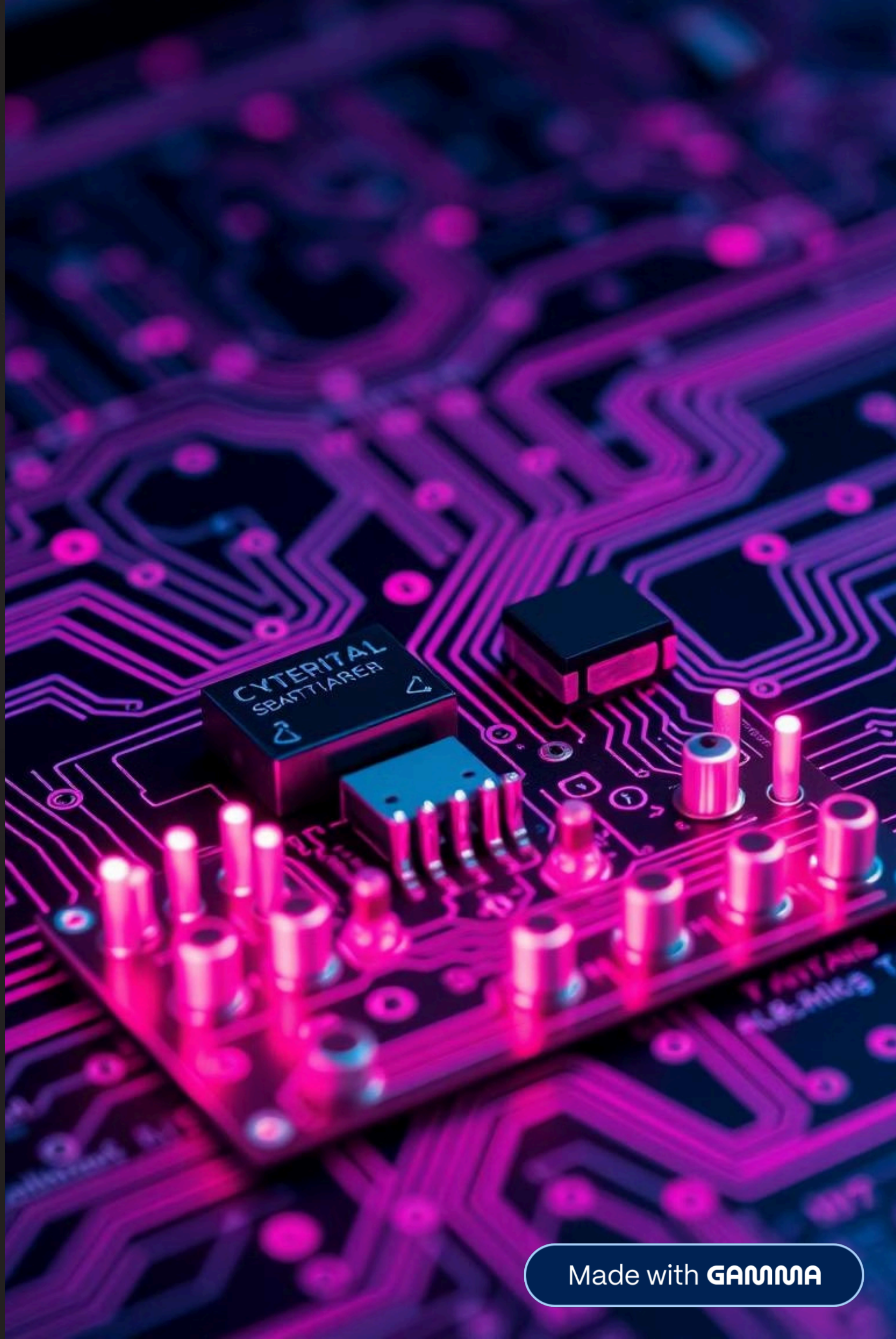
# Problem Statement

Design a Wein bridge oscillator to generate a 1.2 MHz sinusoidal signal using a transistor based amplifier configuration.



# About

### Overview

A Wien-bridge oscillator built with BJTs combines a frequency-selective feedback network (the “Wien bridge”) with a two-stage transistor amplifier and an automatic amplitude stabilization element.

- Consists of a lead–lag RC network: a series RC branch feeding into a parallel RC branch.
- At its resonant frequency
- $f = 1/(2\pi RC)$
- The bridge has unity gain and zero phase shift, so it passes only that frequency back into the amplifier.

## Few Advantages:

*Single-Supply Operation*

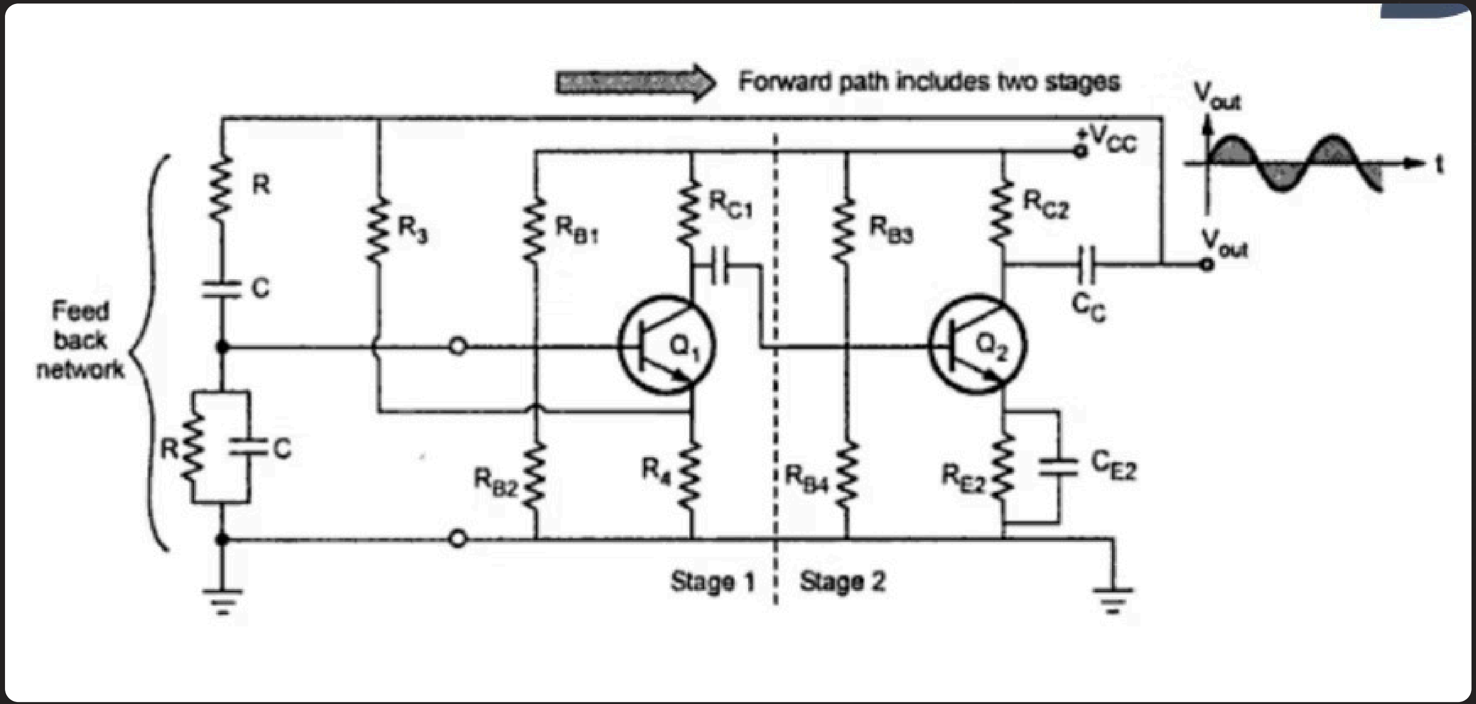
- Runs happily on a single 5–15 V rail; no need for dual ± supplies. That makes it ideal for battery-powered or portable test gear.

*Wide Frequency Range*

- With modern low-tolerance capacitors and small resistor values you can cover from a few kHz up into many MHz with the same topology—just scale R/C.

# Circuit Diagram

2-stage Transistor Amplifier




Q1: Amplifier Stage

Q2: For automatic gain control

# Key Assumptions

## Why is Vce set to 50% of VCC?

- **Maximum Output Swing:** Centering VCE at half of VCC allows the output signal to swing equally in both directions (towards saturation and cutoff) without distortion, maximizing the undistorted output amplitude.
- **Stability:** This setting provides the best margin against variations in transistor parameters and temperature, ensuring the transistor remains in its active region during operation.

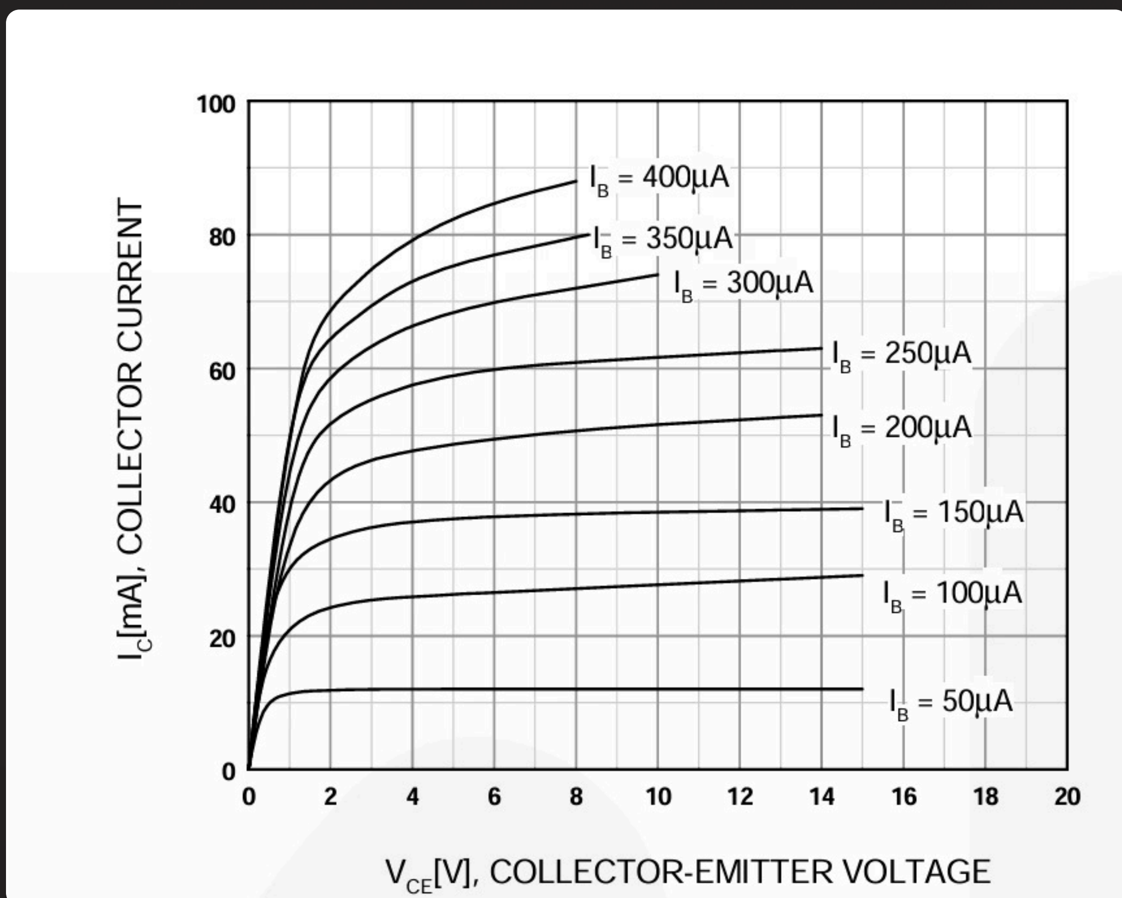
## Why is Vre set to 10% of VCC?

- **Good Bias Stability:** A larger VRE (relative to VBE) makes the bias point less sensitive to variations in VBE and transistor beta (β), improving thermal stability.
- **Predictable Operation:** It provides a straightforward way to select RE for a given emitter current.

## Calculations:

Setting **Vcc** as 12V.

Current gain for this transistor is 110.




For **Ib =13.6uA**, value of **Ic** in active region is 1.5mA. This can also be verified by the datasheet.

docs.google.com

- For Q point we are setting **Vce** to **50% of Vcc** which is equal to 6V.
- Setting **Re** as **10% of Vcc** which is equals to 1.2V.
- **Vre** = **Ic** x **Re**, from here **Re** = 800 ohm (standard value taken as 1kohm).
- **Vrc**= **Vcc**- **Vce** -**Vre** = (**Vcc**= 12V , **Vce** = 6V, **Vre** =1.2V), we get **Vrc** as 4.8V.
- **Rc**= **Vrc/Ic** =3.2k ohm (standard value taken as 3.3k ohm).
- **Ib** =**Ic/hfe** which is equal to 13.6uA.
- Current through **R2 is 11 Ib**, and current through **R6 is 10 Ib.**
- **Vb= Vre +Vbe**. (**Vbe =0.6V, Vre =1.2V**) , we get **Vb as 1.8V.**
- **R2= Vcc-Vb/11IB= 68k ohm.**
- **R6=Vb/10Ib= 12k ohm.**

## Selecting Proper Rl:

For a **gain of 110**, the required **Rl is 4k ohm.**

# Continued...

## Design of coupling capacitance:

- XC1 should be less than the input impedance of the transistor. Here, **Rin** is the series impedance. Then **□□□** ≤ **□□□/□□**. Here **□□□ = □1 // □2 // □□□.** ( R1= 68 k , R2= 12k, hfe= 110 , implies Rin is 108.8376).
- From this the required capacitance must be greater than **5.1uF** (for a lower cutoff frequency of 200Hz), standard value is **10uF.**
- Similarly, **□□2 ≤ □□□□/ 10** , where **Rout = RC**. Then **XCE ≤ 330ohm**.
- This implies we get C value greater than **2.4uF**(or a lower cutoff frequency of 200Hz), standard value is **4.7uF.**

## Design of bypass capacitance:

- To bypass the lowest frequency (say 200 Hz), XCE should be much **less than or equal** to the resistance RE.
- □□□ ≤ □□ /□□ which is □□□ ≤ 800/ 10 i.e. □□□ ≤ 80.
- Further, we should get capacitance value as more than **10uF.**

## Design of Wein bridge circuit:

$$R_3\left[\frac{R_2}{1+j\omega C_2 R_2}\right] = R_4\left[R_1 - \frac{j}{\omega C_1}\right]$$

It can be written as,

$$R_2R_3 = R_4\,(1 + j\omega C_2R_2)(R_1 - j/\omega C_1)$$

Or

$$R_2R_3 - R_4R_1 - R_2R_4 + \frac{jR_4}{\omega C_1} - j\omega C_2R_2R_1R_4 = 0$$

By separating real and imaginary terms we can get

$$R_2R_3 - R_4R_1 - \frac{C_2}{C_1}R_2R_4 = 0$$

$$or\ \frac{C_2}{C_1} = \frac{R_3}{R_4} - \frac{R_1}{R_2}$$

$$\frac{R_4}{\omega C_1} - \omega C_2R_2R_1R_4 = 0$$

..

$$\omega^2 = \frac{1}{C_1C_2R_1R_2}$$

$$\omega = \frac{1}{\sqrt{C_1C_2R_1R_2}}$$

$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

If $C_1 = C_2 = C$ and $R_1 = R_2 = R$, then

$$f = \frac{1}{2\pi CR}$$

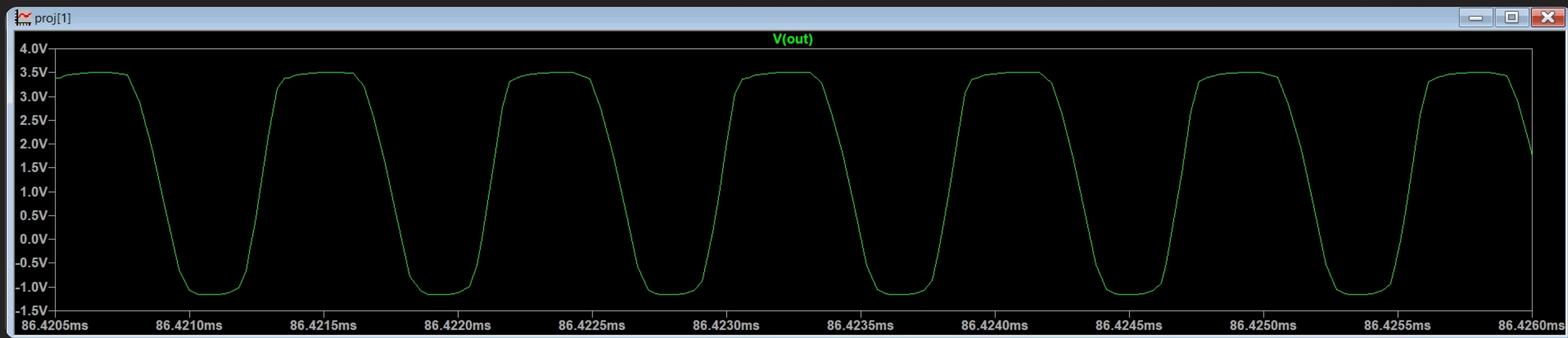
and $R_3 = 2R_4$

Using above equations to get the frequency of **1.2 MHz**, the chosen values are:

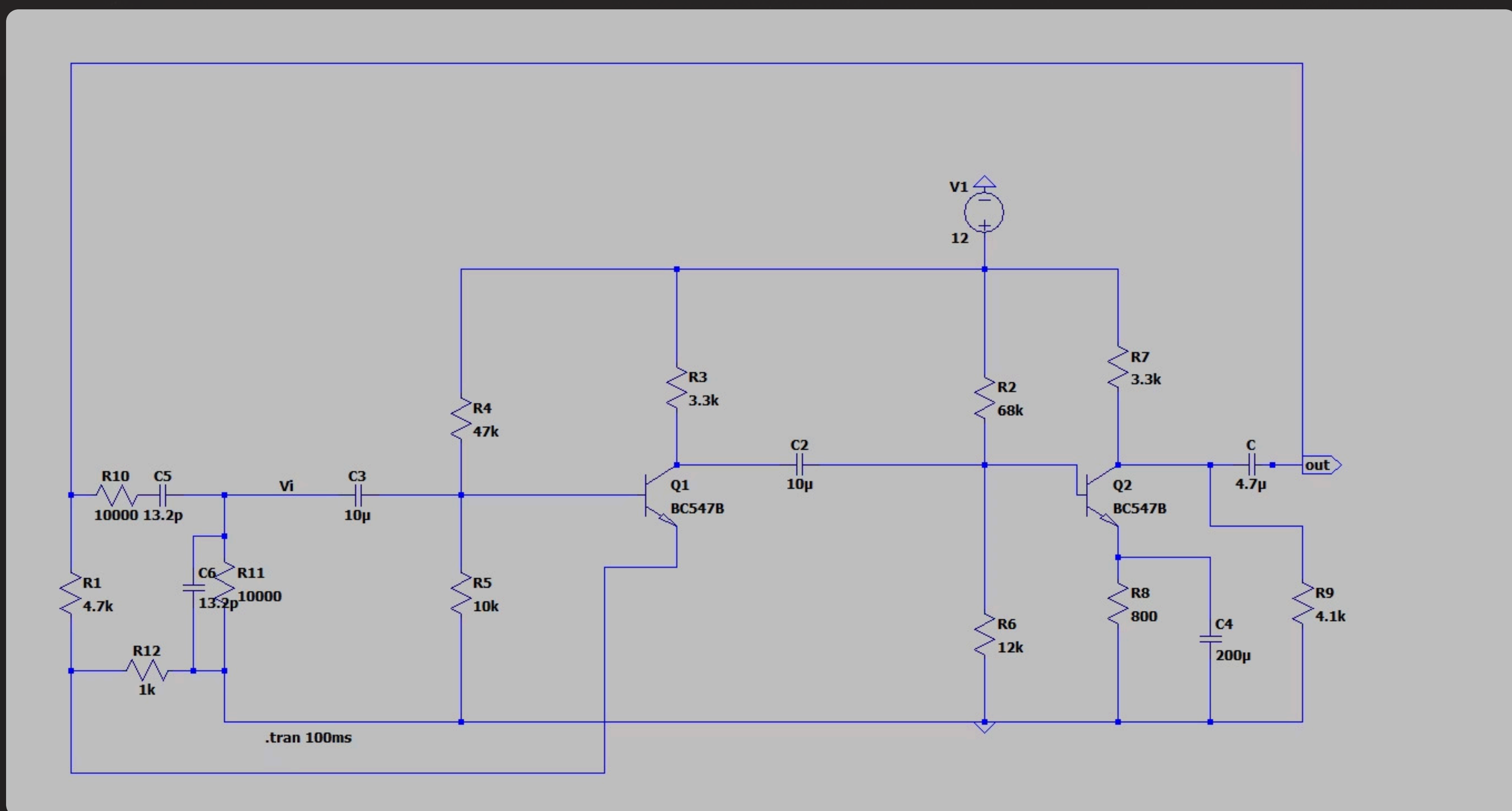
- **R10=R11= 10k ohm.**
- **C5= C6= 13.2pF.**
- **R1 = 4.7k ohm.**
- **R12 =1k ohm.**

# Simulations:

## Output Waveform-




## Schematic:



# Observations:

- Although, the circuit is designed for creating a perfect sine wave. Practically, there were a lot of parasitics (non-Ideality) involved such as resistances of wires, Capacitors, non-Ideality of BJT.
- Difference between the LTspice simulation results and the DSO output is is observable, for which the possible reasons might be inaccurate resistances(Different from labelled), Non-Ideality of Breadboard, etc. ..