CLASS TEST - 4 (COA)

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Q1. ==

Binary address	Hit / miss
10011	Miss
00001	Hit
00110	Hit
01010	Miss
01110	Miss
11001	Miss
00001	Miss
11100	Miss
10100	Miss

a) Hit ratio = $\frac{\text{number of hits}}{\text{number of accesses}} = \frac{2}{9}$

$= 0.2\bar{2}$

b) PTO

b) Final state of cache

Index	V	Tag	Data
000	N		
001	Y	00	Mem[00001]
010	Y	01	Mem[01010]
011	Y	10	Mem[10011]
100	Y	10	Mem[10100]
101	Y	01	Mem[01101]
110	Y	01	Mem[01110]
111	N		

Q2. (a) Average read time = seek time + rotational delay + transfer time + controller delay

$$= 12\,ms + \left(\frac{1}{2}\right) \times \left(\frac{60}{3600}\right) \times 10^3\ ms + \left(\frac{512}{2^{20} \times 3.5}\right) \times 10^{+3}\ ms + 5.5\,ms$$

$= 12\,ms + 8.\bar{3}\,ms + 0.146\,ms + 5.5\,ms$

$= 25.97\,ms$

(b) Here, only the transfer time gets changed.

Disk Access Time

= seek time + rotational delay + transfer time + controller delay

$= 12 + \left(\frac{1}{2}\right) \times \left(\frac{60}{3600}\right) \times 10^3 + \left(\frac{8 \times 1024 \times 1000}{3.5 \times 2^{20}}\right) + 5.5$

$= 28.07\,ms$

Q4. The first level cache minimizes the hit time, therefore its usually small with low associativity.

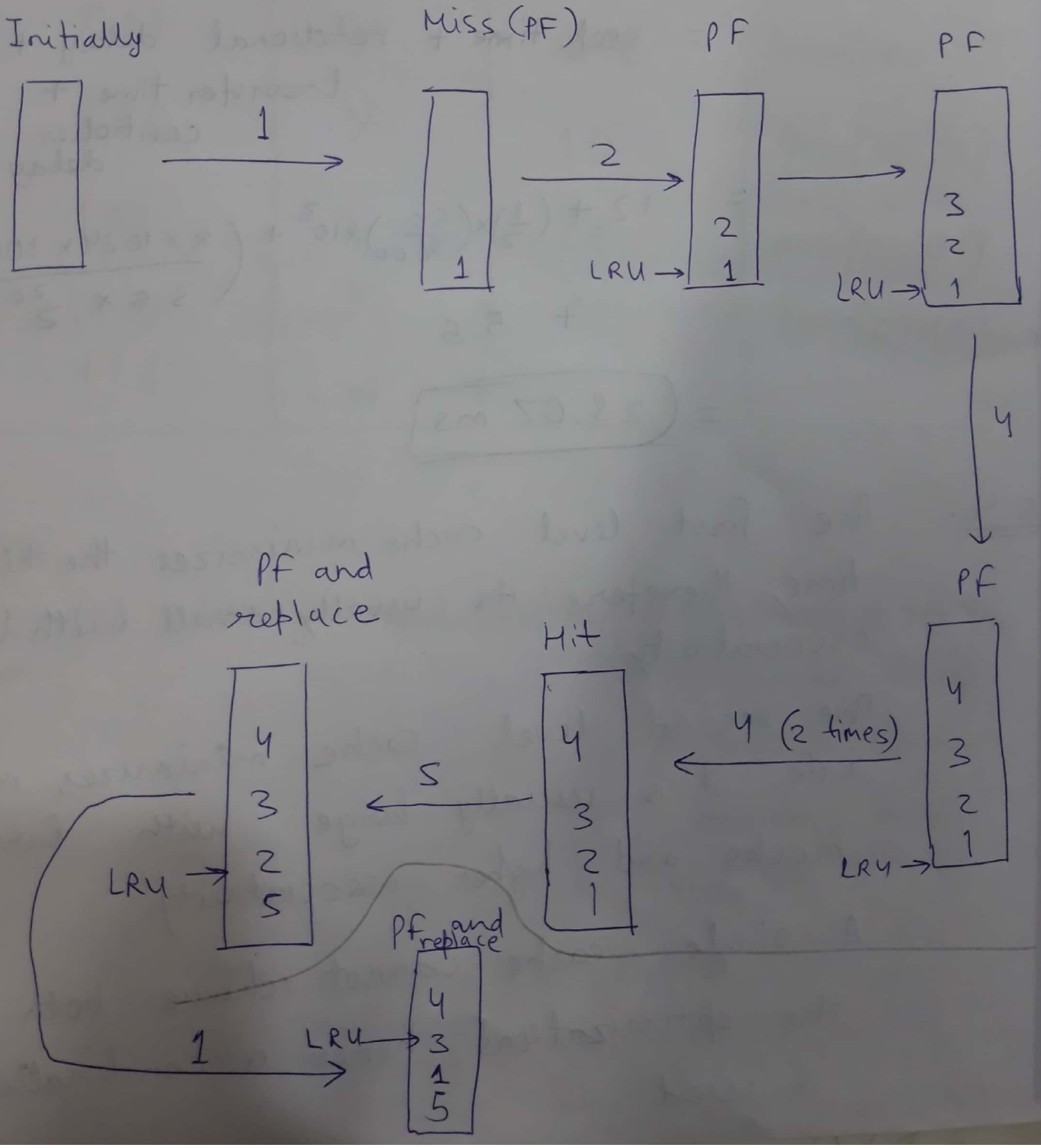
The second level cache minimizes miss rate, it is usually large with large blocks and higher associativity.

A single cache cannot achieve both the optimizations hence a combination is used.

Q3) DRAM capacity — 4 pages
Initially empty

Access sequence : 12344451

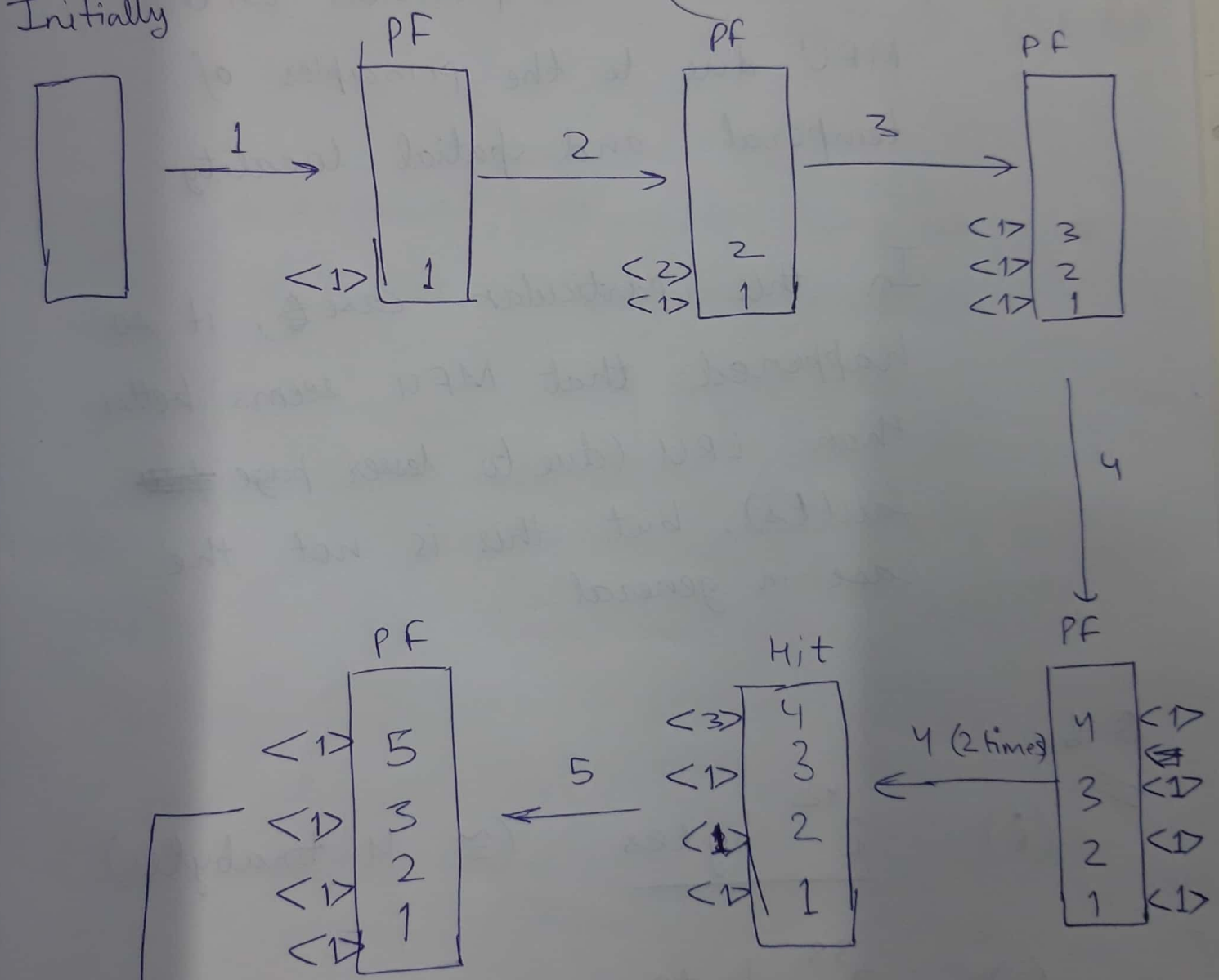
(i) LRU (Least Recently Used):



Hence, total number of Pf's (page faults) in LRU = 6.

(ii) MFU (Most frequently Used)

(frequencies written in <>).



Hence, total number of Pf's (page faults) = 5

(iii) We see, the number of page faults in MFU is lesser than that in LRU

This is unexpected as LRU is preferable in comparision with MFU due to the principles of temporal and spatial locality.

In this particular case, it so happened that MFU seems better than LRU (due to lesser page faults), but this is not the case in general.

Q6.

(i) 2^{42} bytes ($\cong$ 4 terabytes)

(ii) 2^{38} bytes

each PTE = 4 bytes (32 bits)

page size = 16K bytes

a) page offset = $\log_2(16 \times 2^{10} \times 2^3) = 17$ bits

b) for protection

$32 - 8 = 24$ bits for page number

∴ Largest physical memory size

$= \left(2^{17+24}\right) / 2^3 = 2^{38}$ bytes $\cong$ 256 GB

Q5. Maximum allowable time for a cache hit in this microprocessor

$= \underline{0.28 \text{ ns}}$