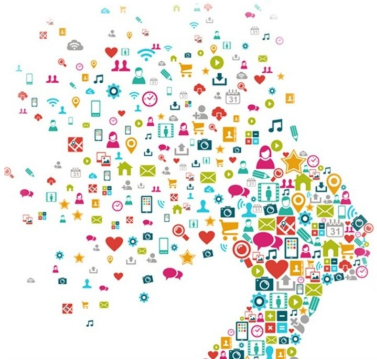

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ARM processor architecture

Basava Prasad S J

Contents

Abbreviations to remember

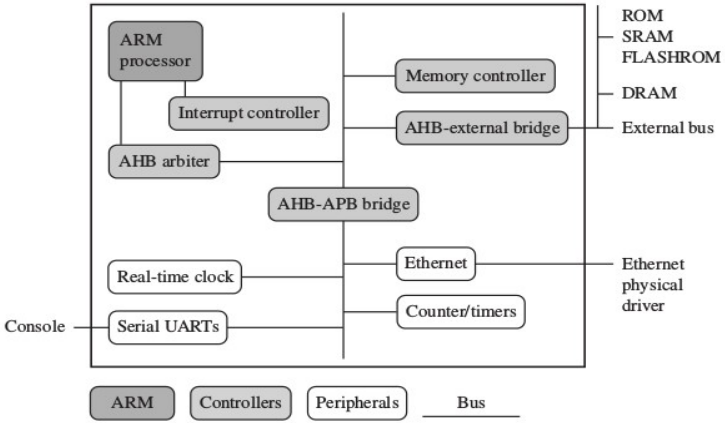
- ARM – **A**dvanced **R**ISC **M**achine
- RISC – **R**educed **I**nstruction **S**et **C**omputer
- AMBA – **A**dvanced **M**icro-controller **B**us **A**rchitecture
- APB – **A**RM **P**eripheral **B**us
- AHB – **A**RM **H**igh-performance **B**us
- ASB – **A**RM **S**ystem **B**us
- CPSR – **C**urrent **P**rogram **S**tatus **R**egister
- SPSR – **S**aved **P**rogram **S**tatus **R**egister

Introduction to ARM processor architecture

- Originally ARM is **A**cron **R**ISC **M**achines, invented by Acron computers in 1980's.
- ARM provides core for the different micro-controllers and microprocessor companies.
- ARM core uses RISC architecture.
- ARM supports most of all the embedded OS, RTOS and mobile phone OS's.
- Presence of Thumb instruction set to increase the code density.
- Key factors for the success of ARM architecture are :
    - Low power consumption
    - High performance
    - Small size implementations

Introduction contd...

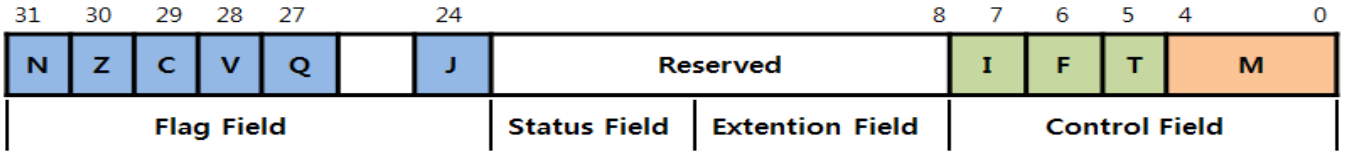
- ARM also incorporates following RISC features :
  - Larger uniform register file
  - Load (LD Register)/Store (ST Register) architecture
  - Simple addressing modes



ARM Register set

- ARM has 37 registers each of 32-bit .
- 31 registers including program counter (PC) are general purpose registers (R0-R15) and 6 program status registers.
- The general-purpose registers R0-R15 can be split into three groups.
  - The unbanked registers, R0-R7
  - The banked registers, R8-R14
  - Register 15, the PC
- Register 13 is treated as stack pointer (SP) and Register 14 as link register.
- Process status registers are :
  - CPSR - Status of current execution mode of processor.
  - SPSR - To save the content of CPSR when mode switch occurs.

Functionalities of ARM status registers



Flag Field	
N	Negative result from ALU
Z	Zero result from ALU
C	ALU operation caused Carry
V	ALU operation oVerflowed
Q	ALU operation saturated
J	Java Byte Code Execution

Control bits	
I	1: disables IRQ
F	1: disables FIQ
T	1: Thumb, 0: ARM

Mode bits M[4:0}	
0b10000	User
0b11111	System
0b10001	FIQ
0b10010	IRQ
0b10011	SVC(Supervisor)
0b10111	Abort
0b11011	Undefined

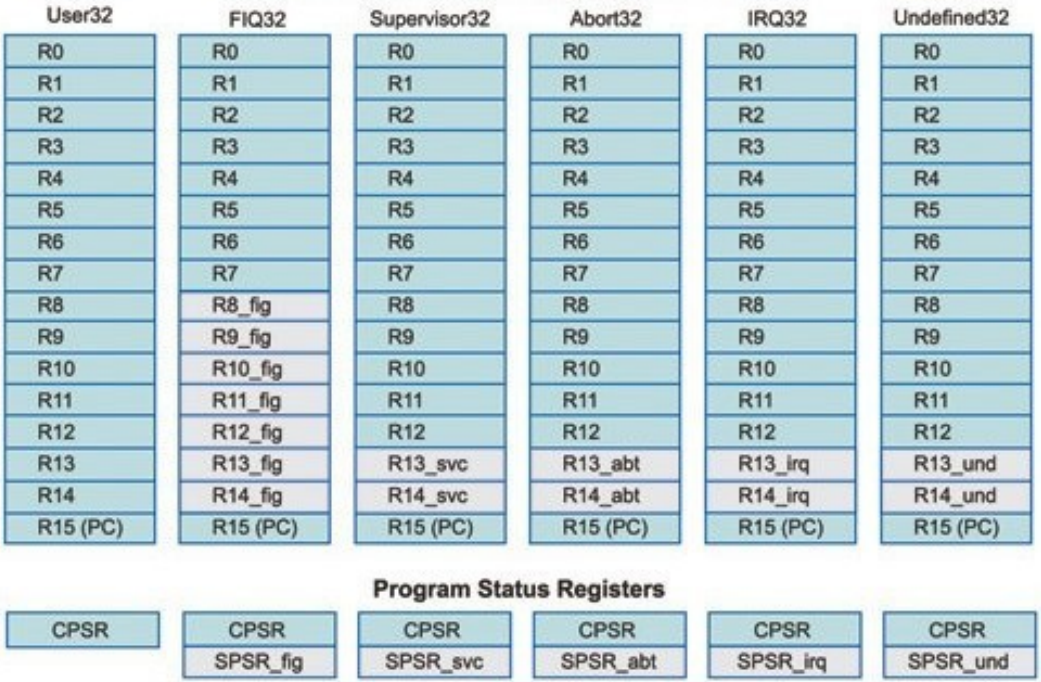
Exceptions handled in ARM processor

Exception type	Mode	Normal address	High vector address
Reset	Supervisor	0x00000000	0xFFFF0000
Undefined instructions	Undefined	0x00000004	0xFFFF0004
Software interrupt (SWI)	Supervisor	0x00000008	0xFFFF0008
Prefetch Abort (instruction fetch memory abort)	Abort	0x0000000C	0xFFFF000C
Data Abort (data access memory abort)	Abort	0x00000010	0xFFFF0010
IRQ (interrupt)	IRQ	0x00000018	0xFFFF0018
FIQ (fast interrupt)	FIQ	0x0000001C	0xFFFF001C

Operating modes in ARM

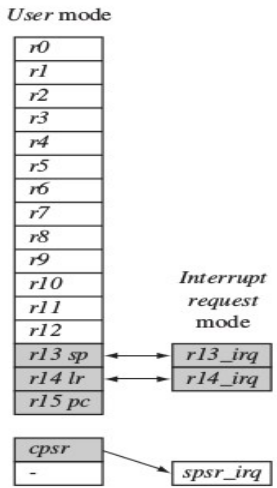
- There are seven modes of operation in ARM processor :
  - ➔ Unprivileged mode
    - User mode
  - ➔ Privileged modes
    - Abort mode
    - System mode
    - Undefined mode
    - Fast interrupt request (FIQ) mode
    - Interrupt request(IRQ) mode
    - Supervisor (SVC) mode

Register organization depending on operating modes



Operating modes contd...

- Example to show how mode switch occurs on exception from User mode to IRQ mode.



Changing mode on an exception.

ARM Instruction set

- All instructions are 32-bit long.
- Thumb instructions are compressed to 16-bit to increase code density.
- Most of the instructions execute in single machine cycle and can be conditionally executed.
- Depending on the operations instructions can be classified as :
    - Data processing instructions
    - Branch instructions
    - Load-Store instructions
    - Swap instructions
    - Software interrupt instruction
    - Program status register instructions

Instruction set contd...

ARM code

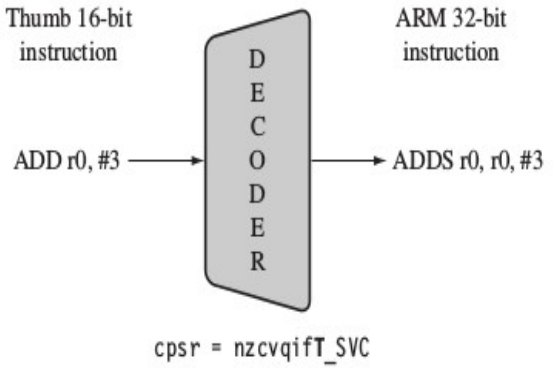
```
ARMDivide
; IN:  r0(value),r1(divisor)
; OUT: r2(MODulus),r3(DIVide)

        MOV     r3,#0
loop
        SUBS    r0,r0,r1
        ADDGE   r3,r3,#1
        BGE     loop
        ADD     r2,r0,r1
```

5 × 4 = 20 bytes

Thumb code

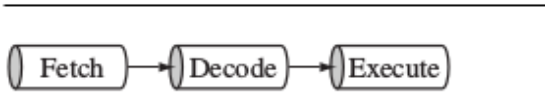
```
ThumbDivide
; IN:  r0(value),r1(divisor)
; OUT: r2(MODulus),r3(DIVide)

        MOV     r3,#0
loop
        ADD     r3,#1
        SUB     r0,r1
        BGE     loop
        SUB     r3,#1
        ADD     r2,r0,r1
```

6 × 2 = 12 bytes

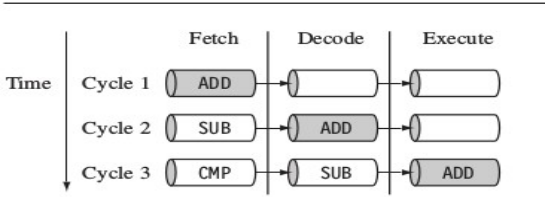


Thumb instruction decoding.

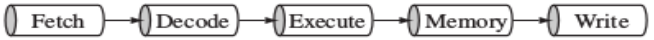
Pipelining in ARM processor



ARM7 Three-stage pipeline.



Pipelined instruction sequence.



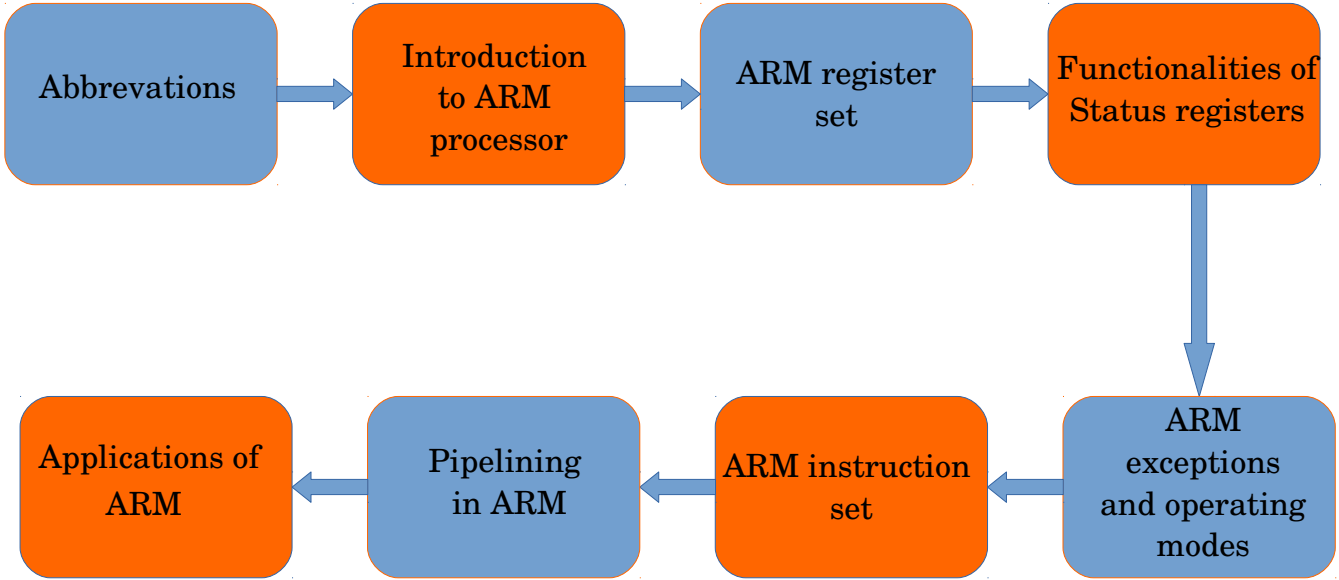
ARM9 five-stage pipeline.

ARM10 six-stage pipeline.

Applications of ARM processor

- Smart phones
- Net-books
- eReaders
- Digital TV
- Home Gateways
- Servers and Networking
- Automotive braking systems
- Mass storage controller
- Networking & printing

Conclusion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ARM register set
Functionalities of Status registers
ARM exceptions and operating modes
ARM instruction set
Pipelining in ARM
Applications of ARM

References

- ARM system developers guide – Designing and optimizing software by Andrew N.sloss, Dominic symes and Chris wright.
- ARM architecture reference manual.
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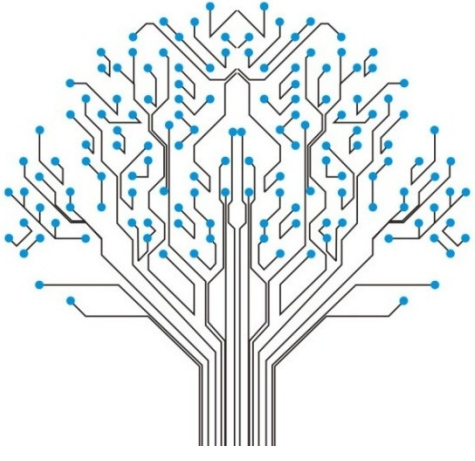
Thank you



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