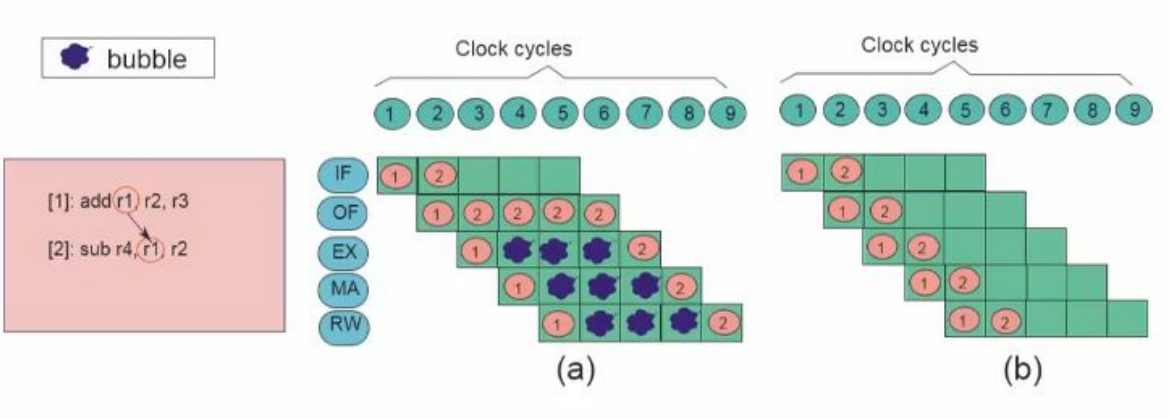
CoA Assignment 6

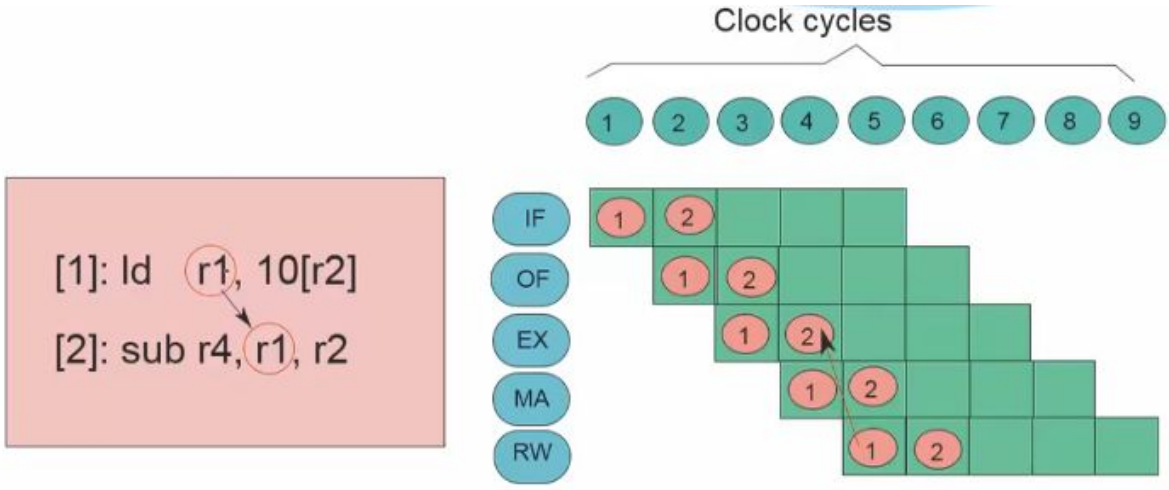
Question 1:
Data hazards can happen when instruction reads incorrect values.
Let's take an example of RAW(Read After Write) condition. When we are in pipeline format Register Write happens in the fifth stage, but after write operation if we have read operation the register read happens in OF stage that is second stage. So in the pipeline when the first instruction is in 3rd stage (Execute), the second instruction is its 2nd stage so it is reading incorrect value as updation of value in register didn't take place.

So to avoid this we introduced bubbles/stalls in pipelines when there is a hazard kind of situation. It stalls the instruction in its respective stage(OF stage) and passes bubble(Nop) instruction forward until register write takes place.



We can see here if there are no stalls OF stage gonna read incorrect values and compute unfavourable results. But if we have Bubbles we can see it compute correct values as it stalls until register writes takes place. So between RW stage of first instruction and OF stage of 2nd instruction we should **atleast have a difference of 3 clock cycles.**

Question 2:
We look carefully at the pipeline and we see that for the above example that value to be stored at r1 is available at end of cycle 3 for first instruction and value needed to compute the result for second instruction should be available at last at start execution that is at cycle 4.
So we have the result prepared at the end of cycle 3 and wanted at cycle 4 so we directly forward the value to EX stage of 2nd instruction. So we can have a forwarding path for that. This way we get the correct value for register and delay has been minimized. Now we have reduced the number of stalls from 3 to zero for this case.
For the general case we need to have an utmost 1 stall for forwarding method.



In this case value to be stored in the register is available at cycle 5 and needed at 4 so to overcome this we should utmost have 1 stall. So that we can stall the instruction 2 for 1 cycle and then forward value.
So stalls needed is utmost 1.