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AKHILESH KUMAR P

VLSI/ASIC Engineer

(ME- Microelectronics and VLSI Fabrication Technology)

Innovative VLSI Engineer with expertise in transistor-level circuit design, front end design and verification, embedded system. Proven ability to optimize workflows and develop solutions for high-performance applications.

Technical Skills

Programming Languages	:	C, C++, Python.
HDL/ HVL/ Methodology	:	Verilog, System-Verilog, UVM.
Protocols	:	APB, AHB, AXI, CHI, SPI, UART, I2C, CAN bus, Etherent.
Tools	:	Vector DaVinci, Vector tools, CANOE, Intel Quartus Prime, Cadence Xcelium, Genus, Innovus, Virtuoso, Synopsys VCS, Verdi, LT SPICE.
Scripting	:	BASH, Python.
Version Control	:	Git.

Work Experiences

Intern Infinity Fabric Team – AMD India Pvt. Ltd. Jul'24 – Present

Implementation of python script for efficient verification environment Jul'24 – Present

- **Developed a robust python script** to capture and summarize transaction packets from UVM log files.
- Enhanced verification accuracy and efficiency using regular expressions for data extraction.
- Reducing manual log analysis time by **70-80%** on average.
- Utilized **parallel processing** and data frames to data aggregation.
- **Optimized performance** to handle larger datasets efficiently.
- Front-end design verification at AMD, utilizing Verdi for debugging and waveform analysis.

Automotive Software Design Engineer – TATA Elxsi Ltd. 2 Years (Aug'21–Aug'23)

AUTOSAR – Diagnostics Development

- Development of Automotive Diagnostic stack and integration of the diagnostic stack with the AUTOSAR Classic for Lidar supplier to OEM.
- **Requirement analysis**, **Design modules** and **implement code** (C) using Davinci developer.
- Flashing the software and debugging the code with JTAG connected with Ozone.
- Version control and **code integration** of a large codebase.
- Conduct peer code reviews and develop MISRA C and ISO26262 compliant systems.

Research Intern – IIT Guwahati June'20 – Aug'20

Implementation of python script for efficient verification environment

- Research project under EICT Academy, IITG, design and analysis of Ka band power amplifier at 27 GHz using fully open-source toolkits and well documentation of it.
- Python-based toolkit called as scikit-rf for the development.
- Simulate the end-to-end gain of the amplifier by using the given S parameter file of the transistor.

Academic Projects

Round Robbin arbiter design Using Verilog. (Jan'24 – Apr'24)

- - Designed and implemented a round-robin arbiter with four master blocks.
- - Developed priority logic using Moore finite state machine (FSM) with AHB.
- - Created combinational grant logic for efficient arbitration control.
- - Integrated AHB protocol for seamless bus communication.
- - Executed physical design including synthesis, placement, and routing.

Design of a full adder using 12 Transistor circuit. (Sep'23 – Dec'23)

- The main objective was to implement a full adder for **low power applications** with min area, with just 12 transistors, with power source from the input signals, implemented on 45nm node.
- It can be used at medium speed, with **very low power** battery operated devices.
- It can be used in area constrained devices where area is a crucial trade off.
- Researching of existing full adders and their drawbacks with respect to the **area**, **Power Optimization Techniques** and **power consumption**.
- Implement the full adder with 12 Transistors, with **2 Transistor mux as core transistor-level circuit design**, Analysis and testing of the simulations.

Academic Profile

Course	Institute	Board/ University	Year	Marks
M.E. Microelectronics & VLSI Technology	Manipal School of Information Sciences (MSIS) (MIT Campus)	Manipal Academy of Higher Education (MAHE), Manipal	2025	8.22 GPA
B. E. (ECE)	Canara Engineering College, Mangalore	Visveswaraya Technological University (VTU), Karnataka	2021	7.79 CGPA
PUC (PCME)	Canara PU College	Karnataka Pre University Board	2017	77.00%
SSLC	Bhagavathi High School	Karnataka Secondary Education Board	2015	88.32%

Certifications and Recognition

- Completed Cadence Online Training Course on "**Cadence RTL to GDSII Flow**"
- Completed Cadence Online Training Course on "**Basic Static Timing Analysis**"
- Completed Cadence Online Training Course on **Artificial Intelligence and Machine Learning Fundamentals v1.0 (Online)"**
- Completed NPTEL Certification on **"Basic Electrical Circuits"**
- Best Technical Presentation award on "**Neuromorphic in Memory Computing"**