Assignment 1 | FPGA Lab

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1 Question

Write the Product of Sum form of function G(U,V,W) for the following truth table representation of F

U	V	W	G
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

2 Solution

2.1 KMAP Implementation

Given truth table can be minimized using a KMap (Figure 1). Using implicants in figure, POS Terms obtained are : $(U + \overline{W}), (V + \overline{W}), (\overline{U} + \overline{V} + W)$

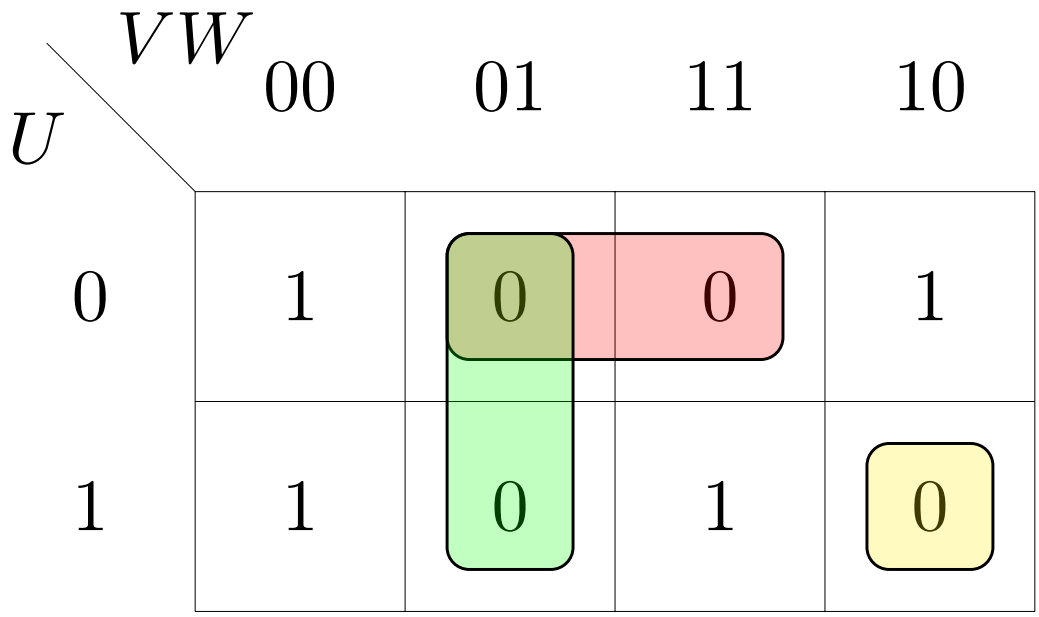

Figure 1: POS for G

2.2 Minimized POS Expression

G = $(U + \overline{W}).(V + \overline{W}).(\overline{U} + \overline{V} + W)$

2.3 NAND Logic Implementation

To implement it using NAND Logic, we first convert it into SOP form, which gives :

$$\overline{V}.\overline{W} + \overline{U}.\overline{W} + U.V.W$$
$$(\overline{V} + \overline{U}).\overline{W} + U.V.W$$
$$\overline{V.U}.\overline{W} + U.V.W$$

The last expression can be implemented using only NAND Gates.