BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI,
HYDERABAD CAMPUS
INSTRUCTION DIVISION, FIRST SEMESTER 2016-17
COURSE HANDOUT (PART-II)

Date: 21-07-2016

In addition to Part I (General Handout for all the courses appended to the time table), this portion gives further specific details regarding the course.

Course No.	**CS / EEE / ECE / INSTR F215**
Course Title	**Digital Design**
Instructor-in-charge	**SOUVIK KUNDU**
Team of Instructors	
Lecture	Souvik Kundu, BVVSN Prabhakar Rao, Syed Ershad Ahmed
Tutorial	Souvik Kundu, Syed Ershad Ahmed, Surya Shankar Dan, BVVSN Prabhakar Rao, Chetan Kumar V.
Practical	Souvik Kundu, Surya Shankar Dan, Chetan Kumar V, Soumya J, Sai Phaneedra, Gautam Makkena, and Avinash
Course Description	This course covers the topics on logic circuits and minimization, Combinational and sequential logic circuits, Programmable Logic devices, State table and state diagrams, Digital ICs, Arithmetic operations and algorithms, Introduction to Computer organization, Algorithmic State Machines
Scope and Objective	The objective of the course is to impart knowledge of the basic tools for the design of digital circuits and to provide methods and procedures suitable for a variety of digital design applications. The course also introduces fundamental concepts of computer organization. The course also provides laboratory practice using MSI devices.

Text Books:

T1: M.Moris Mano and Michael D. Ciletti " Digital Design", PHI, 4th Edition, 2009
T2: G Raghurama, TSB Sudharshan "Introduction to Computer Organization". EDD notes 2007
T3: Laboratory Manual for Digital Electronics and Computer Organization.

Reference Books:

R1: Donald D. Givonne, "Digital Principles and Design" TMH, 2003.
R2: Samir Palnitkar, "Verilog HDL", Prentice Hall; 2 edition, 2003

Course Plan

Lect. No.	Learning Objectives	Topics to be covered	Reference to Text Book
1	Introduction to Digital Systems and Characteristics of Digital ICs.	Digital Systems, Digital ICs	1.1, 1.9, 2.3, 10.1 & 10.2
2-3	Boolean algebra and logic gates, Codes number systems	Boolean functions, Canonical forms, number systems and codes	1.2 - 1.7, 2.4-2.9
4 - 5	Simplification of Boolean functions	K-Maps (4,5 variables)	3.1- 3.8
6	Simulation and synthesis basics	Hardware Description Language	3.11
7	Simplification of Boolean functions	QM Method	3.10
8-10	Combinational Logic, Arithmetic circuits	Adders, Subtractors, Multipliers	4.1 – 4.7
11-12	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	4.8 - 4.11
13	Simulation of Combinational Logic Functions.	HDL for Combinational Logic	4.12
14-15	Sequential Logic	Flip-Flops & Characteristic tables, Latches	5.1 - 5.4
16-18	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction	5.5, 5.7 & 5.8
19-20	Registers & Counters	Shift registers, Synchronous & Asynchronous counters	6.1 - 6.5
21	Simulation of Sequential Logic Functions.	HDL for Sequential Logic	5.6
22-23	Analysis of arithmetic units	Multiplication & Division algorithms	T2: Appendix A & Class Notes
24-27	Modular approach for CPU Design	RTL, HDL description	8.1 & 8.2, 8.4 - 8.8
28-30	Design of Digital Systems	Algorithmic State Machines	R1. Chapter 8
31-33	Design of Asynchronous Circuits.	Asynchronous Sequential Logic	9.1 – 9.4
34-36	Memory and PLDs	RAM, ROM, PLA, PAL	7.2, 7.5 - 7.7
37-39	Memory Organization	Memory Hierarchy & different types of memories	T2: Ch 6 & Class Notes
40-42	Digital Integrated Circuits	TTL, MOS Logic families and their characteristics	10.3, 10.5, 10.7 - 10.10

Lab Experiments

S.No	Experiment	Reference
1	Familiarization of Bench Equipment	A complete Lab Manual is available on CMS and also one hard-copy in the Digital Design Lab
2	Implementation of Boolean Functions using Logic Gates	
3	Write Verilog code at gate level and verify (i) 3-input majority function using AND – OR logic gates (ii) even – odd parity generation (iii) Binary – Gray code conversion	
4	Adders and Subtractors	
5	Write Verilog code at gate level and verify (i) 1-bit full adder and (ii) 4-bit full adder using (a) instantiation and (b) Test bench	
6	BCD Adder	
7	Write Verilog code for (i) 1-bit full adder and (ii) 4-bit full adder using data-flow modeling	
8	Decoders, Multiplexers and Demultiplexers	
9	Comparators & Arithmetic Logic Unit	
10	(i) Latches & Flip- Flops (ii) Write Verilog code for implementing various flip-flops	
11	(i) Counters (ii) Write Verilog code for implementing counters	
12	Shift Registers	

General Instructions for Lab

1. There will be an observation book of 100 pages (white)
2. After every lab, observation book must be signed by Faculty/Research Scholar
3. Lab carries 20% weightage.
    (i) 10% day to day evaluation (including attendance) and
    (ii) 10% Final Lab Examination
4. Only one makeup will be allowed

Evaluation Scheme:

Component	Duration	Weightage (%) and Marks	Date & Time	Nature of Component
Test-I	1 Hour	25% (75)	As per ID	Closed Book
Test-II	1 Hour	25% (75)	As per ID	Open Book

LAB component	Day to Day Evaluation	13.33% (40)	Regular	Demo/Practicals/ (Open Book)
	LAB Exam	6.67% (20)	Will be announced	Closed Book
Comprehensive Exam	3 Hours	30% (90)	As per ID	Closed Book
TOTAL		100% (300)		

Make-up Policy: There will no make-ups unless for genuine reasons. Prior Permission of the Instructor-in-Charge is required to take a make-up for any component.

Chamber Consultation Hour: To be announced in class.

Notices: All notices shall be displayed only on the **EEE/ECE Notice Board / CMS.**

Dr. Souvik Kundu
Instructor-in-charge
(CS/EEE/ECE/INSTR F215)