Birla Institute of Technology and Science, Pilani, Hyderabad Campus
First Semester 2016-2017
Course Handout (Part-II)
CS G524 (Advanced Computer Architecture)

In addition to part-I (General Handout for all courses appended to the time table) this handout gives further details regarding the course.

Course Number : CS G524
Course Title : Advanced Computer Architecture
Instructor-In-Charge : G Geethakumari

Objective

The main objective of this course is to introduce the concepts of advanced computer architectures suitable for high-performance computing.

Scope

The advanced concepts in uni-processor environment will be discussed in detail. The issues in designing and using high performance parallel computers will also be covered. System resources such as memory technology and I/O subsystems needed to achieve proportional increase in performance will be discussed along with the software support required for these systems. This course aims to equip the students with the state of the art in this area through case studies and industry interaction. As this area has lot of scope to pursue research, the course will provide the necessary platform. An insight into latest technologies like multi-core architectures will be given as part of this course work.

Text Books

(T1): Computer Architecture: A Quantitative Approach, J.L Hennessy & D.A.Patterson Morgan Kaufmann, 5th Edition, 2012.

Reference Books:

(R1): Modern Processor Design, John P Shen & Mikko H. Lipasti., Tata McGraw Hill, 2006.
(R2) : Parallel Computer Architecture: A Hardware / Software Approach, David E Culler & Jaswinder Pal Singh., Morgan Kauffmann / Harcourt India, 2000.
(R3): Advanced Computer Architecture, Kai Hwang, Tata McGraw Hill, 2001.
(R4): Computer Architecture & Parallel Processing, Hwang & Briggs, McGraw Hill, latest Edn.

Lecture Schedule

Lecture#	Learning Objectives	Topics To be covered	Reference
1	To understand about the importance of quantitative aspects of computer design	Fundamentals of Quantitative Design and Analysis - Introduction	Ch.1
2-3		Dependability, Quantitative principles of Computer Design	Ch.1
4-5	To learn about ILP, practical challenges of implementing ILP	Instruction Level Parallelism and its exploitation – concepts and challenges	Ch.3, Appendix A, Appendix C
6-7		Basic compiler techniques for exposing ILP, reducing branch costs with advanced branch prediction	Ch.3
8		Overcoming branch hazards with dynamic scheduling	Ch.3
9-11		Dynamic scheduling, examples and algorithm, hardware-based speculation	Ch.3
12-13		Exploiting ILP using Multiple issue and static scheduling, advanced techniques for instruction delivery and speculation	Ch.3, Appendix H(online)
14	To understand data level parallelism, GPUs	Data Level Parallelism -introduction	Ch.4
15-17		Vector Architecture, SIMD Instruction Set Extensions for Multimedia	Ch.4
18-19		Graphics Processing Units, detecting and enhancing loop level parallelism	Ch.4
20-23	To explore and understand TLP	Thread Level Parallelism – centralized shared memory architectures, symmetric shared memory architectures	Ch.5
24-26		Distributed shared memory and directory based coherence, synchronization	Ch.5
27 - 29		Models of memory consistency, multiprocessors and their performance	Ch.5, Appendix I(online)
30	To know about the organization of memroy hierarchy and learn various optimization techniques at each level	Memory Hierarchy Design - Introduction	Ch.2, Appendix B
31 - 33		Memory Organization – Ten advanced optimizations of cache performance	Ch.2
34 - 35		Virtual Memory and virtual machines	Ch.2
36-37	To study the performance aspects of storage systems	Storage Systems- Introduction, Reliability, Availability & RAID	Appendix D (online appendix)
38 - 39		request-level and data-level parallelism	Ch.6
40-42	To get an insight into the latest architectures	Introduction to multi-core architectures, code optimization for multi-core	Latest reference material, industry case studies, Recent research publications

Evaluation

Component	Mode	Date & Time	Weightage
Test-1	Closed Book		15%
Test-2	Closed Book		15%
Term Papers/Term Project/Lab Exercises	Open Book		40%
Comprehensive	Closed Book Open Book		20% 10%

Make-up-Policy
Make-up will be granted strictly based on prior permissions and on justifiable grounds only. There is no make up for the Term Papers/Term Project/Lab Exercises component.

Course Notices
All notices pertaining to this course will be displayed on the CS & IS Notice Board.

Chamber Consultation
To be announced in the classroom.

Instructor-In-Charge
CS G524