BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
INSTRUCTION DIVISION
FIRST SEMESTER 2016 - 2017
COURSE HANDOUT (PART II)

Date: 01 / 08 / 2016

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

Course No : **ECE F434**
Course Title : **Digital Signal Processing**
Instructor-in-charge : S. K. Sahoo
Instructors : Ramakant Yadav, BVVSN Prabhakar Rao, R Venkateswaran, S K Chatterjee, Ganesh Kumar, P Spandana,

1. Course Description:

This course deals with the design of analog filters like Butterworth, Chebyshev, Elliptic., digital filter design for both IIR & FIR filters. Different filter structures for the realization of digital filters will be discussed. Finite word length effects and Multirate DSP will be introduced. DSP Processor architecture and implementation of DSP algorithms will be part of the course, which will be emphasized upon.

2. Scope and Objective:

The course aims at enumerating the theoretical and practical aspects of modern signal processing in a digital environment. It also aims at discussing application areas with particular stress on speech and image data.

3. Text Book:
"Digital Signal Processing", Sanjit K Mitra, TMH, Third Ed., 2006.

4. Reference Books:

1. "Digital Signal Processing : Principles, Algorithms and Application", John G Proakis & D G Manolakis, PHI, 1998.
2. "Digital Signal Processing: A Practical Approach, Second Edition", Emmanuel C. Ifeachor and Barrie W. Jervis, Pearson education.
3. "Digital Signal Processing: Fundamentals and Applications", Li Tan, Elsevier.
4. "Digital Signal Processing", Oppenhiem & Schafer, Pearson Education Asia, 2002.
5. TI DSP Processor User Manuals
6. MATLAB Help
7. IEEE transactions on Computer aided design, circuits and systems, signal processing

5. Course Plan:

Lecture No.	Learning Objectives	Topics to be covered	Reference
1	Overview of the course	Introduction	-------
2	DSP Architectures	General DSP architectural aspects	Class notes

3	DSP Architectures	Numeric representation used in DSP	Class notes
4,5	DSP Architectures	Architectural details of a typical DSP processor	R5
6-9	Z- Transform and its application	Basics of Z- transform and its use for analysis of LTI systems	Chapter 6
10,11	Discrete time Fourier transform	CTFT, DTFT, Phase and group delay	Chapter 3
12	Finite length discrete transform	DFT, FFT	Chapter 5
13-16	Analog filter design	Butterworth,Chebyshev, Elliptic & Bessel Filters	Chapter 4
17	Analog filter design	Design of HP, BP and BS filters	4.5
18	Sampling	Sampling lowpass & bandpass signals	4.2, 4.3
19-21	Simple digital filters	Different LTI systems as frequency selective device.	7.1-7.4
22, 23	Digital Filter design	IIR filter design: IIT, BLT	9
24	Digital Filters	Linear phase FIR filters	7.3
25-28	Digital Filter design	FIR Filter Design	10
29, 30	Digital filter structures	Realization of IIR filters	8.4-8.8
31, 32	Digital filter structures	Realization of FIR filters	8.3, 8.9
33, 34	Finite Word-Length Effects	IIR & FIR Filters	12
35, 36	Multi rate DSP	Decimators & Interpolators	13.1, 13.2
37	Multi rate DSP	Poly phase decomposition	13.3
38	Multi rate DSP	Arbitrary rate sampling rate conversion	13.5
39	Adaptive Digital Filters	Introduction and Concepts of Adaptive filtering, Wiener Filters	RB2 10.1 – 10.3
40	Adaptive algorithms	Basic LMS algorithm	RB210.4
41	Applications of DSP	Various applications	Class note/ Chapter 14
42	Applications of DSP	Various applications	Class note/ Chapter 14

6. Take Home assignments will be announced in the class.

7. Evaluation Scheme:

S. No.	Evaluation Component	Duration Min.	weightage	Date. time, venue	Type
1	Test 1	60	20%	8/9, 8.30-9.30 AM	Closed book
2	Test 2	60	20%	25/10, 8.30-9.30 AM	Closed book
3	Lab	Regular	10%		Open book
4	Lab test		5%		Closed book
4	Assignment		5%		Open book
5	comprehensive	180	40%	12/12 AN	Closed book – 25% Open book – 15%

8. Chamber Consultation Hours: To be announced in the class.

9. Make-up Policy:

Make Up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

10. Notices: Notices regarding the course will be displayed on CMS.

Instructor - in - charge

ECE F434