BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
HYDERABAD CAMPUS
COMPUTER SCIENCE & INFORMATION SYSTEMS
FIRST SEMESTER 2016 - 2017
COURSE HANDOUT (PART II)

01-08-2016

In addition to Part I (General Handout for all courses appended to the timetable) this handout gives further details regarding the course.

Course No : **CS F342**
Course Title : **Computer Architecture**
Instructor-in-charge : **Dr G Geethakumari**
Instructors :Abhishek Thakur, Barsha Mitra

1. Scope and Objective:
This course aims at introducing the concept of computer architecture. It involves design aspects, and deals with the current trends in computer architecture. System resources such as memory technology and I/O subsystems which contribute to proportional increase in performance will also be discussed.

2. Text Book:
T1. Patterson, D.A. & J.L. Hennessy, Computer Organization and Design, Elsevier, 4th ed., 2009

3. Reference Books:
(i)Hamacher et. al, Computer Organisation, McGraw Hill, 5th ed., 2002

(ii)J.L. Hennessy & D.A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kauffmann, 5th Ed, 2012.

(iii)J. P. Hayes, Computer Organisation & Architecture, McGraw Hill, 1998.

(iv)W. Stallings, Computer Organisation & Architecture, PHI, 6th ed., 2004.

(v) Other additional material to be put up in CMS

4. Course Plan:

Lecture No.	Learning Objectives	Topics to be covered	Reference to T1
1 - 2	To understand about the overview of classes of computers	Computer Abstractions and Technology	Ch. 1
3 - 4	To learn about instructions; ISA as well as know about sample ISAs like MIPS, ARM	Instructions- language of the computer	Ch.2
5-7		MIPS Architecture & Instruction Set	Ch. 2, 3rd edn book of T1
8		Introdcution to ARM architecture	Ch 2
9 - 11	To practice arithmetic operations on integers; floating point numbers etc	Arithmetic for computers: floating point arithmetic	Ch 3
12 -13	To understand the basics of processor; learn about data path, control path	Processors: logic design conventions	Ch 4
14 - 15		Role of Performance, pipelining – design issues	Ch 4
16 - 17		Pipelined data path and control	Ch 4
18		Various types of hazards	Ch 4
19		Structural hazards	Ch 4
20 - 21		Data Hazards	Ch 4
22 - 23		Control Hazards	Ch 4
24		Branch prediction techniques	Ch 4
25		Static Branch Prediction	Ch 4
26		Dynamic Branch Prediction	Ch 4
27	To know about the organization of memroy hierarchy and learn various optimization techniques at each level	Exploiting memory hierarchy - introduction	Ch 5
28		Cache Memory Organisation	Ch 5
29-32		Measuring and improving cache performance, cache optimization	Ch 5
33 - 34		Main Memory and Interleaving	Ch 5
35		Virtual Memory and Virtual Machines	Ch 5
36-38		Performance and memory hierarchies: Cache coherence	Ch 5
39	To understand about storage systems and performance	Storage and other I/O topics	Ch 6
40		Dependability, reliability, availability	Ch 6
41 - 42		I/O performance measures, Redundant Array of Independent Disks	Ch 6

5. Evaluation Scheme:

EC No.	Evaluation Component	Duration (min)	Weightage (%)	Date, Time & Venue	Nature of Component
1	Test I	60	20	13/9, 10.00--11 AM	Closed Book
2	Test II	60	20	21/10, 10.00--11 AM	Closed Book
3	Lab exercises, Lab test	-----	20		Open Book
4	Comprehensive	180	40	14/12 AN	Closed Book

6. Chamber Consultation Hours: ***To be announced in the class***

7. Notices: Notices regarding the course will be put up on the CSIS notice board and in CMS.

8. **Makeup Policy:** No makeup exam allowed without prior permission. For lab evaluation component, there is no makeup.

Instructor - in - charge
CS F342