# TASK DISTRIBUTION:

## 👤 Akhil

### `top_mips_zybo.v`

- Connect Zybo board inputs (clock, reset, switches) to CPU.
- Map CPU outputs to LEDs.
- Ensure this module acts as the wrapper between CPU and Zybo hardware.

### `zybo_mips.xdc`

- Verify Zybo pin mappings (clock, reset, LEDs, switches).
- Ensure constraints are correctly applied in Vivado.
- Check that synthesis does not throw I/O mapping errors.

### `.gitignore`

- Keep Vivado build files out of Git.
- Maintain a clean repository by only tracking important source files.

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## 👤 Raghuram

### `mips_simple_cpu.v`

- Implement the simple CPU logic (program counter, instruction memory, basic ALU-like execution).

- Hardcode a sample program inside instruction memory.
- Make sure output is available for LEDs in the top module.

### `tb_mips.v`

- Write the testbench to simulate CPU operation.
- Provide clock and reset signals.
- Monitor outputs (program result should be visible in simulation).

### `README.md`

- Document the purpose of the project.
- Write step-by-step setup for Vivado (add sources, add constraints, simulate, synthesize, generate bitstream).
- Describe expected result on Zybo board (LEDs show `1111` for output 15).