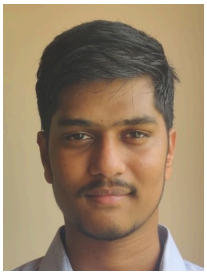
Mantri Vardhan

vardhanmantri1@gmail.com
+91 8790075669
Visakhapatnam, Andhrapradesh
linkedin.com/in/mantri-vardhan-014821304



Profile

A cross-disciplinary team player passionate about Embedded Systems, IoT, Antenna Design, VLSI. Beyond technical expertise, a suite of valuable soft skills, including effective communication, teamwork, adaptability, and a keen problem-solving mindset, are my strengths.

Education

2021 – 2025
India

Bachelor of Technology in Electronics and Communication, Amrita Vishwa Vidyapeetham
CGPA:9.42

Projects

11/2023 – 01/2024

Enhanced Mutual Coupling Reduction Through E-Shaped Resonators in MIMO antenna array systems (5G,RF engineering)

- **Objective**: To design and implement an E-shaped resonator-assisted MIMO antenna design for mutual coupling reduction in order to improve antenna efficiency and performance.
- **Tools Used**: ANSYS HFSS for simulation.
- **Outcome**: Achieved considerable reduction in mutual coupling, confirmed through simulations and experimental tests, significantly improving antenna efficiency and performance.

05/2024 – 07/2024

Real time-Voice Based Gender Recognition using MATLAB (Signal Processing)

- **Objective**: To develop a real-time gender recognition system using voice input, leveraging power spectral density analysis in MATLAB for security-related applications.
- **Tools Used**: MATLAB for signal processing, power spectral density analysis, and real-time voice input handling.
- **Outcome**: Successfully implemented a gender recognition system that accurately classifies gender based on voice input, offering potential applications in security and authentication systems.

05/2022 – 07/2022

Waste Management, An IoT-Based Smart Dustbin System for Waste Segregation

- **Objective**: To develope a smart dustbin that segregates waste into organic, recyclable and non recyclable and also an alert system to alert the sanity workers when the bin is full.
- **Tools used**: Sensors(Ultrasonic sensor, color sensor), Actuators(Servo motors), Communication(Bluetooth module), Buzzer. Arduino UNO
- **Outcome:** Successfully created a system that automatically sorts waste based on bag color and notifies sanitary cleaners via Bluetooth when bins are full enabling more efficient waste management and ensuring timely disposal of waste.

11/2023

Interactive 4-Bit Adder and Subtractor Simulation using LPC2148 and Proteus, Mini Project

- **Objective**: Designed a circuit integrating addition and subtraction functionality with dynamic mode selection.
- **Outcome**: Achieved a functional and interactive simulation of a 4-bit adder/subtractor, demonstrating efficient use of microcontroller and circuit design principles.

03/2024 – 04/2024

Smart and Sustainable: Verilog HDL Integration in Laundry Machine Control (VLSI,FPGA)

- **Objective**: To design and implement a smart and sustainable laundry machine (Mealy finite state machine) control system using Verilog HDL, incorporating weight sensing and safety mechanisms to optimize performance and resource efficiency.
- **Tools Used**: Xilinx Vivado Suite, Model Sim for simulation and synthesis, FPGA Board (Digilent Basys3 Xilinx Artix-7), Verilog Hardware description language.
- **Outcome**: Successfully designed a laundry mealy state machine control system.

10/2023 – 03/2024

Comparative Analysis of Various Adder Architectures using FPGA: Evaluating Delay, Area, Temperature and Power Efficiency Across 4-32 Bit Widths (FPGA,VLSI)

- **Objective**: To compare and evaluate various adder architectures based on delay, area, and power efficiency across varying bit widths to determine the most suitable design for different applications using FPGA.
- **Tools Used**: Xilinx Vivado Suite for simulation, synthesis and Implementation, FPGA Board (Digilent Basys3 Xilinx Artix-7), Verilog Hardware description language.
- **Outcome**: Successfully identified the most efficient FPGA adder designs for each specific bit-width.

09/2024 – present

Low Power-Programmable Feedback Shift Register for Cryptographic Applications

- **Objective:** To develope a Programmable Feedback Shift Register (PFSR) inorder to achieve unpredictability and statistical randomness, outperforming traditional LFSRs in sequence generation and security.

Internships

08/2023 – 09/2023 **Training in Ansys HFSS, Piezo and MEMS,** ARK INFOSOLUTION PVT. LTD.
- Gained comprehensive proficiency in the ANSYS software.

2023 **Telecommunications Intern,** BSNL Visakhapatnam
- Through my internship at BSNL, I gained experience in telecom network operations, encompassing main distribution frames, power plants, switching centers, and more. This exposure provided valuable insights into the intricacies of telecommunications infrastructure and industry practices.

Research Publications (IEEE)

06/29/2024 **Comparative Analysis of FPGA Adder Architectures: Evaluating Delay, Area, and Power Efficiency Across Different Bit Widths,** IEEE International Conference on " Information Science, Computing, Communication, Instrumentation and Automation" 2024
- The paper presents a comprehensive evaluation of various adder architectures using FPGA, focusing on key metrics such as delay, area, and power efficiency. It analyzes performance across different bit widths to identify the most efficient designs for specific applications.

08/24/2024 **Smart and Sustainable: Verilog HDL Integration in Laundry Machine,**
4h IEEE International conference ASIANCON 2024 ,Pune, India and Sponsored by AICTE New Delhi
- The paper explores the integration of Verilog HDL in laundry machines to enhance smart and sustainable functionalities. It examines how Verilog HDL can optimize control systems, improve energy efficiency, and provide advanced features in modern laundry appliances.

09/21/2024 **A Comparative analysis of Electrical Characteristics in Bulk, PD, FD and Optimized SOI MOSFETs,**
2024 IEEE International Conference on Communication, Computing and Energy Efficient Technologies
- The paper offers a detailed comparative analysis of various characteristics of Bulk, Partially Depleted (PD), Fully Depleted (FD), and Optimized SOI MOSFETs. It evaluates their performance metrics to highlight the advantages and limitations of each type for various applications in semiconductor technology.

Areas of Interest

- Microcontrollers and Microprocessors
- IoT
- Analog Electronics
- Digital Electronics
- Real time OS
- VLSI
- Linear Integrated Circuits
- Radio Frequency Engineering

Technical skills

- Digital Circuit Design
- VLSI Design
- Analog Circuit Design
- Antenna Design

Software's used

- Ansys HFSS
- ModelSim-Intel®
- Proteus
- Arduino IDE
- EDA Playground
- CADENCE
- Xilinx Vivado Design Suite
- Keil µVision
- Ltspice

Programming Languages

- C Programming
- Verilog Hardware Description language
- ARM Assembly Level Language
- Embedded C

Certificates and Achievements

C for Everyone, Coursera

AMCAT, Certified in 8 different fields which include both technical and non technical.

Springfield International Mathematics Olympiad (SIMO), Secured all India rank 47th.

Association of Mathematics Teachers of India(AMTI),
Maths olympiad, where i qualified consecutively for 3 years to the final round in 7th, 8th, and 9th grade.

Responsibilities Discharged

04/2024 – present **IEEE-ComSoc Student Society Chairperson,** Special Interest Group in Humanitarian Technology
Heading an IEEE student body group with a core interest in Humanitarian technology
for improving lives and problem solving through Electronics.