universite PARIS-SACLAY

M2 Master E3A Integration Circuits Systems

TD2: Realization of Arithmetic Operator

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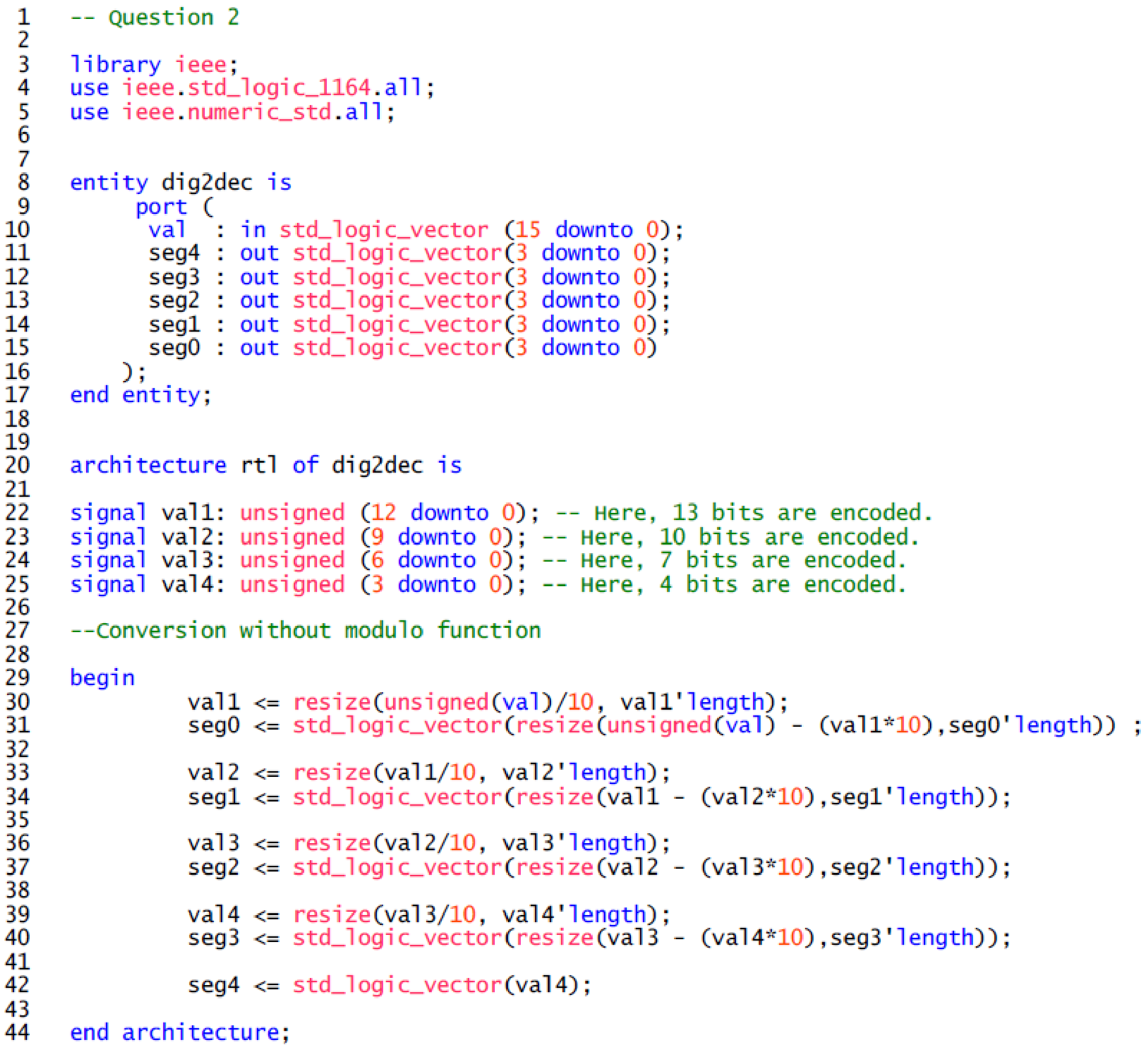
Instructor: Professor Hervé MATHIAS

Realization of Arithmetic operators

Part 1: Conversion with signal and without the modulo function

The snapshot of the code is given below:

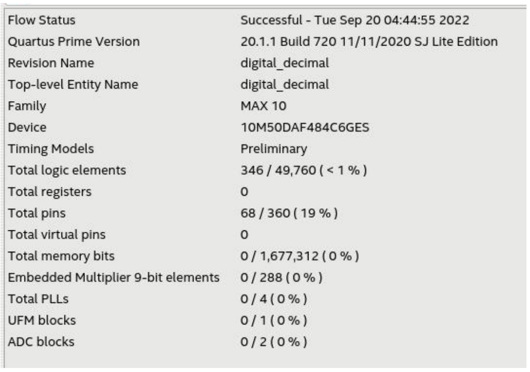


```vhdl
-- Question 2

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity dig2dec is
     port (
      val   : in std_logic_vector (15 downto 0);
      seg4 : out std_logic_vector(3 downto 0);
      seg3 : out std_logic_vector(3 downto 0);
      seg2 : out std_logic_vector(3 downto 0);
      seg1 : out std_logic_vector(3 downto 0);
      seg0 : out std_logic_vector(3 downto 0)
    );
end entity;


architecture rtl of dig2dec is

signal val1: unsigned (12 downto 0); -- Here, 13 bits are encoded.
signal val2: unsigned (9 downto 0); -- Here, 10 bits are encoded.
signal val3: unsigned (6 downto 0); -- Here, 7 bits are encoded.
signal val4: unsigned (3 downto 0); -- Here, 4 bits are encoded.

--Conversion without modulo function

begin
         val1 <= resize(unsigned(val)/10, val1'length);
         seg0 <= std_logic_vector(resize(unsigned(val) - (val1*10),seg0'length)) ;

         val2 <= resize(val1/10, val2'length);
         seg1 <= std_logic_vector(resize(val1 - (val2*10),seg1'length));

         val3 <= resize(val2/10, val3'length);
         seg2 <= std_logic_vector(resize(val2 - (val3*10),seg2'length));

         val4 <= resize(val3/10, val4'length);
         seg3 <= std_logic_vector(resize(val3 - (val4*10),seg3'length));

         seg4 <= std_logic_vector(val4);

end architecture;
```

The table for vectors val1 to val4 is given below:

Vector name	Bit size
val1	13 bits
val2	10 bits
val3	7 bits
val4	4 bits

Compilation report

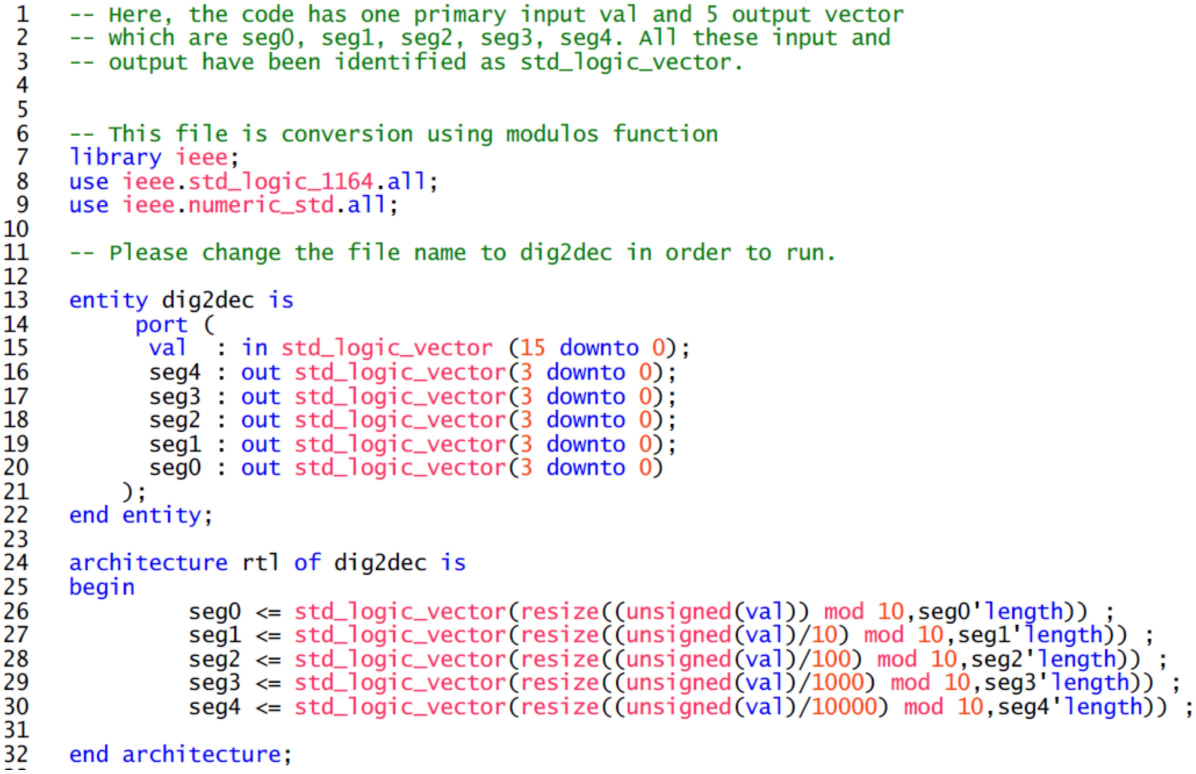


Flow Status	Successful - Tue Sep 20 04:44:55 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	digital_decimal
Top-level Entity Name	digital_decimal
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	346 / 49,760 (< 1 %)
Total registers	0
Total pins	68 / 360 (19 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Number of logic elements used is 346 out of 49760 which represents <1%.

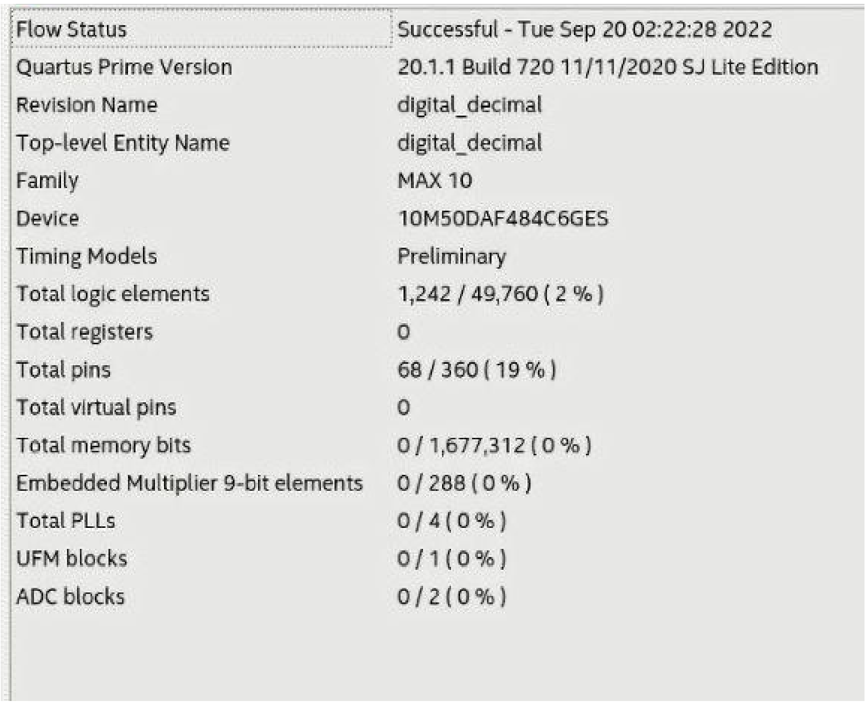
Part 2: Conversion with modulo function

Code:



```
-- Here, the code has one primary input val and 5 output vector
-- which are seg0, seg1, seg2, seg3, seg4. All these input and
-- output have been identified as std_logic_vector.


-- This file is conversion using modulos function
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- Please change the file name to dig2dec in order to run.

entity dig2dec is
     port (
      val  : in std_logic_vector (15 downto 0);
      seg4 : out std_logic_vector(3 downto 0);
      seg3 : out std_logic_vector(3 downto 0);
      seg2 : out std_logic_vector(3 downto 0);
      seg1 : out std_logic_vector(3 downto 0);
      seg0 : out std_logic_vector(3 downto 0)
    );
end entity;

architecture rtl of dig2dec is
begin
         seg0 <= std_logic_vector(resize((unsigned(val)) mod 10,seg0'length)) ;
         seg1 <= std_logic_vector(resize((unsigned(val)/10) mod 10,seg1'length)) ;
         seg2 <= std_logic_vector(resize((unsigned(val)/100) mod 10,seg2'length)) ;
         seg3 <= std_logic_vector(resize((unsigned(val)/1000) mod 10,seg3'length)) ;
         seg4 <= std_logic_vector(resize((unsigned(val)/10000) mod 10,seg4'length)) ;

end architecture;
```

Compilation report:



Flow Status	Successful - Tue Sep 20 02:22:28 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	digital_decimal
Top-level Entity Name	digital_decimal
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	1,242 / 49,760 (2 %)
Total registers	0
Total pins	68 / 360 (19 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

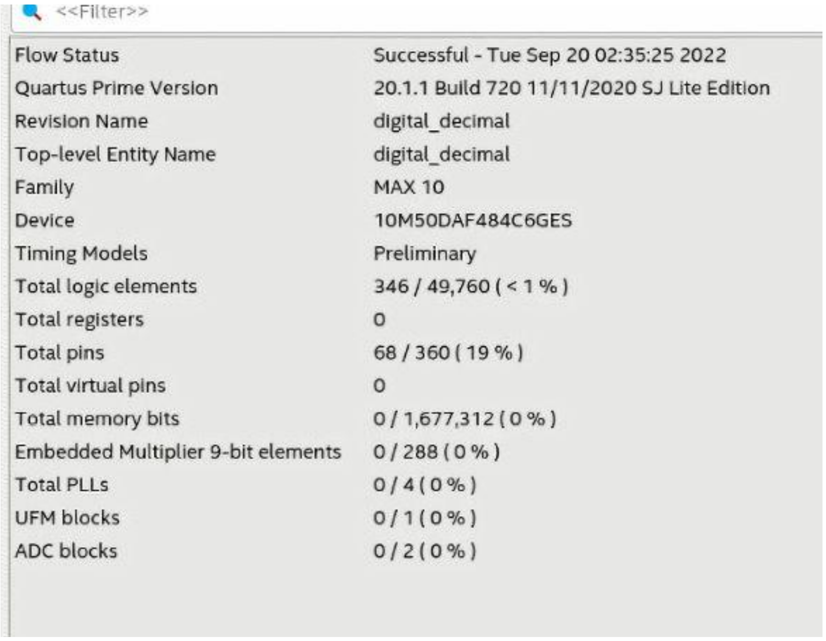
The number of logic elements used is 1,242 out of 49760, representing 2%.

Part 3: Conversion using variable and process

Code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- Please change the file name to dig2dec in order to run.

entity dig2dec is
     port (
      val   : in std_logic_vector (15 downto 0);
      seg4 : out std_logic_vector(3 downto 0);
      seg3 : out std_logic_vector(3 downto 0);
      seg2 : out std_logic_vector(3 downto 0);
      seg1 : out std_logic_vector(3 downto 0);
      seg0 : out std_logic_vector(3 downto 0)
    );
end entity;


architecture rtl of dig2dec is
    begin

      p_decim : process(val)
        variable val4 : unsigned(3 downto 0) ;  -- val4=E(val/10000) between 0 and 5 (minimum 3 bits)
        variable val3 : unsigned(6 downto 0) ;  -- val3=E(val/1000) between 0 and 50 (minimum 6 bits)
        variable val2 : unsigned(9 downto 0) ;  -- val2=E(val/100) between 0 and 500 (9 bits minimum)
        variable val1 : unsigned(12 downto 0) ; -- val1=E(val/10) between 0 and 5000 (minimum 13 bits)
        begin

         val1 := resize(unsigned(val)/10,val1'length) ;     -- we calculate the successive divisions by powers of 10
         val2 := resize(val1/10,val2'length) ;
         val3 := resize(val2/10,val3'length) ;
         val4 := resize(val3/10,val4'length) ;  -- we calculate the successive divisions by powers of 10

         seg0 <= std_logic_vector(resize(unsigned(val) -val1*10,seg0'length)) ;
         seg1 <= std_logic_vector(resize(val1-val2*10,seg1'length)) ;
         seg2 <= std_logic_vector(resize(val2-val3*10,seg2'length)) ;
         seg3 <= std_logic_vector(resize(val3-val4*10,seg3'length)) ;
         seg4 <= std_logic_vector(val4) ;

      end process ;

end architecture;
```

Compilation Report:



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Flow Status	Successful - Tue Sep 20 02:35:25 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	digital_decimal
Top-level Entity Name	digital_decimal
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	346 / 49,760 (< 1 %)
Total registers	0
Total pins	68 / 360 (19 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

The number of logic elements used is 346 out of 49760, representing <1%.

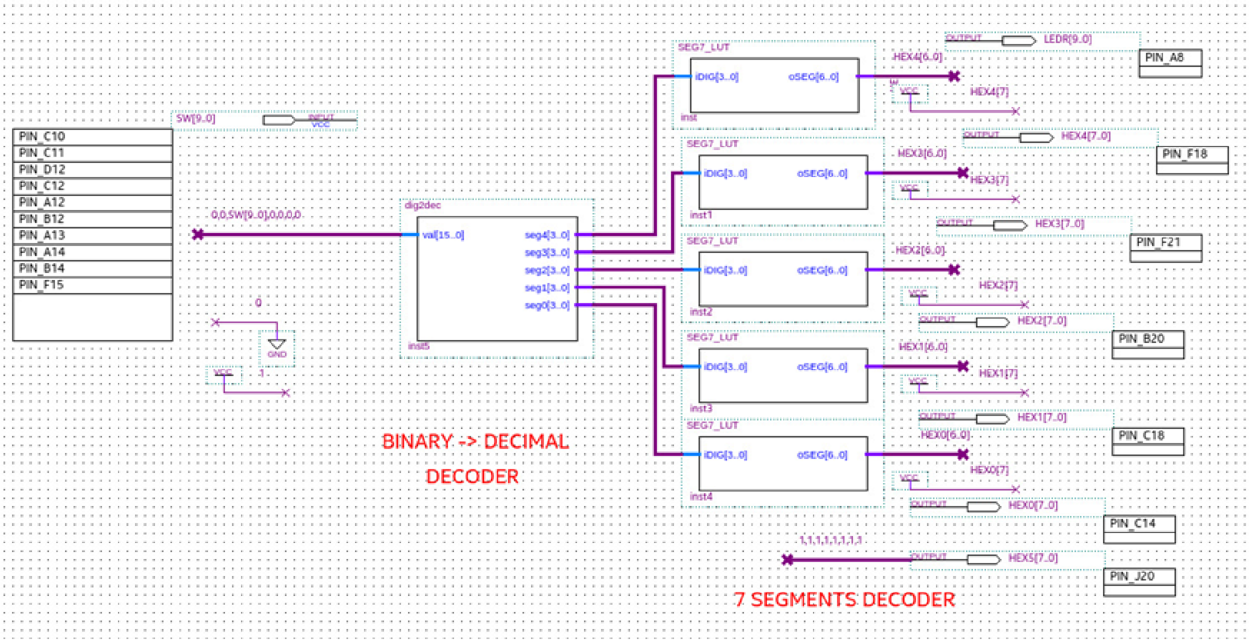

Figure: Circuit Diagram

Conclusion

In this practical session, the realization of a 16-bit binary/decimal converter has been implemented using different architectures while comparing the number of logic elements used in each case. It can be seen that with the use of modulo function, more number of logic elements (1,242 out of 49,760) are utilized whereas using process and variables as well as signals 346 out of 49760 logic elements are used. Notably, with the use of process we arrived at the same result.