

$$\begin{aligned} P &= E/t \\ P &= E/t \\ b \end{aligned}$$

E:

-Vas Mathieu:  $I_s = C \frac{dV}{dt}$   $V_{DS} = V_{GS} - V_{T\pm}$   $\textcircled{A} 3 \text{ nm}$

Cell Design for Digital Integrated Circuits.

$V_{TN} \approx 0.4V$   
 $V_{TP} \approx -0.4V$

freq  $\rightarrow$  3-4 GHz

$$K_n = \frac{1}{2} \mu_{n\text{on}} \cdot C_{\text{ox}} \frac{W_n}{L_n} \rightarrow \text{Nmos}$$

Performance Criterions  
- Area/ Cost of gate

Structural Design of Digital cts

Integrated Logic  
- Physical Variables - e.g. Current, Voltage.

Pmos  $\rightarrow$  logic '1'  
Nmos  $\rightarrow$  logic '0'

P:

$\rightarrow$  function of form  $P = \sum_i X_i$   $\leftarrow$  inputs.

$A \cdot B \rightarrow$  and  
and then  
not gate.

$$P = \frac{CV}{t}$$

$$V = IR$$

④ Primitive?  
A B C  
not needed

or  
Nmos-parallel  
Pmos-series | Nmos → Nand → series and.

$$F = \bar{C} \cdot \bar{A} \cdot \bar{B} = \bar{C} \cdot (\bar{A} + \bar{B})$$

Example  $F = A \cdot B + C$

0 0 0

0 0 1

0 1 0

0 1 1

1 0 0

1 0 1

1 1 0

1 1 1

0 0 0

0 0 1

0 1 0

1 1

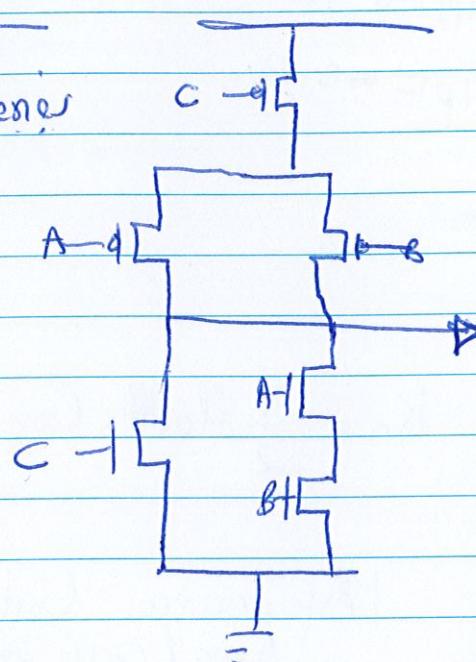
0 0

0 1

1 0

1 1

$$\bar{F} = A \cdot B + C$$



$$\bar{A} \bar{B} + \bar{B} = \bar{B}$$

$$F = \bar{A} \cdot \bar{B} + B \cdot C + A \cdot \bar{C}$$

$$= \bar{A} \cdot B \cdot (A + C) + A \cdot \bar{C} \xrightarrow{\text{so far}} \text{Nmos}$$

Ques.

~~majority~~

$$= \bar{A} \bar{B}, \bar{B} \bar{C}, \bar{A} \bar{C}$$

$$= (\bar{A} + \bar{B}) (\bar{B} + \bar{C}) (\bar{A} + \bar{C})$$

$$= \bar{A} \bar{B} + \bar{A} \bar{C} + \bar{B} \bar{C}$$

$$\text{then } F = \bar{A} \bar{B} + \bar{B} = \bar{B}$$

$$= (\bar{A} \bar{C} + \bar{B}) (\bar{A} \bar{B} + \bar{C}) \xrightarrow{\text{majority}}$$

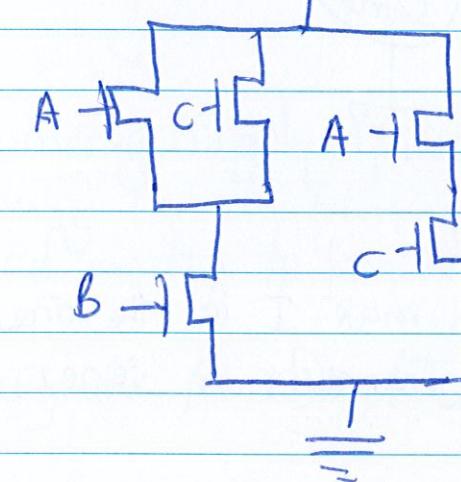
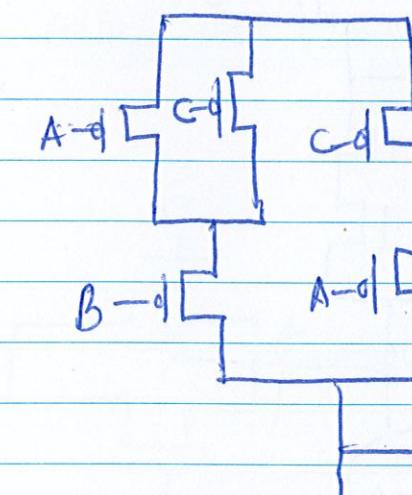
$$= \bar{A} \bar{C} + \bar{B} \bar{A} + \bar{B} \bar{C} \rightarrow \text{Pmos} \rightarrow \text{Same as N but inverted}$$

$$\text{further } = \bar{B} (\bar{A} + \bar{C}) + \bar{C} \bar{A} \checkmark \rightarrow \text{Pmos}$$

→ less propagation time

if carry is C  
→ 2 Tp.

otherwise  
3 Tp in the  
complementary  
design

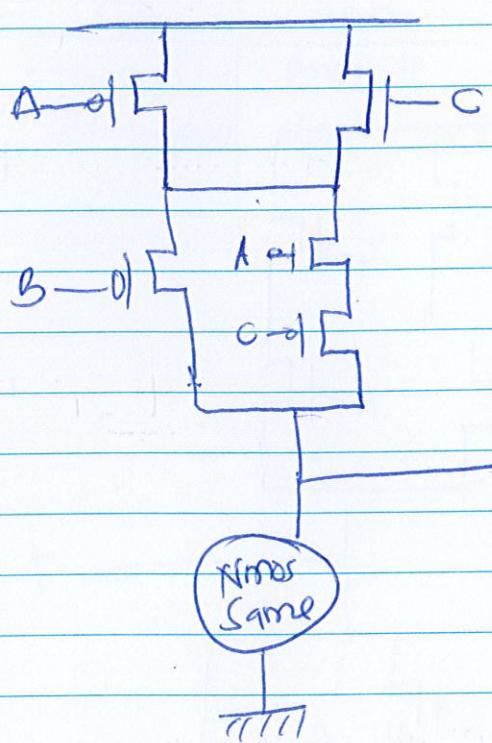


Majority gate

- used for arithmetic. ④ If many of them are 1 we have carry

Using dual network method.

→ Same NMOS.



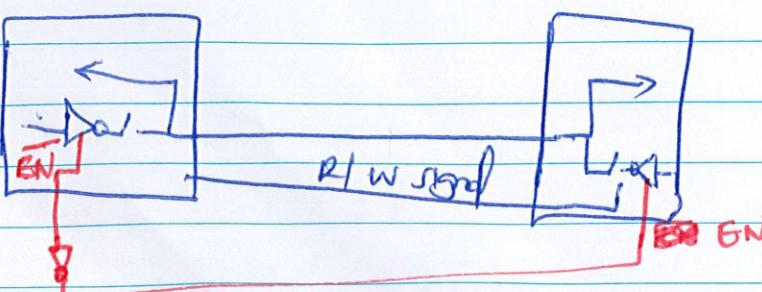
15/ CMOS logic

Body effect  $\rightarrow$  max  $I$  is the one of the less efficient Transistor in series

NAND 6  $\rightarrow$  6 input.

$T_{P2} \rightarrow$  only 2 input changes R  $\rightarrow$  rise, F  $\rightarrow$  fall.  $\downarrow$  propagation time.

Too many transistors in series  $\rightarrow$  too much ~~delay~~  $\rightarrow$  too much ~~delay~~



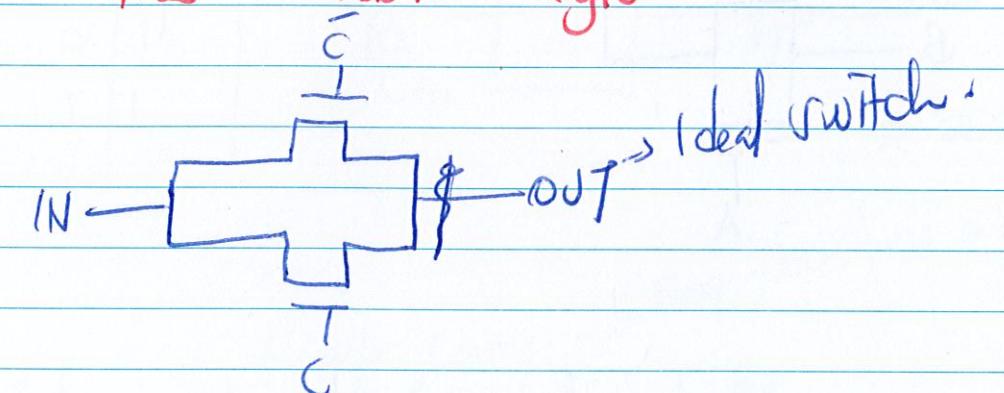
Pg 17

$\rightarrow$  when  $en$  is 1  $\rightarrow$  behaves like inverter  $\rightarrow$

$\rightarrow$  high impedance state (not working).

$\rightarrow$  forbidden case  $\rightarrow$  set hence not wanted.

Pass Transistor Logic



$\rightarrow$  no energy supply (passive)

$\rightarrow$  energy comes from previous gate.

$\rightarrow$  used mainly to transmit  $\delta$  of analog signal.

$P_1, \dots, P_4 \rightarrow$  signals from outside.  $\rightarrow$  kind of MUX. to choose between  $P_1, P_2, \dots$

$\rightarrow$  get A and B.

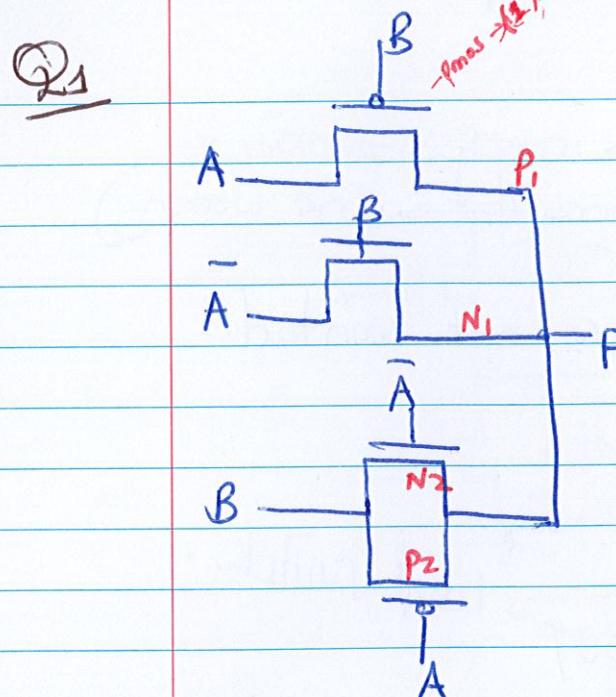
$$\text{green } \overline{A \cdot \overline{B}} = \overline{A} + B$$

$$(\overline{B}, A, \overline{A}) \rightarrow \text{OR gate.}$$

Non-exclusive

If  $C=0$   $\&$  If  $D=1$ .

$$\text{XOR} = A \cdot \bar{B} + \bar{A} \cdot B$$

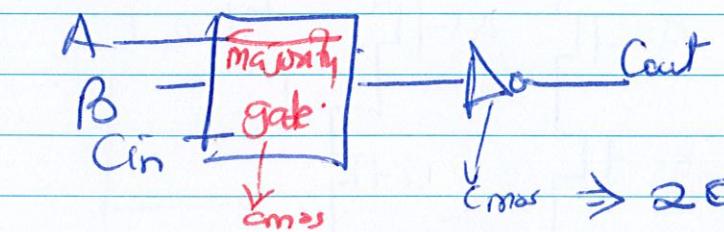
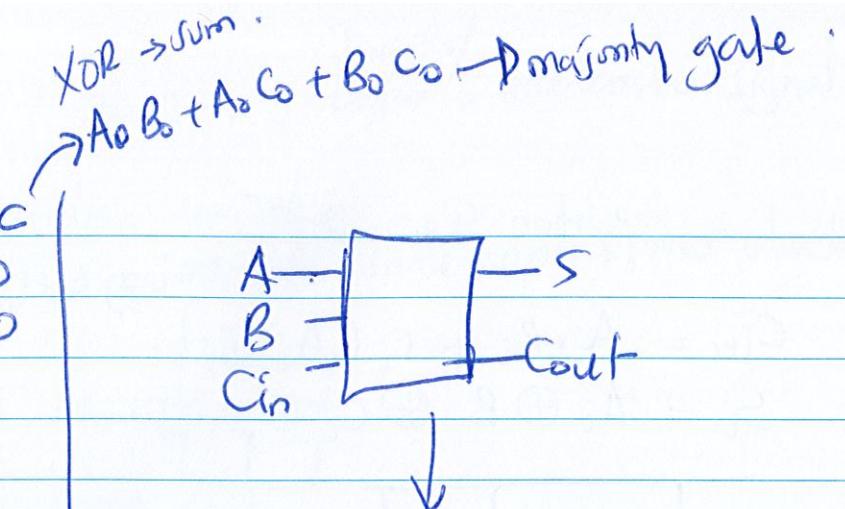


A	B	N <sub>1</sub>	P <sub>1</sub>	N <sub>2</sub>	P <sub>2</sub>	F
0	0	OFF	ON	ON	ON	0
0	1	ON	OFF	ON	ON	1
1	0	OFF	ON	OFF	OFF	1
1	1	ON	OFF	off	off	0

XOR.

Q2

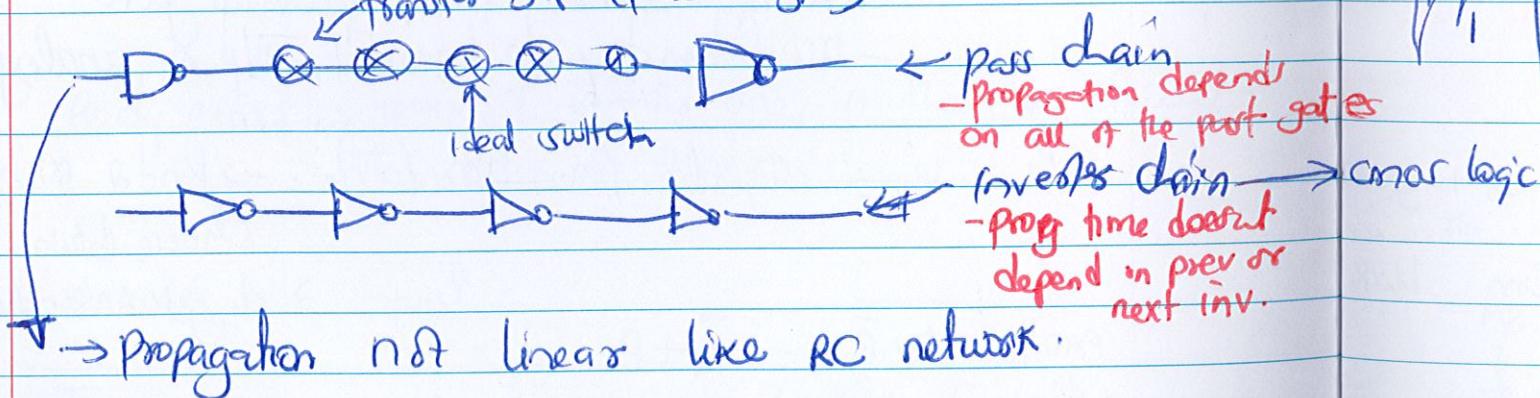
A	B	C	A+B+C	F	S	C
0	0	0	0	0	0	0
0	0	1	1	1	1	0
0	1	0	1	1	0	0
0	1	1	2	0	1	0
1	0	0	1	1	0	0
1	0	1	2	0	1	0
1	1	0	2	0	1	0
1	1	1	3	1	1	1



Propagation time  $\Rightarrow$  Propagation or carry.

30  $\rightarrow$  we accumulate propagation time like an RC network (as it is passive).

transfer gate (pass logic).

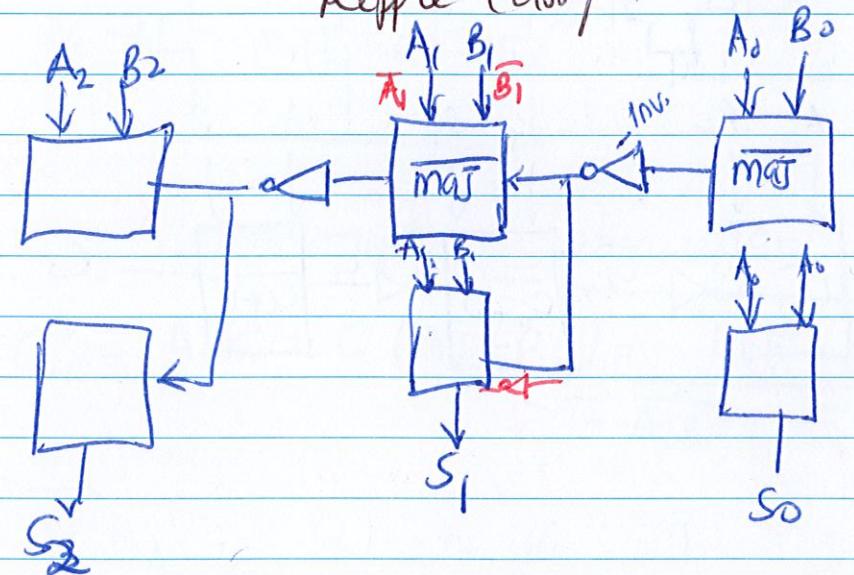


$\rightarrow$  Propagation not linear like RC network.

$\rightarrow$  We want a model with  $T_p$  only for that cell.

$\rightarrow$  use inverters every 2 or 3 pass gate  $\rightarrow$  to regenerate the signal with good rising time  $\rightarrow$  kind of an amplifier

Ripple carry



Majority then inverter

Majority is  $\bar{A}B + \bar{B}C + \bar{A}C$

if we invert  $\bar{A}B + \bar{B}C + \bar{A}C$

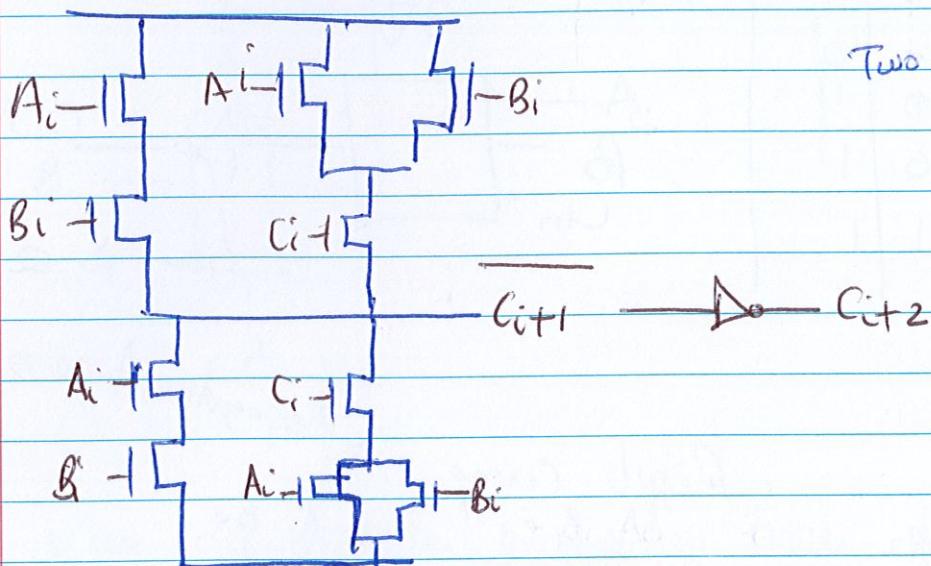
$\bar{A}, \bar{B} \rightarrow$  we remove inverters after majority.

$\rightarrow$  But not optimal has the majority gates are now slower.

Repetition Q2. 2.1

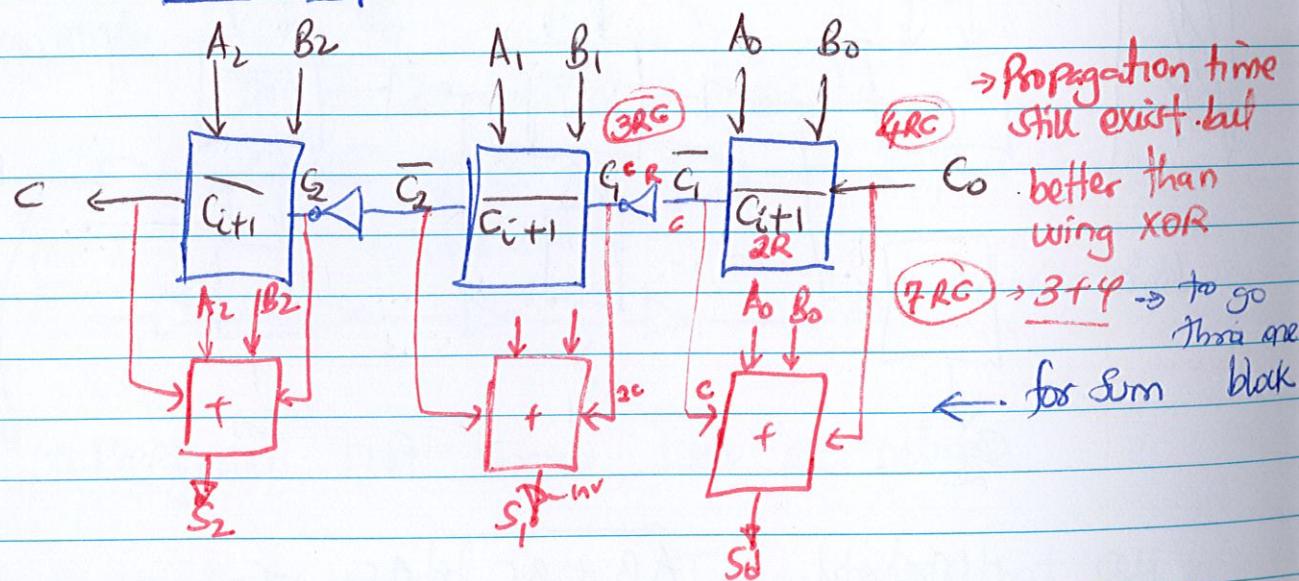
$$C_{i+1} = A_i \cdot B_i + C_i(A_i + B_i) \Rightarrow C_{i+1} = \overline{C_i + 1}$$

$$S_i = A_i \oplus B_i \oplus C_i$$



Two pairs of  $A_i \rightarrow 2C$   
 $\frac{1}{2}R$ .

$RR \rightarrow 2$  transistors



→ with old carry we have some info of sum computation.  
→ A way of using only carry. → all bits are 1. →  $C \Rightarrow 1$   
already computed carry (old carry).

$$S_i = A_i B_i C_i + \overline{C_{i+1}} (A_i + B_i + C_i)$$

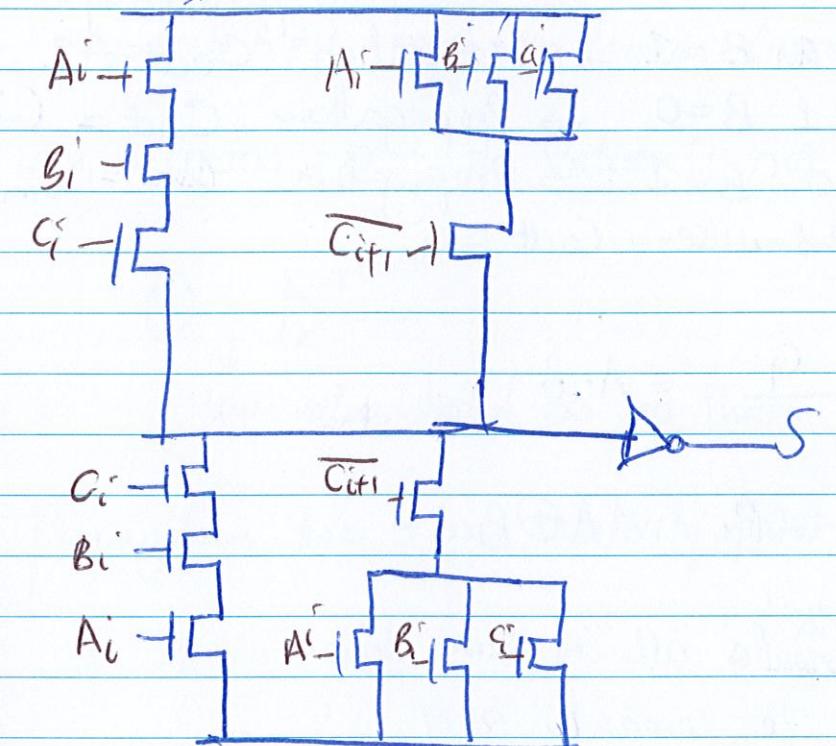
↑  
input  
carry

any old 1 → or

stripped

Computation of sum

→ same as majority gate (same NMOS & PMOS structure).

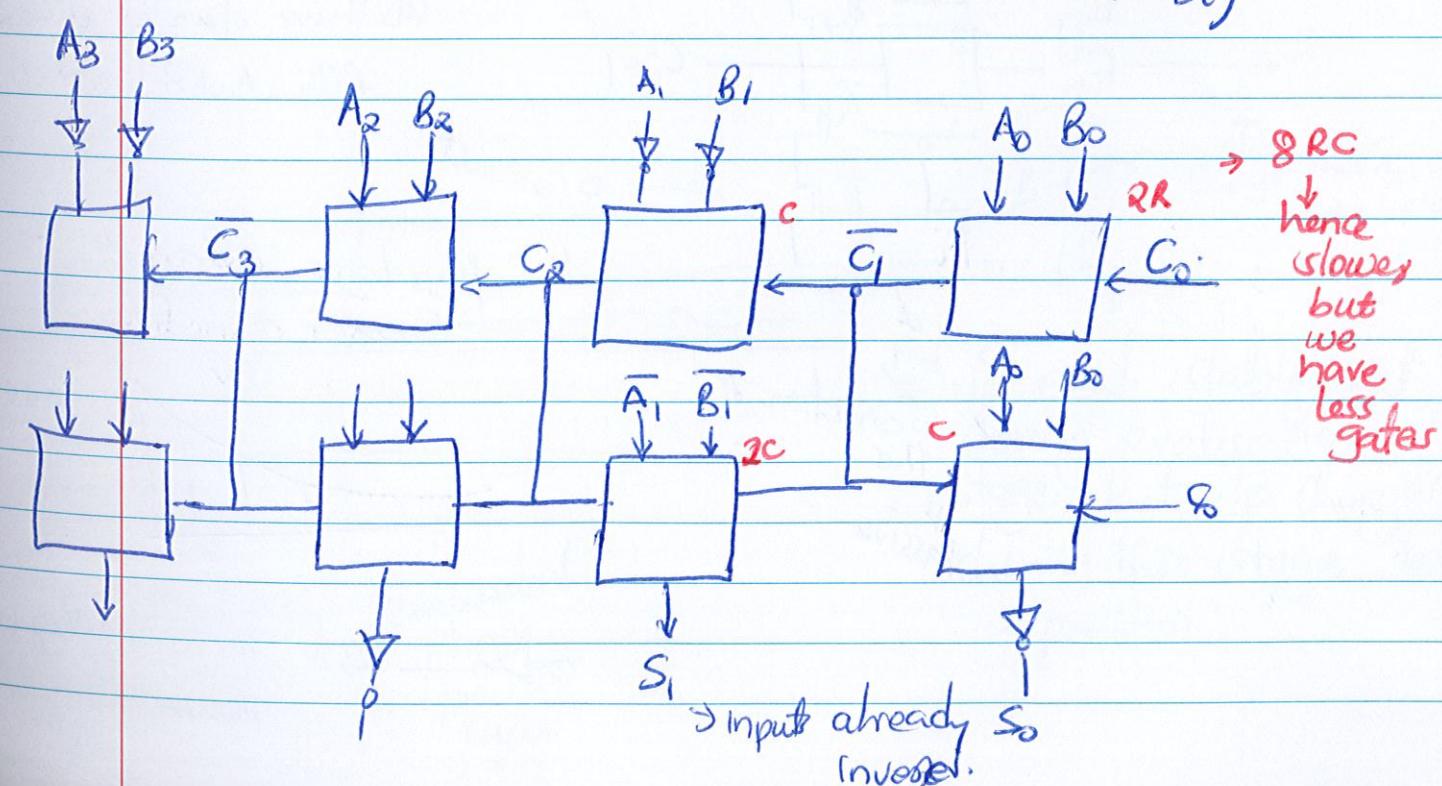


Improvement · Optimization

$$C_{i+1} = A_i B_i + C_i (A_i + B_i) = \overline{\overline{A_i B_i} + C_i (A_i + B_i)}$$

$$= \overline{A_i B_i} + \overline{C_i} (\overline{A_i} + \overline{B_i})$$

input inputs of  
compute carry  
directly

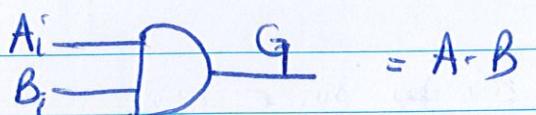


→ input already  
inverted.

Q2.2.

$C_{out} = G + PC_{in}$  if  $A \neq B$  are 1 we have  
Carry already.

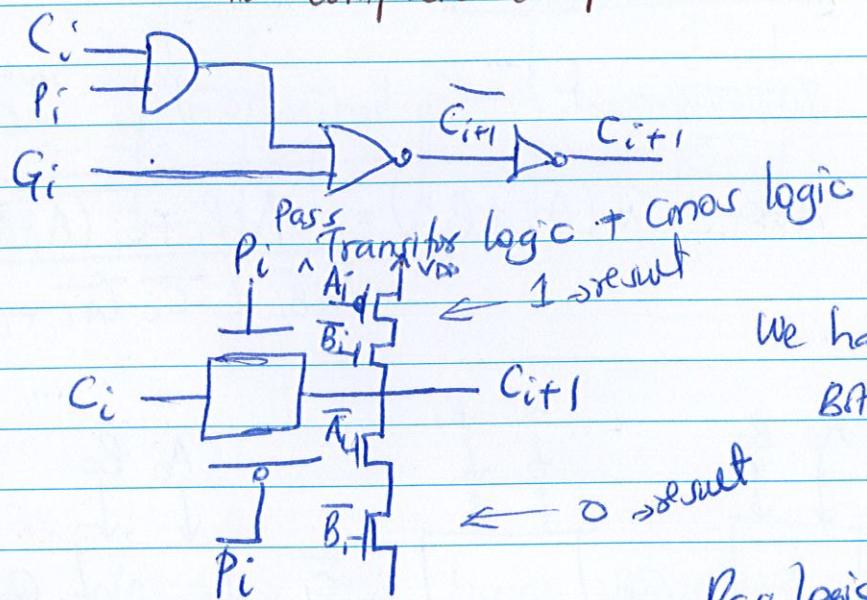
$A=1, B=1 \rightarrow$  Generation  $C_{out} = 1$   
 $A=1, B=0 \rightarrow$  propagation  $C_{out} = C_{in}$   
 $A=0, B=1 \rightarrow$  propagation  $C_{out} = C_{in}$   
 otherwise  $C_{out} = 0$



$$A_i \rightarrow P_i = A \oplus B$$

we can compute all at same time.

To compute carry.



We have  $olp = 0$  when  
Both  $A_i \neq B_i$  are 0

32 bit  
32 connection of  
this  
passive

Pass logic delay curve  
Series connection  
→ increase

hence  
→ to increase signal  
power

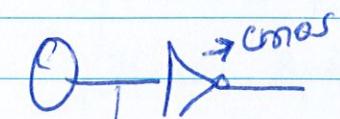
## L2: Structural Design of Digital Circuits

Pseudo-NMOS logic - 1<sup>st</sup> transistor 1970's

→ PMOS → always ON

$A=1 \neq B=1$  hence we have, current thru' gate'

When NMOS = 0, dp value is not 0 → green curve.



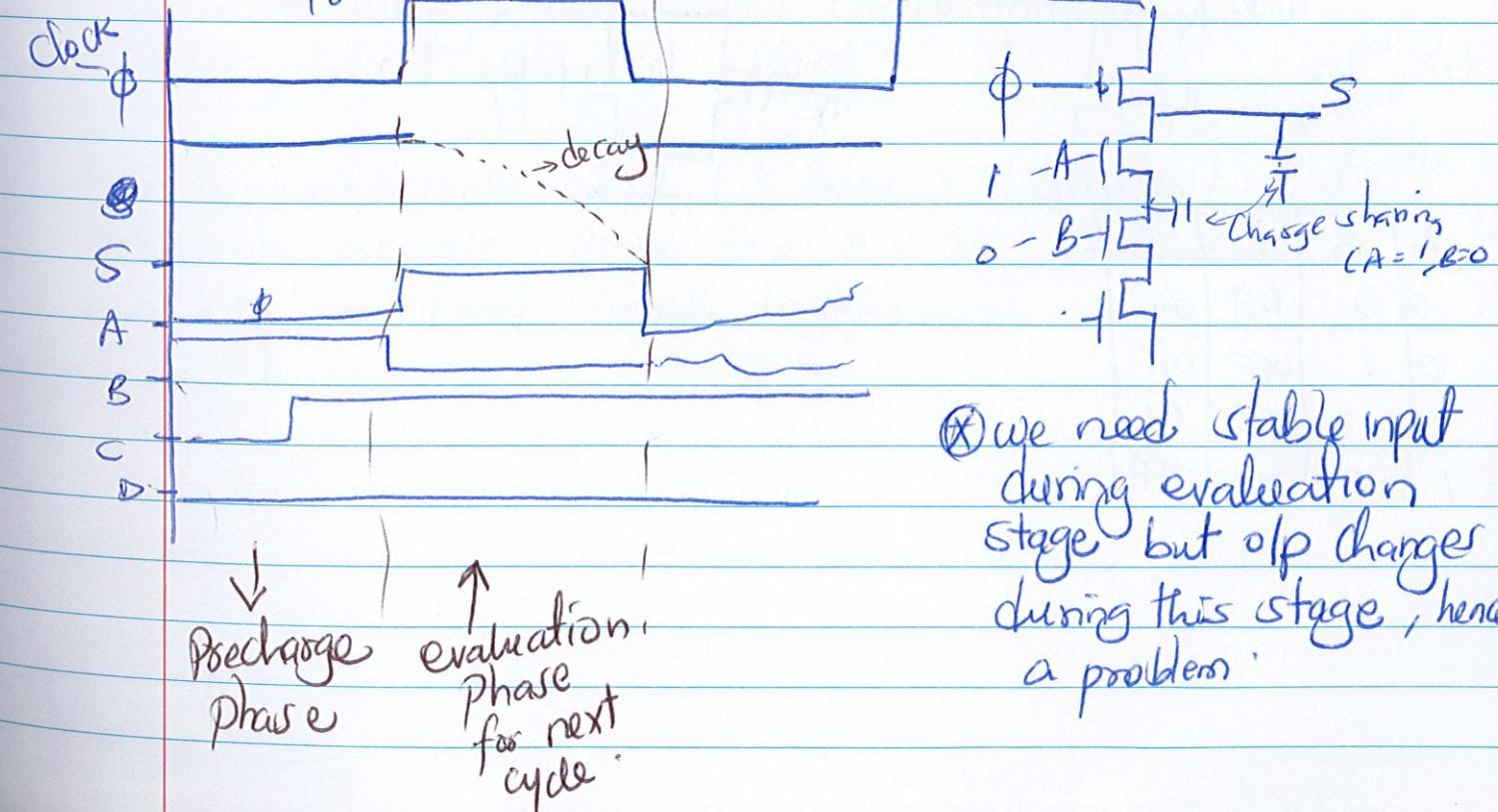
low value should be less than  $V_{TH}$

Propagation time → low resistivity PMOS

Precharge Logic

$\phi \rightarrow$  clock  
 $\phi = 0 \rightarrow S = 1 \rightarrow$  upper tran. is on

→ No path thru' A, B, C, D, E → we keep state '1'



④ we need stable input  
during evaluation  
stage but olp changes  
during this stage, hence  
a problem.

Two phases

→ 2 non-overlapping clocks

Odd-gate  $\rightarrow \phi_1$   
even  $\rightarrow \phi_2$

→ each clock cycle we go thro' one gate.

→ We have one NMOS.

### Domino Logic

→ During precharge all pmos are 0 (off)

→ only one transition 0  $\rightarrow$  1 hence no glitch

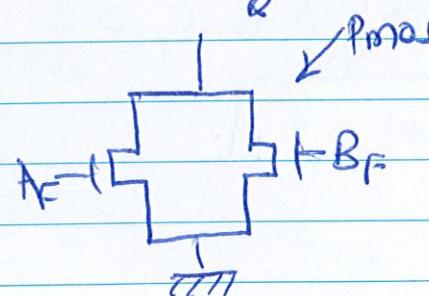
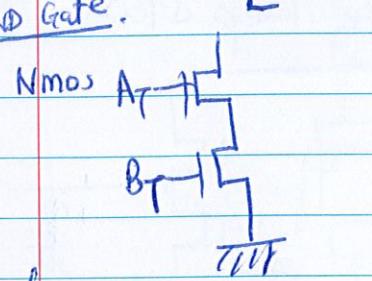
→ high speed carry (1/2 of logic  $\rightarrow$  no double capacitance).

→ Domino because: only one change.

N-P  $\rightarrow$  alternate pmos & NMOS logic

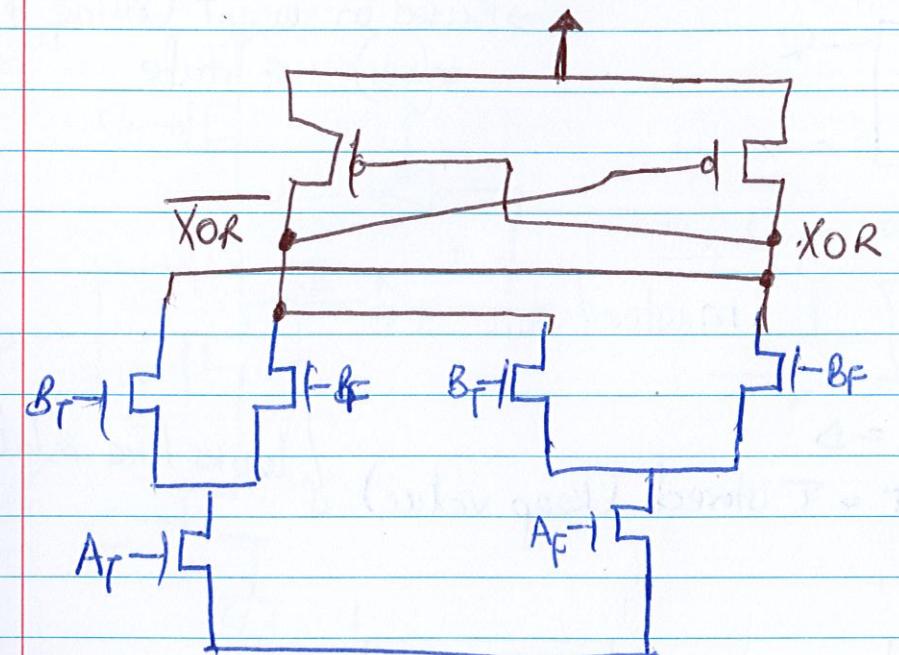
### Cascade

→ we have both the true op & its complementary  
AND gate.



A	B	L	R
0	0	OFF	ON
0	1	OFF	ON
1	0	OFF	ON
1	1	ON	OFF

### Example: XOR gate



### Differential logic

Weak pmos - highly resistive transistor. weak 1

### Applications

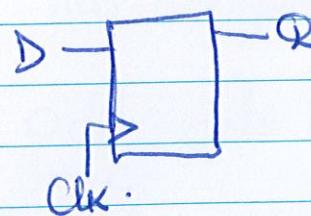
#### Current Mode

→ small swing - less power consumption  
→ using current instead of voltage

#### Adiabatic Mode

→ suppress Joule effect (1/2 power  $\rightarrow$  dissipation)  
→ slowly increase power from 0  $\rightarrow$  1  
→ only for very small logic.

## Sequential Logic

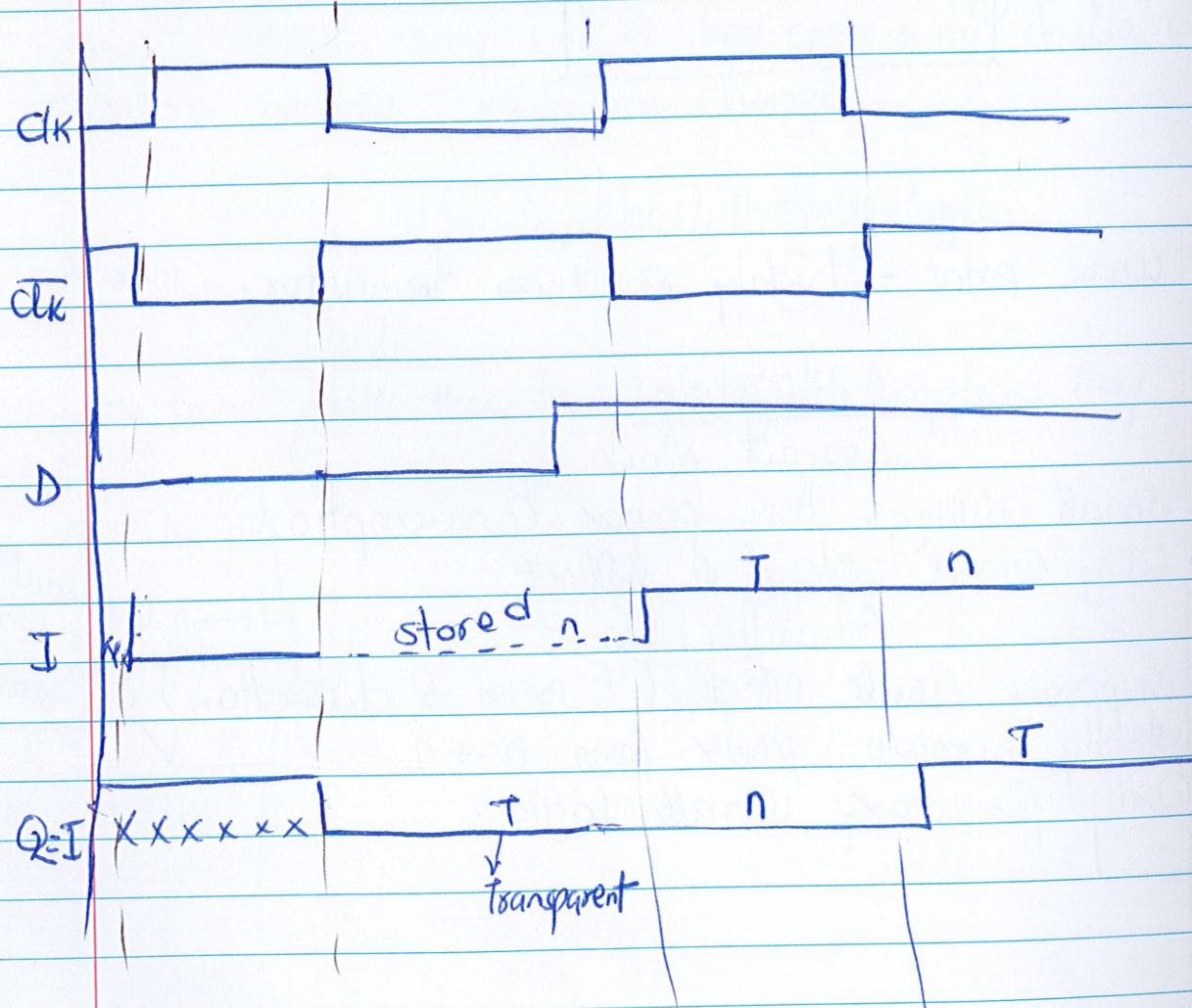


→ Based on event (rising & falling edges), not state

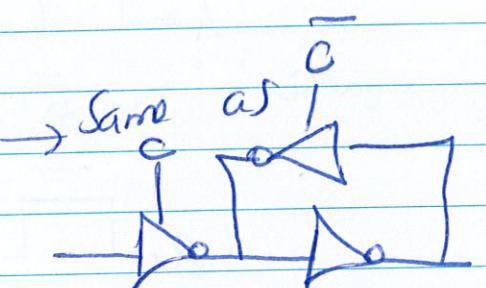
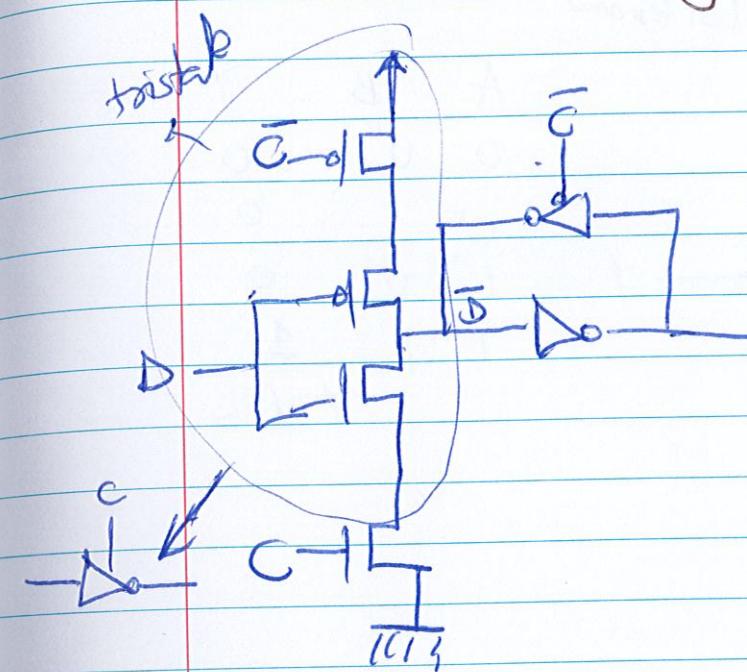
MUX

master/slave FF

state  
 $\text{Clk} = 0 \quad I = D$   
 $\text{Clk} = 1 \quad I = Q$  stored (keep value) } looks like a latch



## Practical Design: tristate inverters



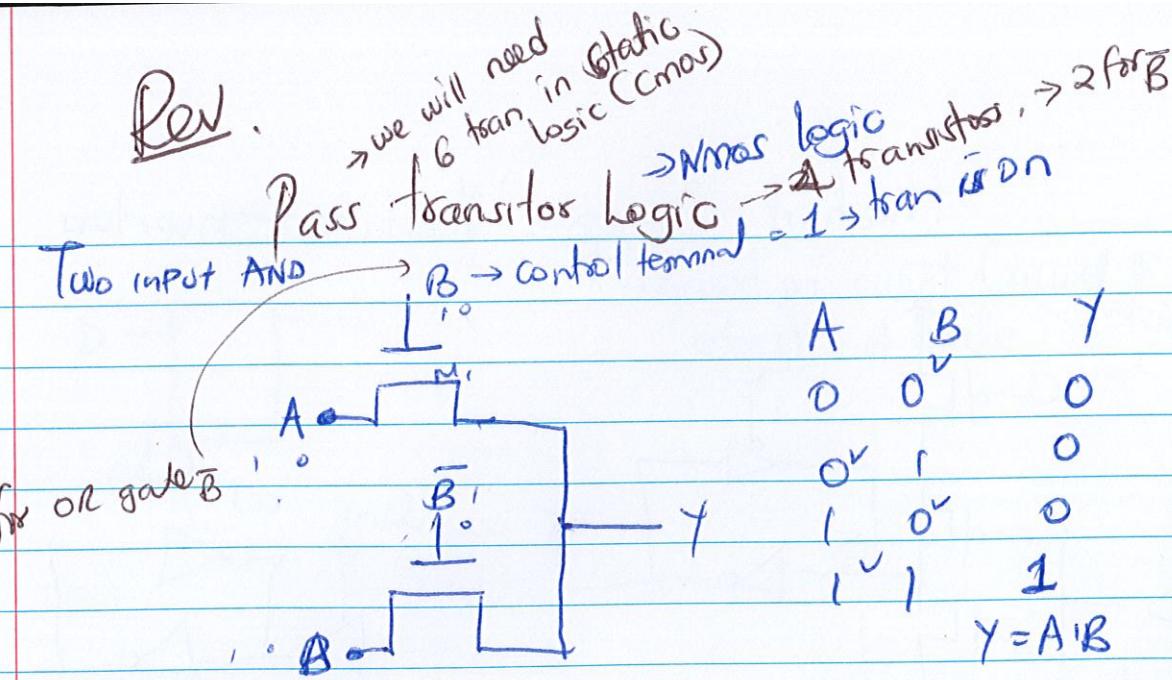
TSPC → High speed logic (in the past)

- Same clock  $\bar{C}K$
- 9 transistors
- Inverter at  $\bar{Q}P \rightarrow$  Buffer
- Clock never stops.
- Use minimum freq. (high freq.).

HW

- 
- all internal ~~clocks~~ <sup>state trans</sup> included  $\times \dots \gamma$
- state of each trans
- Conclude if it is FF

Rev. Pass transistor logic  $\rightarrow$  we will need 6 transistors in static CMOS



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$Y = A \bar{B}$