M2 Master E3A Integration Circuits Systems

Design and optimization of a digital standard-cell

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Contents

Table of Figures

Objective:

The Project aims at designing and characterizing a digital standard-cell by using Virtuoso Platform from Cadence. Moreover, a theoretical demonstration of the TSPC (True Single-Phase Clock) dynamic flip-flop has been presented. A comparison has been drawn between an inverter and that of the TSPCFF cell in terms of the propagation time. Finally, a topology has been proposed on the extraction of hold time of DFF cells.

Theorical demonstration of the behavior of the TSPC DFF cell

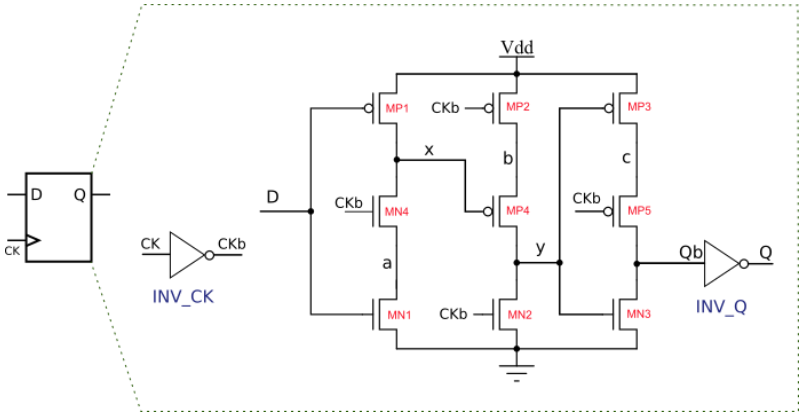

Figure 1:Schematic of the TSPCFF Cells.

The table below exhibits all the possible transition of both transistor and it's internal nodes before and after the input (clock signal or D signal) is initiated.

Table 1: Theorical demonstration of the state of the Transistor and internal nodes.

Input Signal			Internal Nodes					State Of the Transistors									Output Signal	
CK	**CKb**	**D**	**x**	**a**	**b**	**y**	**c**	**MP1**	**MN4**	**MN1**	**MP2**	**MP4**	**MN2**	**MP3**	**MP5**	**MN3**	**Qb**	**Q**
0	1	0	1	1	ZU	0	1	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ZU	U
1	0	0	1	Z1	1	Z0	1	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	1	0
1	0	1	Z1	0	1	Z0	1	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	1	0
0	1	1	0	0	0	0	1	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	Z1	0
0	1	0	1	1	Z0	0	1	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	Z1	0
0	1	1	0	0	0	0	1	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	Z1	0
1	0	1	Z0	0	1	1	0	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	0	1
1	0	0	1	Z0	1	Z1	0	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	0	1
0	1	0	1	1	Z1	0	1	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	Z0	1
1	0	0	1	Z1	1	Z0	1	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	1	0
1	0	1	Z1	0	1	Z0	1	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	1	0
0	1	1	0	0	0	0	1	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	Z1	0

It can be concluded on the basis of the truth table that the cell is functioning only on the positive edged triggered DFF.

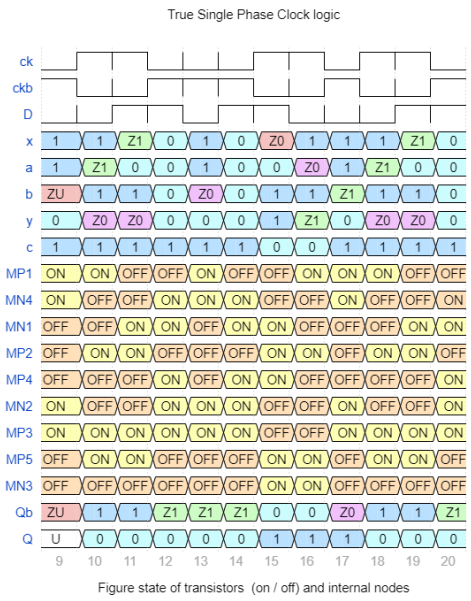

Figure 2: Waveforms of TSPCDFF cell.

From figure 2, it can be concluded that, at rising edge of the clock the output Q waits for some transition of the internal nodes to receive the input D.

Designed Layout

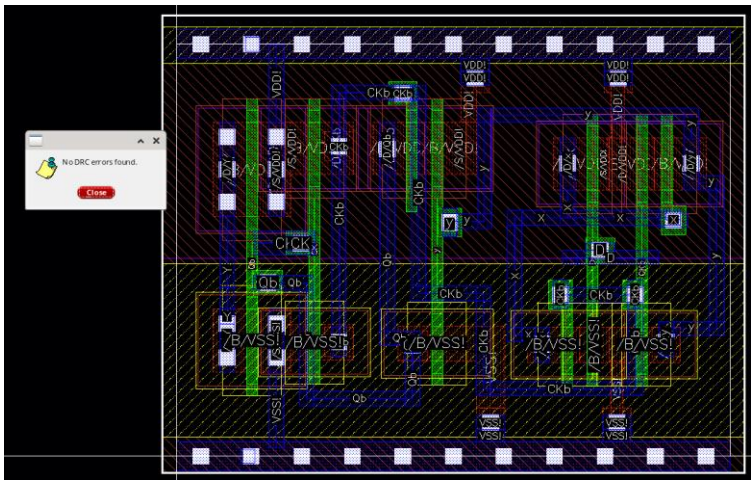

Figure 3: TSPCFF cell layout.

The entire area of the layout of this customized layout is 3.93 µunit^2(height is 1.71µ and width is 2.3 µ). The reduction of the area was made possible by chaining common nodes of the both PMOS and NMOS. The entire layout satisfies the design condition in DRC, LVS and QRC. While designing the layout, it has been kept in mind that the long lines of polysilicon connection should be as minimum. So, the trade-off was to use necessary contacts. In the whole design, around 8 M1/Poly contacts has been used. As a results, the parasitic capacitance has been added to the

design. It has been come to notice that further design optimization is possible. For example, MN4 and MN2 could be connected using polysilicon instead of using contact via. So, again it is entirely depends on the designer how he/she wants to design. While connecting contact in the MP5, an issue of the gate bent arrived. The reason was due to the overlapping of contact and oxide layer, which creates an PMOS of itself. So, a lot of attention needs to be provided. Another issue can be pointed out that some of the VDD/VSS connection was implemented by stretching the oxide layer. A better design may avoid this scenario. Finally, usage of Metal 2 has been avoided at any cost to ease the automatic routing phase.

Propagation time

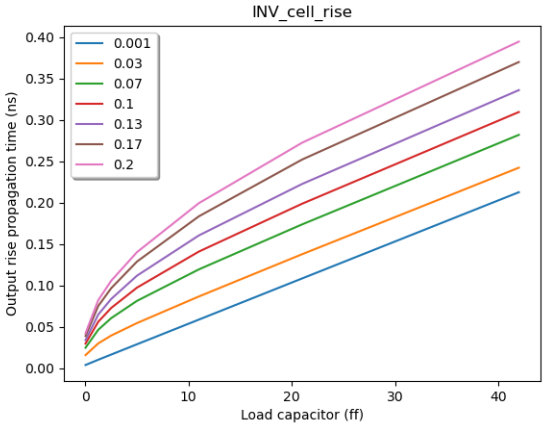

Figure 5: INV cell rise propagation.

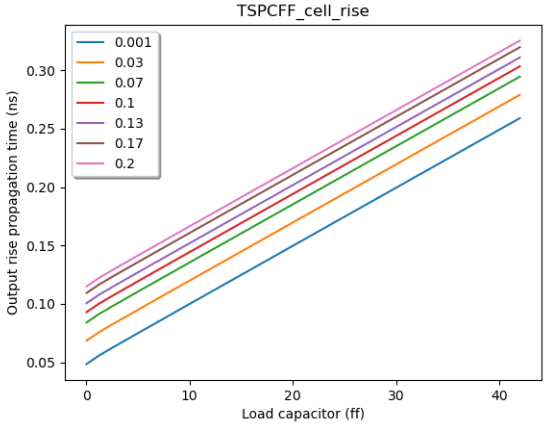

Figure 4: TSPCFF cell rise propagation.

Inverter:

The propagation time of an inverter is the timing difference between the provided falling edge input and a rising edge of output. It depends on several factors, including the technology used to construct the inverter, the input load capacitance, and the supply voltage.

$$t_{PLH} = \frac{C_L V_{DD}}{\frac{W_P}{L_P}\mu_P C_{OX}(V_{DD} + V_{TP})^2}$$

From the equation, it can be concluded that the propagation time is disproportionate to the supply voltage and proportional to the channel length. The propagation time can also be affected by the design of the inverter circuit, such as the size of the transistors used and the layout of the circuit. Additionally, the temperature and operating conditions can also affect the propagation time of the inverter.

TSPCFF:

The timing difference when the FF receives a rising edge as a clock input, and the output capacitive load has produced a rising output. It depends on factor such as specific design of the flip-flop circuit, timing of the clock signal, voltage and temperature conditions, load capacitance, input transition time, noise margin, power supply voltage.

Mean Magnitude:

By comparing the figure 4 and 5, it can be seen that, all the input slopes of the INV are packed together at the minimum load capacitance and it has low propagation time. With the increment of the load capacitance, the slopes are starts to open up and becomes almost parallel to each other and maintain equal distance between them. When it comes to TSPC DFF, the slopes are not packed together which in another word can be said that the propagation time is higher for all the slopes. Then with the increment with the load capacitance, the slope maintains steady growth. One difference can be pointed out here compared to the INV that the mutual distance of the slopes is not equal.

Effect of load capacitance:

There is a correlation between the curves in the inverter. Because only one stage is impacted by the input transition and the load capacitor. On the contrary hand, TSPC DFF has many stages and, despite the input transition being extremely slow, has a very low charge current with merely parasitic capacitance acting as the first stage's load. INV has a low initial delay time, but when input transition and load grow, the propagation time increases dramatically. It has a connection with RC Time Constant. The input slope controls the current that charges the load capacitor. The INV transition time, which is reliant on input transition, is directly related to the cause. The conclusion is that when the INV has a slower transition (low current) and a big load capacitor, the output transition is poor. Another finding is that the transition time is long for input transitions that are highly sharp. When it comes to TSPC DFF, it is not at all reliant on the clock, even under extremely heavy loads. The clock is not directly linked to the inverter. Since it is merely parasitic capacitance, the load on the first stage remains constant in the case of increment of the load capacitance. TSPC initially appears to have the poorest performance, however when load and input transition grow, the propagation duration of TSPC gradually lengthens. Therefore, the ultimate conclusion is that the input stage only relies on the clock transition rather than the load capacitance, whereas the large load capacitance only affects the output (last) stage. So, it can be said that the effect of the input slope is completely isolated from the effect of the load capacitance.

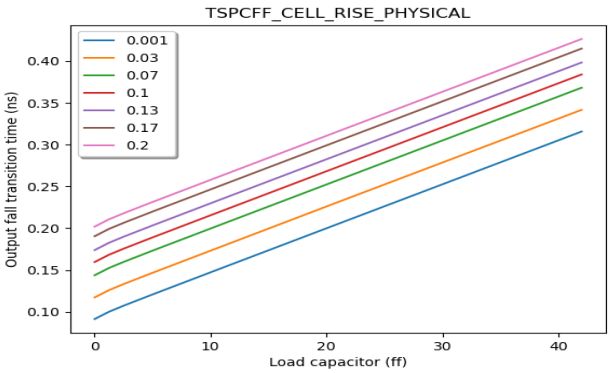

Figure 6: TSPCFF cell rise physical propagation.

Hold Time

Hold time is the minimum duration that the input data must remain steady after the clock event for it to be accurately captured by the synchronous circuit, such as a flip-flop. In other words, the

hold time refers to the amount of time the input data must be stable after the active edge of the clock in order to be reliably sampled by the circuit.

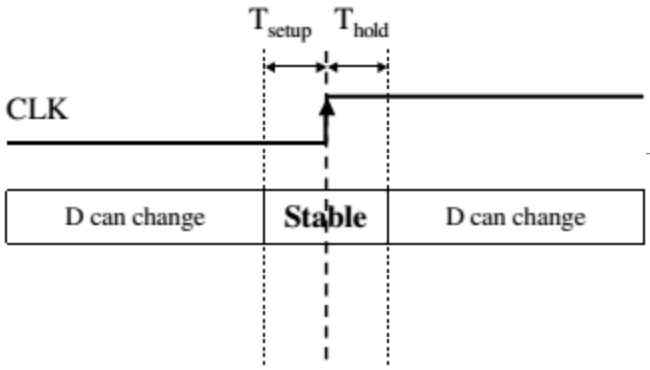

Figure 8: Setup and Hold Time.

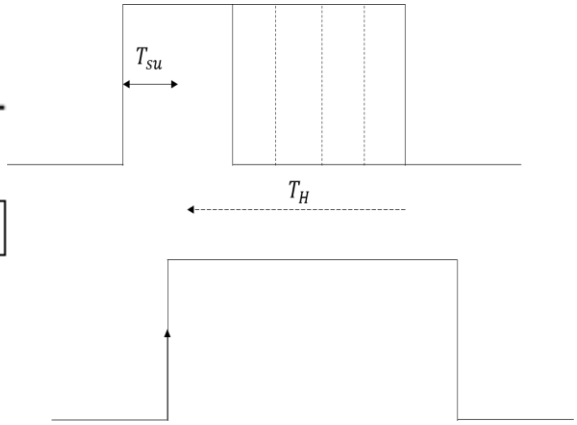

Figure 8: Setup and Hold Time.

To extract the hold time information, the falling edge of the data needs to be bring closer and closer to the active rising edge of the clock signal. The figure should look like the figure 8. At one point, a violation may occur. The point before violation can be considered as the most ideal point to have the hold time. In case, a violation may incurs, the following can be implemented to prevent it.

1. The TSPC may operate with a significant propagation delay by introducing high threshold cells which slow down the rate of state changes.
2. The propagation delay goes up as the load capacitance increases because the capacitor will take longer to charge.
3. By including buffer or delay cells, prolong the Data path's delay such that the second batch of Data does not arrive until the setup and hold time conditions have been satisfied.
4. The cells closest to the capture flip-flop should be reduced first since they are less likely to impact other pathways and introduce additional mistakes.

Conclusion

In this project, TSPC DFF cell's behaviour has been analysed. A comparison has been drawn between the INV and TSPC DFF. Moreover, using cadence, the design of TSPC DFF has been implemented and the overall size has been reduced. Additionally, a proposal has been presented to extract the hold time information.