(1)

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ID: 19101498 Section: 09 Assignment 04

1.  each block size = 1 word / 4 bytes | 32 bit memory address and initially empty

16 blocks cache

A. Total blocks in cache = 16 ⇒ $2^N = 16$, $N = 4$, index, N = 4 bit

Each block size = 1 word ⇒ $2^{m+2} = 2^2$ (4 bytes), $m+2 = 2$, $m = 0$ bit offset

Tag field size = 32 − (4+2) = 26 bit

Decimal Address	Binary Address	Hit/Miss	Cache Block
2	0000 0000 0000 0000 0000 0000 0000 0010	Miss	0000
3	0000 0000 0000 0000 0000 0000 0000 0011	Hit	0000
170	[2405] 1 0,1010 10	Miss	0000 + 1010
45	[2605] 1011 01	Miss	1011
7	[2605] 0001 11	Miss	0001
196	[2405] 11 0001 00	Miss	0001
189	[2406] 10 1111 01	Miss	1111
191	[2405] 10 1111 11	Hit	1111
215	[2405] 11 0101 11	Miss	0101
172	[2405] 10 1011 00	Miss	1011
45	[2605] 1011 01	Miss	1011
187	[2405] 10 1110 11	Miss	1110
254	[2405] 11 1111 10	Miss	1111

(1)	Index	V	Tag	Data
0	0000	0 1	0000 0000 0000 0000 0000 0000 00	Mem[2]
1	0001	0 1	[illegible] [26 05] [2405] 11	Mem[~~196~~ 7]
2	0010	0		
3	0011	0		
4	0100	0		
5	0101	0 1	[2405] 11	Mem[215]
6	0110	0		
7	0111	0		
8	1000	0		
9	1001	0		
10	1010	0 1	[2405] 10	Mem[170]
11	1011	0 1	[26 05] [2405] 10 [26 05]	Mem[~~17~~ 245]
12	1100	0		
13	1101	0		
14	1110	0 1	[2405] 10	Mem[187]
15	1111	0 1	[2405] 10 [2405] 11	Mem[~~255~~ 169]

(iii)

b. Hit Ratio = $\frac{\text{hits}}{\text{accesses}} = \frac{2}{13}$

Miss Ratio = 1 − Hit Ratio = $1 - \frac{2}{13} = \frac{11}{13}$

c. Total number of bits = $2^n \times$ (block size + tag size + valid field size)

2^n = Total blocks in cache
= 16 blocks

block size = $2^m \times 32$
↓
bit address
$= 2^0 \times 32$

tag size = bit address − (~~offset~~ index / n + byte offset)
= 32 − (4 + 2) = 26

valid field size = 1 bit

= 16 × ($2^0 \times 32 + 26 + 1$)
= 944 bits
(Ans)

d. size of Cache = 2^N
$= 2^4$
= 16

(Ans)

(2)

2. P = 32 bytes, each page = 2 bytes, 64 frames

each frame = 2 bytes = each page

A. ~~Each~~ 2 bytes → 1 page

1 bytes → $\frac{1}{2}$ "

32 bytes → $\frac{32}{2}$ = 16 page

B. each frame = each page = 2 bytes

∴ 64 frames = 2×64 = 128 bytes

C.

	Page #	Byte Address
0	0	1
1	2	3
2	4	5
3	6	7
4	8	9
5	10	11
6	12	13
7	14	15
8	16	17
9	18	19
10	20	21
11	22	23
12	24	25
13	26	27
14	28	29
15	30	31

Frame	Main Memory		Page No
7	14	15	0
9	18	19	1
11	22	23	2
13	26	27	3
15	30	31	4
17	34	35	5
19	38	39	6
21	42	43	7
23	46	47	8
25	50	51	9
27	54	55	10
29	58	59	11
31	62	63	12
33	66	67	13
35	70	71	14
37	74	75	15

(a)

Page Table

Page No	Frame NO
0	8
1	9
2	11
3	13
4	15
5	17
6	19
7	21
8	23
9	25
10	27
11	29
12	31
13	33
14	35
15	37

0. byte 8 of the process:

Logical Address

0100	0

Page (4bit) Page offset (1) bit

For: Page = 16, 4 bit required to map/ get page address

As 2 byte in a page, 1 bit is for page offset

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E. Physical Address:

Frame numbers = 64

bits required to reach 64 bits, $2^N = 64$

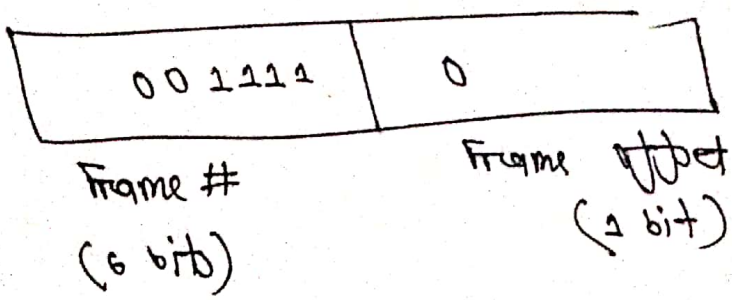
$\Rightarrow 2^N = 2^6$

$N = 6$

$\therefore$ Frame # = 6 bits

As each frame has 2 spots, 0 or 1, 1 bit is enough for Frame offset.

Physical Address of byte number 8 of the process



(Ans)