Final Exam

Question 1 (Marks: 5)

Write the MIPS code for the following C code. Consider K,Y are in registers $s0, $s1. The base address of Z is in register $s2.

Please remember you can not use MULT and DIV instructions. Also, you need to write a MIPS code that is optimum.

```
int main()

{

   int  K, Y, Z ;

   Y=10;

   K=11;

   Z[Y]  =  Y   -  35  *  (  K /8     +  110)  ;

}
```

OPEN RESPONSE ASSESSMENT

Status

You have completed this assignment. Your final grade will be available when the assessments of your response are complete.

Your Response due Jan 1, 2029 06:00 +06 (in 6 years, 11 months) ✔ COMPLETE

Status

Your response has been submitted. You will receive your grade after all steps are complete and your response is fully assessed.

The question for this section

Read Question 1 and write down the answer here.

Your response

```
main:
addi $s1, $zero,10 # Y =10
addi $s0, $zero,11 #K=11
srl $s0,$s0,3
addi $s0, $s0,110
add $t0,$zero,$s0
sll $s0,$s0,5
add $t1,$zero,$t0
sll $t0,$t0,2
add $s0,$s0,$t0
sub $s0,$s0,$t1
sub $t0,$s1,$s0
sll $t1, $s1,2
add $t1,$t1,$s2
sw $t0,0($t1)
```

Staff Grade NOT AVAILABLE

Waiting for a Staff Grade

Check back later to see if a course staff member has assessed your response. You will receive your grade after the assessment is complete.

Your Grade: Waiting for Assessments

You have completed your steps in the assignment, but some assessments still need to be done on your response. When the assessments of your response are complete, you will see feedback from everyone who assessed your response, and you will receive your final grade.

Question 2 (Marks: 5 = 4*1.25)

Numerical Input

5.0/5.0 points (graded)

If your answer is 0x02ABCDED, only put 02ABCDED in the response box (use all CAPITAL).

Encode `LUI $31,100` and write the equivalent hexadecimal value. The processor can uniquely identify this instruction using the value:15. Hint: The given register does not work as source/rs.

3C1F0064 ✔

Encode `SRL $31, $4, 5` and write the equivalent hexadecimal value. The processor can uniquely identify this instruction using the value: 2. Hint: The given register does not work as source/rs.

0004F942 ✔

Now suppose, you are executing the following the code:

```
ADDI $s5, $zero, 2022
SRL $s5, $s5, 5
NOR $s6, $s5, $zero
```

After executing the SRL instruction, what would be the value stored in $s5?

0000003F ✔

After executing the NOR instruction, what would be the value stored in $s6?

FFFFFFC0 ✔

Submit You have used 2 of 2 attempts

Question 3 (Marks: 10 = 4*2.5)

Question

10.0/10.0 points (graded)

Assume a pipelined processor with five pipeline stages where each stage takes one clock cycle. Further, assume that the processor has to execute the following instruction sequence:

```
ADD $t2, $t3, $t5
SUB $t5, $t2, $t5
LW $s1, 40($t5)
LW $s3, 32($s1)
AND $s1, $s3, $t1
```

If the procssor only implements stall cycles, how many clock cycles would it need to execute the above instructions?

17 ✔

17

If the procssor only implements stall cycles, what would be the average CPI?

3.4 ✔

3.4

If the procssor implements stall cycles as well as forwarding, how many clock cycles would it need to execute the above instructions in the most optimum way?

11 ✔

11

If the procssor implements stall cycles as well as forwarding, what would be the CPI if the above instructions were executed in the most optimum way?

2.2 ✔

2.2

Submit You have used 2 of 2 attempts

Question 4 and 5 (Marks: 10 = 5 + 5. Each sub part carries 1.25 marks)

Numerical Input

5.0/5.0 points (graded)

Consider a direct-mapped cache with a storage of 64 KiB of data. Now, if there are 128 words in each block, and the address length is 67 bit, answer the following questions:

Calculate the number of blocks in the cache?

128 ✔

128

Calculate the number of data bits required for the cache?

16 ✔

16

Calculate the number of tag bits required for the cache?

51 ✔

51

To what block number does byte address 38118 map?

74 ✔

74

Submit You have used 2 of 2 attempts

Numerical Input

3.75/5.0 points (graded)

Assume a cache has 1024 blocks, and each block can hold 32 bytes.

Determine the total number of bits (in kilobits) needed to store the cache considering the Valid bits, tags, and data for the blocks if the cache is direct-mapped.

274 ✔

274

Determine the cache block index in decimal number that contains data for the 32-bit address represented by the hexadecimal number 02AF013C.

9 ✔

9

```
AF0F3012
AF0F300F
AF0F4011
AF0F401A
AF0F3012
```

If the above hexadecimal numbers represent 32-bit byte addresses the CPU reads/writes consecutively from/to the memory, then calculate the total number of cache misses for the memory accesses.

3

3

Suppose that the hardware designer decided to increase the size of each cache block to 64 bytes and decrease the number of blocks by half. What will be the percentage increase/decrease of cache size with this change, (round your answer to have only one digit after the decimal point)?

0

0

Submit You have used 2 of 2 attempts