CSE340: Computer Architecture

Assignment 3

Chapter 4 (The Processor)

Total Marks: 20 (Marks are indicated in third brackets after each question)

Question 1 [Marks: 4]

Consider the code sequence below:

lw $t0,36($t1)

lw $t2,40($t0)

lw $t3,44($t2)

sll $t3,$t2,2

sub $t0,$t3,$t2

addi $t0,$t0,2

srl $t0,$t3,2

For the next questions, you will need to **draw** the appropriate diagram showing the pipeline stages and hazard removal methods.

   a) If you only use **Stall** to overcome the data hazard how many clock cycles would you need for executing the above code sequence? **Draw the diagram for pipelining as well as calculate the CPI.**

   Answer: **CPI = 2.714**

   Number of clock cycles = 19

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		CPI	2.714																	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Lw $t0,36($t1)	IF	ID	EX	MEM	WB														
		x	x	x	x	x													
			x	x	x	x	x												
Lw $t2,40($t0)				IF	ID	EX	MEM	WB											
					x	x	x	x	x										
						x	x	x	x	x									
Lw $t3,44($t2)							IF	ID	EX	MEM	WB								
Sll $t3,$t2,2								IF	ID	EX	MEM	WB							
									x	x	x	x	x						
										x	x	x	x	x					
Sub $t0,$t3,$t2											IF	ID	EX	MEM	WB				
												x	x	x	x	x			
													x	x	x	x	x		
Addi $t0,$t0,2														IF	ID	EX	MEM	WB	
Srl $t0,$t3,2															IF	ID	EX	MEM	WB

b) If you use **Stall and Forwarding** to overcome the data hazard how many clock cycles would you need for executing the above code sequence? **Draw the diagram for pipelining as well as calculate the CPI.**

Answer: **CPI = 1.857**

Number of clock cycles = 13

		CPI	1.857									

	1	2	3	4	5	6	7	8	9	10	11	12	13
Lw $t0,36($t1)	IF	ID	EX	MEM	WB								
		x	x	x	x	x							
Lw $t2,40($t0)			IF	ID	EX	MEM	WB						
				x	x	x	x	x					
Lw $t3,44($t2)					IF	ID	EX	MEM	WB				
Sll $t3,$t2,2						IF	ID	EX	MEM	WB			
Sub $t0,$t3,$t2							IF	ID	EX	MEM	WB		
Addi $t0,$t0,2								IF	ID	EX	MEM	WB	
Srl $t0,$t3,2									IF	ID	EX	MEM	WB

Question 2 [Marks: 8]

Consider the below set of instructions. Identify the data hazards and overcome the hazards using all the available methods **[Stalling, Stalling + Forwarding, Stalling + Forwarding + Code Scheduling]**. Your answer should contain all the necessary diagrams, required total cycle count in each solution along with average CPI. You will need to draw the diagrams clearly using 2B or darker pencils.
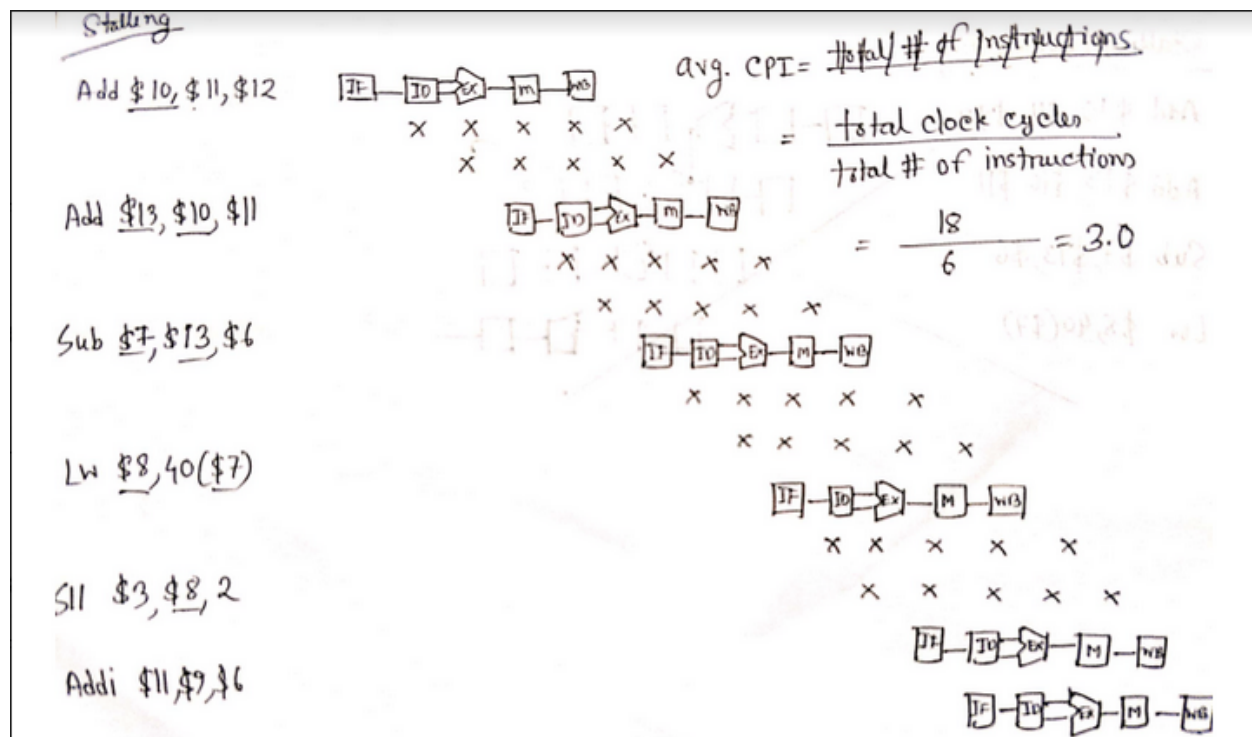
add $10,$11,$12

add $13,$10,$11

sub $7,$13,$6

lw $8,40($7)

sll $3,$8,2

addi $11,$9,$6

Answer:

1. **Stalling: Average CPI = 3**

2. Stalling + Forwarding: Average CPI = 1.83
Correction: the last instruction is Addi. The solution would be the same.

Stalling + forwarding

add $10, $11, $12

add $13, $10, $11

Sub $7, $13, $6

lw $8, 40($7)

SII $3, $8, 2

idd $11, $9, $6

Avg. CPI $= \dfrac{11}{6} = 1.83$
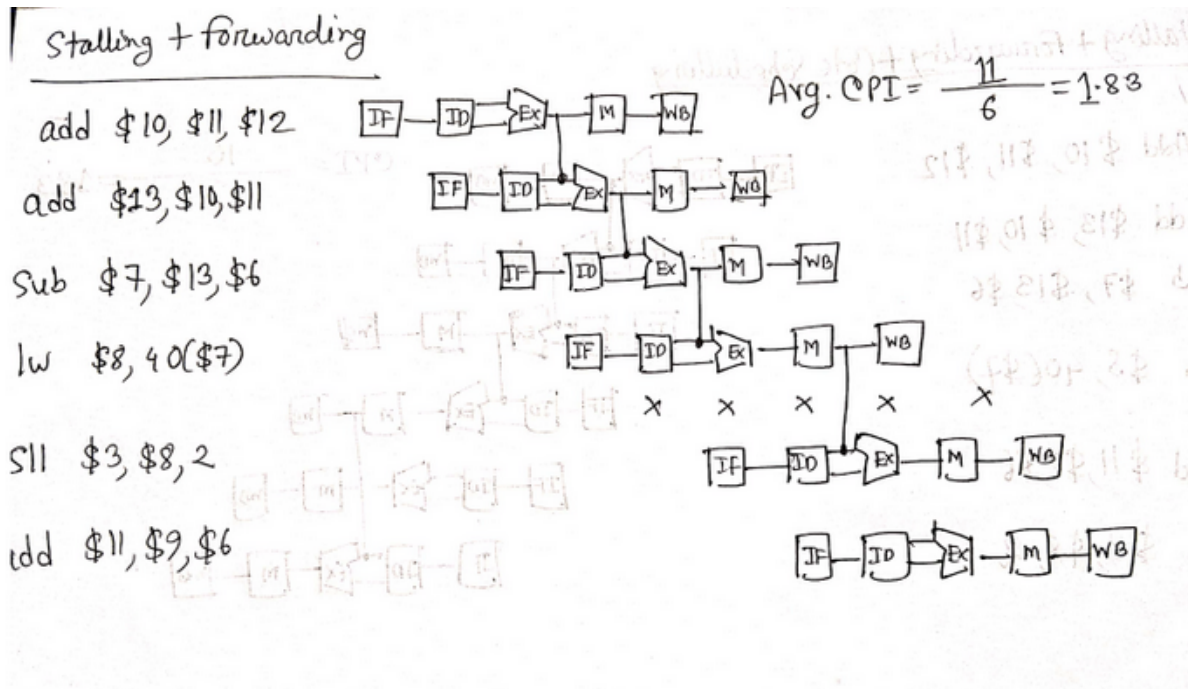
3. Stalling + Forwarding + Code Scheduling: Average CPI = 1.67
Correction: the 2nd last instruction is Addi. The solution would be the same.

Stalling + Forwarding + Code Schedulling

Add $10, $11, $12

Add $13, $10, $11

Sub $7, $13, $6

Lw $8, 40($7)

Add $11, $9, $6

SII $3, $8, 2

$CPI = \dfrac{10}{6} = 1.67$
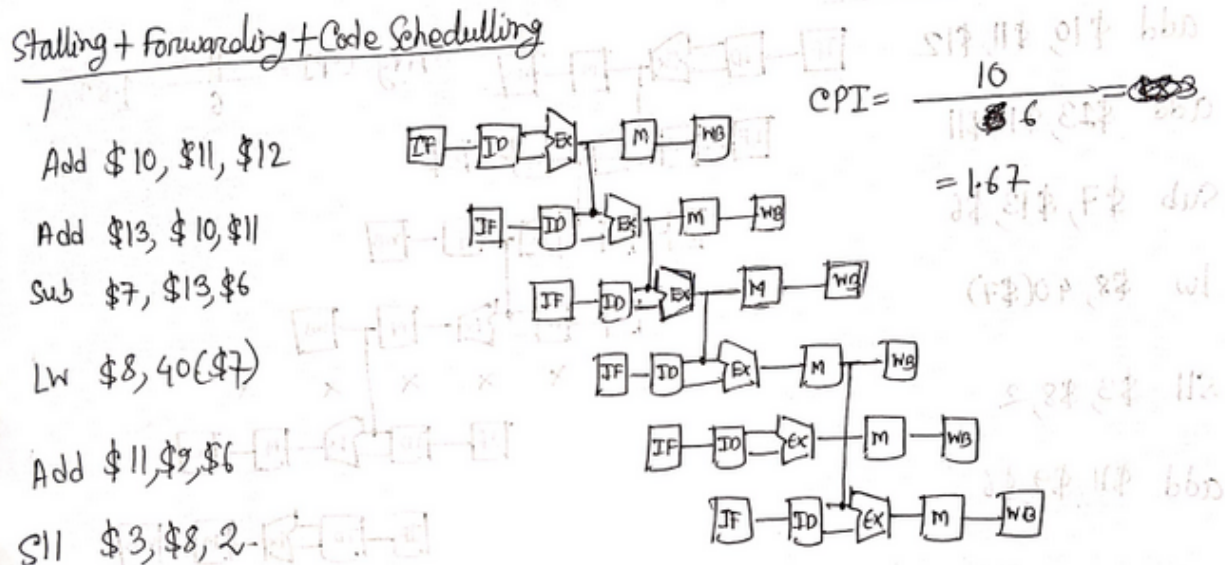
Question 3 [Marks: 2]

Consider the following duration for each stage:

IF = 260 ns

ID = 270 ns

EX (addition) = 450 ns

EX (subtraction) = 350 ns

MEM = 200 ns

WB = 290 ns

Now answer the following questions:

a) By how many ns the single cycle datapath clock period is greater than the 5 stage
pipeline clock period?

Answer: 1470 - 450 = 1020

b) For a single cycle datapath, what is the duration, in ns, to execute 6 sub instructions, 8
lw instructions and 1 add instruction?
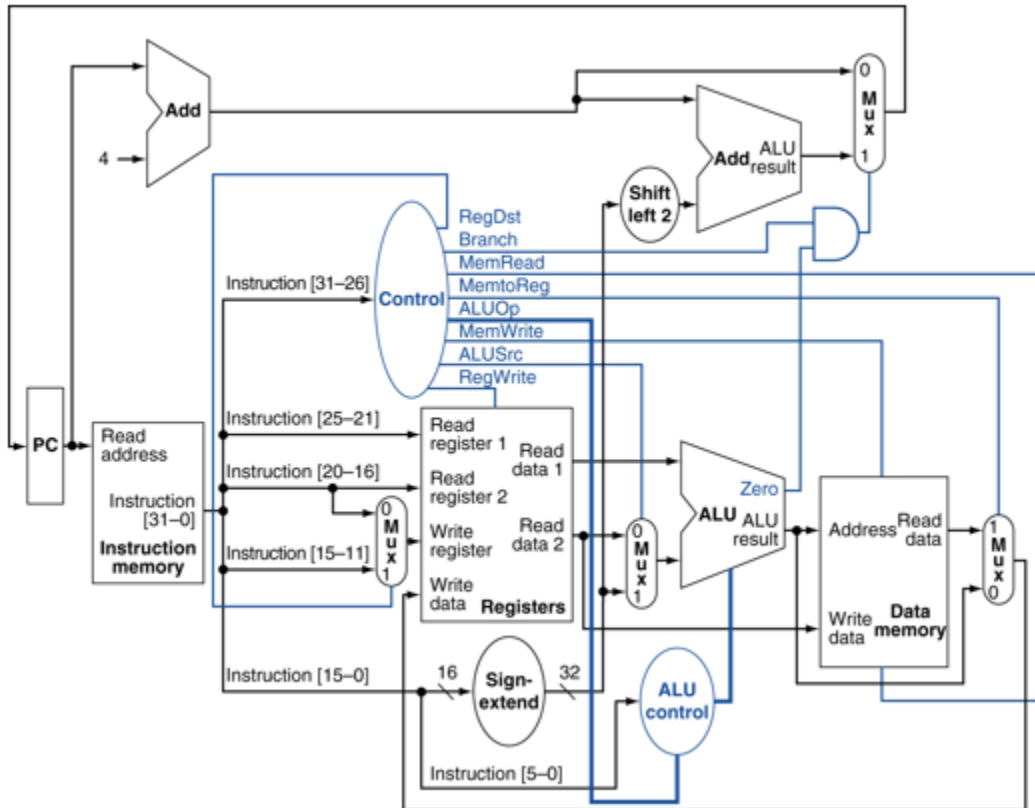
Answer:

Total number of instructions: 6 +8 +1 = 15

So total time = Total number of instructions * single cycle clock period = 15 *1470 =
22050 ns

Question 4 [Marks: 6]

a) Draw a complete single cycle datapath having control units and control signals.

Answer:

b) Draw the datapath for the instruction **lw $9, 16($11)**. (You can use a colored pen to specify the wires used).

Answer:

Load Instruction

lw $9, 16($11)

op	01011	01001	0000000000010000
op	rs	rt	offset