

## 340 Assignment 1

1

In our code, we have multiple lines in it and they containing multiple operations. When these codes converted into mips instructions, the cpu needs to keep track ~~what~~ which line of instruction is executing. And for this task cpu has a register called program counter. The program counter holds the current instruction address. Again, \$0 or \$zero register is actually the constant '0'. It can only hold 0 in it and for this it not be overwritten. We use \$zero register in different instructions, for example, we can move one register value into another register by simply add the \$zero register with that register which value we want to move. ~~add~~ (add \$s1, \$s0, \$zero).

We know that, main ~~more~~ memory contains slots of 8 bits, so for sequential instruction execution

For (64)

$$\frac{64}{8} = 8 \text{ will be the increment}$$

and for (128)

$$\frac{128}{8} = 16 \text{ will be the increment.}$$

### question 2

Instruction given : lw \$4, X(\$5)

we know,

lw ; \$register, increment \* offset(\$base)

$$\therefore \text{increment for 256 architecture, } \frac{256}{8} = 32$$

$$\therefore \text{offset in } \text{A}[5] \text{ is } = 5$$

$$\therefore X = 32 \times 5$$

$$= 160$$

(Ans)

### Question 3

A is in \$S0

f is in \$S2

i is in \$S1,  $\therefore f = A[i]$

MIPS

add \$t0, \$S0, \$S1

lb \$S2, 0(\$t0)

### Question 4

X is in \$S0, Y is in \$S1, Addr is in \$S4

i)  $X = 15Y - 5$

For  $15Y \Rightarrow$  sll \$t0, \$S1, 4 [R type]

000000	00000	\$S1, \$17 10001	\$t0, \$8 01000	00100	XXXXXXXX
op	rs	rt	rd	shamt	function

ii) Sub \$t0, \$t0, \$S1 [R type]

000000	\$t0, \$8 01000	\$S1, \$17 10001	\$t0, \$8 01000	00000	XXXXXXXX
op	rs	rt	rd	shamt	function

addi \$s0, \$t0, -5 [I type]

xxxxxx	\$t0, \$8 01000	\$s0, \$16 10000	-5 1111111111111011
op	rs	rt	offset

Again, (11)  $Arr[5] = 2x + Arr[10]$

For 2x, add \$t0, \$s0, \$s0 [R type]

000000	\$s0, \$16 10000	\$s0, \$16 10000	\$t0, \$8 01000	00000	xxxxxxx
op	rs	rt	rd	shamt	function

Now,  $Arr[10] \Rightarrow lw $t1, 40($s4)$  [I type]

xxxxxx	\$s4, \$20 10100	<del>\$t2, \$20</del> \$t1, \$20 010001	40 0000 0000 0010 1000
op	rs	rt	offset

Now,  $\text{add } \$t2, \$t0, \$t1$  [R type]  
 $[2x + \text{Addr}[10]]$

000000	$\$t0, \$t2$ 01000	$\$t1, \$t0$ 01001	$\$t2, \$t0$ 01010	00000	xxxxxx
op	rs	rt	rd	shamt	func

For,  $\text{Addr}[5] = \text{Addr}[10]$

$\text{sw } \$t2, 5 \times 4 [54]$   
 $\Rightarrow \text{sw } \$t2, 20(\$54)$  [I type]

xxxxxx	$\$54, \$t2$ 10100	$\$t0, \$t2$ 01000	20 00000000000010100
op	rs		offset

### Question 5

Given Instruction,  $\text{beq } \$9, \$8, 124$

Here the offset is 124

16 bit binary form of 124 = 000000001111100



Now we have to left shift 2 bit of that binary value of 124 or 0000000001111100

after 2 bit left shift : 0000000111110000

Now extend the sign into 32 bit : 0.....0111110000

PE holds : 0x1278A4B1

In binary : ~~0001001000110~~

0001001001110001010010010110001

Now adding 4 or 100 with the PE number

$$\begin{array}{r}
 0001\ 0010\ 0111\ 1000\ \dots\ 0001 \\
 (+) \quad 000\ \dots\ 0100 \\
 \hline
 \underline{0001\ 0010\ 0111\ 1000\ 1010\ 0100\ 1011\ 0101}
 \end{array}$$

Now we have to add this with that 32 bit offset value again,

$$\begin{array}{r}
 0001\ 0010\ 0111\ 1000\ 1010\ 0100\ 1011\ 0101 \\
 0000\ 0000\ 0000\ 0000\ 0000\ 0001\ 1111\ 0000 \\
 (+) \quad \underline{0001\ 0010\ 0111\ 1000\ 1010\ 0110\ 1010\ 0101}
 \end{array}$$

∴ branch destination address of that instruction :

0x 1278A6A5

(Ans)

Ques 6

Given instruction : J 1590

PC holds : 0x 00AB1203

binary : 0000 0000 1010 1011 0001 0010 0000 0011

we know the machine format of J type

6 bit

OP	26 bit address
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So the address we have = 1590

26 bit binary form = 00.....11000110110

26 bit

After 26 bit left shift : 000.....1100011011000

28 bit

Now the PC MSB 4 bit will copy and add on the MSB of that 28 bit address.

∴ MSB 4 bit of PC : 0000

Now after adding this to the 28 bit address we get :

~~0000 0000 0000 0000 0000 0110 0011 0110~~  
0000 0000 0000 0000 0001 1000 1101 1000

∴ Hexa decimal form: 0x 0000 18D8

(Ans)

### Question 7

Given Instruction : lw \$8, 52(\$17)

base address : 0x 156 32017

binary form : 0001 0101 0110 0011 0010 0000 0001 0111

32 bit binary form of 52 is:

0000 0000 0000 0000 0000 0000 0011 0100



∴ The memory address of the data that will be loaded in \$8 is,

$$\begin{array}{r}
 0001 \ 0101 \ 0110 \ 0011 \ 0010 \ 0000 \ 0001 \ 0111 \\
 + 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0011 \ 0100 \\
 \hline
 0001 \ 0101 \ 0110 \ 0011 \ 0010 \ 0000 \ 0100 \ 1011
 \end{array}$$

∴ In Hexadecimal: 0x1563204B

(Ans)

Ques no 8

• MIPS:

add \$S3, \$S3, \$zero → i=0

Loop:

blt i, \$t0, \$S3, 10 → i < 10

beq \$t0, \$zero, Exit

~~beq~~

slt \$t1, \$S3, 2

add \$t1, \$S1, \$t1

lw \$t2, 0(\$t1)

[loaded A[i]]

A → \$S1

B → \$S2

i → \$S3

5 → \$S4

1 → \$S5

beq \$t2, \$s4, Else

sll \$t1, \$s3, 2

add \$t1, \$t1, \$s2

lw \$t2, 0(\$t1) [loaded B[i]]

sll \$t1, \$t2, 2

add \$t1, \$s1, \$t1

lw \$t2, 0(\$t1) [loaded A[B[i]]]

add \$t2, \$t2, \$s5

add \$s3, \$s3, \$s5 [i++]

↪ loop

Else :

add \$t1, \$s3, \$s5

sll \$t1, \$t1, 2

add \$t1, \$s2, \$t1

lw \$t3, 0(\$t1) [loaded B[i+1]]

sw \$t3, 0(\$t2) [stored in \$t2 = A[i]]

add \$s3, \$s3, \$s5 [i++]

↪ Loop

Exit :

### Ques 9

MIPS code:

~~\$s1~~

addi \$s1, \$zero, 20

addi \$s2, \$s1, -10

addi \$s0, \$zero, 7

add \$s3, \$s2, \$s0

jal sum

sum:

addi \$sp, \$sp, -4

sw \$s0, 0(\$sp)

add \$t0, \$a0, \$a1

add \$t0, \$t0, \$a2

add \$v0, \$s0, \$zero

lw \$s0, 0(\$sp)

addi \$sp, \$sp, 4

jr ra

Given,

a → \$s0

x → \$s1

y → \$s2

z → \$s3

→ [stored value of s0  
in stack]

[ x = a0  
y = a1  
z = a2 ]

→ [retrieve the value of  
\$s0 from stack]