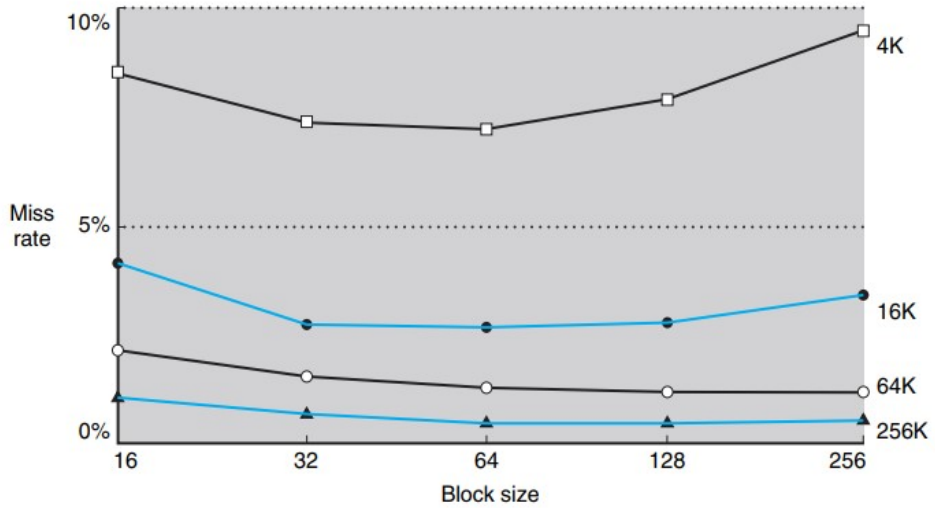
Quiz 4

Answer the questions below. Each carries 1 mark.

Multiple Choice

1.0/1.0 point (graded)



If the initial block size is 64 bytes and we incerase it by 300%, then what would be the approximate hit ratio for a 4KB cache memory?

In the given diagram, each line represents caches of different sizes specified in the right side of the graph. X and Y axis legends are given in the diagram

- ◯ 2%
- ◯ 3%
- ◯ 9%
- ◯ 10%

- ◯ 80%
- ◉ 91%
- ◯ 96%
- ◯ 99%

✔

Submit You have used 1 of 1 attempt

Multiple Choice

1.0/1.0 point (graded)

In case of a direct mapped cache with 64 blocks, if the blocks are of size 4 words, how many bits do you need to represent the byte offset?

- ◯ 2
- ◯ 3
- ◉ 4
- ◯ 5
- ◯ 6

✔

Submit You have used 1 of 1 attempt

Multiple Choice

1.0/1.0 point (graded)

If a cache is of size 8 Kilobytes, then how many 2-word blocks does it contain?

- ◯ 3

- (●) 4
- ( ) 5
- ( ) 6
- ( ) 7

✔

Submit You have used 1 of 1 attempt

Multiple Choice

1.0/1.0 point (graded)

Suppose, A process P has 225 bytes and each page contains 15 bytes. What should be the bit length of the Logical Address?

- ( ) 2
- ( ) 5
- ( ) 7
- (●) 8
- ( ) 10
- ( ) 16
- ( ) 32
- ( ) 64

✔

Submit You have used 1 of 1 attempt

Checkboxes

1.0/1.0 point (graded)

Index	Valid Bit	Dirty Bit	Tag Bits	Data
...	...	...	...	...
1010	1	1	11011	A7B12
...	...	...	...	...

For the above cache, Which of the following statements are true for write back approach?

- [ ] In Main Memory, the Address 110111010 contains the data A7B12
- [ ] The address 110111010 in main memory will be only updated when the cache block of index 1101 will be updated
- [x] Dirty bit will be 0 only when the Address 110111010 in both main memory and cache contains the same data
- [ ] the dirty bit should be 1 when the same main memory and cache address contains the same data
- [x] In Main Memory, the Address 110111010 does not contain the data A7B12

✔

Submit You have used 1 of 1 attempt

Multiple Choice

1.0/1.0 point (graded)

Suppose a cache has 256 blocks and each block contains 20 bytes. To map the byte address 99, what should be the block number?

- ○ 12.8
- ○ 13
- ◉ 99
- ○ 12

- ◯ 12.5
- ◯ 95

✔

Submit You have used 1 of 1 attempt

Checkboxes

1.0/1.0 point (graded)

Suppose, you are researching on building an ideal memory device based on the characteristics of the following devices:

1. An SRAM with 0.5ms response time with 12 kilobyte capacity with a cost of 350$/GB

2. An SRAM with 0.7ms response time with 35 kilobyte capacity with a cost of 300$/GB

3. An DRAM with 12ms response time with 4 gigabyte capacity with a cost of 25$/GB

4. An DRAM with 10ms response time with 8 gigabyte capacity with a cost of 30$/GB

5. A magnetic disc with 15s repose time with 120 gigabyte capacity with a cost of 5$/GB

The ideal memory should have which of the following characteristics of the given devices? Select all that apply.

- ☑ 0.5ms response time
- ☐ 0.7ms response time
- ☐ 10ms response time
- ☐ 12ms response time
- ☐ 15s response time
- ☐ 12 kilobyte capacity
- ☐ 35 kilobyte capacity
- ☐ 4 gigabyte capacity

- [ ] 8 gigabyte capacity
- [x] 120 gigabyte capacity
- [ ] cost of 350$/GB
- [ ] cost of 300$/GB
- [ ] cost of 25$/GB
- [ ] cost of 30$/GB
- [x] cost of 5$/GB

✔

Submit You have used 1 of 1 attempt

Checkboxes

1.0/1.0 point (graded)

Memory hierarchy is based on-

- [x] response time
- [x] memory capacity
- [ ] architecture of the CPU using that memory device

✔

Submit You have used 1 of 1 attempt

Multiple Choice

1.0/1.0 point (graded)

For cache write, which approach keeps the data consistent between the cache and main memory at any given time?

- ◯ Write-Back
- ◯ Write-Around
- ◉ Write-Through
- ◯ Write-Both

✔

Submit You have used 1 of 1 attempt

The following question has 3 parts. Each part carries 2 Mark. You can press the submit button maximum 2 times (Number of attempts: 2)

Numerical Input

6.0/6.0 points (graded)

Address		
Tag Bits	Index Bits	Byte Offset
Tag Bits	Data Bits	

Assume a direct-mapped cache with 32 KiB of data and 2048 words per block holding 106 -bit addresses. The address is divided into 2 main part: Tag and Data Bits (Refer to the diagram).

Now answer the following questions:

Calculate the total number of blocks in the cache.

4 ✔

How many data bits are required for the cache?

15 ✔

How many tag bits are required for the cache?

91 ✔

91

Submit You have used 2 of 2 attempts