Quiz 3

Answer the question below. It carries 1 mark.

Question 1

1.0/1.0 point (graded)

Which instruction does not write anything in the WB (Write back) Stage?

- ○ lw
- ○ lb
- ◉ sb
- ○ addi

✔

Submit You have used 1 of 1 attempt

The following question has 7 parts. Each part carries 2 marks. Make sure to check the number of attempts in the question

Question 2

14.0/14.0 points (graded)

```
add $t0, $t2, $t3
addi $s0, $t0, -7
sub $s1, $s0, $t5
sw $t6, 8($s1)
add $s0, $t6, $t2
```

Cosider the given code sequence and answer the following questions

If you only use Stall to overcome the data hazards in the above code sequence, how many stalls would be needed?

6 ✔

6

If you use Stall and code scheduling to overcome the data hazards, what will be the number of clock cycles?

14 ✔

If you use Stall and Forwarding to overcome the data hazards, how many stalls would be reduced?

6 ✔

What will be the CPI, If you use Stall and Forwarding to overcome the data hazards?

1.8 ✔

Consider the clock period is 500ps. Suppose, the Register Write takes 450ps and Register Read takes 350ps, how many stalls would be needed to overcome the data hazard if we use only stall as a solution?

9 ✔

If the `sw $t6, 6($s1)` instruction in the above code sequence is replaced with `lw $t6, 6($s1)`, what will be the number of clock cycles If you use Forwarding and Stall to overcome the data hazards?

10 ✔

If the instruction `add $s7, $t2, $t3` is added at the end of the above code sequence, what will be the total number of clock cycles if only stall and forwarding is used to overcome the data hazards?

10 ✔

You have used 2 of 2 attempts

Submit