

# Exploring the Usefulness of Varactor loaded Nonlinear Transmission Lines

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**Abstract**—In this paper we will discuss the use of nonlinear elements within a transmission line to study their effects on the speed and shape of an input pulse, and how the next group which takes over our work may use this information to design similar circuits with improved bandwidth and/or performance.

## I. INTRODUCTION

The goal of this project was to explore how non-linear transmission lines behave when loaded with varactors and how they can be used. Using design methodologies taken from previous studies and IEEE research, we have constructed a varactor loaded transmission line and attempted to observe and replicate the pulse sharpening effect shown in the literature.

First, we discuss the necessity of non-linear components in such a Nonlinear Transmission line or *NLTL* for short. We then discuss ways in which the devices we use in our simulations are modeled, and the obstacles we faced in constructing these models. We simulated these nonlinear lines using MICROCAP and discuss possible reasons for the discrepancies we have seen between research and simulations.

To verify the characteristic capacitance-voltage or CV curves of our chosen components, we constructed a simple test fixture and measured capacitance vs. th voltage using a DC power supply to reverse bias the varactor diodes and a handheld LCR meter.

## II. THEORY

### A. Why use Nonlinear Devices?

Non-linear devices in transmission lines have been widely used for pulse sharpening in particular. Similar sharpening can be observed by use of non-linear inductors and theoretically by strategic placement of dielectric material in the line [1]. The non-linearity is due to the voltage dependence impedance on the line. When a wave is sent through such a line and its voltage begins to rise, this causes different parts of the wave to propagate at different speeds.

Much like a wave traveling in the ocean towards the shore, certain sections of the wave travel at different speeds despite the travel of the wave as a whole. This can be seen first hand by a surfer utilizing their position on the wave to have

the right speed and stability. This same concept is present in optical fibers or waveguides. As we transmit a signal beam into a guide, the phase velocity can actually exceed the speed of light, however the speed of the information characterized by the group velocity is what we care about. While there is no information in the phase velocity, we are able to use this phenomena to create faster discrete pulses.

### B. Types of NLTL waves

While treating the physics of non-linear waves is beyond the scope of this paper, the use of NLTL's in transmission lines is founded upon the existence of waves that do not behave like the pure sine waves we usually consider in electronics. Both types of waves can be present and used in technology to lessen the time it takes for an input waveform to reach its final value as well as lessen the time to return to its “off” voltage state. In other words, these can be used to sharpen both rising and falling edges of a square wave input [2].

Informally, *Solitons* are much like the type of wave we see traveling in the open ocean without breaking and are characterized by their ability to interact with other waves without losing energy. This means that after passing another wave it largely maintains its shape and is only shifted in phase (experiences time delay).

*Shockwaves* are more easily visualized by a wave approaching the shore and breaking. This is the type of wave we utilize when considering non-uniform NLTL's. As the wave moves closer to the beach and the shoreline rises dramatically, the wave can no longer move in the same way due to the shore interrupting the circulating water and the momentum carried by it. With this sudden discharge of energy, we see the wave “break” and momentarily create a large vertical column of water.

### C. Non-linearity vs Wave Dispersion

One of the main issues we face with these types of circuits is the need for non-linearity to outweigh possible wave dispersion. Dispersion is a concept commonly discussed relative to optical fiber cable as a limiting factor of transmission speed. The idea is that traveling through any medium will cause a small amount of pulse spreading. This means that, if dispersion is strong enough, the pulse can spread or even break apart into

several smaller pulses. To overcome this, we need enough non-linearity in the line primarily in terms of voltage/amplitude dependence such that the wave remains narrow.

Figure 1 [3], shows how construction of NLTL's follows catch up theory and how pulse sharpening is achieved by these types of circuits.

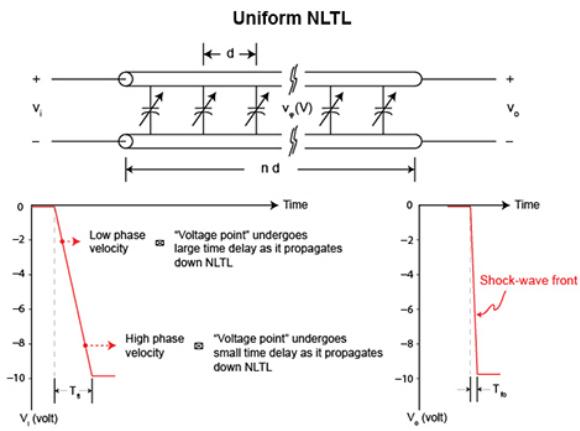


Figure 1. This graphic taken from an ANRITSU application note shows the basic principle of catch-up theory, and how it can be used to sharpen input pulses

#### D. Varactors vs. Nonlinear Capacitors

While nonlinear capacitors have been used in many [4] in high voltage applications, varactor diodes have the advantage of a larger capacitance range for a given varying voltage. This allows us to get the nonlinear benefits without the safety concerns of working with high voltage. Further, the overall design is simplified with the use of Varactors because only one bias voltage is needed. Nonlinear capacitors are often modeled using equation (1) to describe the voltage dependence of the capacitance [5].

$$C(v) = \frac{C_0}{\sqrt{1 + v/V_o}} \quad (1)$$

where  $C_0$  and  $V_o$  are zero bias capacitance and the reference voltage, respectively. Equation (2) becomes useful as we start looking at larger pulses with large amplitude and should allow for scaling of our design.

$$C_{ls}(V_l, V_n) = \frac{1}{V_n - V_l} \int_{V_l}^{V_n} C(v) dv \quad (2)$$

This leads to an important constraint when designing passive NLTL's made up of series low-pass LC circuits. The fastest wave we can propagate down the NLTL can be approximately found by using equation (3) [6] to find the cutoff frequency of the network as a function of the voltage across the varactors. This equation also describes the phase velocity for every harmonic within our circuit bandwidth assuming no dispersion in the line [7].

$$f_{bragg} \approx \frac{1}{2\pi\sqrt{LC(v)}} \quad (3)$$

This equation is used in section III-A indirectly to estimate the amount of pulse sharpening we can expect for a given step input

#### E. Methods of Modeling Varactors

In order to properly simulate and make predictions with these simulations, we need first to determine how to model the non-ideal parasitics of the line and particularly the behavior of the chosen varactor diode loading the NLTL. There are several ways to accomplish this. The most standard and the method chosen by our group is SPICE modeling.

Another industry standard used to do this is by modeling via Verilog code. Specifically, Verilog-AMS or Verilog-A modules can more accurately capture the non-idealities in capacitors and varactors. This is a useful tool to explore as it can be integrated with many commercial simulation programs such as ADS.

#### F. Modeling Board Characteristics

When constructing a test fixture for measurements of NLTL's of higher frequency, we must also take into account the properties of the board we are working with. For our low-frequency model and with limited access to robust VNA's, the procedure was not necessary but we recommend using the two-line pencil method to approximate the board permittivity and loss tangent as utilized to do the same for flex PCB's due to its simplicity and limited need for equipment [8].

For our board, we used a simpler method which may prove useful as a quick and dirty alternative to the one described above. To find the permittivity of the board we used a simple LCR Meter (DE-5000) and the following formula of a parallel plate capacitor as shown in equation (4). This method was suggested by our faculty advisor due to the fact that a double-sided copper clad board is simply two conducting plates separated by a dielectric material. By definition, this is a parallel plate capacitor.

$$C = \frac{\epsilon A}{d} \quad (4)$$

Where we treat the width of the dielectric as plate spacing  $d$ , the board area as area,  $A$ , and measured capacitance as  $C$ . Solving for permittivity  $\epsilon$ , we found a relative permittivity of  $\epsilon_r \approx 3.54$ . For this measurement, a figure normally given for FR4 is roughly 4.0 to 4.4. A few possible things could cause this error.

The device used to measure the FR4 board generates a test frequency of 100kHz at maximum. Relative permittivity is usually given for FR4 at much higher frequencies in the Mhz range. Another is the precision achievable when measuring the dielectric thickness. While we used a simple ruler with mm markings, a caliper would be much better suited for this task. Alternative methods do exist and are quite simple but do necessitate access to a VNA [9].

1) *SPICE Models:* SPICE models are typically easier to find and use in most circuit simulation software and what we used for our low-frequency prototype as it seemed to be sufficient for our purposes. We chose to use software from the company SpectrumSoft due to its vast array of built-in SPICE models and capabilities such as parameter optimization tools and the ability to import touchstone data from VNA measurements. MICROCAP ships with SPICE models for the BBY40 and SMV1249 varactor diodes, both of these with desirable qualities for building NLTL's. Previously a software found in the industry for a high price, SpectrumSoft is now no longer in business and has released this program free.

2) *Verilog-A Modules:* We were unable to utilize this modeling method. In section VI, we go over some potentially useful references to help you create models for higher frequency/bandwidth designs. Most Verilog modules we have come across utilize equation 1 in order to model non-linear capacitors and varactors.

### III. SIMULATIONS

In this section, we will discuss the basics behind catch-up theory [1] and how we confirmed this with simulation. As discussed previously, we use the voltage dependence of the circuit capacitance to create a wave comprised of sections traveling at different speeds. The time delay difference between an arbitrary high and low voltage level,  $\Delta$  can be estimated using equation 5. To find the time delay of the  $N_{th}$  node, we simply multiply this result by N.

The equation is nothing more than the period for our estimated bragg frequency from equation 3. This tells us that as we make our NLTL longer, we expect more and more pulse sharpening. However, this approximate equation does not account for loss on the line which introduces more dispersion of our wave.

#### A. Simulating Rise Time

In our simulations, we use an input step of 5 volts with a defined risetime of  $1\mu s$ . Using equation (5), we calculate a pulse sharpening of  $8.44ns$  at our  $10^{th}$  node and  $84.37ns$  at our  $100^{th}$  node. To make these calculations, we used the CV plots obtained by measuring the BBY40 with the test fixture discussed in section V-A.

$$\Delta T = N(\sqrt{LC_o} - \sqrt{LC_s}) \quad (5)$$

For a lossless line, the sharpest pulse we can achieve can be estimated by first using equation 6 [1]. We notice that this utilizes the equation of our estimated Bragg frequency as seen in (3) and describes the difference in cutoff frequencies at maximum and minimum bias voltage multiplied by the number of sections, N.

This gives us the ideal cutoff frequency of the line which is about  $f_c \approx 290MHz$ . The period of a wave moving at this rate is  $T \approx 3.4ns$ . While we have not been able to achieve a rise time of this magnitude, we need to remind ourselves of the inherent parasitics we are dealing with. Using a basic model with values from our inductor and varactor diode datasheet. We

have a per section series resistance of roughly  $R_s = 122m\Omega$  at DC, and a parallel resistance given by the resistance inherent in the varactor packaging as well as of the trace itself. This value was taken from the SPICE model used and was  $R_p = 1m\Omega$

$$\omega_c = \frac{2}{\sqrt{LC_s}} \quad (6)$$

In figure 3 we can see that when simulating our ideal line, equation 5 is proven to be a very rough estimate to what we see. while at the  $10^{th}$  section, we see a very similar value of about 6ns compared to the 8.4ns calculated earlier, at the  $100^{th}$  section we see about half of the expected pulse sharpening with our simulated value of 45ns compared to 84ns calculated.

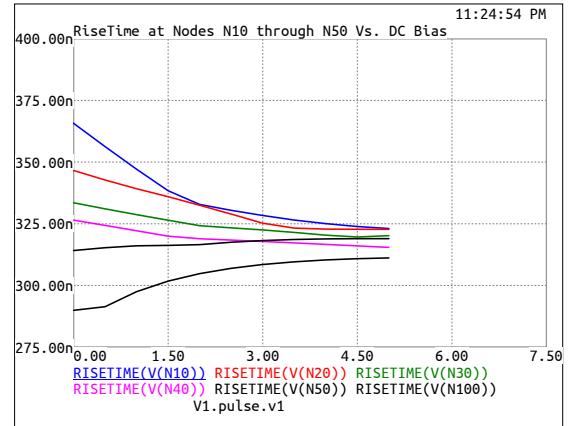


Figure 2. Risetime Vs. Line Length vs. DC Bias Voltage

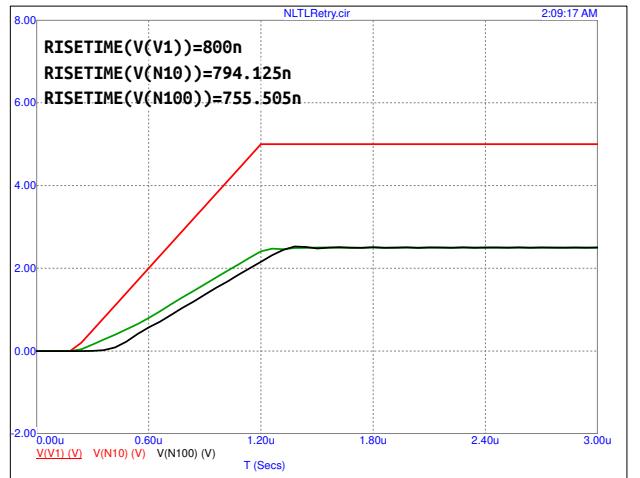


Figure 3. Rise time at source, node 10 and node 100 simulated with no resistive loss

In figure 4, we add the series DC resistance of the inductor ( $R_s \approx 122m\Omega$ ) and the  $1m\Omega$  resistance of the BBY40. From this, we see that not much has changed in this model and in fact, we see an increased sharpening effect if anything. We do notice, however, that the amplitude of the wave is much more attenuated at our  $100^{th}$  node. This would lead us to expect a decrease in the pulse sharpening in the circuit instead of a relatively constant value due to the lessened effect on varactor capacitance as the pulse climbs.

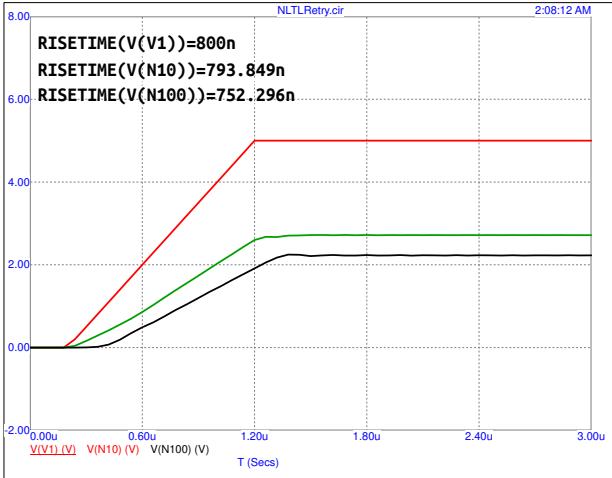


Figure 4. Rise time at source, node 10 and node 100 simulated with resistive loss of  $0.122\Omega$  per ladder section

Figure 2 explores the effect of different biasing on our line as well as how long a line we can practically use for sharpening purposes. As our DC resistance grows with our line length, we expect our amplitude to keep dropping. As the amplitude of the traveling wave is reduced, we effectively trace out less of our varactor CV curves. Due to this, the CV relationship will begin to look more and more linear as we add ladder sections to our design. We have used a parametric plot to show the limits of this pulse sharpening as we increase the line length and plotted rise-time vs. DC bias for each 10<sup>th</sup> node of the ladder. The input pulse used in this case was 400ns.

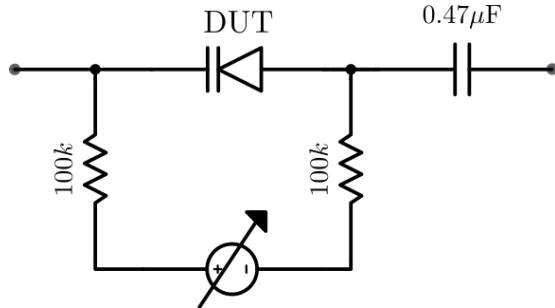


Figure 5. Schematic for testing varactor CV characteristics. Taken from a design by W2AEW.

Figure 5 shows the schematic of the test fixture constructed and used for measuring the CV curve of the BBY40 varactor. The two 100k resistors prevent the DC source from drawing any current. The capacitor is chosen to be a large value so that the capacitance measured with the two in series is close to the capacitance of the varactor alone. This is because the varactor and  $0.47\mu F$  capacitor are effectively in series.

#### IV. BOARD DESIGN

In order to test all these simulated values, we designed a discrete version of our transmission line using Altium Designer. We emphasized traces being as short as possible

and used Altium's built-in impedance profile tool to match our path between each pair of SMA connectors to  $50\Omega$ . The circuit we constructed is shown assembled in figure 6.



Figure 6. Assembled Tx Line Board made for 144Mhz

### V. MEASUREMENT RESULTS

#### A. Varactor CV Curves

To measure and find the capacitance vs Voltage of our chosen varactors we created a small ugly style circuit based on a design by W2AEW. Two 100k resistors are added to limit the current flowing to the power supply. A ceramic capacitor of value much greater than our varactor is placed to protect the meter from excessive voltage. Since this larger capacitance effectively in parallel with our varactor, our meter measurement is approximately only the capacitance of the varactor diode itself.

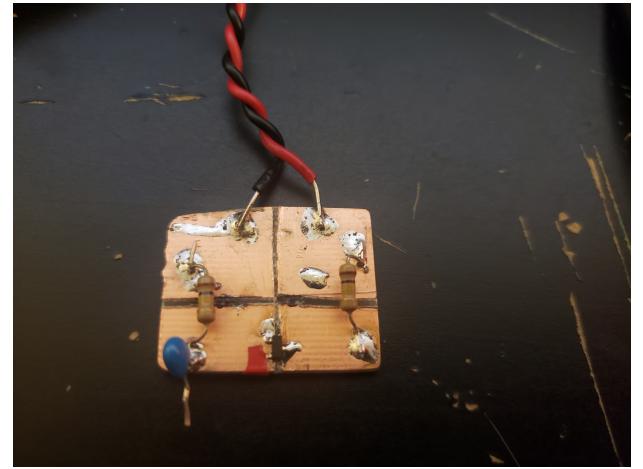


Figure 7. Test Fixture used for plotting CV Curve of BBY40

Through the use of this fixture, we were able to generate the curves shown in figures 8 and 9. These were in close agreement to curves found on datasheets for the BBY40 and SMV1249 respectively.

#### B. AC Response

The frequency response of our circuit effectively tells us the operating bandwidth of our circuit. With a 10 ladder long

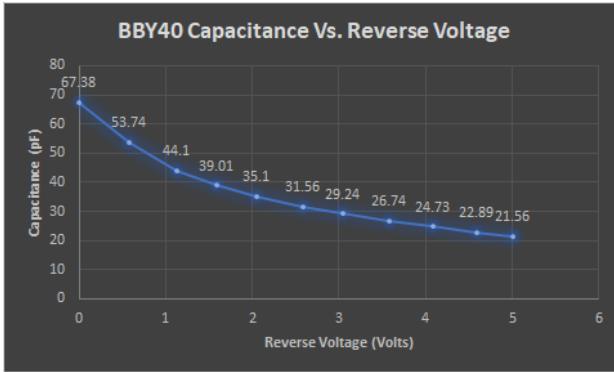


Figure 8. Measured CV Characteristics of BBY40

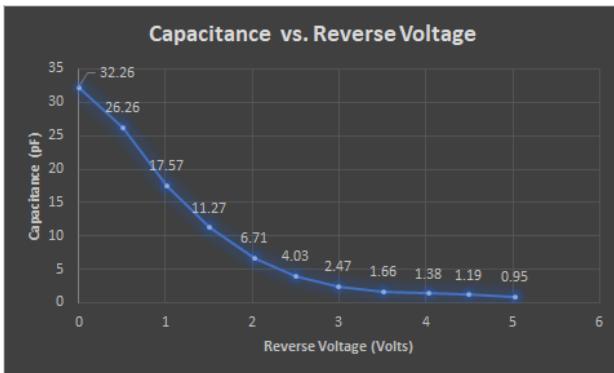


Figure 9. Measured CV Characteristics of SMV1249

circuit, our cutoff can be calculated to be around 103Mhz. We also notice that as we near the corner, the nonlinearities present in the circuit cause increased amounts of resonance as expected. The circuit topology inherently has multiple resonant frequencies. These are frequencies we may want to consider when measuring circuit quality factor as only the strongest resonance will produce an accurate Q.

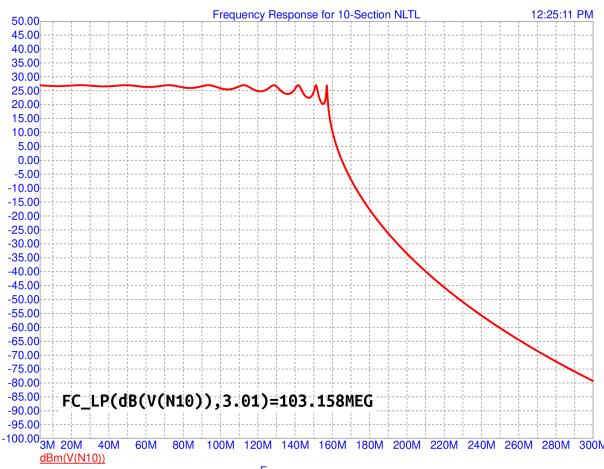
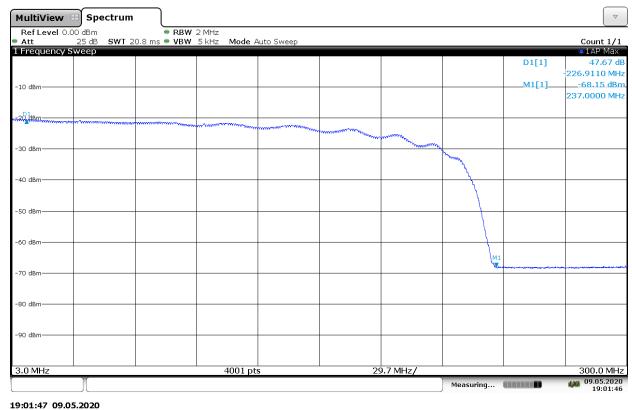


Figure 10. Simulated AC Response for Board 1

Comparing figures 10 and 11, we see a similar pattern however with an additional -10dBm loss at DC and less pronounced resonant frequencies. The additional loss could be

Figure 11. Measured Frequency Response for Board 1 ( $L = 56\text{nH}$ )

due to the cables or due to improper modeling of our series resistance in the line.

### C. Rise Time

We had great difficulty in measuring the rise time of our circuit and the main problems we faced were not understanding the theory well enough to have done proper testing. While our components were chosen on the basis of working at 144Mhz, we failed to see that driving our circuit below this bandwidth and performing similar simulations may be adequate to prove rise time performance increase.

Another complication was keeping in mind the biasing conditions of the varactors. We did not design for a port in which to introduce a dc bias to our circuit and relied on equipment being able to accomplish this. Care must be taken when using analog generators to supply the DC bias to the circuit. Our particular model begins sweeping with a negative bias before reaching a positive one. This effectively puts the varactors into forward bias and allows them to hold a charge.

Figure 12 shows the lab setup used to take the time-domain measurements. A bias-Tee is used to provide a DC bias to our NLT and is adjusted by a bench power supply. A picosecond pulse generator is used to send in a well-behaved high-speed signal into the DUT.

The input wave is a 1Mhz 1Vpp Square wave with 10ns rise and fall times and the bias is adjusted from 0 to 3V to further investigate its effect on the the capacitance of the varactor.

Figure 13 shows the expected rise time improvement for a circuit like ours with 240 ladders sections in an ideal environment. Once we account for the series resistance,  $R_{ser} = 0.7\Omega$  for the purposes of figure 14. We see in this case the loss is great enough to overcome the linearity of the line and we see a rise time increase instead.

Figures 15 and 16 show the measured response to a square wave with  $V_{dc} = 1V$  and  $V_{dc} = 2V$ , respectively. While we seem some pulse sharpening in both cases, we don't see the increase shown in figure 2.

To compare measurements and simulations more clearly, we performed new simulations designed for an input with a true 10nS rise time. In the previous figures, we see that despite setting up a waveform to have a rise time of 10nS, the

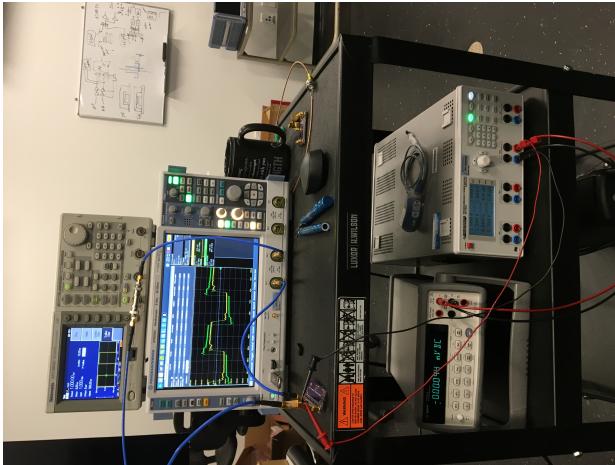
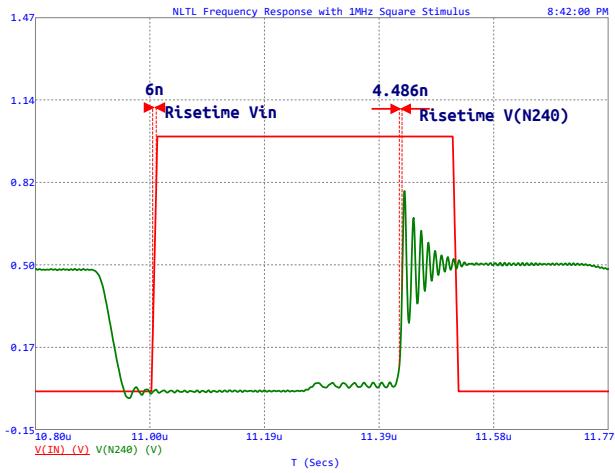


Figure 12. Test Setup for Measuring Risetime With Bias

Figure 13. Simulated Risetetimes for Input pulse, and the 240<sup>th</sup> node

plots consistently show this as 6nS. This is due to the way the simulation software defines a sources input risetime. In calculation we found the risetime of a wave form is calculated as the time it takes for the signal to go from 20% to 80% of the final value. This is one of the standard ways it is defined. However, when defining a voltage source, the rise time parameter is the time it takes for the signal to go from its lowest to highest value. To find the value that actually results in a 10nS measured risetime, we used the built in optimization tools to find the corresponding voltage risetime.

In other words, we used the software to iterate values of the voltage defined rise time until it found a value for a signal which takes 10nS to transition from 20% to 80% of its final value. We found this to be 12.5nS. Using this new input, we generated the values in table II and compared it to the measurements in table I. We notice that there is a non trivial difference between the two sets of data. This tells us that there are parameters present in the circuit that we have not yet captured with our model. While the pulse sharpening can still be seen to exist, it is not nearly as dramatic.

An interesting note when viewing this data is the effect of our circuit on the fall time of the signal. Due to polarity of the

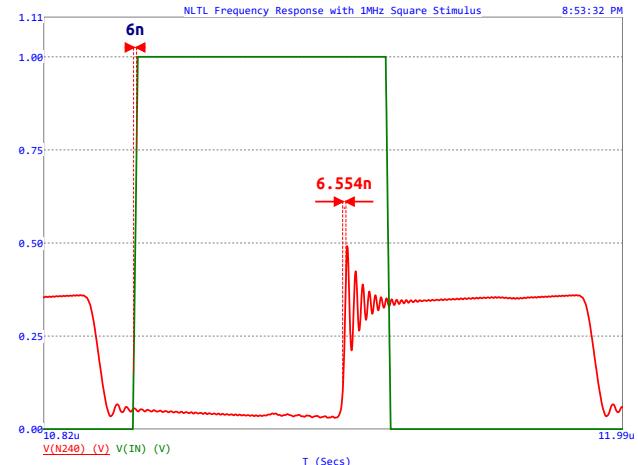


Figure 14. Accounting for Series Resistance shows that there is a certain point where no more sharpening takes place



Figure 15. Measured Risetime with 1V DC Bias

varactor in our current circuit, only rise time is affected since the negative pulse puts the varactor into further forward bias. To overcome this, more sophisticated designs are needed. As it is now, the fall time of the pulse is unchanged and is in some cases slowed down.

We now change the stimulus to a 1Vpp Sine wave at 1Mhz and find the power spectrum of the NLT output. In figure 18, it is shows that as a non-linear circuit there is a great deal of

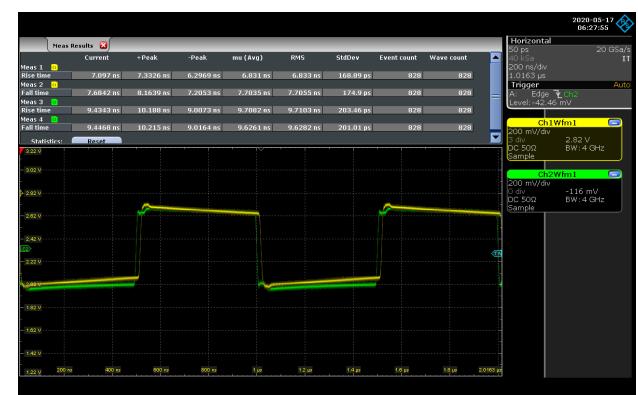


Figure 16. Measured Risetime with 2V DC Bias

Board 1 Measurements		
Offset (Volts)	Input Risetime (nS)	Output Risetime (nS)
0	10.522	5.9004
0.5	10.522	5.9004
1	10.133	6.6826
1.5	10.037	6.736
2	9.7556	6.7021
2.5	9.7082	6.831
3	9.674	7.022
0	195.09	137.12
Offset (Volts)	Input Falltime (nS)	Output Falltime (nS)
0	10.352	9.563
0.5	10.352	9.561
1	10.07	8.282
1.5	9.9755	7.9952
2	9.6713	7.7307
2.5	9.6261	7.7035
3	9.6033	7.8376
0	198.64	143.45

Table I

DATA FROM TRANSIENT RISETIME MEASUREMENTS.

Board 1 Simulations		
Offset (Volts)	Input Risetime (nS)	Output Risetime (nS)
0	10	9.186
0.5	10	9.18
1	10	9.178
1.5	10	9.191
2	10	9.285
2.5	10	9.376
3	10	9.45
0	200	198.242
Offset (Volts)	Input Falltime (nS)	Output Falltime (nS)
0	10	11.261
0.5	10	11.019
1	10	10.832
1.5	10	10.7
2	10	10.694
2.5	10	10.696
3	10	10.698
0	200	201.794

Table II

DATA FROM TRANSIENT RISE TIME SIMULATION RESULTS

harmonic content generated due to non-linearity. We expect to see odd and even harmonics throughout the entire sweep.

Figure 17 is the simulated power spectrum of our output signal. Comparing this to figure 11 tells us that our board does not produce as much harmonic content as expected from our circuit model. To get a better view the data we apply a hanning window before performing the FFT. The results for this are shown in figure 18. This time we see that the magnitudes of the harmonics in relation to the fundamental frequency more closely resemble the measured results. We chose the hanning window to focus more on the magnitudes of each harmonic since the noise floor resolution does not give us any meaningful information.

To further test this assumption, we can adjust the inductor model or include the other classic parasitic components of a transmission line as shown and discussed in [5].

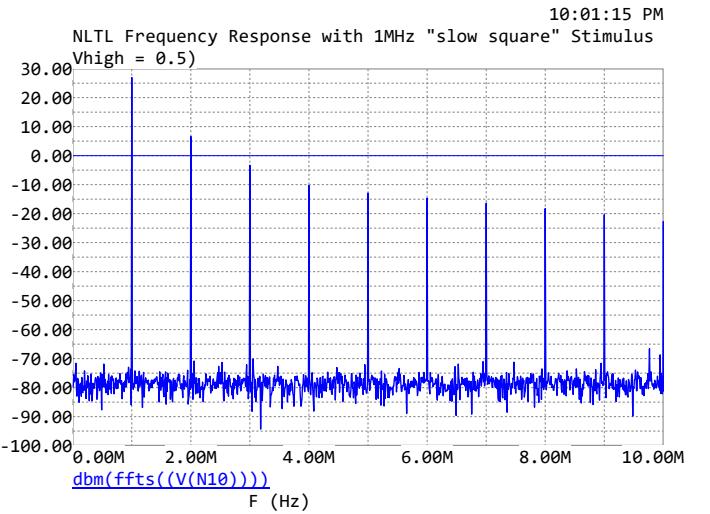


Figure 17. Expected Power Spectrum when DUT fed with 1Mhz 1Vpp Sine Wave

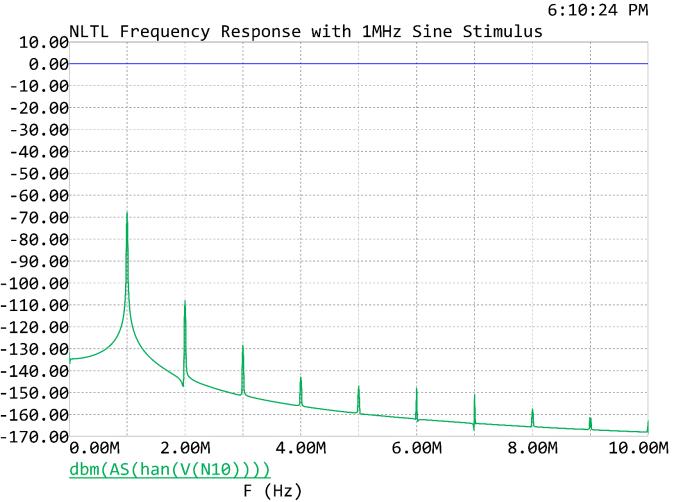


Figure 18. when DUT fed with 1Mhz 1Vpp Sine Wave

#### D. S-parameters

Figure 20 shows the schematic used to measure and compare our measured s-parameters. These were measured with a NanoVNA and The circuit simulations include signal loss with series resistances. The NanoVNA data is imported through the use of n-port components and define statements are utilized to calculate other parameters such as generated power in dBm, VSWR, etc...

To produce figure 21, we parameterized the values of our parasitic elements in the circuit and within the BBY40 model itself. We changed these values to match our measured data more closely to see the accuracy of our model. While we were able to achieve relatively agreeing data we still see a large discrepancy in our S11 data. At 10MHz, we see our measured data is roughly  $-10\text{dbm}$  lower than our expected simulation. This is likely due to the extra loss on the physical PCB not included in our model. NLTL's are also inherently mismatched for when operated in broadband applications. This

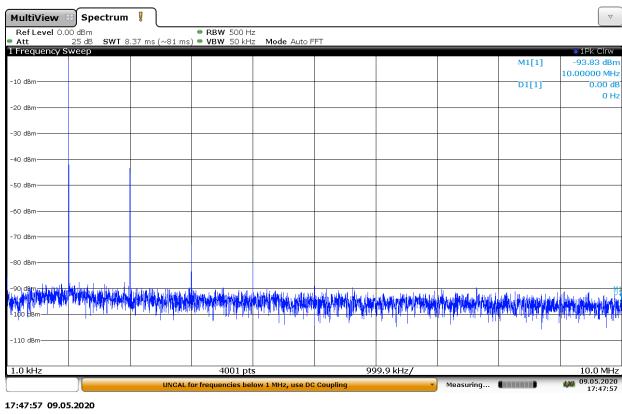


Figure 19. Measured Power Spectrum of Board 1. We see a lack of the harmonics we expected from simulation

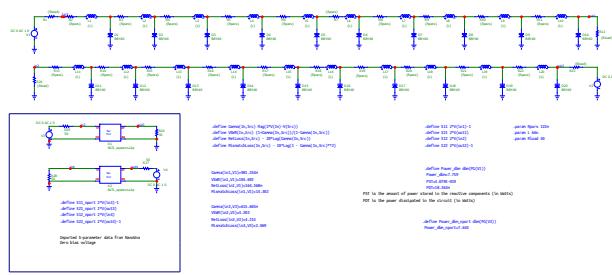


Figure 20. Schematic used to generate S-parameter plots. The top line measures S11 and S12, and bottom line measures S21 and S22.

is due to the impedance shifting caused by the change in varactor capacitance [1].

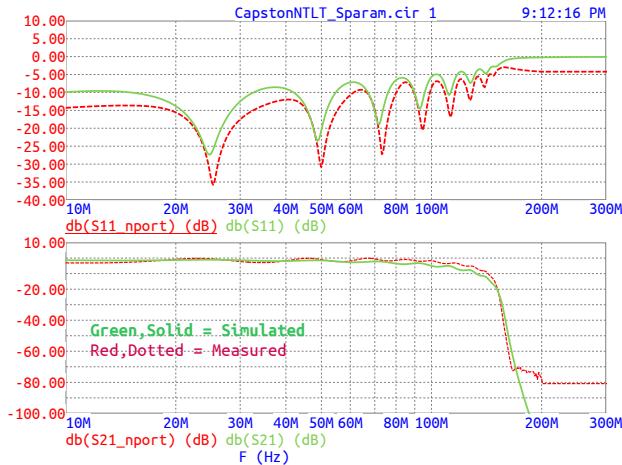


Figure 21. Simulated vs. Measured  $S_{11}$  and  $S_{21}$ . Corrections to make on next draft include more sensible scaling of axes

In figure 22, we see that our measured and simulated are almost identical except for a sharp rise in VSWR near the resonant frequency of our LC network (144MHz). After this point, we expect our VSWR to start rising dramatically. What we see is a much more subtle increase from about 1.5 to 5. Still, a much larger ratio than was present within our operating bandwidth, but certainly not the expected value of  $\approx 100$ .

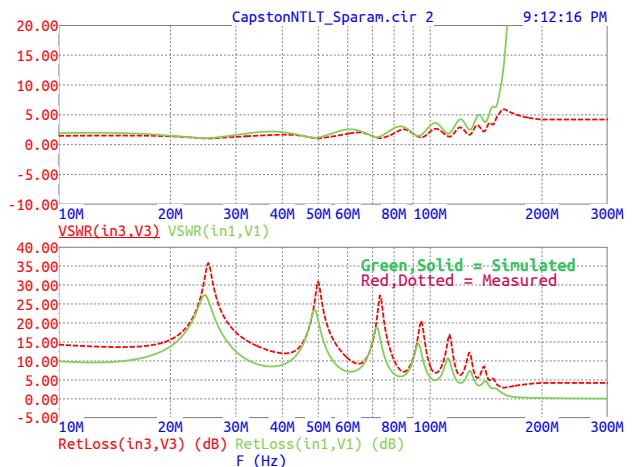


Figure 22. Simulated vs. Measured Return Loss and VSWR

### E. Estimating Circuit-Q



Figure 23. Transient Waveform for Estimating Q

To estimate our circuit Q, we employ a technique called ring-down method [10]. Driving the circuit with a square wave much slower than the expected resonance frequency of the LC network, we simply count the number of cycles it takes for the signal envelope to decay to roughly 50% of the maximum amplitude. Observing figure 23, we see that the ringing dies down in about 1 cycle. To get our Q estimate, we simply multiply this value by 4.53. This yields an approximate Q of 4.53 for our transmission line. This seems a little lower than expected however, we can see that the ringing is not as clean as we expected. It is unsurprising that our non-linear circuit results in a fluctuating impedance on the line causing reflections and is prone to generating harmonic content.

By feeding in a 1Vpp Sine wave and measuring the frequency response of our circuit, we see that many harmonics should be present in our line. Since we are using this simulation to stand in place of physical measurement, this interference makes sense.

To repeat this process for our physical circuit is a good next step to confirm the observed value of  $Q \approx 5$ .

## VI. NEXT STEPS

### A. Verilog-A Module

While we were able to draft a preliminary Verilog-A module for this project, we were unable to fully debug, implement,

or optimize this code. Introductory literature exists explaining how these models are constructed and used [11]. There also exists literature specifically geared toward creating RF models using Verilog-A [12].

### B. Using varying physical circuit geometry

figure 24 shows a possible implementation of pulse sharpening by taking advantage of the circuit's physical geometry to produce further non-linearities and mismatches in the circuit. This type of geometry should be used with much higher frequencies than the designs we created for this report as it relies on the lines themselves to act as inductive components. This exploration may have several advantages including easier reproduction and less resistive losses on the line due to lack of discrete inductors.

As an intermediate step, it may be beneficial to conduct further simulation with varied inductance and parasitics to emulate the behavior of this topology. "non-uniform" topologies have other applications and some examples can be found in spectroscopy [13] with use as antenna tuners [14] or even in bandpass filter designs [15].

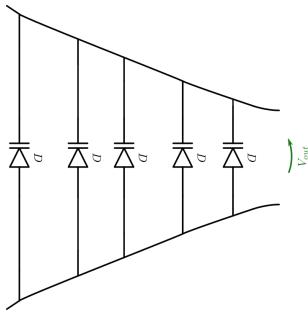


Figure 24. Potential circuit geometry to be simulated and built going forward

## VII. CONCLUSION

In this paper, we have summarized the work we have done in understanding the use of NLTL's and nonlinear waves in general and attempted to reproduce these results using simulation and measurement. While it was a good first attempt, there are many areas to explore further such as the simulation, building and measurement of a model dealing with higher bandwidths (0-6GHz), Non-uniform geometry, simultaneous edge sharpening, and writing a more accurate Verilog-A module. For much higher frequencies, the design may need to be constructing using ADS and momentum as this necessitates much smaller components and boards.

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