Circuit Simulation of Varactor Loaded Line Phase Shifter

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Abstract— This paper describes circuit simulation of analogue phase shifter based on distributed CPW transmission lines loaded by Varactor diodes. The expression of phase shifting is obtained using the global (S_{ij}) matrix of 9 units of proposed phase shifter. The simulations are carried out on ADS simulator. Comparison between our simulated results and published measurements of the studied phase shifter is made and a good agreement is obtained.

1. INTRODUCTION

Over the last decades, several advances have been made in analogue and digital. These devices are used to change the insertion phase of transmitted signal. The main and interesting phase shifters are those providing low insertion and return loss, and equal amplitude in all phase states. These criteria are becoming very important for several wireless communications. Most of phase shifters are reciprocal networks, meaning that they work effectively on signals passing in either direction. Phase shifters can be controlled electrically, magnetically or mechanically [1]. The main important application is within a phased array antenna system in which the phase of a large number of radiating elements can be controlled to force the electromagnetic signal to add up at a particular angle to the array.

In this paper, distributed phase shifter consists of a high impedance line ($180\,\Omega$) capacitively loaded by the periodic placement of varactors. By applying a single bias voltage on the line, the distributed capacitance can be changed, which in turn changes the velocity of the line and creates a phase shift [2]. The phase shift can be varied in a large variation range depending on the bias voltage and the length of the distributed line.

2. LOADED LINE THEORY

The first step in understanding loaded phase shifter is the basic "electrically NonLinear Transmission Line" (NLTL). NLTL is consisting of coplanar waveguide (CPW) periodically loaded with reverse biased varactor diodes. Nonlinearity is created by the voltage controlled capacitance. The Figure 1 presents two models of our phase shifter unit: the circuit model (Figure 1(a)) and the equivalent model (Figure 1(b)).

Basically, the transmission line model using series L ($\mathrm{H \cdot m^{-1}}$) and shunt C ($\mathrm{F \cdot m^{-1}}$) lumped elements [4], has a phase velocity defined by (1).

$$v_p = \frac{1}{\sqrt{LC}} \tag{1}$$

With a line of constant physical length, a phase shift can then be introduced by varying the phase velocity. A variable L or C is needed to vary v_p. In a transmission line shunt loaded with diodes shown in Figure 1 the total capacitance, and hence the phase velocity become a function of DC bias voltage defined and shown in Equation (2) where l_{sec} is the physical length of a transmission

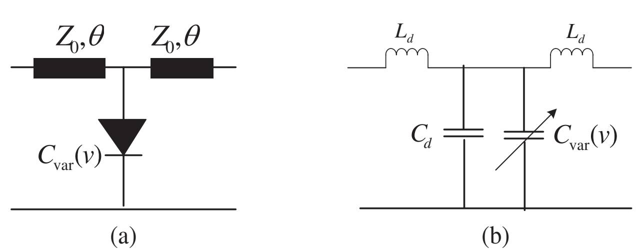


Figure 1: Circuit model of NLTL unit [3].

line section in meters [2]. The parameters C_d and L_d are the inductance and capacitance of each unit cell. L_d, C_d and C_{var} have the same units as L and C respectively.

$$v_p = \frac{1}{\sqrt{L_d\left(C_d + \frac{C_{var}}{l_{\text{sec}}}\right)}} \tag{2}$$

The model of periodic sections transmission line has a Bragg frequency defined and shown in Equation (3), it is similar to optical Bragg diffraction.

$$f_{Bragg} = \frac{1}{\pi\sqrt{L_d\left(C_d + C_{var}\right)}} \tag{3}$$

The first decision is, which transmission line topology have we to use. Coplanar wave guide (CPW) was chosen for our phase shifter structure. CPW has some immediate advantages. First, both ground and signal lines are on the same plane affording easy access for shunt mounting of elements without drilling. Second, CPW has a canonical closed form model from [7] that can be used to obtain design equations.

To maintain a balanced CPW line, a balanced shunt loading topology was chosen with two shunt diodes per transmission line cell unit, one to each of the ground planes.

The variable capacitance parameters are set by the choice of diodes. From (3), a larger C_{var} will cause a reduction in the maximum operating frequency. Also, the range from $C_{var\_\max}$ to $C_{var\_\min}$ will affect the variability of the phase velocity of Equation (2) and hence the phase shift. This affects some of variations in the characteristic impedance Z_0 of the line versus C_{var} [5] as shown in Equation (4), which is desired to be $50\,\Omega$ or impedance matching.

$$Z_0 = \sqrt{\frac{L_d[H]}{C_d[F] + C_{var}[F]}} \tag{4}$$

3. DIODE VARACTOR MODEL

After studying several diodes models, and matching schemes in simulation, the given model by Equation (5) was chosen. With specified $C_{var\_\max}$ to $C_{var\_\min}$ ratio this diode affords reasonable phase shift while allowing the transmission line to be well matched to 50 ohms without additional circuitry.

Diodes have two origins of nonlinearity: conductive and reactive [3]. The conductive nonlinearity is shown in the $I(v)$ curves and the reactive nonlinearity is shown in the $C(v)$ curves.

This model of diode varactor has a series resistance R_s, parasitic series inductance L_s, and parasitic parallel capacitance C_p. Equation (5) gives the mathematical model of simulated varactor diode [8].

$$C_j(V_j) = \frac{C_{j0}}{\left(1 - \frac{V_j}{\phi}\right)^M} \tag{5}$$

where C_j is the fitted junction capacitance, C_{j0} is the zero-bias junction capacitance, V is the junction potential, ϕ is the fitted potential barrier and M is the grading coefficient.

4. LOADED LINE PHASE SHIFTER

After choosing an appropriate diode model the remaining degrees of freedom are substrate choice and loading factor as defined by [5] and shown in the Equation (6). For our simulation RG4003 substrate was chosen to apply the ideal closed form CPW equations.

$$x = \frac{C_{\max}/l_{\text{sec}}}{C_d} \tag{6}$$

From that choice, the required CPW line parameters can be computed to give a $50\,\Omega$ matched line. From [5], the relation between loading factor and the characteristic impedance of the CPW line is shown in (7). From $C_{var\_\max}$ and x from (8), the desired C_d is obtained. The open CPW closed form expressions given by [7] can be used to compute the C [F/m] of the CPW line shown in Equation (11), given Z_i from CPW Equations (9) and (10). The length of each T-line section cell, l_{sec}, is given by (12). Z_i is the characteristic impedance of each section.

$$Z_i[\Omega] = 50\sqrt{1+x} \tag{7}$$

$$C_d = \frac{C_{\max}}{x} \tag{8}$$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} \tag{9}$$

$$KK = Z_i \frac{4\sqrt{\varepsilon_e}}{120\pi} \tag{10}$$

$$C = \frac{4\varepsilon_0\varepsilon_e}{KK} \tag{11}$$

$$l_{\text{sec}} = \frac{C_d\,[F]}{C\left[\frac{F}{m}\right]} \tag{12}$$

For $x = 5$, the simulation parameters are: $Z_i = 122\,\Omega$, $C_d = 0.4\,\text{pF}$, and $l_{\text{sec}} = 8.9\,\text{mm}$. These parameters are then introduced into ADS simulator, and the diode model given by the Figure 2 with a grading coefficient $M = 0.5$, for simulating this phase shifter. The corresponding dimensions of $Z_i = 122\,\Omega$ (CPW) are $W = 2.5\,\text{mm}$ for a conductor width, and $G = 3\,\text{mm}$ for a gap. The input line CPW ($Z_i = 50\,\Omega$) for the biasing sections was computed to have the dimensions $W = 2.5\,\text{mm}$ and $G = 0.25\,\text{mm}$. The Figure 3 gives the circuit model of our studied phase shifter.

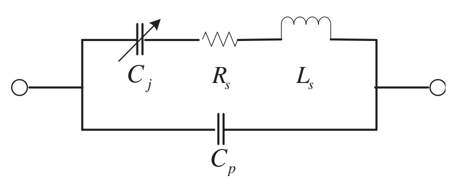


Figure 2: Circuit model of diode Varactor [8].

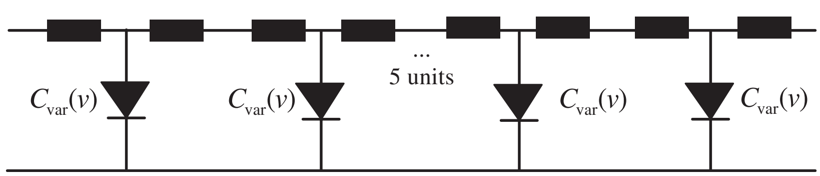
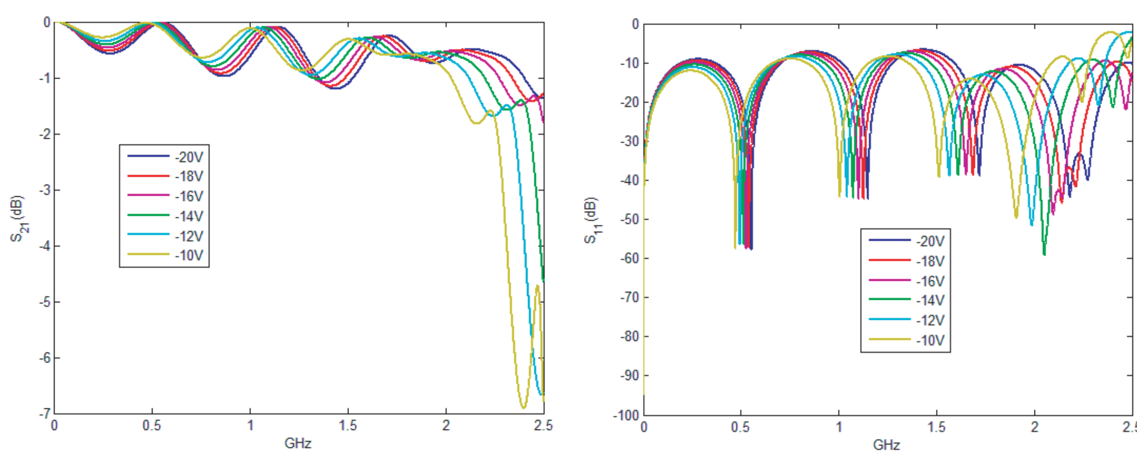


Figure 3: Circuit model of phase shifter.



(a) (b)

Figure 4: Insertion and return losses of our phase shifter.

The number of segments is chosen for the desired phase shift at operating frequency, and we have in our case nine sections.

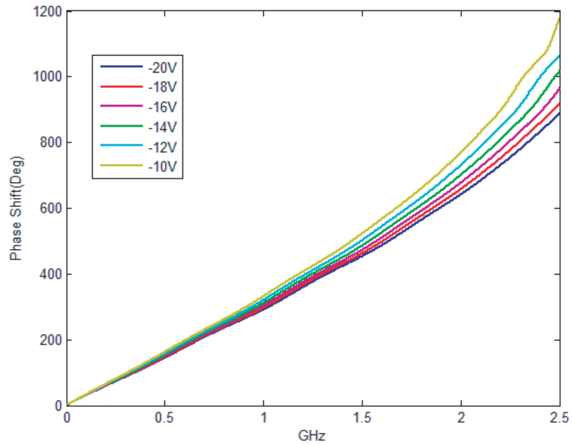


Figure 5: Phase variation over voltage.

5. SIMULATION RESULTS

ADS simulator of Agilent was chosen as circuit simulator. All of the components can be modeled in a circuit simulator. As shown in Figure 4, the return loss S_{11} (Figure 4(b)) of our studied phase shifter is no less than 10 dB up to 2 GHz and the insertion loss S_{21} (Figure 4(a)) is no more than 1 dB.

Figure 5 shows the phase shift versus bias voltage. In our simulation, we can see 1dB of insertion loss at $V_{bias} = -10\,\text{V}$, the phase shift can reach approximately 800° at 2 GHz.

6. CONCLUSIONS

In this work, we have developed a circuit modeling for analogue distributed phase shifter, the measurements of which were published. We used varactors diodes controlled by bias voltages. We have also shown that significant phase shift can be generated using a loaded line phase shifter. The phase shift obtained was linear from 100 MHz up to 1.5 GHz. Then the phase shift has a quadratic variation from 1.5 GHz up to 2.5 GHz. The values obtained by authors of [6] extend up to 800 rad/s according to varactors polarisation voltage. The obtained results are good, but the main drawback is the non linear variation of phase shift as function of frequency due to varactors.

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