

# Exploring the Usefulness of Varactor loaded Nonlinear Transmission Lines

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**Abstract**—In this paper we will discuss the use of nonlinear elements within a transmission line to study their effects on the speed and shape of an input pulse, and how the next group which takes over our work may use this information to design similar circuits with improved bandwidth and/or performance.

## I. INTRODUCTION

The goal of this project was to explore how non-linear transmission lines behave when loaded with varactors and how they can be used. Using design methodologies taken from previous studies and IEEE research, we have constructed a varactor loaded transmission line and attempted to observe and replicate the pulse sharpening effect shown in the literature.

First, we discuss the necessity of non-linear components in such a Nonlinear Transmission line or *NLT* for short. We then discuss ways in which the devices we use in simulation are modeled and the obstacles we faced in constructing these models. We simulate these nonlinear lines using MICROCAP and discuss possible reasons for the discrepancies we have seen between research and simulations.

To verify the characteristic capacitance-voltage or CV curves of our chosen components, we construct a simple test fixture and measure capacitance vs. voltage using a DC power supply to reverse bias the varactor diodes and a handheld LCR meter.

## II. THEORY

### A. Why use Nonlinear Devices?

Non-linear devices in transmission lines have been widely used for pulse sharpening in particular. Similar sharpening can be observed by use of non-linear inductors and theoretically by strategic placement of dielectric material in the line [1]. The non-linearity helps us because it allows for voltage dependence impedance on the line. When an input pulse is sent through such a line, the voltage dependence causes a change in line impedance and a change in the behavior of the lumped element stubs which are also essentially low pass filters.

### B. Varactors vs. Nonlinear Capacitors

While nonlinear capacitors have been used in many studies [2] when implementing this design in high power systems, varactor diodes have the advantage of a larger capacitance range, and allow us to perform measurements using lower voltages. In addition, the overall design is simplified with the use of Varactors because only one bias is needed.

In any case, non linear capacitors are often modeled using equation 1 to describe the voltage dependence of the capacitance [3].

$$C(v) = \frac{C_o}{\sqrt{1 + v/V_o}} \quad (1)$$

where  $C_o$  and  $V_o$  are zero bias capacitance and reference voltage, respectively.

### C. Methods of Modeling Varactors

In order to properly simulate and predict data using these simulations, we need first to determine how to model the non-ideal parasitics of the line and particularly the behavior of the chosen varactor diode loading the NLT. There are several ways to accomplish this. The most standard and the method chosen by our group is SPICE modeling. The disadvantage of this route is that nonlinear behavior can be particularly hard to model with SPICE alone at higher frequencies and voltage levels (find source for this, think it's in SKYWORKS application note).

Another industry standard used to do this is by modeling via Verilog code. Specifically, Verilog-AMS or Verilog-A modules can more accurately capture the non-idealities in capacitors and varactors. This is a useful tool to explore as it can be integrated with many commercial simulation programs such as ADS.

### D. Modeling Board Characteristics

When constructing a test fixture for measurements of NLT's of higher frequency, we must also take into account the properties of the board we are working with. For our low frequency model and with limited access to robust VNA's this procedure was not necessary but we recommend using the two-line pencil method to approximate the board permittivity and loss tangent as utilized to do the same for flex PCB's due to its simplicity and limited need for equipment [4].

For our board, we used a simpler method which may prove useful as a quick and dirty alternative to the one described above. To find the permittivity of the board we used a simple LCR Meter (DE-5000) and the following formula of a parallel plate capacitor as shown in equation 2.

$$C = \frac{\epsilon A}{d} \quad (2)$$

Where we treat the width of the dielectric as plate spacing  $d$ , the board area as area,  $A$ , and measured capacitance as  $C$ . Solving for Permittivity  $\epsilon$ , we found a relative permittivity of  $\epsilon_r \approx 3.54$ . For this measurement a figure normally given for FR4 is roughly 4.0 to 4.4. A few possible things could cause this error.

The device used to measure the FR4 board generates a test frequency of 100kHz at maximum. Relative permittivity is usually given for FR4 at a much higher frequency in the MHz range. Another is the precision achievable when measuring the dielectric thickness. A caliper would be much better suited for this task. Alternative methods do exist and are quite simple but do necessitate access to a VNA [5].

*1) SPICE Models:* SPICE models are typically easier to find and use in most circuit simulation software and what we used for our low frequency prototype as it seemed to be sufficient for our purposes. We chose to use software from the company SpectrumSoft. We chose this tool due to its vast array of built-in SPICE models and capabilities. For example, it ships with SPICE models for the BBY40 and SMV1249 varactor diodes. Previously a software found in industry for a high price, SpectrumSoft is now no longer in business and has released this program free. It can be downloaded from SpectrumSoft's home page.

Additionally, the SPICE model for the hyper-abrupt varactor SMV1249 is found in application notes from their manufacturer, SKYWORKS Inc.

*2) Verilog-A Modules:* We were unable to utilize this modeling method. In section VII, we go over some potentially useful references to help you create models for higher frequency/bandwidth designs. Most verilog modules we have come across utilize equation 1 in order to model non-linear capacitors and varactors.

### III. SIMULATIONS

In this section we will discuss the basics behind catch-up theory [1] and how we confirmed this with simulation.  $\Delta T$  represents the time delay at the  $N^{th}$  node and is found by the difference period the line cutoff frequency at zero-bias varactor capacitance and the period of the line cutoff where varactor capacitance is defined by the step input maximum. This result is multiplied for every ladder section the pulse passes. Catch-up theory suggests that this delay is accounted for the variation in phase velocity as the rising pulse effects the varactor capacitance.

#### A. Simulating Rise Time

In our simulations we use an input step of 5 volts which takes  $1\mu s$  to reach its final value. Using equation 3, we

calculate a pulse sharpening of  $8.44ns$  at our  $10^{th}$  node and  $84.37ns$  at our  $100^{th}$  node. To make these calculations, we used the CV plots obtained by measuring the BBY40 with the test fixture discussed in section V-A.

$$\Delta T = N(\sqrt{LC_o} - \sqrt{LC_s}) \quad (3)$$

For a lossless line, the sharpest pulse we can achieve can be estimated by first using equation 4 taken from [1]. This gives us the ideal cutoff frequency of the line which in Hz is about  $f_c \approx 290MHz$ . The period of a wave moving at this rate is  $T \approx 3.4ns$ . While we have not been able to achieve a rise time of this magnitude, we need to remind ourselves of the inherent parasitics we are dealing with. Using a basic model with values from our inductor and varactor diode datasheet. We have a per section series resistance of roughly  $R_s = 122m\Omega$  at DC, and a parallel resistance given by the resistance inherent in the varactor packaging as well as of the trace itself. This value was taken from the SPICE model used and was  $R_p = 1m\Omega$

$$\omega_c = \frac{2}{\sqrt{LC}} \quad (4)$$

In figure 1 we can see that when simulating our ideal line, equation 3 is proven to be a very rough estimate to what we see. while at the  $10^{th}$  section, we see a very similar value of about 6ns compared to the 8.4ns calculated earlier, at the  $100^{th}$  section we see about half of the expected pulse sharpening with our simulated value of 45ns compared to 84ns calculated.

At this time, we are unsure as to what has caused the discrepancy between calculation and simulation but we suspect it may have to do with our inability to properly model the nonlinear nature of the varactor diodes.

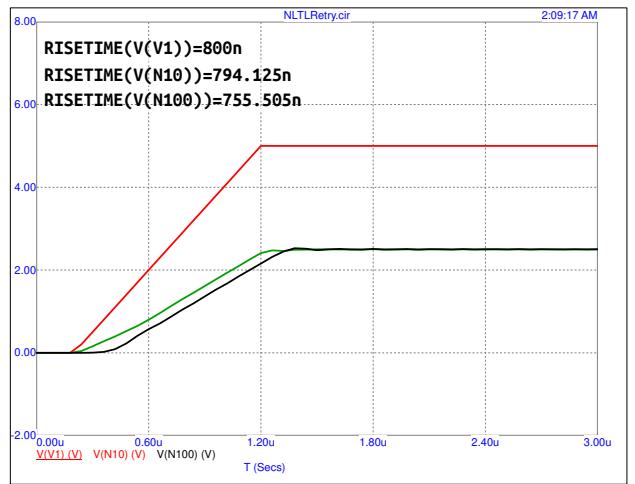


Figure 1. Rise time at source, node 10 and node 100 simulated with no resistive loss

In figure 2, we add the series DC resistance of the inductor ( $R_s \approx 122m\Omega$ ) and the  $1m\Omega$  resistance of the BBY40. From this, we see that not much has changed in this model and in fact we see an increased sharpening effect if anything. We do notice however, that the amplitude of the wave is much more attenuated at our  $100^{th}$  node. This would lead us to expect a decrease in the pulse sharpening in the circuit instead of a

relatively constant value due to the lessened effect on varactor capacitance as the pulse climbs.

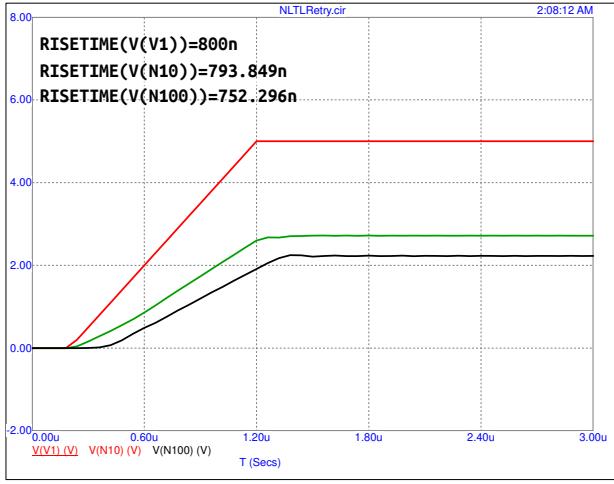


Figure 2. Rise time at source, node 10 and node 100 simulated with resistive loss of  $0.122\Omega$  per ladder section

Figure 3 explores the effect of different biasing on our line as well as how long a line we can practically use for sharpening purposes. As our DC resistance grows with our line length, we expect our amplitude to keep dropping. As the amplitude of the traveling wave is reduced, we effectively trace out less of our varactor CV curves. Due to this, the CV relationship will begin to look more and more linear as we add ladder sections to our design. We have used a parametric plot to show the limits of this pulse sharpening as we increase the line length and plotted rise-time vs. DC bias for each 10<sup>th</sup> node of the ladder. The input pulse used in this case was 400ns.

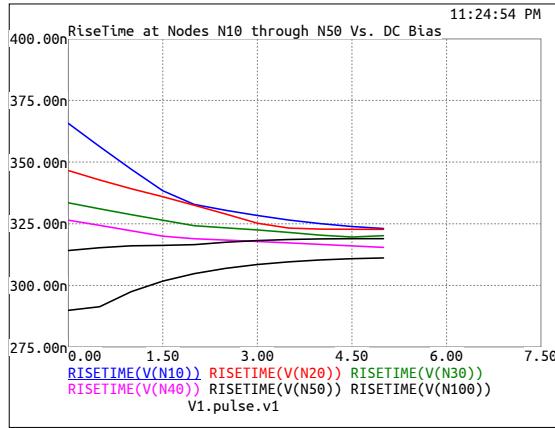


Figure 3. Risetime Vs. Line Length vs. DC Bias Voltage

#### IV. BOARD DESIGN

In order to test all these simulated values we designed a discrete version of our transmission line using Altium Designer. We emphasized traces being as short as possible and used Altium's built-in impedance profile tool to match our path between each pair of SMA connectors to  $50\Omega$ . The circuit we constructed is shown assembled in figure 4.

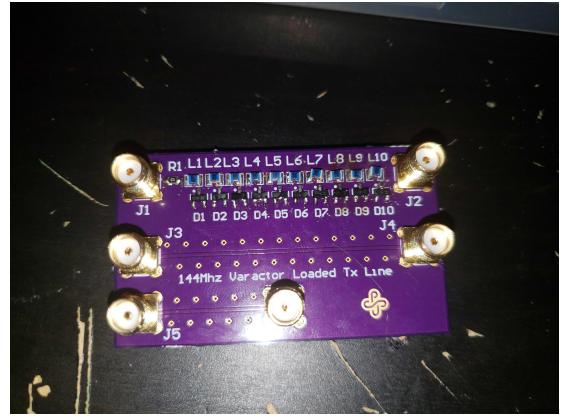


Figure 4. Assembled Tx Line Board made for 144Mhz

### V. MEASUREMENT RESULTS

#### A. Varactor CV Curves

To measure and find the capacitance vs Voltage of our chosen varactors we created a small ugly style circuit based on a design by W2AEW. Two 100k resistors are added to limit current flowing to the power supply. A ceramic capacitor of value much greater than our varactor is placed to protect the meter from excessive voltage. Since this larger capacitance is in effectively in parallel with our varactor, our meter measurement is approximately only the capacitance of the varactor diode itself.

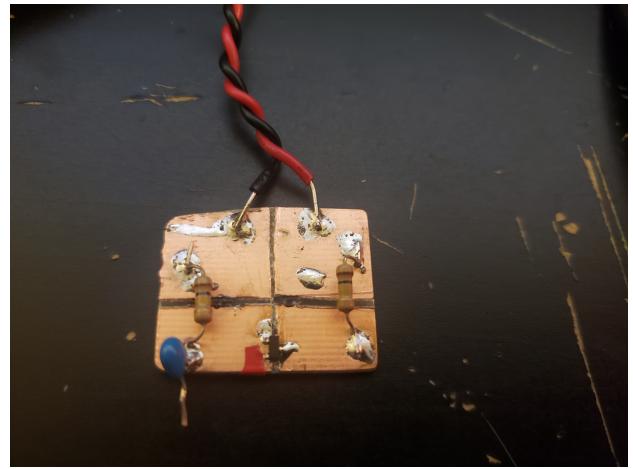


Figure 5. Test Fixture used for plotting CV Curve of BBY40

Through use of this fixture, we were able to generate the curves shown in figures 6 and 7. These were in close agreement to curves found on datasheets for the BBY40 and SMV1249 respectively.

#### B. AC Response

#### C. Rise Time

We had great difficulty in measuring rise time of our circuit and the main problems we faced were not understanding the theory well enough have do proper testing. While our components were chosen on the basis of working at 144Mhz,

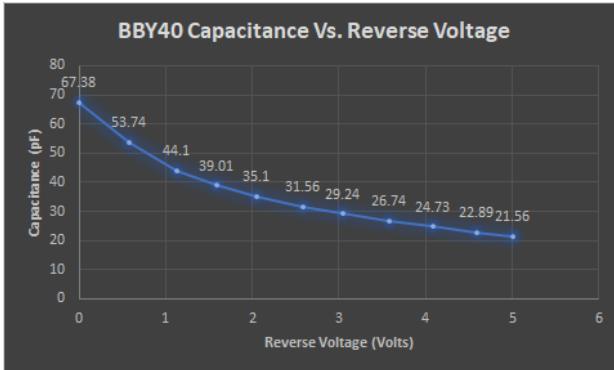


Figure 6. Measured CV Characteristics of BBY40

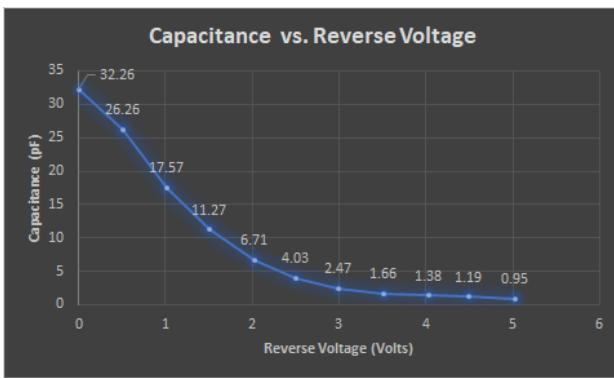


Figure 7. Measured CV Characteristics of SMV1249

we failed to see that driving our circuit below this bandwidth and performing similar simulations may be adequate to prove rise time performance increase. Another complication was keeping in mind the biasing conditions of the varactors. We did not design for a port in which to introduce a dc bias to our circuit and relied on equipment being able to accomplish this. Care must be taken when using analog generators to supply the DC bias to the circuit. Our particular model begins sweeping with a negative bias before reaching a positive one. This effectively puts the varactors into forward bias and allows

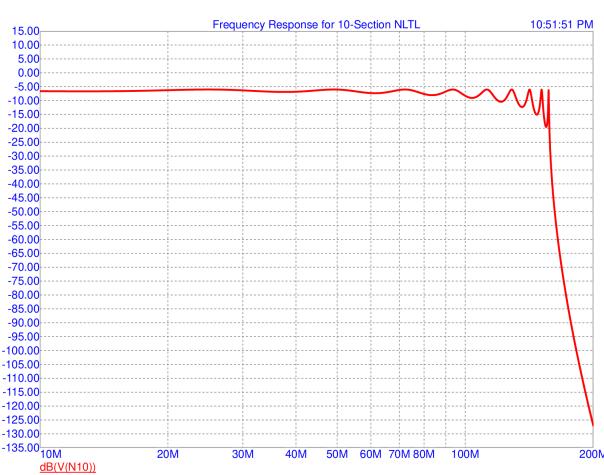


Figure 8. Simulated AC Response for Board 1

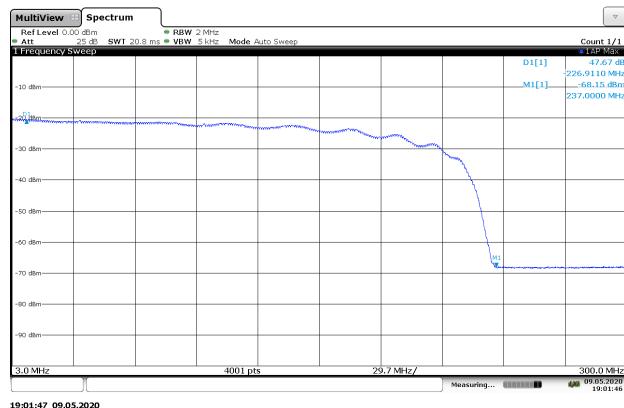


Figure 9. Measured Frequency Response for Board 1 (L= 56nH)

them to hold a charge.

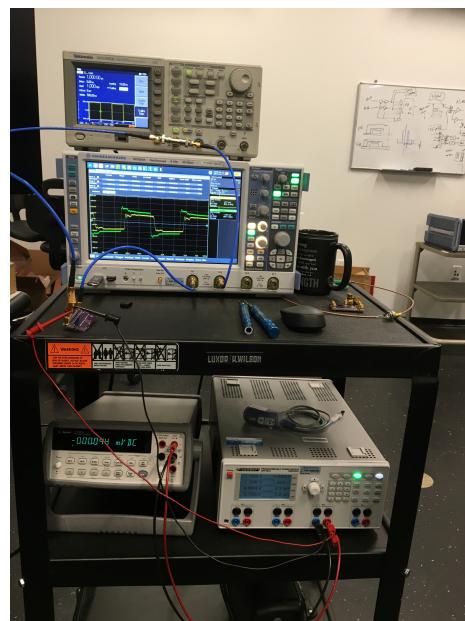


Figure 10. Test Setup for Measuring Risetime With Bias

#### D. S-parameters

In figure 18 shows the schematic used to measure and compare our measured s-parameters taken through a NanoVNA to our simulated circuit with parasitics included. The NanoVNA data is imported through use of the n-port components and define statements are utilized to calculate other parameters such as generated power in dbm, VSWR, etc...

To produce figure 19, we parameterized the values of our parasitic elements in circuit and within the BBY40 model itself. We changed these values to match our measured data more closely to see the accuracy of our model. While we were able to achieve relatively agreeing data we still see a large discrepancy in our S11 data. At 10MHz, we see a our measured data is roughly  $-10\text{dbm}$  lower than our expected simulation. This could be due to incorrect modeling of our load impedances and requires further study. Some have mentioned that when using NLTL's, there is bound to always be some

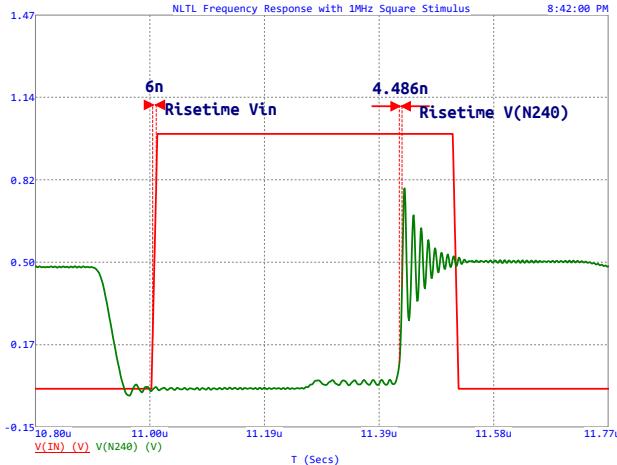


Figure 11. Simulated Risetimes for Input pulse, 10<sup>th</sup> node, and the 240<sup>th</sup> node

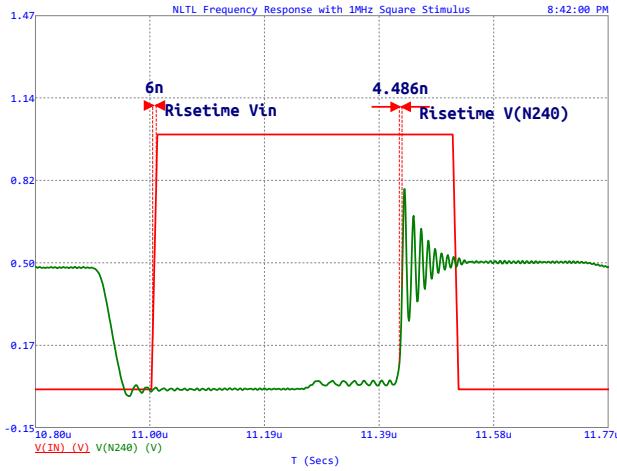


Figure 12. Accounting for Series Resistance shows that there is a certain point where no more sharpening takes place

impedance mismatch due to the changing impedance caused by varactor capacitance [1]. This may be the case here, but the issue is worth further simulation.

In figure 20, we see that our measured and simulated are almost identical except for a sharp rise in VSWR near the resonant frequency of our LC network (144Mhz). After this point, we expect our VSWR to start rising dramatically. What we see is a much more subtle increase from about 1.5 to 5. Still a much larger ratio than was present within our operating bandwidth, but certainly not the expected value of  $\approx 100$ .

## VI. MODEL ACCURACY/ PREDICTIONS

Under Construction: Using this section for generating bibliography for the the time being. We will work on predictions and further flesh things out during the next revision. [6] [7], [8], [9], [10], [11], [2], [3], [4], [12]

### A. Estimating Circuit-Q

To estimate our circuit Q, we employ a technique called ring-down method [13]. Driving the circuit with a square wave



Figure 13. Risetime Measurement from Board 1 (L=56nH)



Figure 14.

much slower than the expected resonance frequency of the LC network, we simply count the amount of cycles it takes for the signal envelope to decay to roughly 50% of the maximum amplitude. Observing figure /reffig:EstimatingQ, we see that the ringing dies down in about 1 cycle. To get our Q estimate, we simply multiply this value by approximate 4.53. This yields an approximate Q of 4.53 for our transmission line. This seems a little lower than expected however, we can see that the ringing is not as clean as we expected. It is unsurprising that our non-linear circuit results in a fluctuating impedance on the line causing reflections and is prone to generating harmonic



Figure 15.

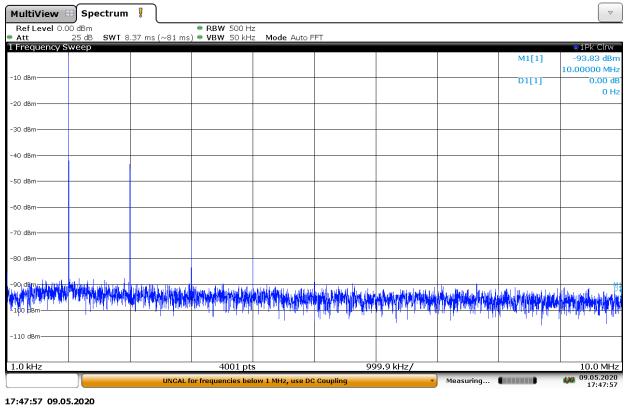


Figure 16.

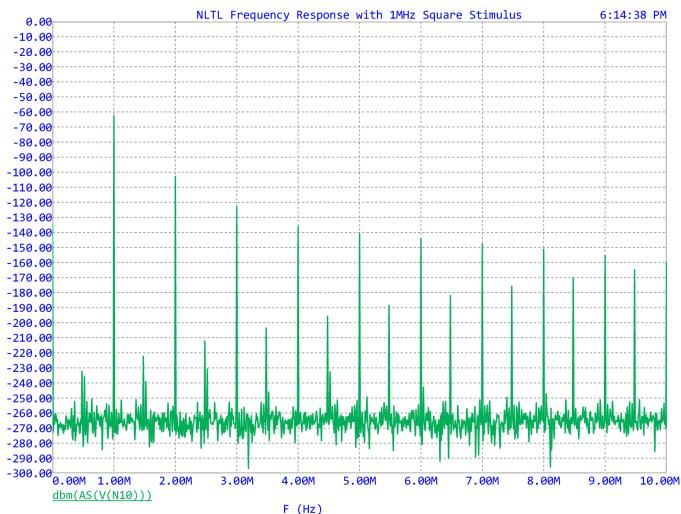


Figure 17. Expected Power Spectrum when DUT fed with 1Mhz 1Vpp Sine Wave

content.

By feeding in a 1Vpp Sine wave and measuring the frequency response of our circuit, we see that many harmonics should be present in our line. Since we are using this simulation to stand in place of a physical measurement, this interference makes sense.

To repeat this process for our physical circuit is a good next step to confirm the observed value of  $Q \approx 5$ .

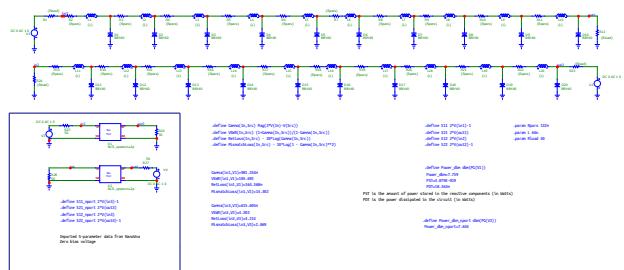


Figure 18. Schematic used to generate S-parameter plots. The top line measures S11 and S12, and bottom line measures S21 and S22.

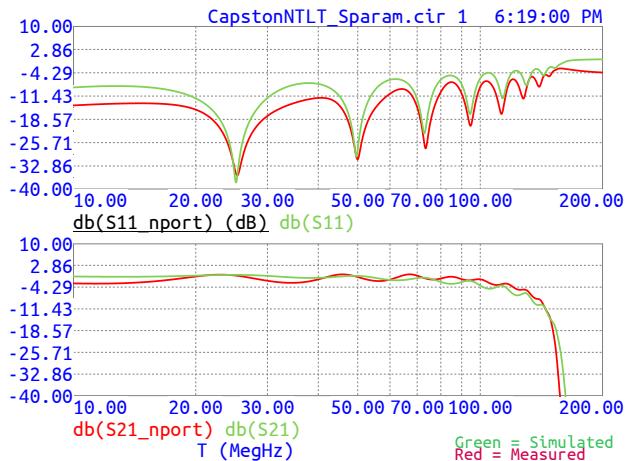
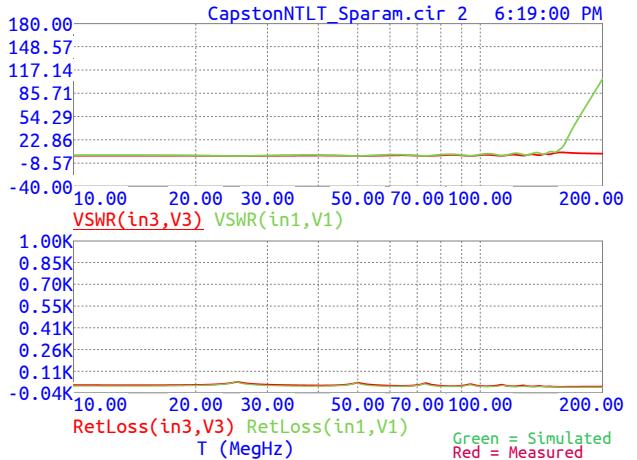
Figure 19. Simulated vs. Measured  $S_{11}$  and  $S_{21}$ . Corrections to make on next draft include more sensible scaling of axes

Figure 20. Simulated vs. Measured Return Loss and VSWR

## VII. NEXT STEPS

### A. Verilog-A Module

While we were able to draft a preliminary Verilog-A module for this project, we were unable to fully debug, implement, or optimize this code. Introductory literature exists explaining how these models are constructed and used [14]. There also exists literature specifically gear toward creating RF models



Figure 21. Transient Waveform for Estimating Q

using Verilog-A [15].

### B. Using varying physical circuit geometry

figure 22 shows a possible implementation of pulse sharpening by taking advantage of the circuit's physical geometry to produce further non-linearities and mismatches in the circuit. This type of geometry should be used with much higher frequencies than the designs we created for this report as it relies on the the lines themselves to act as inductive components. This exploration may have several advantages including easier reproduction and less resistive losses on the line due to lack of discrete inductors.

As an intermediate step, it may be beneficial to conduct further simulation with varied inductance and parasitics to emulate the behavior of this topology. "non-uniform" topologies have other applications and some examples can be found in spectroscopy [16] with use as antenna tuners [17] or even in bandpass filter designs [18].

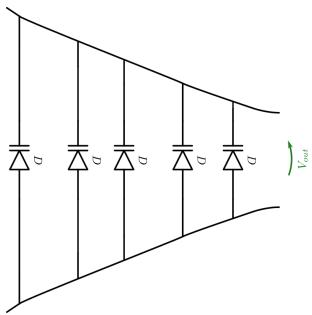


Figure 22. Potential circuit geometry to be simulated and built going forward

## VIII. CONCLUSION

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