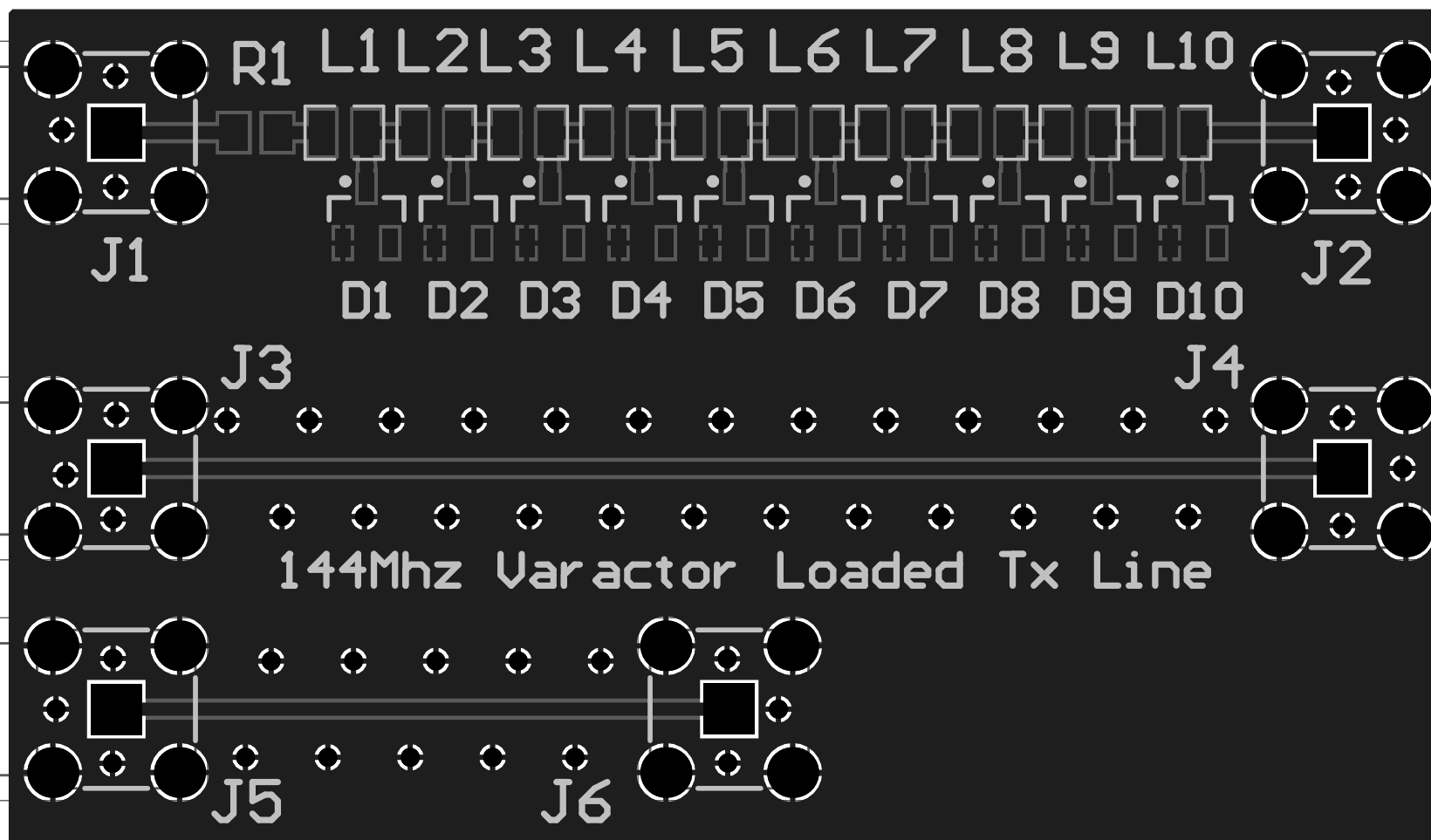


This is a discrete Tx Line to experiment with phase shifting and/or pulse shaping.
 The four sets of connected SMA jacks are included on the same board for calibration and de-embedding of the test fixture
 Calibration will be down with appropriate terminators using a 2x Thru. and a second line to be used in conjunction with the first to determine board characteristics using Two-Line method

Title		
Discrete Varactor Loaded Tlines (144Mhz)		
Size	Number	Revision
Orcad B		1.0
Date:	3/21/2020	Sheet of
File:	C:\Users\Redesign\VaractorTime144Mhz\Sh	Drawn By:



Bill of Materials

Bill of Materials for BOM Document [VaractorTline144Mhz.BomDoc]

Source Data From: VaractorTline144Mhz.BomDoc

Project: VaractorTline144Mhz.PrjPcb

Variant: None

Creation Date: 3/21/2020 1:22 PM

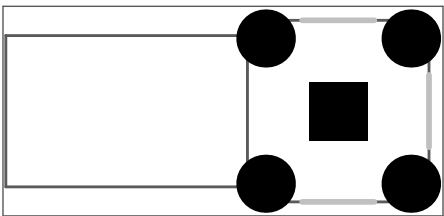
Print Date: 43911 43911.5577

Footprint	Name	LibRef	Designator	Description	Quantity
SOT23_N	Diode BBY40	Diode BBY40	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10	SOT23 Silicon Planar Variable Capacitance Diode	10
MOLX-731000114_V	731000114	CMP-2000-05487-1	J1, J2, J3, J4, J5, J6	SMA Right-Angle PCB Jack Receptacle, Brass Body, Gold Plated, 50 Ohm, 5-Pin THD, RoHS, Tray	6
0805HQ-SERIES	0805HP-56NXJRC	0805HP-56NXJRC	L1, L2, L3, L4, L5, L6, L7, L8, L9, L10	0805HP-56NXJRC Coilcraft Variable Inductor	10
RESC2013X70X40NL20T20	Jumper	CMP-1665-00002-5	R1	Chip Resistor, 0 Ohm, +/- 1%, 0.125 W, - 55 to 155 degC, 0805 (2012 Metric), RoHS, Tape and Reel	1

27

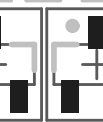
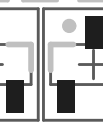
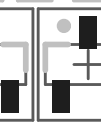
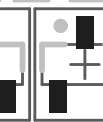
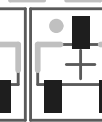
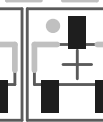
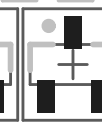
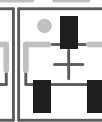
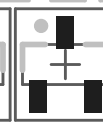
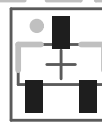
Approved Notes

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J1

R1 L1 L2 L3 L4 L5 L6 L7 L8 L9 L10



D1

D2

D3

D4

D5

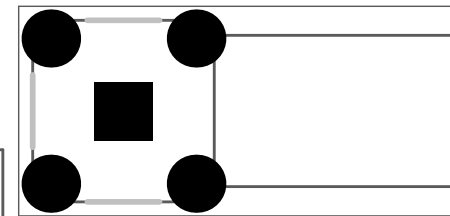
D6

D7

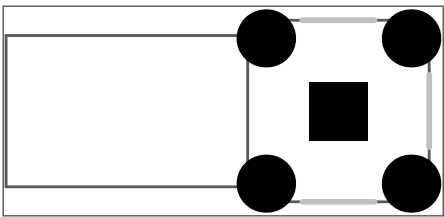
D8

D9

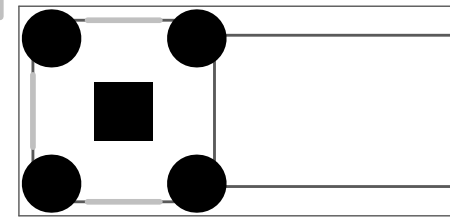
D10



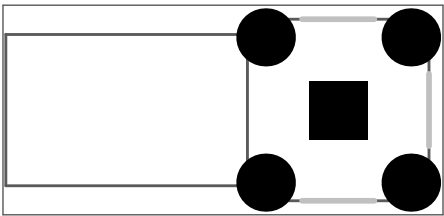
J2



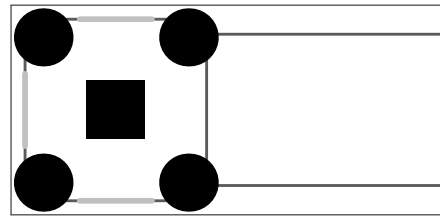
J3



J4

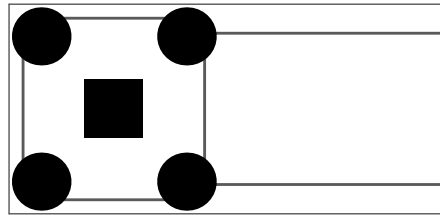
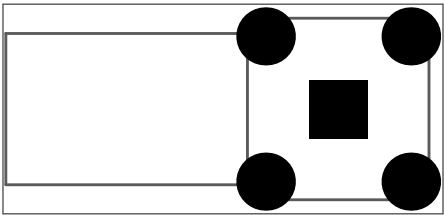
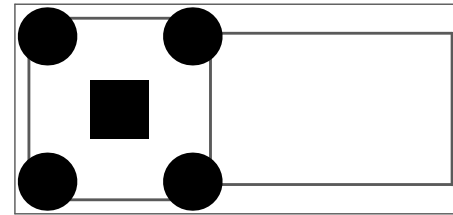
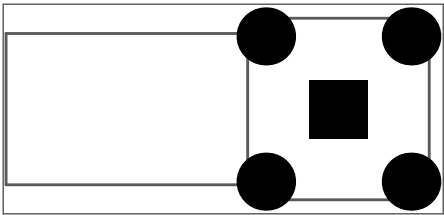
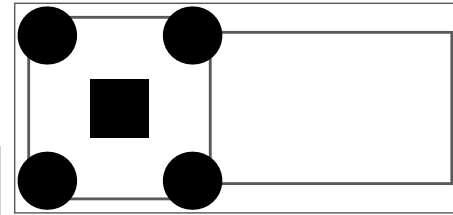
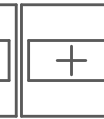
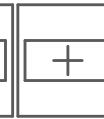
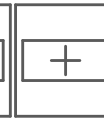
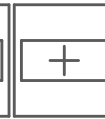
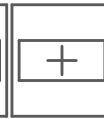
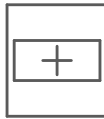
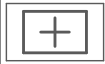
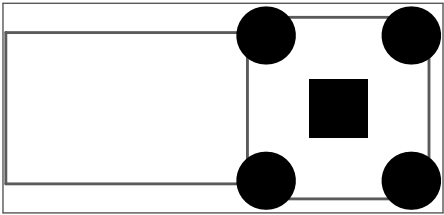


J5



J6

144Mhz Varactor Loaded Tx Line



Design Rules Verification Report

Filename : C:\Users\Public\Documents\Altium\Projects\Varactor_TxCap_new\RedesignVarac

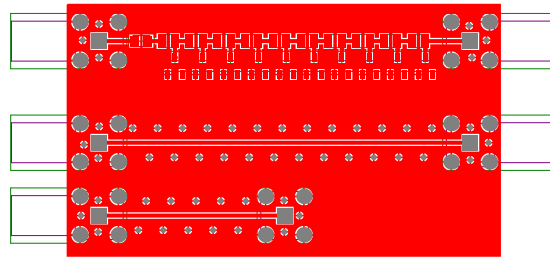
Warnings 0
Rule Violations 0

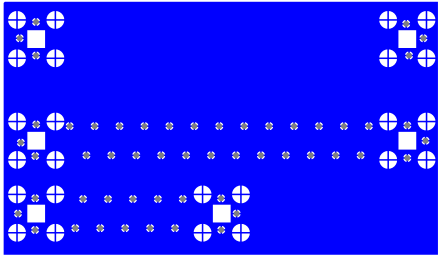
Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=6mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=50.00ohms) (Max=50.00ohms) (Preferred=50.00ohms) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=16mil) (Conductor Width=6mil) (Air Gap=6mil) (Entries=4) (All)	0
Minimum Annular Ring (Minimum=7mil) (All)	0
Hole Size Constraint (Min=13mil) (Max=265mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Room RedesignVaractorTline144Mhz (Bounding Region = (2475mil, 0mil, 4475mil, 1000mil	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for VaractorTline144Mhz.PrjPct





144Mhz Varactor Loaded Tx Line





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