A Nonlinear Lattice for High-Amplitude Picosecond Pulse Generation in CMOS

Wooram Lee, *Student Member, IEEE*, Muhammad Adnan, *Student Member, IEEE*, Omeed Momeni, *Member, IEEE*, and Ehsan Afshari, *Senior Member, IEEE*

***Abstract*—In this paper, we study an electrical nonlinear medium consisting of voltage-dependent capacitors and inductors to generate sharp pulses from a lower frequency sinusoid. First, we analyze the optimum conditions for maximum harmonic generation in a uniform nonlinear line. Next, we extend the nonlinear line to a two-dimensional nonlinear lattice that is compatible with CMOS technology. Compared with the nonlinear line, the lattice relies on spatial power combining, higher cut-off frequency, and nonlinear wave interaction to enhance the pulse amplitude and sharpness. To show the feasibility of this method, we implement the first CMOS nonlinear lattice in a 0.13-μm CMOS process, and successfully demonstrate 2.7-$V_{\rm pp}$, 6.3-ps pulses from a 22-GHz input signal.**

***Index Terms*—CMOS, harmonic generation, nonlinearity, sharp pulse generation, transmission line, varactor.**

I. Introduction

RECENTLY, there has been growing interest in generating picosecond pulses for high-speed sampling, time-domain reflectometry, sensing and imaging, radar, and pulse-based wireless communication [1]–[5]. To generate a sharp pulse, a special form of nonlinear wave known as a soliton has been extensively studied in optics and electronics [6]–[12]. To implement an electrical nonlinear medium, a transmission line periodically loaded with voltage-dependent capacitors, e.g., Schottky diodes, was proposed in a GaAs technology in the early 1990s [11], [12]. Recently, a nonlinear transmission line in a CMOS technology has been proposed using accumulation-mode MOS varactors [13]. However, generating sharper pulses in CMOS is more challenging due to the high loss of passive components, lowering the effect of nonlinearity. For instance, the quality factor of varactors is less than 5 above 100 GHz in a typical CMOS technology.

To overcome this limit, the concept of the nonlinear transmission line has been extended to a two-dimensional nonlinear lattice to boost the harmonic generation resulting in higher-amplitude, narrower pulses [14]–[17]. Our prior work in [14] analyzed the optimum input frequency for the maximum harmonic generation based on numerical analysis, and the lattice was fabricated on a printed circuit board (PCB) for an input frequency of around 20 MHz. We also numerically analyzed a lossless nonlinear lattice based on a discrete model using a perturbative method [15], [16]. Although our recent work in [17] showed promising simulation results of the nonlinear lattice in a CMOS process, there are several implementation challenges that need to be addressed, including the selection of an output node without pulse distortion as well as input power distribution with high enough power level to fully exploit nonlinearity.

In this paper, by addressing the above issues, we implement an integrated nonlinear lattice in a standard 0.13-μm CMOS process to demonstrate 2.7-$V_{\rm pp}$, 6.3-ps pulses from a 22-GHz sinusoidal input. To the best of our knowledge, among the high-amplitude pulses (>1 V), this work shows the sharpest pulse in a CMOS process. This paper also has a significant theoretical extension towards the insightful understanding of a nonlinear lattice. First, we develop a continuous model of a nonlinear transmission line to obtain an analytical form of harmonic generation based on coupled wave equations in the presence of loss and dispersion. Based on this result, we analyze the limitation of a lossy nonlinear transmission line in a CMOS process and introduce a nonlinear lattice as an alternative. We show that the proposed structure exploits spatial power combining, higher cut-off frequency, and two-dimensional nonlinear interference to significantly enhance both the amplitude and pulse width, compared with a 1-D nonlinear transmission line.

The rest of the paper is organized as follows. Section II explains the theory of the harmonic generation in a nonlinear transmission line. Then, Section III proposes a two-dimensional nonlinear lattice as an extension of the transmission line and discusses its operation principle. Section IV presents the design, simulation results, and the implementation details. Section V presents the measurement results and Section VI concludes our work.

II. Distributed Harmonic Generation Theory

Fig. 1 shows a 1-D transmission line consisting of inductors l and voltage-dependant capacitors $c(V)$. As a sinusoid of frequency ω_0 travels along the line, the nonlinearity causes input energy at ω_0 to be transferred into multiple harmonics of the signal. This process results in sharpening the signal in the time domain, generating a narrow pulse. If the ratio of the energy of the higher-order harmonics to the total energy of the signal is larger, the resulting pulse becomes sharper. To describe the harmonic generation in a low-loss nonlinear transmission line,

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W. Lee, M. Adnan, and E. Afshari are with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14850 USA (email: wl287@cornell.edu).

O. Momeni is with the Department of Electrical and Computer Engineering, University of California, Davis, CA 95616 USA.

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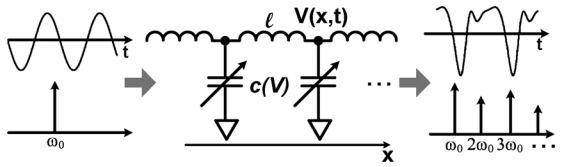

Fig. 1. Nonlinear transmission line for harmonic generation and pulse sharpening.

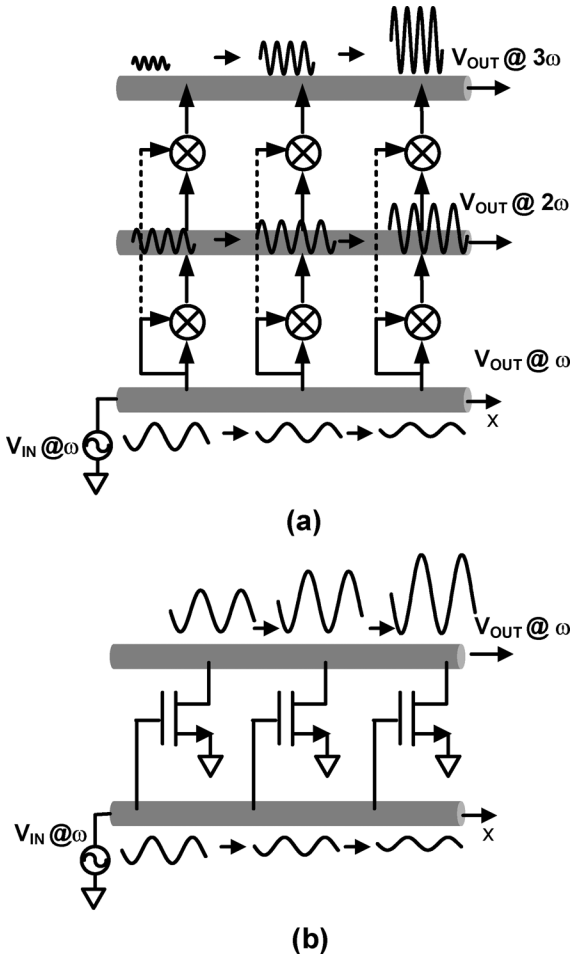

Fig. 2. (a) Distributed harmonic generation principle similar to (b) distributed amplification.

soliton propagation can be a useful model, which is reduced to the Burgers equation (zero-dispersion case) or the KdV equation (dispersion case) [8], [9]. However, the problem with this method is that it presents only the steady-state solution. In this paper, to capture the harmonic generation as the signal propagates along the transmission line, we use coupled-wave equations.

The basic principle of harmonic conversion along the nonlinear transmission line is illustrated in Fig. 2. We conceptually model a nonlinear transmission line as multiple coupled transmission lines, each for a different harmonic. The generated harmonic component at each section is constructively added on the upper lines during the propagation only if the fundamental and harmonic components are phase-matched. This is very similar to the principle of distributed amplification, in which phase matching between the two lines is necessary to achieve a gain that is proportional to the section number [20].

To analyze the harmonic generation on the nonlinear transmission line, we apply Kirchhoff's law at one section of the line and use approximated partial derivatives with respect to distance x from the beginning of the line, as shown in Fig. 1 [13]. This results in the wave equation for the voltage on the line $V(x,t)$ as

$$\frac{\partial^2 V}{\partial x^2} = L\frac{\partial}{\partial t}\left[C(V)\frac{\partial V}{\partial t}\right] + 2\sqrt{LC_0}\alpha\frac{\partial V}{\partial t} \tag{1}$$

where

$$\alpha = \frac{1}{2}\left(GZ_0 + \frac{R}{Z_0}\right) \tag{2}$$

and L, C, G and R are unit length inductance, capacitance, parasitic conductance, and parasitic resistance, respectively. Z_0 is the characteristic impedance for zero-biased varactors, which is $\sqrt{L/C_0}$. We also approximate the nonlinear capacitors with a first-order function $C(V) = C_0(1 + bV)$ where b is the slope of C/V characteristic. Next, we apply a sinusoidal signal at ω_0 to the left end of the transmission line and use the Fourier series to find the steady-state solution as

$$V(x,t) = \sum_{n=1}^{3}\left[V_n(x)e^{jn\omega_0 t} + V_n^*(x)e^{-jn\omega_0 t}\right] \tag{3}$$

where "*" represents complex conjugate and V_n is the voltage of the nth harmonic. In (3), for simplicity, it is assumed that the maximum generated harmonic component is the third. This assumption is valid if we introduce an ideal dispersion-less low-pass filter with the cut-off frequency around the fourth harmonic in each section of the line. In a real scenario, this filtering can be done by adjusting the Bragg frequency of the transmission line. However, this introduces dispersion into the line, which will be discussed in Section II-A.

Substituting (3) into (1), we obtain three traveling-wave equations for V_n's as

$$\frac{\partial^2 V_1}{\partial x^2} - \gamma_1^2 V_1 = -b\omega_0^2 LC_0[V_2 V_1^* + V_3 V_2^*] \tag{4a}$$

$$\frac{\partial^2 V_2}{\partial x^2} - \gamma_2^2 V_2 = -b\omega_0^2 LC_0\left[2V_1^2 + 4V_3 V_1^*\right] \tag{4b}$$

$$\frac{\partial^2 V_3}{\partial x^3} - \gamma_3^2 V_3 = -b\omega_0^2 LC_0[9V_1 V_2] \tag{4c}$$

where γ_n is the complex propagation constant for $n\omega_0$, given by

$$\gamma_n^2 = 2j\sqrt{LC_0}\alpha(n\omega_0) - (n\omega_0)^2 LC_0. \tag{5}$$

Equation (5) can be approximated as

$$\gamma_n = \sqrt{-\beta_n^2(1 - j2\alpha/\beta_n)} \simeq j\beta_n\left(1 - \frac{j}{2Q_n}\right) \tag{6}$$

where $\beta_n = n\omega_0\sqrt{LC_0}$ is the propagation constant for the nth harmonic in the absence of dispersion, and $Q_n = \beta_n/2\alpha \gg 1$ is the quality factor of the line for the nth harmonic. The propagation velocity for the nth harmonic is

$$v_{p,n} = \frac{n\omega_0}{\beta_n} = \frac{1}{\sqrt{LC_0}}. \tag{7}$$

Equation (7) shows that all harmonics are phase-matched, since the propagation velocity is the same for all frequencies due to the continuous line approximation. In other words, we have neglected the dispersion of the line due to discreteness, which will be discussed in the next section.

To solve (4), we use the perturbation theory and expand V_n in terms of b using coefficients V_{nm} up to the second order

$$V_n = \sum_{m=0}^{2} b^m V_{nm} = V_{n0} + bV_{n1} + b^2 V_{n2} \tag{8}$$

By substituting (8) into (4) and sorting by the powers of b.

For b^0

$$\frac{\partial V_{10}^2}{\partial x^2} - \gamma_1^2 V_{10} = 0. \tag{9}$$

For b^1

$$\frac{\partial V_{21}^2}{\partial x^2} - \gamma_2^2 V_{21} = -2\beta_1^2 V_{10}^2. \tag{10}$$

For b^2

$$\frac{\partial V_{32}^2}{\partial x^2} - \gamma_3^2 V_{32} = -9\beta_1^2 V_{10} V_{21} \tag{11}$$

where we applied boundary condition $V_2(x=0) = V_3(x=0) = 0$ which results in $V_{20}(x) = V_{22}(x) = V_{30}(x) = V_{31}(x) = 0$. From (9), we can obtain a traveling-wave solution given by

$$V_{10}(x) = V_{10}(0)e^{-\gamma_1 x} \tag{12}$$

and plug this into the equation for V_{21} in (10) to study the second-order harmonic generation:

$$\frac{\partial V_{21}^2}{\partial x^2} - \gamma_2^2 V_{21} = -2\beta_1^2 V_{10}^2(0) e^{-2\gamma_1 x} \tag{13}$$

which shows that the square of the voltage at the fundamental frequency is a forcing function for the wave equation of the second harmonic.

Using the boundary conditions $V_2(x=0) = V_2(x=\infty) = 0$ (beginning of the line and the effect of loss at infinity), the solution of (13) is calculated as

$$V_{21}(x) = -\frac{2\beta_1^2 V_{10}^2(0)}{2\gamma_1 + \gamma_2}\left[\frac{e^{-(2\gamma_1-\gamma_2)x} - 1}{2\gamma_1 - \gamma_2}\right] e^{-\gamma_2 x}. \tag{14}$$

Based on (6), (14) can be simplified to

$$|V_{21}(x)| = \frac{\beta_1 V_{10}^2(0)}{2} x e^{-\alpha_2 x}. \tag{15}$$

Equation (15) shows that the coherent addition at each section results in a linear increase of the second harmonic component with respect to distance x, while the transmission line loss causes an exponential decay. The maximum amplitude of the second harmonic is

$$V_2|_{\max} = b|V_{21}(x_{\text{opt}})| = \frac{bQ_2}{2e} V_{10}^2(0) \tag{16}$$

where $x_{\text{opt}} = 1/\alpha_2$ is the length of transmission line that maximizes the second harmonic. We can also calculate the equivalent optimum phase shift as $\phi_{2,\text{opt}} = \beta_2 x_{\text{opt}} = 2Q_2$, which is a function only of the line quality factor.

Similarly, we calculate the third order harmonics from (11). It is interesting that the forcing function is the mixing term between V_{10} and V_{21}, which shows that cascading second-order nonlinearity generates the third-order harmonics without a third-order nonlinear medium. By inserting (12) and (14) into (11) with the boundary condition $V_3(x=0) = V_3(x=\infty) = 0$, we have

$$|V_{32}(x)| = \frac{3\beta_1^2 V_{10}^3(0)}{8} x^2 e^{-\alpha_3 x}. \tag{17}$$

This result shows that the third-order harmonics are proportional to x^2. When $x = x_{\text{opt}} = 2/\alpha_3$ or the propagation phase shift is $\phi_{3,\text{opt}} = \beta_3 x_{\text{opt}} = 4Q_3$, (17) has its maximum of

$$V_3|_{\max} = b^2|V_{32}(x_{\text{opt}})| = -\frac{2(bQ_3)^2 V_{10}^3(0)}{3e^2}. \tag{18}$$

Equation (18) shows greater dependence on the nonlinearity, loss, and input amplitude, compared with the second harmonic generation in (16).

A. The Effect of Dispersion

So far, we have approximated the line with a continuous line and neglected the effect of dispersion that arises from the discreteness of the line. However, in a real transmission line with lumped varactors, the dispersion changes phase velocity with respect to frequency, especially close to the cut-off frequency. In the presence of the dispersion, (14) for the second harmonic becomes

$$V_{21}(x) = -\frac{\beta_1 V_{10}^2(0)}{2} e^{-j\Delta\beta_2 x/2} \text{sinc}(\Delta\beta_2 x/2) x e^{-\gamma_2 x} \tag{19}$$

where $2\gamma_1 - \gamma_2$ is approximated as $j\Delta\beta_2 = j(2\beta_1 - \beta_2)$ using (6). Here, $\beta_2 \neq 2\beta_1$ due to the phase mismatch caused by dispersion. Equation (19) is proportional to the sinc function of the accumulated phase mismatch $\Delta\beta_2 \cdot x$. When $\Delta\beta_2 \cdot x$ increases, the sinc function decreases from unity, decreasing the amplitude of the second harmonic. If $\Delta\beta_2 \cdot x = 2\pi$, the amplitude of the second harmonic becomes zero. The dispersion degrades the third harmonic generation even more severely since the third harmonic is closer to the cut-off frequency.

B. Simulation Results

Fig. 3 shows the Cadence simulation of harmonic generation on the nonlinear transmission line, compared with our analysis in the presence of dispersion. The simulations are performed using a standard 0.13-μm CMOS process. Accumulation-mode MOS varactors and ground-shielded coplanar waveguides are used as varactors and inductors, respectively. For the input frequency of 25 GHz, the line is designed to have a cut-off frequency of 80 GHz to suppress any harmonics that are higher than the third one. In this simulation, the characteristic impedance of the line is around 20 Ω and the input power at 25 GHz is 3.5 dBm.

As shown in Fig. 3, the optimum length of the transmission line for maximum harmonic generation is only around 6 sections. Furthermore, the best conversion losses at the second

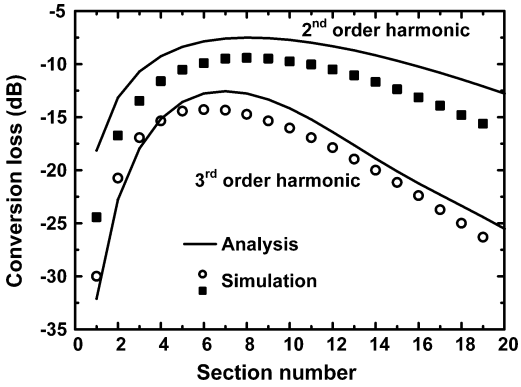

Fig. 3. Simulated 2nd and 3rd harmonic generation on the nonlinear transmission line in comparison with the analysis.

and third harmonics are higher than 10 dB. This is because of two major challenges. First, since the quality factor of the CMOS nonlinear transmission line is low, the optimum length is short according to (16) and (18). In other words, before enough harmonic power is generated, the effect of loss becomes dominant. The second challenge is dispersion that degrades the harmonic generation due to the phase mismatch. As we can see from Fig. 3, the loss and phase mismatch have greater influence on the third harmonic, as it is closer to the cut-off frequency. This example demonstrates that the high loss and phase mismatch of the nonlinear transmission line in CMOS lowers the efficiency of the harmonic conversion. This limits the minimum pulse width and amplitude that can be generated using this structure.

III. Nonlinear Lattice for Sharp Pulse Generation

For a given quality factor, input amplitude, and varactor nonlinearity, we can significantly increase harmonic generation by extending a nonlinear transmission line to a 2-D nonlinear lattice as shown in Fig. 4. A series of in-phase sinusoidal sources are applied to the left and bottom of the lattice, generating two incident perpendicular plane waves. The top and right boundaries are terminated with matched resistors. These two waves interact diagonally to produce high-amplitude, sharp pulses at the center of the lattice. The lattice improves the harmonic generation by three mechanisms: 1) spatial power combining; 2) higher cut-off frequency; and 3) nonlinear constructive interference to generate more harmonics from each traveling wave. Next, we discuss these three effects that result in sharper and higher-amplitude pulses.

Fig. 5 shows the simulated voltage amplitude of different points of the lattice as a plane wave propagates from the left to the right in a 12×12 lattice. The input amplitude is 1 $V_{\rm pp}$ at 20 GHz, and the inductors and capacitors are 80 pH and 200 fF, respectively. The propagation of the plane wave in the lattice is similar to wave propagation in a transmission line. However, the simulation results show that the plane wave has the maximum amplitude of 1.5 $V_{\rm pp}$ after six sections, which is 25-% larger than the maximum amplitude in a nonlinear transmission line with the same component values.

a) Spatial Power Combining: This voltage increase is partly due to the spatial combining mechanism inside the

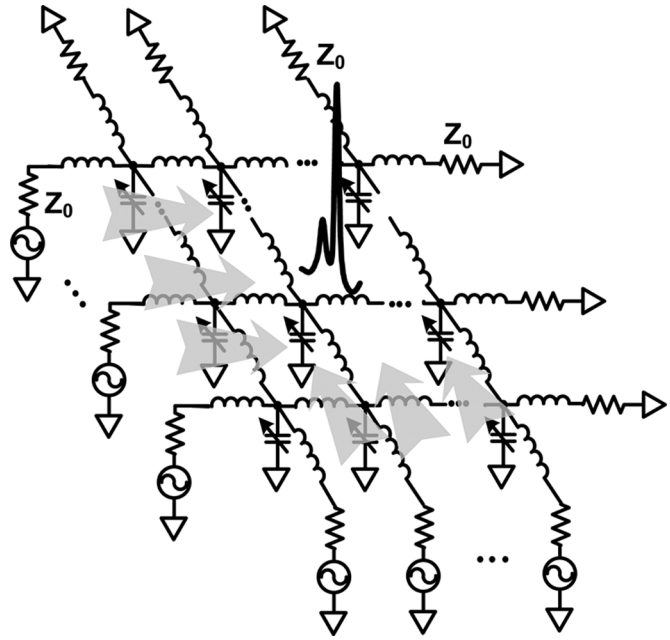

Fig. 4. Proposed nonlinear LC lattice as a two-dimensional extension of a nonlinear transmission line.

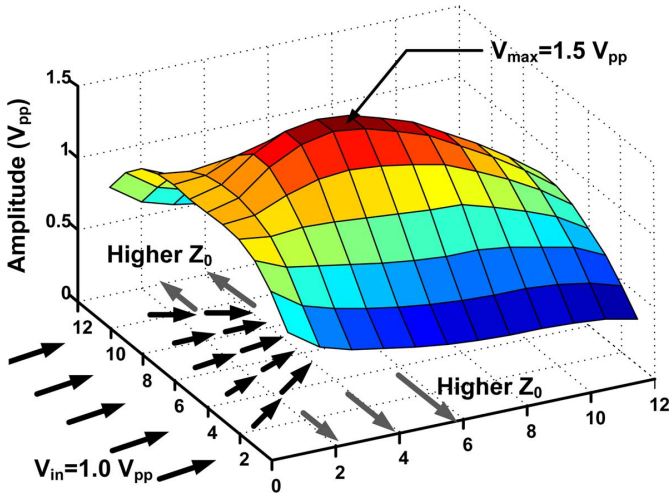

Fig. 5. Simulated voltage amplitude of different points of a 12 × 12 nonlinear lattice driven by a plane wave propagating from the left to the right. The top, bottom, and right boundaries are terminated with matched loads.

lattice. In the previous simulation in Fig. 5, since the top and bottom boundaries are terminated with matched resistors, the effective shunt impedance of the lattice closer to its boundaries is lower. As shown in Fig. 5, this results in higher characteristic impedance at the top and bottom, which pushes some of the signal to the center of the lattice where the characteristic impedance is relatively lower.

b) Higher Cut-Off Frequency: In addition, the lower characteristic impedance at the center of the lattice creates some diagonal wave component. For a plane wave that propagates diagonally, the cut-off frequency of the lattice is

$$\omega_{c,\rm diagonal} = \frac{2\sqrt{2}}{\sqrt{LC}} \tag{20}$$

which is higher than the cut-off frequency of the transmission line with the same L and C by a factor of $\sqrt{2}$ [21]. This higher

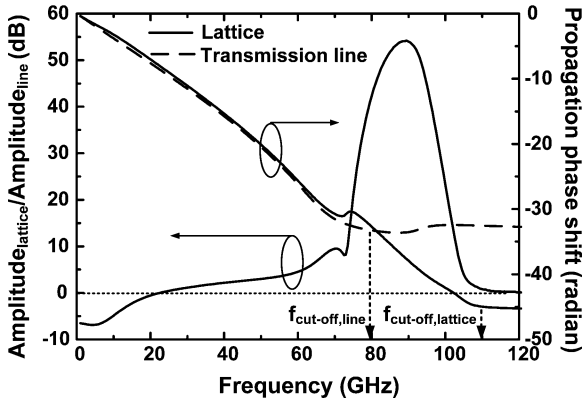

Fig. 6. Simulated amplitude and phase response of the lattice compared with the line.

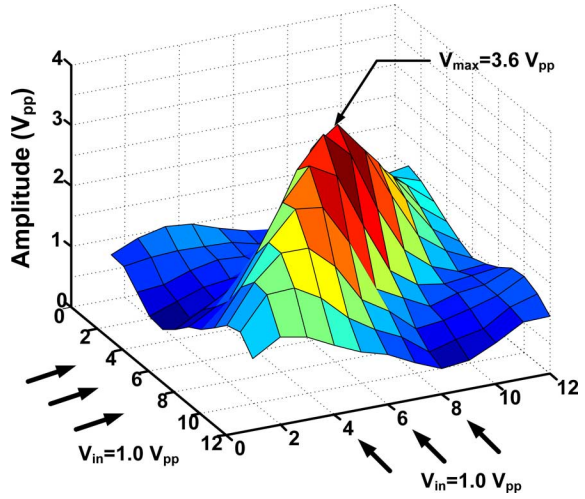

Fig. 7. Nonlinear constructive interference in a 12 × 12 nonlinear lattice.

cut-off frequency improves the phase matching and loss for higher frequency components.

To summarize these two effects, Fig. 6 shows the small-signal response of the lattice and a transmission line with the same values of L and C. The amplitude and propagation phase shift are simulated at the middle node when the input is applied only to the left. As shown in Fig. 6, the signal amplitude in the lattice is higher than the transmission line for frequencies higher than 20 GHz due to the power-combining effect. After 70 GHz, the lattice shows significantly larger voltage amplitude due to its higher cut-off frequency. This higher cut-off frequency also results in better phase matching in the lattice at above 70 GHz.

c) Nonlinear Constructive Interference: Next, we add the second plane wave to the bottom of the lattice as shown in Fig. 7. The two waves interact nonlinearly, which means that the amplitude of the generated pulse is greater than the sum of two incoming waves despite its passive structure. This is because the nonlinear interaction focuses the energy both in time and space, resulting in higher localized power. This phenomenon has been observed in plasma and fluid mechanics [22] and more recently in the simulation of the discrete LC lattices [15]. Fig. 7 shows the maximum amplitude of 3.6 $V_{\rm pp}$, which is more than twice of the maximum amplitude of each plane wave.

To compare the lattice performance to a nonlinear transmission line, we simulate both structures with different cut-off frequencies for a given propagation phase shift (i.e., the same effective electrical length) as shown in Fig. 8. The input frequency and amplitude are set at 20 GHz and 500 mV, respectively. The input source impedance and termination resistance are matched to the characteristic impedance. Figs. 8(a) and (b) show the spectrum of the output normalized to the amplitude of the input frequency for the transmission line and the lattice, respectively. As shown here, the lattice has significantly higher harmonic components due to the spatial combining, better phase matching, and nonlinear wave interaction. Fig. 8(c) and (d) shows the output waveforms of the transmission line and the lattice, respectively. The lattice has higher amplitude at all harmonics that results in a much sharper pulse with higher amplitude. The output amplitude of the lattice is around four times higher than that of the transmission line. Finally, since the lattice output has more high frequency components, it approaches a single pulse.

IV. Lattice Design in CMOS

In this section, we overview the design of a nonlinear lattice in a standard 0.13-μm CMOS technology.

A. Passive Elements

Accumulation-mode MOS varactors are employed as voltage-dependent capacitors that generate nonlinearity in the lattice. The nonlinearity is determined by $C_{\rm max}/C_{\rm min}$ and the slope of the capacitance-voltage curve. As shown in Fig. 9, the varactor capacitance is a series combination of $C_{\rm ox}$ and $C_{\rm var}$, where $C_{\rm ox}$ is oxide capacitance and $C_{\rm var}$ is depletion capacitance under the gate oxide changing with the bias voltage. In parallel with $C_{\rm ox}$ and $C_{\rm var}$, parasitic capacitances exist due to fringing fields and poly and drain/source overlap, degrading the capacitance nonlinearity. Hence, the channel length $L_{\rm ch}$ and width $W_{\rm ch}$ should be sufficient to minimize the portion of parasitics to the total capacitance. On the other hand, the varactors are the dominant source of loss in the lattice for frequencies higher than 50 GHz, and hence their quality factor needs to be maximized.

Fig. 10 shows the simulated varactor capacitance as well as its quality factor as a function of the bias voltage for different channel lengths. In this simulation, the signal frequency is 20 GHz, and the capacitance at zero bias (C_0) is kept constant. When $L_{\rm ch}$ increases, $C_{\rm max}/C_{\rm min}$ increases due to the lower portion of parasitics. However, the increase in $L_{\rm ch}$ also decreases the quality factor since the bias-dependent channel resistance $R_{\rm ch}$ is proportional to $L_{\rm ch}$, as illustrated in Fig. 9. From the simulation, we found that the optimum channel width and length are 1.5 μm and 0.3 μm, respectively. These values result in nonlinearity of $b \simeq 2{\rm V}^{-1}$ and a quality factor of $\sim$10 at 50 GHz.

The lattice inductors are implemented using a coplanar waveguide with ground shielding [26]. The signal and ground lines are on the top metal layer (a 4-μm aluminum layer), and the ground shield is made of the bottom metal. The individual inductors as well as their coupling are simulated using an E/M simulator, SONNET. Fig. 11 shows the simulated quality

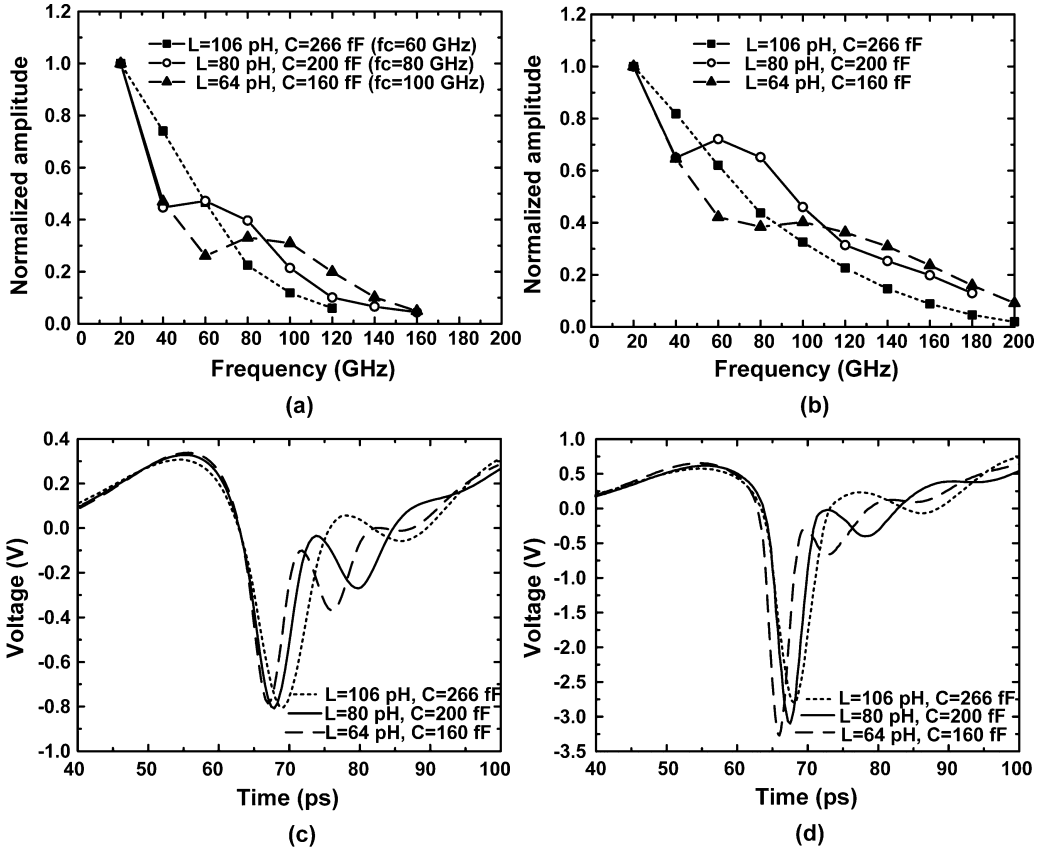

Fig. 8. Simulated output spectrum for: (a) the transmission line and (b) the lattice, and time-domain response for: (c) the transmission line and (d) the lattice.

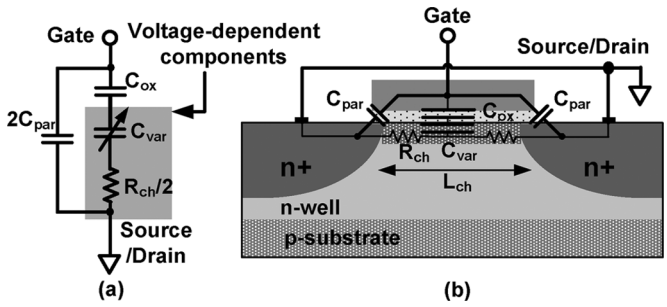

Fig. 9. (a) A simple model of an accumulation-mode NMOS varactor and (b) its physical structure.

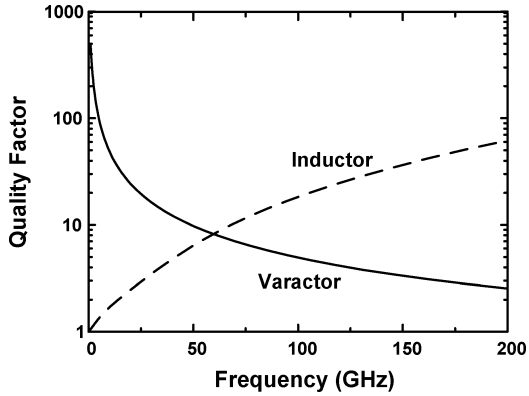

Fig. 11. Quality factor of the employed inductor and varactor versus frequency.

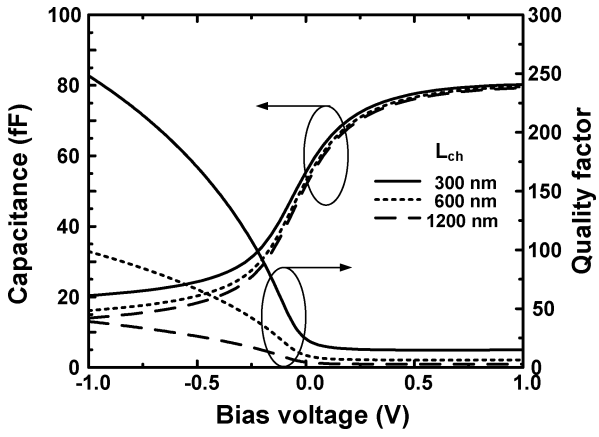

Fig. 10. Varactor capacitance and quality factor vs. bias voltage.

factors of stand-alone inductors and varactors for a range of frequencies.

B. Optimization and Simulation

The design parameters of the lattice are the cut-off frequency, the size, and the characteristic impedance. For a given input frequency of 20 GHz, the cut-off frequency of 110 GHz is selected from Fig. 8, considering the trade-off among the pulse width, the amplitude, and the side peak. Then, to determine the optimum size, we simulate the lattice for different sizes as shown in Fig. 12. As the lattice size increases, the signal travels longer, resulting in higher harmonic generation. On the other hand, for lattices larger than 16×16, the loss becomes dominant, and the

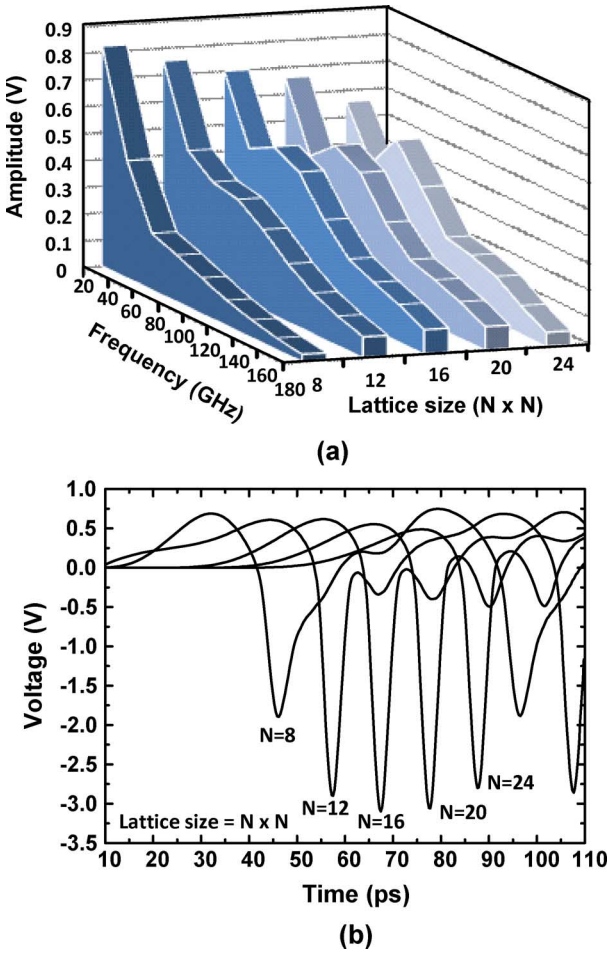

Fig. 12. Lattice size optimization in: (a) a frequency spectrum and (b) a time domain.

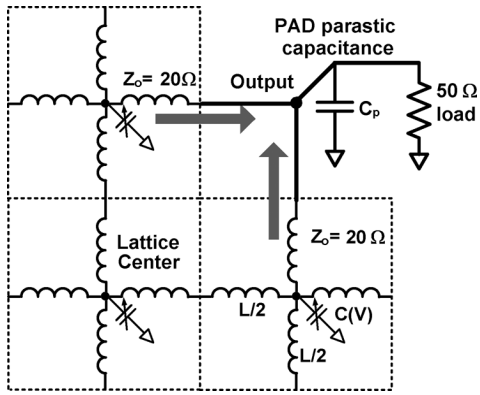

Fig. 13. Output is connected to two symmetric adjacent nodes to the center of the lattice to minimize the output loading.

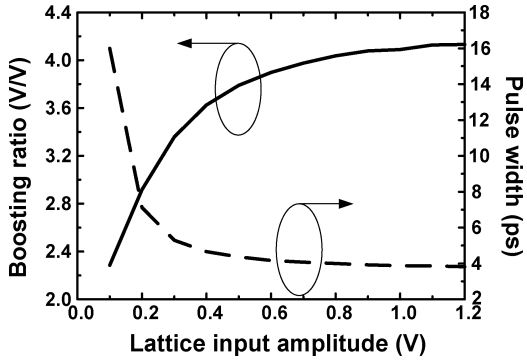

Fig. 14. Simulated boosting ratio and pulse width versus input amplitude for the 16×16 lattice.

harmonic generation is degraded, as discussed in Section II. Consequently, we select a 16×16 lattice for this design.

To determine the optimum characteristic impedance of the lattice, we observe that the output pulse is a result of interference between the two plane waves and is not a traveling wave. This means that ideally the load impedance at the center of the lattice should be much higher than the characteristic impedance to avoid the disturbance of the flow of two incoming waves. For values of inductors and capacitors that are integrable in CMOS, our simulation shows that the output pulse is narrower than 5 ps if the characteristic impedance is lower than 10 Ω for a 50-Ω load. This low characteristic impedance requires higher input power for a fixed input voltage amplitude to the lattice. To alleviate this effect, two nodes of the lattice are connected to the output instead of the center of the lattice, as shown in Fig. 13. Since these two symmetric points have the same voltage, the effective output load for each one of them is 100 Ω. This means that the characteristic impedance of the lattice can be increased to 20 Ω. This output configuration also halves the effective output parasitic capacitance C_p, which reduces the loading effect of the output pad. To easily probe the output and to reduce the chip area, the upper left quarter of the lattice is cut off, as shown in Fig. 17. With proper termination, this has no significant effect on the lattice performance.

Fig. 14 shows the simulated boosting ratio and the pulse width with respect to the input amplitude for the designed 16×16 lattice and a 20-GHz input signal. The amplitude of the steady-state output signal nonlinearly depends on the amplitude of the input signal. We characterize this effect using the boosting ratio, defined as the ratio of output amplitude to input amplitude. As shown in Fig. 14, the higher input amplitude boosts the harmonic generation, resulting in higher boosting ratio and narrower pulse width. However, as the input amplitude becomes larger than ∼0.5 V, the boosting ratio and the pulse width saturate to 4.1 V/V and 3.8 ps, respectively. This saturation occurs due to the varactor saturation, as shown in Fig. 10.

C. Distribution Network

Fig. 15 shows the power divider that distributes input power into 32 ports in the left and bottom boundaries of the 16×16 lattice. The input impedance of 50 Ω is also transformed to 20 Ω, which is the characteristic impedance of the lattice. The power divider has a tree structure that consists of different L-matches at each division point. The impedance transformation ratios of all L-matches are not higher than three for the broad bandwidth. The input pad capacitance and the inductance of transmission lines of the distribution network are absorbed into the matching network. Transmission lines are implemented with a coplanar

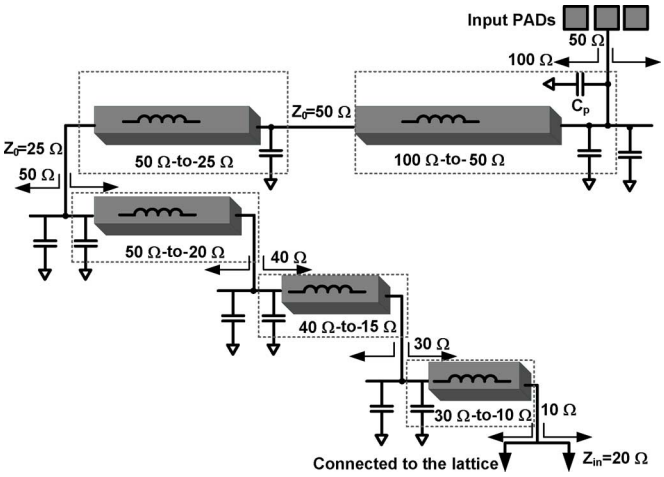

Fig. 15. Distribution network from input to the lattice.

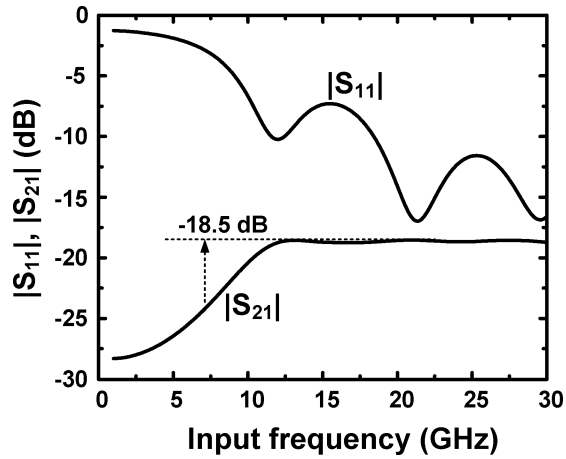

Fig. 16. Simulated S-parameter of the distribution network.

waveguide to minimize the loss for a given inductance. The vertical natural capacitors (VNCAPs) are used as the matching capacitors [29]. Fig. 16 shows the simulated S-parameter of the designed power divider when the output ports are connected to 20-Ω terminations. The $|S_{21}|$ is around -18.5 dB at around 20 GHz. Since the ideal loss for 32 divisions is $-20\log(32) = -15$ dB, each L-match has an insertion loss of around 0.5 dB, considering that the signal passes through seven L-match networks. The power divider also has $|S_{11}|$ of below -10 dB at around 20 GHz.

V. Measurement

A 15×15 lattice is fabricated in a standard 0.13-μm CMOS technology as shown in Fig. 17. The size of the chip is 3 mm×3 mm, including the distribution network and the lattice. As mentioned, to probe the center of the lattice, the upper left quarter of the lattice is cut off.

Fig. 18 shows the experimental setup to measure the output waveform of the lattice. An external power amplifier, which has a 1-dB compression point of 34 dBm, is placed after the signal source to provide enough power into the distribution network. The input power level is controlled using the signal generator. Both input and output are connected using GSG probes. The output signal is attenuated and connected to an 80-GHz sampling oscilloscope. The loss of cables, connectors, and the attenuator is measured by a broadband signal generator, a spectrum analyzer, and the oscilloscope. The response of the oscilloscope is estimated from its user manual, which is based on the measurement by a wideband power meter [33]. The total loss of the output measurement setup including the oscilloscope is shown in Fig. 19. Since this loss is due mainly to the skin effect and limited bandwidth, we model the transfer function of the test setup as

$$H(j\omega) = 10^{-A/20} e^{-\alpha\sqrt{\omega}}/(1 + j\omega/\omega_B) \qquad (21)$$

where ω_B is the bandwidth of the system, and α is a parameter that represents the loss of the cable, connectors, and pads. "A"

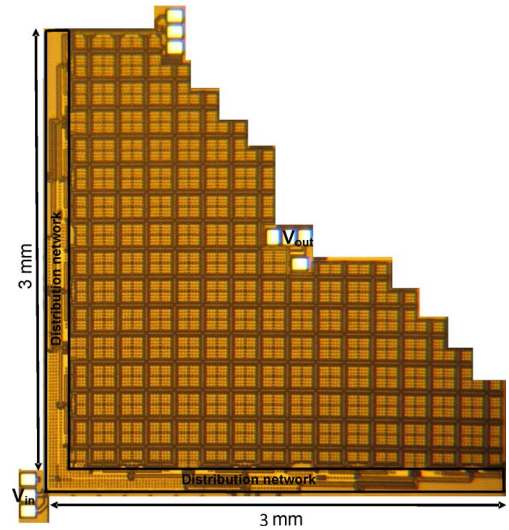

Fig. 17. Die photograph of the chip.

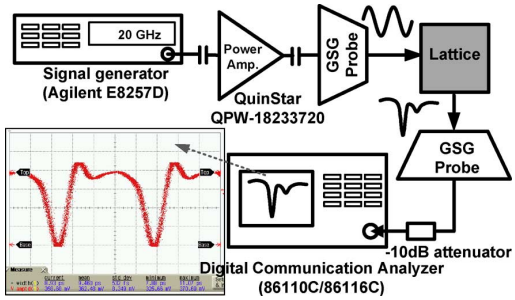

Fig. 18. Experimental setup.

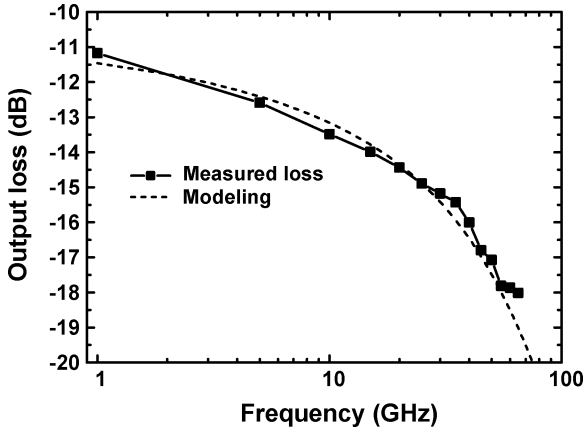

Fig. 19. Measured loss of the output test setup and its model.

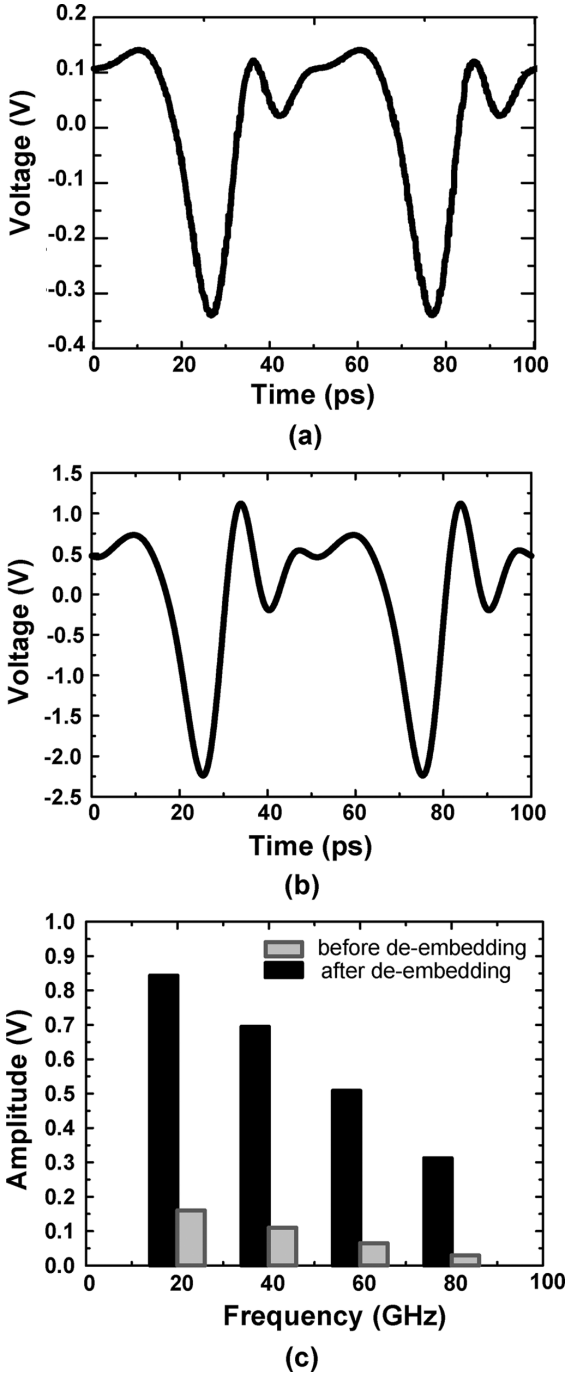

Fig. 20. Measured output waveforms (a) before and (b) after de-embedding the loss of the measurement setup and (c) their frequency spectrum.

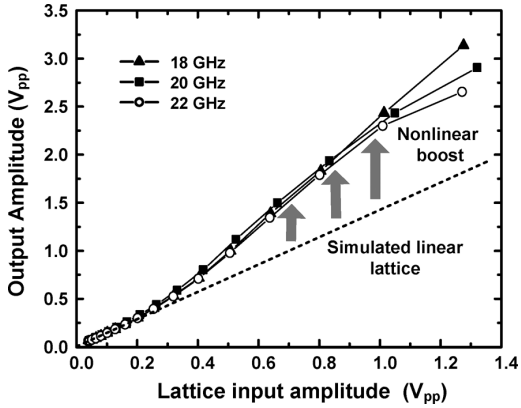

Fig. 21. Measured output amplitude versus input amplitude for different frequencies.

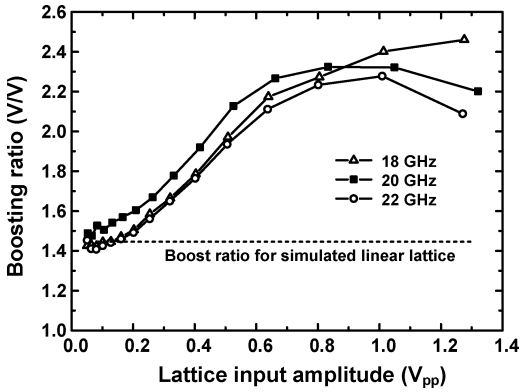

Fig. 22. Measured boosting ratio versus input amplitude for different frequencies.

is a frequency-independent attenuation that mainly results from the 10-dB attenuator in Fig. 18. To fit the measured loss with $|H(j\omega)|$, A and α are estimated to be 10.6 dB and 1.1×10^{-7}, respectively. Due to the limited bandwidth of the measurement setup, capturing the output pulse without distortion is very challenging. In simulation, the lattice output pulse has a significant power even at the 9th harmonic frequency around 180 GHz. For a conservative estimation of the output pulse amplitude, we first perform the Fourier analysis of directly measured waveform from the oscilloscope, and neglect the harmonic components beyond the electrical bandwidth of the oscilloscope. Then, output loss measured in Fig. 19 is compensated at each harmonic frequency in terms of magnitude and phase. Finally, we perform the inverse Fourier transform to recover the waveform in the time domain.

When a 20-GHz sinusoid is applied into the lattice and its amplitude at the lattice input is around 1.3 $V_{\rm pp}$, the measured output waveforms are shown in Fig. 20(a) and (b), before and after de-embedding the loss of the measurement setup, respectively. The lattice input amplitude is calculated from the input power and the simulated loss of the distribution network. Fig. 20(c) shows the measured frequency spectrum of the output pulse.

Next, we change both input frequency and amplitude, and measure the amplitude of the output pulse as shown in Fig. 21. For comparison, we also simulate the same lattice with linear capacitors. Since the nonlinearity is a function of signal amplitude, the output amplitude increases nonlinearly with the input amplitude. To quantify this nonlinear behavior, the boosting ratio, i.e., the ratio of output and input amplitudes, is also measured, as shown in Fig. 22. When the input amplitude is low and harmonic generation rarely occurs, the nonlinear lattice behaves much like the simulated linear lattice with the boosting ratio of 1.4 V/V. However, as the input amplitude increases, the boosting ratio increases up to 2.3 V/V. The increase in the boost ratio is saturated at an input amplitude of around 0.9 $V_{\rm pp}$ to 1 $V_{\rm pp}$ since the varactors saturate, as shown in Fig. 10. Another reason for this saturation is the bandwidth limitation of the test setup shown in

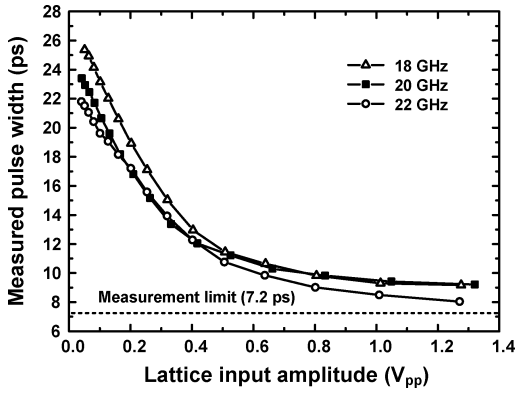

Fig. 23. Measured pulse width suppression versus input amplitude for different frequencies.

TABLE I
COMPARISON WITH PRIOR ART

	Pulse width (ps)	Duty cycle (%)	Amplitude (V_{pp})	Technology	Type
[12]	5.5	4.4	3.9	GaAs	Transmission line
[13]	23	21	0.95	0.18-μm BiCMOS	Transmission line
[18]	293	33	1.5	0.18-μm CMOS	Oscillator
[19]	16	30	0.5	GaAs	Oscillator
This work	**9.6 (6.3*)**	**21 (14*)**	**2.7**	**0.13-μm CMOS**	**Lattice**

Pulse width and duty cycle are measured directly from sampling-circuit or oscilloscope without de-embedding the bandwidth of the measurement setup.
* is the estimated value after de-embedding.

Fig. 19. As the input amplitude increases, the generated signal has a higher portion of its energy above the cut-off frequency of the measurement setup.

The pulse width is also measured in Fig. 23. As the input amplitude increases, the measured pulse width is reduced to 8 ps for an input frequency of 22 GHz. To investigate the minimum pulse width that can be measured with our experimental setup, the 10%–90% rise time is calculated based on the loss equation in (21). The calculated rise time is 7.2 ps, and, under the assumption that the waveform is symmetric, the minimum pulse width that can be measured in our setup is also around 7.2 ps. The actual pulse width can be estimated from the measured pulse width and the bandwidth of the setup as [34]

$$t_{\text{meas}} = \sqrt{t_{\text{pulse}}^2 + t_{\text{system}}^2} \tag{22}$$

where $t_{\text{meas}} = 9.6$ ps is the minimum measured pulse width before de-embedding the loss, $t_{\text{system}} = 7.2$ ps is the response of the measurement system to an ideal impulse, and t_{pulse} is the actual pulse width. Based on the measured results and (22), the actual pulse width is around 6.3 ps. To the best of our knowledge, this is the sharpest pulse with amplitude higher than 1 V in a CMOS process, as depicted in Table I.

VI. CONCLUSION

In this paper, we have demonstrated the generation of very narrow and high-amplitude pulses using a nonlinear 2-D lattice in a lossy CMOS process. This has been accomplished by exploiting the constructive interference of two plane waves traveling perpendicular to each other in an optimally-designed nonlinear medium. Despite its large chip area, the nonlinear lattice enables picosecond pulse generation in a standard CMOS process, opening a new door to several new applications, such as millimeter-wave imaging, spectroscopy, and ultra-wideband systems.

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Wooram Lee received the B.Sc. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Seoul, Korea, in 2001 and 2003, respectively, and is currently working towards the Ph.D. degree at Cornell University, Ithaca, NY.

He has held a summer internship at the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he worked on a millimeter-wave frequency multiplier in a 90-nm SiGe process. Before joining Cornell University, he was a research engineer at the Electronics and Telecommunications Research Institute (ETRI), Korea, where he worked on optical transceivers and links from 2003 to 2007. His research interests include high performance RF IC design exploiting nonlinear electronics for low noise amplification and oscillation.

Mr. Lee received the IEEE Solid-State Circuits Society Pre-Doctoral Fellowship for 2010–2011 and the Samsung Graduate Fellowship for 2007–2012. He was a recipient of the Best Paper Award of the IEEE Radar Conference in 2009, and the Silver Medal at the National Physics Competition in 1996.

Muhammad Adnan received the B.E. degree in electrical and computer engineering from National University of Sciences and Technology, Pakistan, in 2005. He was recipient of the President Gold medal and Rector Gold medal for his B.E. degree. He is currently working toward the Ph.D. degree in the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY.

Before joining Cornell University, he was a hardware design engineer at the Center for Advanced Research in Engineering (CARE), Pakistan. His current research is focused on developing different linear and nonlinear techniques to address fundamental challenges in mm-wave and radio-frequency circuit design.

Omeed Momeni received the B.Sc. degree from Isfahan University of Technology, Isfahan, Iran, the M.S. degree from University of Southern California, Los Angeles, and the Ph.D. degree from Cornell University, Ithaca, NY, in 2002, 2006, and 2011, respectively, all in electrical engineering.

He joined the faculty of Electrical and Computer Engineering Department at University of California, Davis, in 2011. He is currently a visiting professor in Electrical Engineering and Computer Science Department at University of California, Irvine. From 2004 to 2006, he was with the National Aeronautics and Space Administration (NASA), Jet Propulsion Laboratory (JPL), Pasadena, CA, to design L-band transceivers for synthetic aperture radars (SAR) and high power amplifiers for Mass Spectrometer applications. His research interests include mm-wave and terahertz integrated circuits and systems.

Prof. Momeni is the recipient of the Best Ph.D. Thesis Award from the Cornell ECE Department in 2011, the Outstanding Graduate Award from Association of Professors and Scholars of Iranian Heritage (APSIH) in 2011, the Best Student Paper Award at the IEEE Workshop on Microwave Passive Circuits and Filters in 2010, the Cornell University Jacob's fellowship in 2007 and the NASA-JPL fellowship in 2003.

Ehsan Afshari was born in 1979. He received the B.Sc. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran and the M.S. and Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2003, and 2006, respectively.

Since August 2006, he has been a member of the faculty in Electrical and Computer Engineering at Cornell University, Ithaca, NY. His research interests are mm-wave and terahertz electronics and low-noise integrated circuits for applications in communication systems, sensing, and biomedical devices.

Prof. Afshari serves as the chair of the IEEE Ithaca section, as the chair of Cornell Highly Integrated Physical Systems (CHIPS), as a member of International Technical Committee of the IEEE Solid-State Circuit Conference (ISSCC), as a member of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society, as a member of the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC), and as a member of Technical Program Committee of the IEEE International Conference on Ultra-Wideband (ICUWB). He was awarded National Science Foundation CAREER award in 2010, Cornell College of Engineering Michael Tien excellence in teaching award in 2010, Defense Advanced Research Projects Agency (DARPA) Young Faculty Award in 2008, and Iran's Best Engineering Student award by the President of Iran in 2001. He is also the recipient of the best paper award in the Custom Integrated Circuits Conference (CICC), September 2003, the first place at Stanford-Berkeley-Caltech Inventors Challenge, March 2005, the best undergraduate paper award in Iranian Conference on Electrical Engineering, 1999, the recipient of the Silver Medal in the Physics Olympiad in 1997, and the recipient of the Award of Excellence in Engineering Education from Association of Professors and Scholars of Iranian Heritage (APSIH), May 2004.