Varactor Loaded Transmission Lines for Phase Shifting T/M Applications

Capstone Final Report

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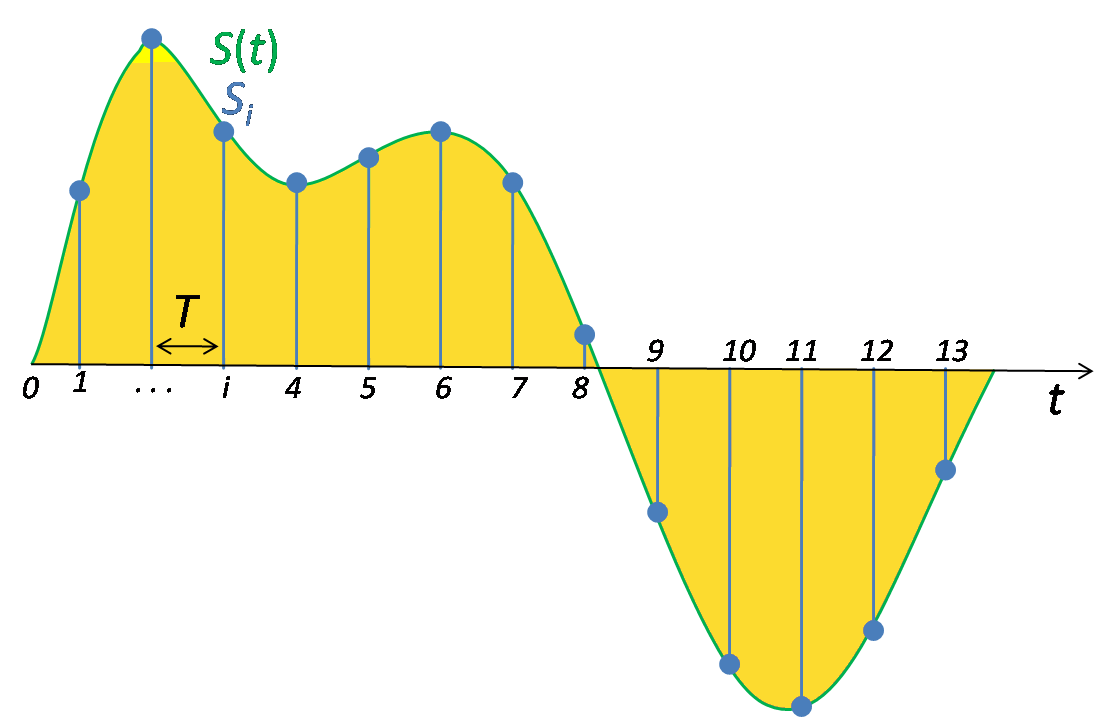
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## Executive Summary

The goal of this project is to explore the possible applications of varactor diodes. We are interested in their usefulness when building Nonlinear Transmission Lines used for “pulse sharpening”. Going forward, the term NLTL is used for brevity. Among other things, NLTL’s are used in measurement equipment to increase and improve our ability to sample electrical signals. This sampling is the process extracting information from a given signal, normally a varying voltage. To do this, we must send in a known voltage signal with which to compare the unknown signal against.

Fourier analysis is the theory which tells us how often we must send in this comparison signal. In order to fully capture the behavior of a waveform. Figure 1 below shows an example of how we can reconstruct a waveform using sampled values achieved by comparison to a train of narrow “pulses”.



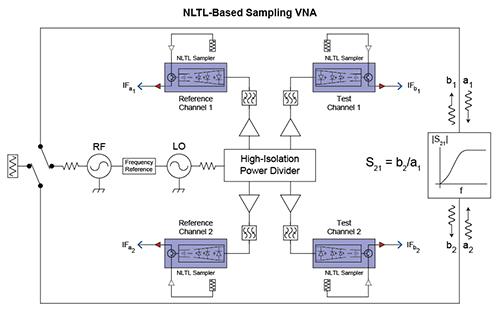
*Figure 1: Basic signal sampling by use of a train of comparison pulses. Image taken from* [*http://en.wikipedia.org/wiki/File:Signal\_Sampling.png*](http://en.wikipedia.org/wiki/File:Signal_Sampling.png) *, Public Domain*

While there are many different documented uses and construction strategies, the scope of this project has narrowed to the construction of circuit blocks to speed up these waveforms using discrete circuit components. This includes research, software simulation, PCB (printed-circuit board) construction of the NLTL block, and the drafting of a “white-paper” document for use by our project sponsors.

## Problem Background

The usefulness of this work is to build a foundation for further prototyping and modeling of high bandwidth NLTL’s to be used at our sponsors discretion. Among many things, Rohde and Schwarz is a company which specializes in the designing and building of high-speed test equipment for use in everything from automobiles, radios, wireless networks and everything in between. Fully utilizing NLTL’s to continue innovation and increase the range of frequencies we can practically measure is of great use and is becoming more important as circuits get smaller and circuits operate at faster speeds.

This technology can be expanded significantly, and already finds use in current technology such as shown in Figure 2. Anritsu has not only leveraged NLTL’s but has further used the physical structure of the transmission line to improve desirable characteristics. Using geometry in this way creates what are called “Non-Uniform NLTL’s” and also of interest to our sponsors.



*Figure 2: Example use of NLTL's in current technology.*

*taken from* [*https://www.anritsu.com/en-GB/test-measurement/technologies/shockline-nltl*](https://www.anritsu.com/en-GB/test-measurement/technologies/shockline-nltl)

## Objective Statement

As discussed, the main goal of this particular project was to look more closely at the practicality of NLTL’s and to lay a proper foundation for further experimentation for our sponsors. As an end to that goal, we were tasked with documenting this research and preliminary testing in an accompanying white paper. To do this, we simulate and construct a small prototype with 10 sections of a certain device pattern. What these sections look like in practice are discussed in the implementation section of this document. For now, we can just say that our prototype NLTL block is made up of 10 repeating component patterns connected in a chain.

The PCB is tested, and these measurements compared to simulation run using circuit simulator tools with SPICE models. The goal of which is to capture the behavior we see in the physical circuit in a repeatable simulation environment. This is important as the scope of the project widens and more applications explored.

## Deliverables

A successful capstone project involves delivering the following items. While some physical prototypes are included in this list, they are used mainly in the generation of the documentation requested by Rohde and Schwarz. As a part of the white paper document, we are requested to compile a list of the relevant research.

* Project Proposal Presentation to Sponsor
* Weekly Progress Reports to Faculty Advisor
* (Qty 3) PCB’s of 10-ladder long 144MHz Varactor Loaded Tx Line. With ports to allow for S-parameter De-embedding.
* Detailed and complete documentation for research, modeling data and Simulation results.
  + In form of “white-paper” design guide
* Bill of Materials for Modeled Design and board materials
* Rough Draft of Design guide submitted for sponsor revision. Final Report
* Revised copy of Design guide submitted to industry sponsor. (At least 1 cycle of revision)
* Bill of Materials for Modeled Design and board materials

## Requirements

Due to the open-endedness of the project description. The requirements below have changed somewhat since the first draft of the product specification document or PDS. To summarize, the complete modeling of our device

### MUST

* Complete and record transient simulations and measures of risetime
* Complete and record frequency domain simulation (AC Response and S-Parameters)
* Be modeled based on easily sourced components i.e. Digikey.
* Construct methodology of scaling design for use in higher frequencies
* Submit a “White-paper” style IEEE formatted document detailing design procedure for low frequency model (144Mhz Bandwidth)

### SHOULD

* Keep costs to <100$ US per assembled board a minimum
* Construct methodology of scaling design for use in higher frequencies
* Construct a scalable model of transmission line
* Design module which optimizes power delivery across the entire bandwidth of operation.
* Design module which optimizes scattering parameters and minimizes undesired signal reflection.
* Design module which creates the shortest output pulses possible to generate higher harmonic content.
* Have 50Ω input and output impedance
* Have a network with a continuously adjustable phase shift
* Perform Rise time vs. NLTL Length and Rise time vs. DC Bias freq. Domain measurements for 144Mhz Bandwidth Design
* Create method for analyzing effects of narrowing and widening line geometry for 6Ghz Bandwidth

### MAY

* Fully characterize a varactor in MATLAB.
* Simulate different transmission line geometries in ADS
* Construct Design full scale (DC-6Ghz) model with most viable geometry
* Build model with increased bandwidth (DC-64Ghz is the goal)
* Design a model with Have reliable behavior at different ambient temperatures
* Perform memento simulations on transmission line models

## Initial Product Design

This project was handed to us with almost unlimited possibilities and required first that we familiarize ourselves with how these circuits function and the main design considerations necessary to build them. The theory involved with NLTL’s are not a part of our undergraduate coursework and a large portion of the time spent on the project was in this stage of reading (and largely not fully understanding) IEEE articles which use this technology and reviewing physics concepts related to Electromagnetics.

The decision to build a small prototype was made early as many papers detailed similar circuit constructions. The reduced bandwidth in which we were operating 0 – 144MHz, allowed us to build a model using a diode with large “tunability” and high-quality inductors with minimal need for complex design techniques. These components were chosen specifically with the bandwidth in mind.

After construction, we continued simulations and attempted measurements on our assembled prototype before attempting simulations looking at the possibility of chaining these circuit blocks together.

## Block Diagram

Figure 3 shows the simplicity of this circuit from a black box perspective. In essence, the block itself is designed to be chained together and be made up of passive components. As a result, this deceptively simple model is how we treated the circuit for the majority of this project. These lines are meant to be as long as possible, so little internal testing, besides that of individual components, was called for.

## 

|  |  |
| --- | --- |
| *Module* | Varactor Loaded Transmission Line (NLTL) |
| *Inputs* | Input pulse or square wave with arbitrarily slow rise time (50 Ohm Termination) |
| *Outputs* | Sharpened pulse with nonlinearities and/or ringing (50 Ohm Termination) |
| *Functionality* | Uses nonlinearities to lessen the time for a voltage to transition from it’s low to high level. (Tested with 1 Volt signals in mind) |

*Figure 3: Level 0 "Black Box" block diagram*

## Implementation

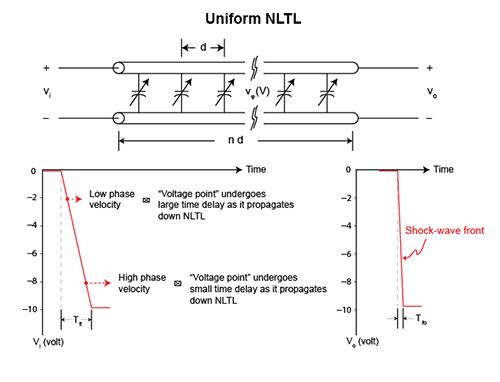
### Concept of Operation

To properly model each section of our NLTL we used a very basic lumped element model. The spice model included in our simulation software was checked against the one provided by the manufacturer of our chosen varactor the BBY40. Due to this, only the addition of series resistance for the inductor and diode comprised one NLTL ladder section. This lumped element model is shown in Figure 4 below.

### 

*Figure 4: Ladder section model used for simulation*

The varactor diode acts a voltage variable capacitor which can change the way the incoming waveform interacts with the circuit. Namely, the changing voltage level inherent in an impulse pulse causes different portions of the wave to travel at different speeds. In general terms, this is what gives us the desirable sharpening we are after. To illustrate this point, the following graphic taken from an application note by [Anritsu](https://www.anritsu.com/en-GB/test-measurement/technologies/shockline-nltl) shows how this may look.



*Figure 5: Visualizing the ability for an NLTL to sharpen an input pulse.*

As we add more and more sections to the NLTL, the wave should keep sharpening in theory. In practice, loss in the system given by heat modeled by the resistances in Figure 4, prevent this from being physically realizable.

### Software

NLTL’s as we have constructed them require no external program or interfacing. The NLTL we have studied is a purely analog device. The software aspect of this project was the use of circuit simulation software and CAD software for production of the actual circuit.

Altium designer was used to construct the CAD models and MICROCAP-12 was used to carry out all simulations on the circuit. The latter was used as well for other functions such as optimizing the input wave to match our measured input in the lab.

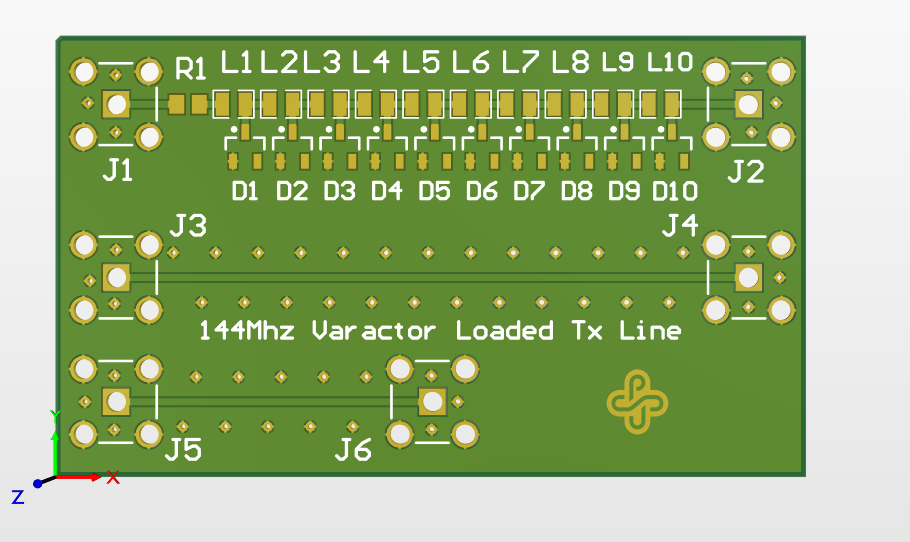
By use of MICROCAP we were also able to investigate S-parameter measurements and import touchstone data retrieved from measurement with a VNA. This allowed us to use sliders to tweak circuit parameters and more accurately model our circuit.

### Hardware

Barring test equipment needed to perform tests on our circuit, the passive nature of our NLTL and the scope of our project mostly involving theory of operation, we required no extra amplification, power sources, or integration into a larger existing hardware system. An optional requirement is the application of an external power source to bring our nonlinear varactors into a desirable operating region.

Physical circuit testing was done using hobbyist tools such as the NANOVNA for S-Parameter measurements. Transient/risetime measurements were carried out by our sponsors due their ability to access lab instruments during the COVID-19 pandemic.

Altium designer was used as well to extract board properties such as physical dimensions and stackup as well as material properties such as permittivity. It was further used to define the impedance properties of the traces as we desire both inputs and outputs to be as close to 50 Ohms as possible for matching with test equipment or PCB sections.



*Figure 6:Altium generated 3D Model of NLTL PCB design*

### 

### White Paper

### The white paper was constructed using LaTeX for maximum flexibility, easy cross-referencing, and reproducibility. As the project went on, it was a requirement to constantly revisit simulations and update plots and graphs. LaTeX was desirable for this as it allowed easy updating by the uploading of an updated image of the same name. This paper is a living document and can be found in the following GitHub repository along with other relevant project files.

### <https://github.com/akier900/Capstone_Rohde-Schwarz_Team13/tree/master/RohdeAndSchwarzWhitePaper>

## Test Plan

We performed many tests on our circuit. In most cases, this required an emphasis on revisiting previous results and finding errors as we changed simulation parameters. In terms of simulation, we implemented parametric tests for observing rise time behavior of a wave passing through our circuit, Whitebox testing via changing circuit parameters such as loss resistance, as well as device specifications like inductance of the series inductor and zero bias capacitance of the varactor diode.

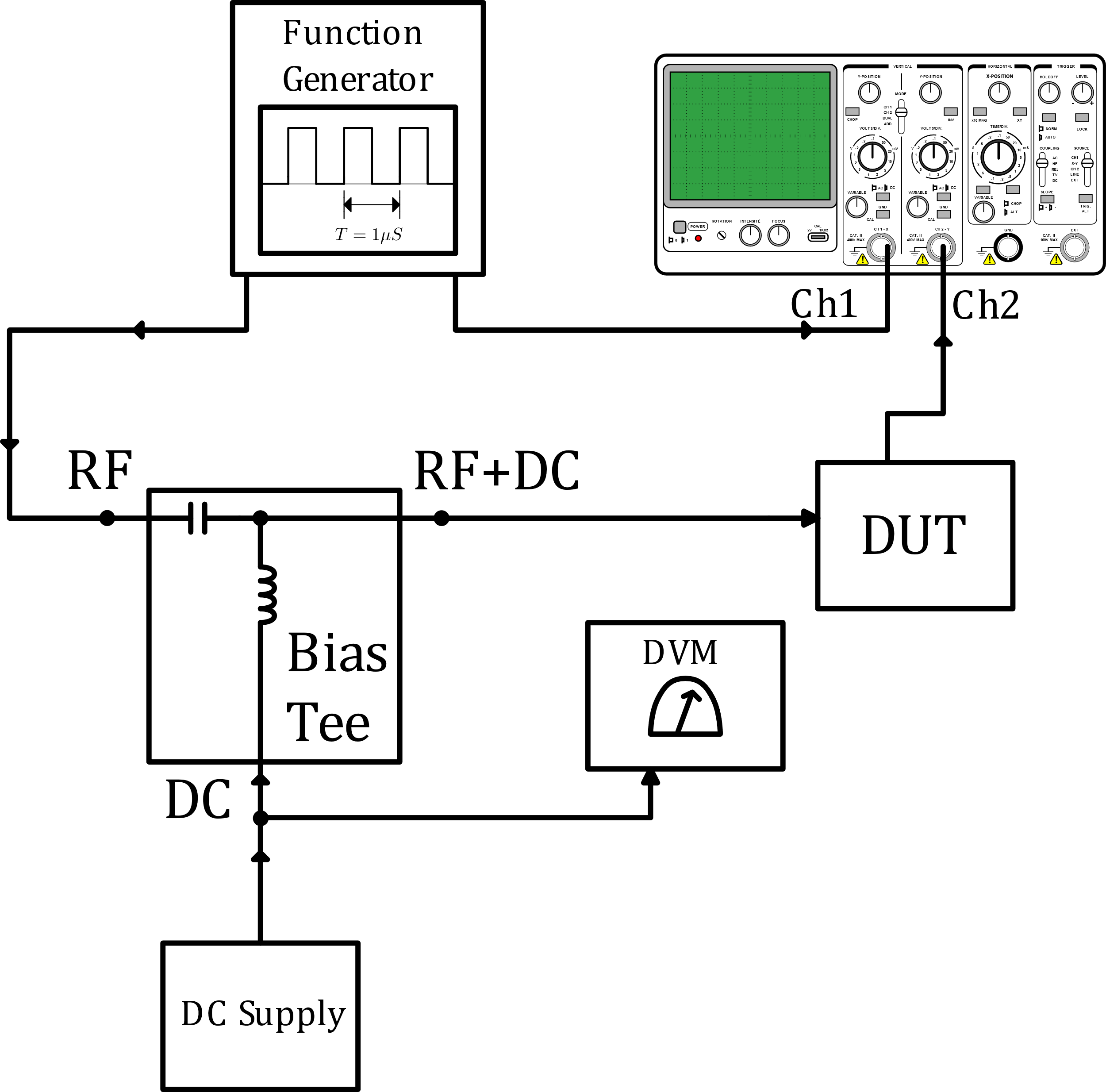
Functional testing was done on the completed circuit boards via continuity checks and impedance measurements of individual components. This ensured ahead of time that the components were within specification and that no time would be wasted in debugging a poorly executed solder joint.

### Individual Component Testing

This testing was done to ensure the devices we acquired were within specification. It involved the measuring of our inductors using a basic LCR meter and the construction of a simple test fixture to use the same meter to measure capacitance of our varactor over a given voltage range.

### Transient Measurement Test Setup

To perform measurements of our circuit as a function of time, we used the setup shown in Figure 6. The Period of the input wave form was chosen arbitrarily as we were looking for a signal that we could practically measure without overly expensive equipment. Since our board was designed without a dedicated port for biasing our components, a bias tee was used to accomplish this. This was a parametric test to confirm and quantify the risetime sharpening.



*Figure 7: Transient Measurement Setup*

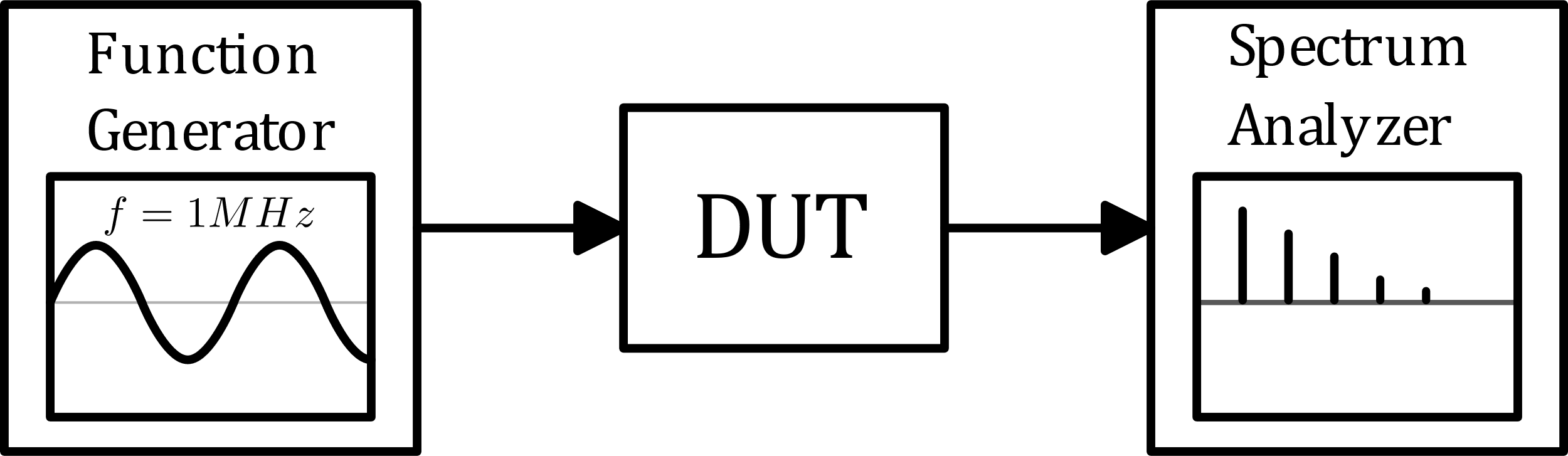
After incrementing the bias level of the input wave from 0 to 3 volts, we fed another square input waveform. This time, the waveform was given large transition times and looked almost trapezoidal. With this, we investigated how dramatic the sharpening is for a very slow waveform and the types of waves our NLTL can improve.

### Power Spectrum Test Setup

To measure the response of our circuit to signals of different frequencies, we utilized the test setup in Figure 7. This was used to find the operating bandwidth of our circuit and to observe how the nonlinear components (namely, the varactor) introduce harmonic distortion. This was used to compare side by side with similar simulations of the same setup, but this is useful to know for other applications of NLTL’s as well, such as frequency multiplication.

### Equipment Used

The tables with the data obtained from these transient measurements and the equipment used can be found in the team [GitHub](https://github.com/akier900/Capstone_Rohde-Schwarz_Team13/tree/master/Measurements/RohdeAndSchwarzMeasurements) repository.



*Figure 8: Spectrum Analysis Test Setup*

## Results

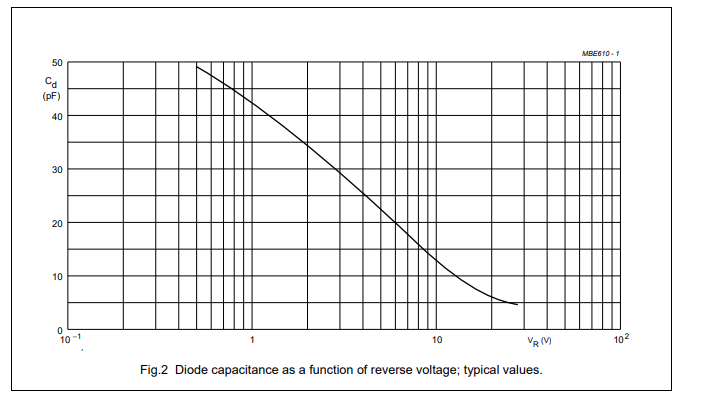
After careful setup and re-setup, we were able to observe the pulse sharpening we expected to see in our testing. We simulated risetime many times and found sharpening did take place. During the making of this document, further errors in our setup were found and corrected to produce the table in Figure 8. While we confirmed pulse sharpening still, there was a stark contrast between the amount of sharpening taking place. This implies that our model is currently incomplete, and further investigation is needed to fix this before building on the design further.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Board 1 Transient Simulations** | | | | | | |
| **Wave Type** | **Amplitude (Volts)** | **Offset (Volts)** | **Input Risetime (nS)** | **Input Falltime (nS)** | **Output Risetime (nS)** | **Output Falltime (nS)** |
| Square | 1Vpp | 0 | 10.00 | 10.00 | 9.19 | 11.26 |
| Square | 1Vpp | 0.5 | 10.00 | 10.00 | 9.18 | 11.02 |
| Square | 1Vpp | 1 | 10.00 | 10.00 | 9.18 | 10.83 |
| Square | 1Vpp | 1.5 | 10.00 | 10.00 | 9.19 | 10.70 |
| Square | 1Vpp | 2 | 10.00 | 10.00 | 9.29 | 10.69 |
| Square | 1Vpp | 2.5 | 10.00 | 10.00 | 9.38 | 10.70 |
| Square | 1Vpp | 3 | 10.00 | 10.00 | 9.45 | 10.70 |
| “Slow Square” | 1Vpp | 0 | 200.00 | 200.00 | 198.24 | 201.79 |

*Figure 9: Transient Simulation Results*

The measured data shown in Figure 9 illuminates the fact that there is still more to modeling NLTL’s than what we currently understand. The rise times did improve however, we expected a more dramatic change with different biasing voltages. This is likely due to the specific capacitance range of the BBY40 since the nonlinearity is produced by a large change in capacitance for a small change in biasing voltage.

Upon further inspection of the CV curve in the [datasheet](https://www.nxp.com/docs/en/data-sheet/BBY40.pdf) and shown below in Figure 10, we do see that this behavior may not be that surprising. As the voltage across the varactor rises, the slope of the CV curve is relatively constant. As a bit of an oversimplification, since the changing of capacitance gives us the sharpening effect, a relatively constant change equates to a consistent amount of sharpening. This may well explain the small variance in rise time improvements.



*Figure 10: CV Curve taken from BBY40 Datasheet*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Board 1 Transient Measurements** | | | | | | |
| **Wave Type** | **Amplitude (Volts)** | **Offset (Volts)** | **Input Risetime (nS)** | **Input Falltime (nS)** | **Output Risetime (nS)** | **Output Falltime (nS)** |
| Square | 1Vpp | 0 | 10.52 | 10.35 | 5.90 | 9.56 |
| Square | 1Vpp | 0.5 | 10.52 | 10.35 | 5.90 | 9.56 |
| Square | 1Vpp | 1 | 10.13 | 10.07 | 6.68 | 8.28 |
| Square | 1Vpp | 1.5 | 10.04 | 9.98 | 6.74 | 8.00 |
| Square | 1Vpp | 2 | 9.76 | 9.67 | 6.70 | 7.73 |
| Square | 1Vpp | 2.5 | 9.71 | 9.63 | 6.83 | 7.70 |
| Square | 1Vpp | 3 | 9.67 | 9.60 | 7.02 | 7.84 |
| “Slow Square” | 1Vpp | 0 | 195.09 | 198.64 | 137.12 | 143.45 |

*Figure 11: Transient Measurement Results*

Figure 11 above shows the measured risetimes of our 10-ladder NLTL. The sharpening is quite evident in these results. The most dramatic change can be seen in the slow square wave case. This tells us that there is a limit to the sharpening and the faster the original pulse, the less benefit the circuit has. It is also important to note that our NLTL has little effect on the fall time of our input pulses and in many cases causes a slowing down of those transitions. There have been many published papers addressing this shortcoming and the design of more complex circuitry is needed to create a similar effect for fall time.

## Conclusion

This project had many difficult aspects to it. The most prevalent was an incomplete understanding of project specifications and deliverables. From the capstone problem statement and initial meetings with our sponsors, we were under the impression that the NLTL would be designed with the intent to produce phase shifting NLTL’s.

While research on this topic helped us to gain some footing in understanding the complex theory involved, it kept us from creating an accurate test plan and construction strategy. In particular, the parametric tests we designed to eventually investigate rise time could not be fully fleshed out until we knew what we were looking for. To be fair, a part of the blame falls on the inability to take time and construct formal testing plan documentation *before* actual testing.

Other major obstacles included the setup of the simulation circuits. Many simulation results had to be thrown out due to improper plot ranges, poor windowing techniques for frequency analysis, and poor modeling of our input source waveforms.

That being said, A lot was learned during the course of this project and we were able to construct and confirm the utility of NLTL’s in regards to increasing waveform speeds and have shown that further development and research in this area would be beneficial for our sponsors and/or future capstone teams to invest in.

## Archive of project documents

Our team documentation including simulation files and results, PCB design files, and our white paper with more details can all be found at our public GitHub Repository.

<https://github.com/akier900/Capstone_Rohde-Schwarz_Team13>