

**EC2304                      MICROPROCESSORS AND ITS APPLICATIONS****AIM**

To learn the architecture programming and interfacing of microprocessors and microcontrollers.

**OBJECTIVES**

- To introduce the architecture and programming of 8085 microprocessor.
- To introduce the interfacing of peripheral devices with 8085 microprocessor.
- To introduce the architecture and programming of 8086 microprocessor.
- To introduce the architecture, programming and interfacing of 8051 micro controller.

**UNIT I                      8085 CPU                      9**

8085 Architecture – Instruction set – Addressing modes – Timing diagrams – Assembly language programming – Counters – Time Delays – Interrupts – Memory interfacing – Interfacing, I/O devices.

**UNIT II                      PERIPHERALS INTERFACING                      9**

Interfacing Serial I/O (8251)- parallel I/O (8255) –Keyboard and Display controller (8279) – ADC/DAC interfacing – Inter Integrated Circuits interfacing (I<sup>2</sup>C Standard)- Bus: RS232C-RS485-GPIB

**UNIT III      8086 CPU                      9**

Intel 8086 Internal Architecture – 8086 Addressing modes- Instruction set- 8086 Assembly language Programming-Interrupts.

**UNIT IV      8051 MICROCONTROLLER                      9**

8051 Micro controller hardware- I/O pins, ports and circuits- External memory – Counters and Timers-Serial Data I/O- Interrupts-Interfacing to external memory and 8255.

**UNIT V                      8051 PROGRAMMING AND APPLICATIONS                      9**

8051 instruction set – Addressing modes – Assembly language programming – I/O port programming -Timer and counter programming – Serial Communication – Interrupt programming –8051 Interfacing: LCD, ADC, Sensors, Stepper Motors, Keyboard and DAC.

**TEXT BOOKS**

1. Ramesh S Gaonkar, Microprocessor Architecture, Programming and application with 8085, 4<sup>th</sup> Edition, Penram International Publishing, New Delhi, 2000. (Unit I, II)
2. John Uffenbeck, The 80x86 Family, Design, Programming and Interfacing, Third Edition. Pearson Education, 2002.
3. Mohammed Ali Mazidi and Janice Gillispie Mazidi, The 8051 Microcontroller and Embedded Systems, Pearson Education Asia, New Delhi, 2003. (Unit IV, V)

**REFERENCES**

1. A.K. Ray and K.M.Burchandi, Intel Microprocessors Architecture Programming and Interfacing, McGraw Hill International Edition, 2000
2. Kenneth J Ayala, The 8051 Microcontroller Architecture Programming and Application, 2<sup>nd</sup> Edition, Penram International Publishers (India), New Delhi, 1996.
3. M. Rafi Quazzaman, Microprocessors Theory and Applications: Intel and Motorola prentice Hall of India, Pvt. Ltd., New Delhi, 2003.

## MICROPROCESSORS AND ITS APPLICATIONS

### UNIT-I 8085 CPU

1. What is microprocessor?

A microprocessor is a multipurpose, programmable, clock-driven, register-based electronic device that reads binary information from a storage device called memory, accepts binary data as input and processes data according to those instructions, and provides result as output.

2. Write the features of 8085 microprocessor?

- It is an 8-bit processor capable of addressing 64 KB of memory.
- The device has 40 pins, requires a +5V power supply.
- It has 16 address lines and the lower 8 address lines are multiplexed with data bus ( $AD_0 - AD_7$ ).
- It is an enhanced version of its predecessor 8080A.
- It can operate with 3MHZ single-phase clock.

3. What is Accumulator?

The Accumulator is an 8-bit register that is part of the arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified as register A.

4. Why  $AD_0 - AD_7$  signal lines are multiplexed?

The signal lines  $AD_0 - AD_7$  are bidirectional. They serve a dual purpose. They are used as the lower order address bus as well as data bus. In executing an instruction during the earlier part of the cycle, these lines are used as lower order bus. During the later part of the cycle, these lines are used as data bus. This is known as multiplexing the bus.

5. Give the format of flag register in 8085. explain each flag.

$D_7 \quad D_6 \quad D_5 \quad D_4 \quad D_3 \quad D_2 \quad D_1 \quad D_0$

S	Z		AC		P		CY
---	---	--	----	--	---	--	----

S- Sign flag. This flag is set when the result of operation is negative number.

Z- Zero flag. This flag is set when the result of operation is zero.

AC- Auxiliary carry flag. In an arithmetic operation, when a carry is generated by digit  $D_3$  and passed onto digit  $D_4$ .

P- Parity flag. After an arithmetic or logical operation, if the result has an even number of 1's, the flag is set.

CY- Carry flag. If an arithmetic operation results in a carry, then the carry flag is set.

6. What is the use of PC and SP in 8085?

There are 2 special purpose registers in 8085.

1. Program Counter(PC): It is an 16-bit register and it is used to carry memory address of the next instruction to be executed.

2. Stack Pointer(SP): The stack is a reserved area of memory in the RAM where temporary information may be stored. A 16-bit Stack Pointer is used to hold the address of the most recent stack entry.

7. What is the use of CLKOUT and RESET OUT signals?

CLKOUT: Clock Output. This signal can be used as the system clock for other signals.

RESET OUT: this signal indicates that the microprocessor is being reset. The signal can be used to reset other devices.

8. Describe the function of following pins in 8085.

a. READY      b. RESET IN

READY: this signal is used to delay the microprocessor read or write cycles until a slow responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

$\overline{\text{RESET IN}}$ : When the signal on this pin goes low, the program counter is set to zero, the buses are tri-stated and microprocessor is reset.

9. List the status signals in 8085.

$\text{IO}/\overline{\text{M}}$ : This is a status signal used to differentiate between I/O and memory operation. When it is high, it indicates I/O operation; when it is low it indicates memory operation.

$S_0, S_1$ : These signals can identify various operations opcode fetch, memory read etc.

10. What is the use of ALE signal?

ALE- Address Latch Enable: This is a positive going pulse generated every time when the 8085 begins an operation. It indicates that the bits on  $\text{AD}_0 - \text{AD}_7$  are address bits.

11. What is the use of HOLD & HLDA signals?

HOLD: this signal indicates that a peripheral such as a DMA (Direct Memory Access) controller is requesting the use of address and data buses.

HLDA: This signal is the o/p signal from  $\mu$ p. This signal acknowledges HOLD Request.

12. How the instructions are classified according to word size?

- i. one-word or one byte instructions
- ii. two-word or two byte instructions
- iii. three-word or three byte instructions

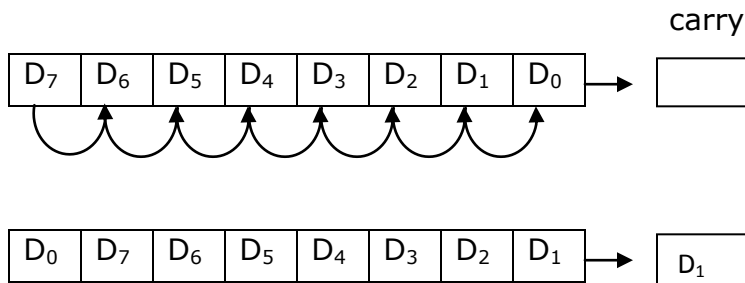
13. Explain the operation performed by 8085 when the following instructions are executed?

- a. SBB C      b. RRC

SBB C: The contents of C register and carry flag are subtracted from the Accumulator content. The result is stored in the Accumulator.

RRC: The Accumulator content is rotated to the right side by one position.

The bit  $D_0$  is shifted to both carry and  $D_7$ .



14. Explain the operation performed by 8085 when the following instructions are executed?

- a. LDAX B      b. XTHL

LDAX B: This instruction copies the data from the memory location specified by BC pair into Accumulator.

XTHL: This instruction exchanges the memory location pointed by stack pointer with the contents of L register and the contents of the next memory location with the H register.

15. Explain the various steps involved when executing CALL instruction.

The Call instruction is used to transfer the program control to a subroutine or Subprogram. There are 4 internal steps are performed when this instruction is executed.

CALL 16 bit addr: This instruction transfers the program sequence to a subroutine address unconditionally. The internal operations performed are:

- i. saves the contents of program counter on stack.

- ii. decrements the stack pointer register by 2.
- iii. Jumps unconditionally to memory location specified by the second and third byte.

16. What is stack?

The stack is a group of memory locations in the R/W memory that is used for temporary storage of binary information during the execution of a program.

17. Differentiate between Jump and Call instructions.

JUMP addr16: This instruction is used to transfer the program control unconditionally from the current memory location to the specified memory location within the program.

CALL addr16: This instruction is used to transfer the program control to the subroutine program. The subroutine program starts from the specified memory location.

18. What is a subroutine program?

A subroutine is a group of instructions written separately from the main program to perform a function that occurs repeatedly in the main program. Thus subroutines avoid the repetition of same set of instructions in the main program.

19. Define instruction and instruction format.

An instruction is a command to the microprocessor to perform a given task on Specified data. Each instruction has 2 parts:

- 1. operation code(opcode): it specifies the operation to be performed.
- 2. operand: it specifies the data to be operated on.

20. Define addressing mode.

Addressing mode is used to specify the way in which the address of the operand is specified within the instruction.

21. List the various types of addressing modes in 8085.

- Register Addressing mode
- Direct Addressing mode
- Indirect Addressing mode
- Immediate Addressing mode
- Implied or inherent Addressing mode

22. What is the use of PUSH and POP instruction?

PUSH rp: This instruction copies the contents of specified register pair on the Stack.

POP rp: This instruction is used to retrieve the contents of specified register pair from stack.

23. Explain the operational difference between the pair of instructions.

SPHL and XTHL

SPHL: This instruction is copies the contents of HL register pair into the memory location pointed by the stack pointer register.

XTHL: This instruction exchanges the contents of memory location pointed by stack pointer with the contents of L register and the contents of the next memory location with the contents of H register.

24. What is the use of Timing diagrams?

Timing diagram is graphical representation instruction execution with respect to time. It is used to show the status of various signals of  $\mu p$  when a instruction is executed.

25. Define instruction cycle.

It is defined as the time required to complete the execution of an instruction. The 8085 instruction cycle consists of 1 to 6 machine cycles.

26. Define machine cycle.

It is defined as the time required to complete one operation of accessing memory, I/O, or acknowledging an an external request. This cycle may consists of 3 to 6 T-states.

27. Define T-state.

It is defined as one subdivision of the operation performed in one clock period. The subdivisions are internal states synchronized with the system clock and each T-state is precisely equal to 1 clock period.

28. Write the machine cyles and no. of T-states for the given instructions.

i. IN 01H      ii. STA 5000 H

Instruction	Machine cycles	Total no. of T-states
IN 01 H:	1. opcode fetch(4T)	10
	2. Memory read(3T)	
	3. I/O read(3T)	
STA 5000 H	1. opcode fetch(4T)	10
	2. Memory read(3T)	
	3. Memory read(3T)	

29. List the interrupt signals in 8085.

TRAP, RST 7.5, RST 6.5, RST 5.5, INTR

30. Write the various types of machine cycles in 8085.

- Opcode fetch
- Memory read
- Memory write
- I/O read
- I/O write
- Interrupt acknowledgement
- Bus idle

31. What is the use of SIM instruction?

SIM: Set Interrupt Mask.

It is a 1 byte instruction and can be used for 3 different functions.

- i. Set mask for RST 7.5, 6.5 and 5.5 interrupts
- ii. Reset RST 7.5 flip-flop.
- iii. Implement serial I/O.

32. What is function of RIM instruction?

RIM: Read Interrupt Mask.

This is a 1-byte instruction that can be used for the following functions

- i. To read interrupt masks.
- ii. To identify pending interrupts
- iii. To receive serial data.

33. What is nonmaskable interrupt?

TRAP is the nonmaskable interrupt in 8085. It has the highest priority among Interrupt signal. When this interrupt is triggered, the program control is transferred to location 0024H without any hardware or Interrupt enable instruction EI.

34. What are the different ways to disable the interrupt process?

The entire interrupt process is disabled by resetting the interrupt enable flip-flop. The flip-flop can be reset in one of 3 ways.

- i. Instruction DI
- ii. System Reset
- iii. Recognition of an interrupt request

35. What do you mean by vectored interrupts?

The vectored interrupts are automatically vectored to specific locations on memory without any external hardware. In 8085, there are 4 vectored interrupts. The interrupts and their call locations are listed below.

**Interrupts****call location**

TRAP	0024H
RST 7.5	003CH
RST 6.5	0034H
RST 5.5	002CH

36. What is memory mapped I/O?

This is one of the techniques for interfacing I/O devices with  $\mu$ p. In memory mapped I/O, the I/O devices assigned and identified by 16-bit addresses. To transfer the data between MPU and I/O devices memory related instructions ( such as LDA, STA etc.) and memory control signals ( MEMR, MEMW) are used.

37. What is I/O mapped I/O?

This is one of the techniques for interfacing I/O devices with  $\mu$ p. In I/O mapped I/O, the I/O devices assigned and identified by 8-bit addresses. To transfer the data between MPU and I/O devices I/O related instructions ( IN and OUT ) and I/O control signals (IOR, IOW) are used.

38. Differentiate between Absolute and partial decoding.

Absolute decoding: All 8 address lines are decoded to generate one unique output pulse for selecting an I/O device.

Partial decoding: one address line is decoded to generate unique for selecting an I/O device. The remaining address lines are don't care lines. As a result the device has multiple addresses.

39. Calculate the time delay for the program given below, when clock period =  $0.5\mu$ s.

MVI C, F0 H	
LOOP: DCR C	
JNZ LOOP	
	No. of T states
MVI C, EF	--- 7 T states
LOOP: DCR C	--- 4 T states
JNZ LOOP	--- 10 / 7 T states

$$\text{Time delay } T_D = (14 \times 0.5 \times 10^{-6} \times 240) - 3 \times 0.5\mu\text{s} + 7 \times 0.5 \mu\text{s} \\ = 1.68 \text{ ms.}$$

40. Write a time delay program using 16-bit register.

```
LXI H, 2345 H
LOOP: DCX H
      MOV A,C
      ORA B
      JNZ LOOP
```



## UNIT-II PERIPHERAL INTERFACING

### 1. What is simplex and duplex transmission?

Simplex transmission: data are transmitted in only one direction.  
 Duplex transmission: data flow in both directions. If the transmission goes one way at a time, it is called half duplex; if it goes both way simultaneously, then it is called full duplex.

### 2. Define Baud.

The rate at which the bits are transmitted, bits per second is called Baud.

### 3. What are the signals available for serial communication?

SID – serial input data

SOD – serial output data

### 4. What is the use of checksum technique?

The checksum technique is used when blocks of data are transferred.  
 It involves adding all the bytes in a block without carries. Then the 2's Complement of the sum is transmitted.

### 5. Write the functions of RTS and CTS signals.

RTS – Request to send

It is the output from data terminal equipment(DTE).

CTS –Clear to send

It is a general purpose input to DTE. It can be used as a handshake signal.

### 6. List some serial I/O standards.

RS-232C, RS-422A, RS-423A.

### 7. Write the control signals in 8251A.

$\overline{CS}$  – chipselect

$\overline{C} / \overline{D}$  - Control/ Data

$\overline{WR}$  - Write

$\overline{RD}$  - Read

### 8. What is USART?

It is a programmable device. Its function and specification for serial I/O can be determined by writing instructions in its internal registers. The Intel 8251A USART is a device widely used in serial I/O.

9. What is use of control register?

It is a 16-bit register used to store the control word. The control word consists of 2 independent bytes: the first byte is called mode instruction and the second byte is called command instruction.

10. Write the features of 8255A.

The 8255A has 24 I/O pins that can be primarily grouped primarily in two 8-bit Parallel ports: A and B, with eight bits as port C. The 8-bits of port C can be used as two 4-bit ports:  $C_{UPPER}$   $C_U$  and  $C_{LOWER}$   $C_L$ .

11. What is BSR mode?

All functions of 8255 are classified according to 2 modes. In the controlword, if  $D_7 = 0$ , then it represents bit set reset mode operation. The BSR mode is used to set or reset the bits in port C.

12. What is mode 0 operation of 8255.

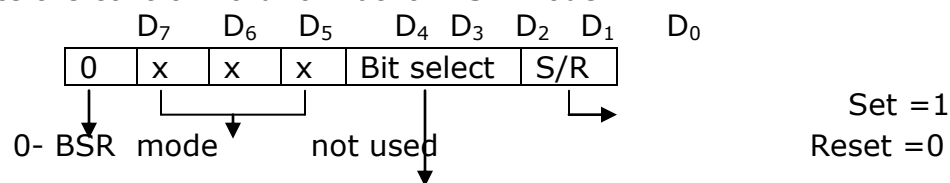
In this mode, ports A and B are used as two simple 8-bit I/O ports and port C as two 4-bit ports. Each port can be programmed to function as an input port or an output port. The input/ output features in mode 0 as follows:

- i. outputs are latched
- ii. inputs are not latched
- iii. ports do not have handshake or interrupt capability.

13. What are the modes of operation supported by 8255?

- i. Bit set reset mode(BSR)
- ii. I/O mode
  - Mode 0
  - Mode1
  - Mode2

14. Write the control word format for BSR mode.



000 = bit 0

000 = bit 1

000 = bit 2

000 = bit 3

000 = bit 4

000 = bit 5

000 = bit 6

000 = bit 7

15. What is the function of  $\overline{\text{STB}}$  signal?

This signal is generated by a peripheral device to indicate that it has transmitted a byte of data.

16. What is the function of IBF signal?

IBF (Input buffer full): This signal is an acknowledgement by the 8255A to indicate that the input latch has received the data byte.

17. What is mode 2 operation?

In this mode, port A can be configured as the bidirectional port and port B either in mode 0 or mode 1. Port A uses 5 signals from port C as handshake signals for data transfer.

18. What is ADC and DAC?

The electronic circuit that translates an analog signal into a digital signal is called analog-to-digital converter (ADC).

The electronic circuit that translates a digital signal into an analog signal is called Digital-to-analog converter (DAC).

19. Define conversion time.

It is defined as the total time required to convert an analog signal into a digital output. It is determined by the conversion technique used and by the propagation delay in various circuits.

20. What are the functions to be performed by  $\mu\text{p}$  while interfacing an ADC?

- i. Send a pulse to the START pin.
- ii. Wait until the end of conversion
- iii. Read the digital signal at an input port.

21. Write the different types of ADC.

- i. Single slope ADC
- ii. Dual slope ADC
- iii. Successive approximation ADC
- iv. Parallel comparator type ADC
- v. Counter type ADC

22. What is resolution time in ADC?

It is defined as a ratio of change in value of input voltage  $V_i$ , needed to change the digital output by 1 LSB. If the full scale input voltage required to cause a digital output of all 1's is  $V_{\text{IFS}}$ . Then the resolution can be given as

$$\text{Resolution} = V_{\text{IFS}} / (2^n - 1)$$

23. List the functions performed by 8279.

- i. It has built-in hardware to provide key debounce.
- ii. It provides a scanned interface to a 64 contact key matrix.
- iii. It provides multiplexed display interface with blanking and inhibit options.
- iv. It provides three input modes for keyboard interface.

23. What is key debounce?

The push button keys when pressed, bounces a few times, closing and opening the contacts before providing a steady reading. So reading taken during bouncing may be faulty. Therefore the microprocessor must wait until the key reach to steady state. This is known as key debounce.

24. What are the operating modes in 8279?

- i. Scanned keyboard mode
- ii. Scanned sensor matrix
- iii. Strobed input.

25. What is N-key rollover?

In N-key rollover each key depression is treated independently from all others. When a key is depressed, the debounce logic is set and 8279 checks for key depress during next two scans.

26. Write a command word to read data from FIFO RAM.

0	1	0	AI	X	A	A	A
---	---	---	----	---	---	---	---

AI - Autoincrement flag

AAA - RAM Address

27. Write the features of RS-232.

- It operates in single-ended mode.
- The maximum cable length can be up to 50 feet.
- It supports maximum data rate of up to 20 K.
- It offers receiver input resistance in the range of  $3k\Omega$  to  $7k\Omega$ .

28. Write the features of I<sup>2</sup>C bus.

- i. Two bus lines are required, serial data line and serial clock line.
- ii. Serial, 8-bit oriented, bidirectional data transfers can be made at up to 100kbits/s in standard mode, up to 400kbits/s in fast mode or up to 3.4 Mbit/s in the high-speed mode.
- iii. Onchip filtering rejects spikes on the bus data line to preserve data Integrity.

29. What is the mode of operation in RS-232?

The mode of operation in RS-232 is single -ended mode.

30. What are the advantages I<sup>2</sup>C bus.

- i. Good for communication with onboard devices that are accessed occasionally.
- ii. Easy to link multiple devices because of addressing schemes.
- iii. Cost and complexity do not scale up with the no. of devices.

31. What are the applications of I<sup>2</sup>C.

It is used as the control interface to signal processing devices that have Separate data interfaces, e.g. RF tuners, video decoders and encoders and Audio processors.

32. What are the operation modes of standard-mode I<sup>2</sup>C bus.

- i. Fast mode
- ii. High speed mode
- iii. 10-bit addressing

33. What are the output modes in 8279?

- i. Left entry
- ii. Right entry

34. What is strobed input mode?

In the strobed input mode, data is entered to FIFO RAM from the returned lines. The data is entered at the rising edge of the CNTL/ STB signal.

35. What is the significance of end of conversion signal while interfacing A/D Converter to a  $\mu$ p?

The end of conversion signal indicates that the A/D conversion is completed so that microprocessor can read digital data from ADC.

36. What is the internal operating frequency of 8279? How can you derive it from Clock signal?

All timing and multiplexing signals for 8279 are generated by an internal Prescaler. This prescaler divides the external clock by a programmable integer Value given in the programclock command word, to generate internal frequency. The format of program clock command word is

0	0	1	P	P	P	P	P
---	---	---	---	---	---	---	---

Where P P P P P determine the value of integer ranges from 2 to 31. To give proper Scan and key debounce times, the internal frequency should be 100 kHz.

37. Find the program clock command word if external clock frequency is 2 MHz.

$$\begin{aligned}\text{Prescalar value} &= (2 \times 10^6) / (100 \times 10^3) \\ &= (10100)_2\end{aligned}$$

Therefore command word =  $(00110100)_2$

38. What is the voltage level used in RS-232?

The maximum common mode voltage is  $\pm 25$ .

39. What is the ATN signal?

The attention line when asserted low indicates that the controller is putting a Universal command or an address command such as "listen" on the data bus. When ATN is high, the data bus contains data or a status byte.

40. What are the management lines in GPIB bus?

- Interface clear
- Attention line
- Service request
- Remote enable
- End or identity

### **UNIT-III 8086 CPU**

1. What are the functional parts of 8086 CPU?

The two independent functional parts of the 8086 CPU are:

- i. Bus Interface Unit (BIU):  
BIU sends out addresses, fetches instruction from memory, reads data from ports and memory and writes data to ports and memory.
- ii. Execution Unit (EU):  
EU tells the BIU where to fetch instructions or data, decodes instructions and executes instructions.

2. What is the purpose of a decoder in EU?

The decoder in EU translates instructions fetched from memory into a series of actions, which the EU carries out.

3. Give the register classification of 8086.

The 8086 contains:

- i. General purpose registers:  
They are used for holding data, variables and intermediate results temporarily.
- ii. Special purpose registers:

They are used as segment registers, pointers, index register or as offset storage registers for particular addressing modes.

4. What are general data registers?

The registers AX, BX, CX and DX are the general data registers.

AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL

L and H represents the lower and higher bytes of particular register.

- AX register is used as 16-bit accumulator.
- BX register is used as offset storage for forming physical addresses in case of certain addressing modes.
- CX register is used as a default counter in case of string and loop instructions.
- DX register is used as an implicit operand or destination in case of a few instructions.

5. Give the different segment registers.

The four segment registers are:

- Code segment register:  
It is used for addressing a memory location in the code segment of the memory, where the executable program is stored.
- Data segment register:  
It points to the data segment of the memory, where data is resided.
- Extra segment register:  
It also contains data.
- Stack segment register:  
It is used for addressing stock segment of memory. It is used to store stack data.

CS
SS
DS
ES

Segment registers





- ii. Allows the placing of code, data and stack portions of the same program in different parts of memory for data and code protection.
- iii. Permits a program and/or its data to be put into different areas of memory, each times program is executed i.e., provision for relocation may be done.

11. What is pipelining ?

Fetching the next instruction while the current instruction executes is called pipelining.

12. What are the two parts of a flag register ?

The two parts of the 16 bit flag register are:

- i. Condition code or status flag register:  
It consists of six flags to indicate some condition produced by an instruction.
- ii. Machine control flag register:  
It consists of three flags and are used to control certain operations of the processor.

13. Draw the format of 8086 flag register.

8086 flag register:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF

U-Undefined

CF - Carry flag  
 PF - Parity flag  
 AF - Auxiliary flag  
 ZF - Zero flag  
 SF - Sign flag  
 TF - Single step trap flag  
 DF - Direction flag  
 IF - Interrupt enable flag  
 OF - Overflow flag

14. Explain the three machine control flags.

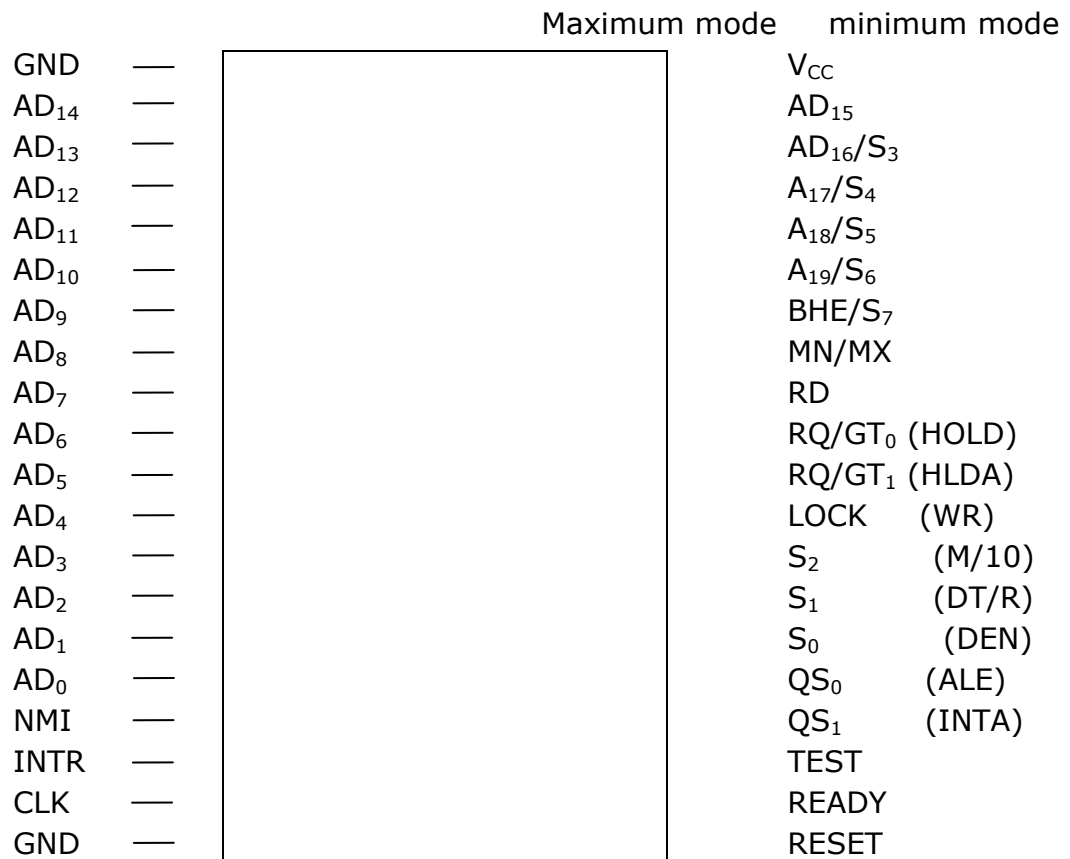
- i. Trap flag:  
If this flag is set, the processor enters the single step execution.
- ii. Interrupt flag:

If this flag is set, the maskable interrupts are recognized by the CPU, otherwise they are ignored.

iii. Direction flag:

This is used by string manipulation instructions. If this flag bit is '0', the string is processed from the lowest to the highest address i.e., auto incrementing mode. Otherwise, the string is processed from highest address to lowest address, i.e., auto decrementing mode.

15. Draw the pin configuration of 8086.



Pin configuration of 8086

16. What are the three groups of signals in 8086 ?

The 8086 signals are categorized in three groups.

They are:

- The signals having common functions in minimum and maximum mode.
- The signals having special functions for minimum mode.
- The signals having special functions for maximum mode.

17. What are the uses of  $AD_{15} - AD_0$  lines ?

$AD_{15} - AD_0$  are time multiplexed memory I/O address and data lines. Address remains on the lines during  $T_1$  state, while data is available on data bus during  $T_2$ ,  $T_3$ ,  $T_w$  and  $T_4$  states. These lines are active high and float to a tristate during interrupt acknowledge and local bus hold acknowledge cycles.

18. What is the operation of RD signal ?

RD is an active low signal. When it is low, it indicates the peripherals that the processor is performing a memory or I/O read operation.

19. Give the function of i. Ready and ii. INTR signal.

i. Ready signal:

It is an acknowledgement from slow devices of memory that they have completed data transfer. The signal is synchronized by 8284 A clock generator to give ready input to 8086. The signal is active high.

ii. INTR signal:

It is a level triggered input. This is sampled during the last cycle of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle. This can be internally masked by resetting the interrupt enable flag. The signal is active high and internally synchronized.

20. What is the operation performed when TEST input is low ?

When the TEST input is low, execution will continue, else, the processor remains in an idle state.

21. What is NMI (Non-Maskable Interrupt) ?

NMI is an edge-triggered input, which causes a type 2 interrupt. It is not maskable internally by software and transition from low to high initiates the interrupt response at the end of the current instruction. This input is internally synchronized.

22. What is the purpose of clock input ?

The clock input provides the basic timing for processor operation and bus control activity. It is an asymmetric square wave with 33% duty cycle. The range of frequency varies from 5MHz to 10MHz.

23. What is the function of MN/MX pin?

The logic level at MN/MX pin decides whether processor operates in minimum or maximum mode.

24. What happens when a high is applied to RESET pin ?

When a high is given to RESET pin, the processor terminates the current activity and starts executing from FFFF0H. It must be active for at least four clock cycles. It is internally synchronized.

25. What will happen when a DMA request is made, while the CPU is performing a memory or I/O cycles ?

When a DMA request is made, while the CPU is performing a memory or I/O cycles, it will request the local bus during  $T_4$  provided:

- i. The request occurs on or before  $T_2$  state of the current cycle.
- ii. The current cycle is not operating over the lower byte of a word.
- iii. The current cycle is not the first acknowledge of an interrupt acknowledge sequence.
- iv. A lock instruction is not being executed.

26. Differentiate between minimum and maximum mode.

Minimum mode	Maximum mode
<ol style="list-style-type: none"> <li>i. A processor is in minimum mode when MN/MX pin is strapped to +5V.</li> <li>ii. All the control signals are given out by microprocessor chip itself.</li> <li>iii. There is a single microprocessor.</li> </ol>	<p>A processor is in maximum mode when MN/MX is grounded.</p> <p>The processor derives the status signals <math>S_2</math>, <math>S_1</math> and <math>S_0</math>. Another chip called bus controller derives control signals using this status information.</p> <p>There may be more than one microprocessor.</p>

27. Give any four pin definitions for the minimum mode.

Symbol	Description
i. INTA	Indicates recognition of an interrupt request. Consists of two negative going pulses in two consecutive bus cycles.
ii. ALE	Outputs a pulse at the beginning of the bus cycle and to indicate an address available on address pins.
iii. HLDA	Outputs a bus grant to a requesting master.
iv. HOLD	Receives bus requests from bus masters.

28. What is a bootstrap loader ?

When a "1" is applied to reset input, PSW, IP, DS, ES, CS and instruction queue are cleared and CS is set to FFFF. With IP = 0000 and CS = FFFF, the processor will begin executing from FFFF0. This location would be in read-only section of memory and contains a JMP instruction to a program for initializing the system and loading the operating system. Such a program is called as a bootstrap loader.

29. What are the pins that are used to indicate the type of transfer in minimum mode ?

The M/IO, RD, WR lines specify the type of transfer. It is indicated in the following table:

M/IO	RD	WR	
0	0	1	I/O Read
0	1	0	I/O Write
1	0	1	Memory read
1	1	0	Memory write.

30. What is the operation of  $S_0$ ,  $S_1$  and  $S_2$  pins in maximum mode ?

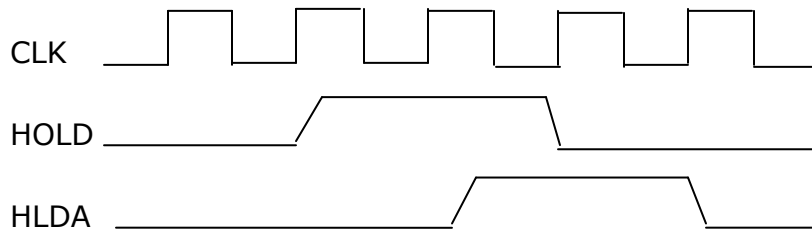
$S_2$ ,  $S_1$ ,  $S_0$  indicates the type of transfer to take place during the current bus cycle.

$S_2$	$S_1$	$S_0$		
0	0	0	-	Interrupt acknowledge
0	0	1	-	Read I/O port
0	1	0	-	Write I/O port
0	1	1	-	Halt
1	0	0	-	Instruction fetch
1	0	1	-	Read Memory
1	1	0	-	Write Memory
1	1	1	-	Inactive.

31. Give any four pin definitions for maximum mode.

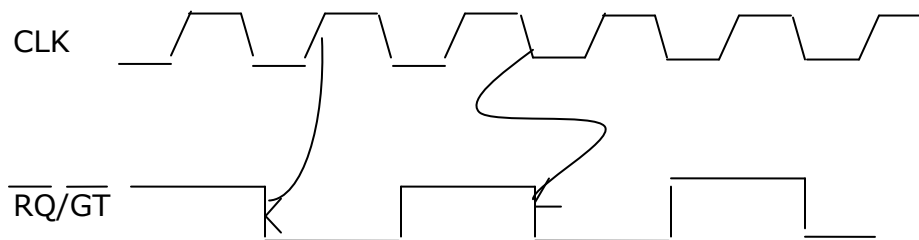
Symbol	Description
QS1, QS0	Reflects the status of the instruction queue. This status indicates the activity in the queue during the previous clock cycle.
$\overline{\text{LOCK}}$	Indicates that the bus is not to be relinquished to other potential bus masters.
$\overline{\text{RQ/GT1}}$	For inputting bus requests and outputting bus grants.
$\overline{\text{RQ/GT0}}$	Same as $\overline{\text{RQ/GT1}}$ except that a request on $\overline{\text{RQ/GT0}}$ has higher priority.

32. Draw the bus request and bus grant timings in minimum mode system.



Bus request and bus grant timings in minimum

33. Draw  $\overline{\text{RQ/GT}}$  timings in maximum mode.



34. Write a program to add a data byte located at offset 0500H in 2000H segment to another data byte available at 0600H in the same segment and store the result at 0700H in the same segment.

MOV AX,2000H ; initialize DS with value

```

MOVDS, AX ; 2000H
MOV AX, [500H] ; Get first data byte from 0500H offset
ADD AX, [600H]; Add this to the second byte from 0600H
MOV [700H],AX; store AX in 0700H
HLT ; Stop.

```

35.What is the main use of LOCK prefix?

- i. The lock prefix allows a microprocessor to make sure that another processor does not take control of the system bus while it is in the middle of a critical instruction which uses the system bus.

36.What are the different types of addressing modes of 8086 instruction set ?

The different addressing modes are:

- i. Immediate
- ii. Direct
- iii. Register
- iv. Register indirect
- v. Indexed
- vi. Register relative
- vii. Based indexed
- viii. Relative based indexed

37.What are the different types of instructions in 8086 microprocessor?

The different types of instructions in 8086 microprocessor are:

- i. Data copy / transfer instructions
- ii. Arithmetic and logical instructions
- iii. Branch instructions
- iv. Loop instruction
- v. Machine control instruction
- vi. Flag manipulation instruction
- vii. Shift and rotate instruction
- viii. String instruction.

38.What is multiple interrupt processing capability?

Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have multiple interrupt processing capability.

39.What is hardware interrupt?

An 8086 interrupt can come from any one of three sources. One source is an external signal applied to the nonmaskable interrupt (NMI) input or to the interrupt (INTR) input pin. An interrupt caused by the signal applied to one of these inputs is referred to as a hardware interrupt.

40. What is software interrupt?

The interrupt caused due to execution of interrupt instruction is called software interrupt.

41. What is assembly level programming?

A program called 'assembler' is used to convert the mnemonics of instruction and data into their equivalent object code modules. The object code modules are further converted into executable code using linker and loader programs. This type of programming is called assembly level programming.

42. What is a stack ?

Stack is a top-down data structure, whose elements are accessed using a pointer that is implemented using the SS and SP registers. It is a LIFO data segment.

43. How is the stack top address calculated ?

The stack top address is calculated using the contents of the SS and SP register. The contents of stack segment (SS) register is shifted left by four bit positions (multiplied by (0h)) and the resulted 20-bit content is added with the 16-bit offset value of the stack pointer (SP) register.

SS	-	5000H	
SP	-	2050H	
		SS	- 0101 0000 0000 0000
		10H * SS	- 0101 0000 0000 0000 0000
		SP	- 0010 0000 0101 0000
		Stack- top	0101 0010 0000 0101 0000
		Address	5 2 0 5 0

44. What are the two types of interrupts in 8086 ?

The two types of interrupts are:

i. External interrupts:

In this, the interrupt is generated outside the processor.

Example : Keyboard interrupt.

ii. Internal interrupts:

It is generated internally by the processor circuit or by the execution of an interrupt instruction.

Example : Zero interrupt, overflow interrupt.



## UNIT-IV 8051 MICROCONTROLLER

### UNIT-V 8051 PROGRAMMING AND APPLICATIONS

#### 1. WHAT ARE THE SPECIAL FUNCTION REGISTER?

The special function registers are stack pointer, index pointer (DPL and DPH), I/O port addresses, status (PSW) and accumulator.

#### 2. WHAT ARE THE USES OF ACCUMULATOR REGISTER?

The accumulator registers (A and B at addresses 0E0h and 0F0h, respectively) are used to store temporary values and the results of arithmetic operations.

#### 3. WHAT IS PSW?

Program status word (PSW) is the set of flags that contains the status information and is considered as one of the special function registers.

#### 4. WHAT IS STACK POINTER (SP)?

- Stack pointer (SP) is a 8 bit wide register and is incremented before the data is stored into the stack using PUSH or CALL instructions.
- It contains 8-bit stack top address. It is defined anywhere in the on-chip 128-byte RAM.
- After reset, the SP register is initialised to 07.
- After each write to stack operation, the 8-bit contents of the operand are stored onto the stack, after incrementing the SP register by one.
- It is not a top-down data structure. It is allotted an address in the special function register bank.

#### 5. WHAT IS DATA POINTER (DTPR)?

- It is a 16-bit register that contains a higher byte (DPH) and lower byte (DPL) of a 16-bit external data RAM address.
- It is accessed as a 16-bit register or two 8-bit registers.
- It has been allotted two addresses in the special function register bank, for its two bytes DPH and DPL.

#### 6. WHAT IS A SERIAL DATA BUFFER?

- Serial data buffer is a special function register and it initiates serial transmission when byte is written to it and if read, it reads received serial data.
- It contains two independent registers internally.
- One of them is a transmit buffer, which is a parallel-in serial-out register. The other is a receive buffer, which is a serial-in parallel-out register.

### 7. WHAT ARE TIMER REGISTERS?

Timer registers are two 16-bit registers and can be accessed as their lower and upper bytes. TLO represents the lower byte of the timing register 0, while THO represents higher bytes of the timing register 0. Similarly, TLI and THI represent lower and higher bytes of timing register 1. These registers can be accessed using the four addresses allotted to them, which lie in the special function registers address range, i.e., 801 H to FF.

### 8. WHAT IS THE USE OF TIMING AND CONTROL UNIT?

Timing and control unit is used to derive all the necessary timing and control signals required for the internal operation of the circuit. It also derives control signals that are required for controlling the external system bus.

### 9. WHY OSCILLATOR CIRCUIT IS USED?

Oscillator circuit is used to generate the basic timing clock signal for the operation of the circuit using crystal oscillator.

### 10. WHAT IS THE PURPOSE OF USING INSTRUCTION REGISTER?

Instruction register is used for the purpose of decoding the opcode of an instruction to be executed and gives information to the timing and control unit generating necessary signals for the execution of the instruction.

### 11. GIVE THE PURPOSE OF ALE/PROG SIGNAL.

- ALE/PROG is an address latch enable output pulse and indicates that valid address bits available on the respective pins.
- The ALE pulses are emitted at a rate of one-sixth of the oscillator frequency. The signal is valid only for external memory accesses.
- It may be used for external timing or clockwise purpose. One ALE pulse is skipped during each access to external data memory.

### 12. EXPLAIN THE TWO POWER SAVING MODE OF PERATION.

The two power saving modes of operation are:

#### I. Idle mode:

In this mode, the oscillator continues to run and the interrupt, serial port and timer blocks are active, but the clock to the CPU is disabled. The CPU status is preserved. This mode can be terminated with a hardware interrupt or hardware reset signal. After this, the CPU resumes program execution from where it left off.

#### II. Power down mode:

In this mode, the on-chip oscillator is stopped. All the functions of the controller are held maintaining the contents of RAM. The only way to terminate this mode is

hardware reset. The reset redefines all the SFRs but the RAM contents are left unchanged.

#### 14. DIFFERENTIATE BETWEEN PROGRAM MEMORY AND DATAMEMORY.

- i. It stores the programs to be executed.
- ii. It stores only program code which is to be executed and thus it need not be written, so it is implemented using EPROM. It stores the data, line intermediate results, variables and constants required for the execution of the program. The data memory may be read from or written to and thus it is implemented using RAM.

#### 13. GIVE THE ADDRESSING MODES OF 8051?

There are six addressing modes in 8051. They are

- Direct addressing
- Indirect addressing
- Register instruction
- Register specific(register implicit)
- Immediate mode
- Indexed addressing

#### 14. WHAT IS DIRECT ADDRESSING MODE?

The operands are specified using the 8-bit address field, in the instruction format. Only internal data Ram and SFRS can be directly addressed. This is known as direct addressing mode.

Eg: Mov R0, 89H

#### 15. WHAT IS INDIRECT ADDRESSING MODE?

In this mode, the 8-bit address of an operand is stored in a register and the register, instead of the 8-bit address, is specified in the instruction. The registers R0 and R1 of the selected bank of registers or stack pointer can be used as address registers for storing the 8-bit addresses.

The address register for 16-bit addresses can only be 'data pointer' (DPTR).

Eg : ADD A, @ R0.

#### 16. WHAT IS MEANT BY REGISTER INSTRUCTIONS ADDRESSING MODE?

The operations are stored in the registers R0 – R7 of the selected register bank. One of these eight registers (R0 – R7) is specified in the instruction using the 3-bit register specification field of the opcode format. A register bank can be selected using the two bank select bits of the PSN. This is called as register instruction addressing mode

Eg: ADD A, R7.

#### 19. WHAT ARE REGISTER SPECIFIC INSTRUCTION?

In this type of instructions, the operand is implicitly specified using one of the registers. Some of the instructions always operate only on a specific register.

Eg: RLA; This instruction rotates accumulator left.

#### 20. WHAT IS IMMEDIATE ADDRESSING MODE?

An immediate data ie., a constant is specified in the instruction, after the opcode byte.

Eg: MOV A, #100

The immediate data 100 (decimal) is added to the contents of the accumulator. For specifying a hex number, it should be followed by H. These are known as immediate addressing mode.

#### 21. WHAT IS INDEXED ADDRESSING?

This addressing mode is used only to access the program memory. It is accomplished in 8051 for look-up table manipulations. Program counter or data pointer are the allowed 16-bit address storage registers, in this mode of addressing. These 16-bit registers point to the base of the look-up table and the ACC register contains a code to be converted using the look-up table. The look-up table data address is found out by adding the contents of register ACC with that of the program counter or data pointer.

In case of jump instruction, the contents of accumulator are added with one of the specified 16-bit registers to form the jump destination address.

Eg: MOV C, A @ A + DPTP

JMP @ A + DPTR

#### 22. WHAT IS ENCAPSULATION?

Encapsulation is a method used to protect the chip and the interconnect technology used the chip electrically to the printer circuit card. It has a significant impact on the final application's cost, size and quality.

#### 23. WHAT ARE THE SPECIALISED FUNCTIONS OF THE I/O PINS?

The specialized functions of the I/O pins are serial ports, analog I/O, external device buses, etc.

#### 24. IF THE I/O PINS ARE ALWAYS BEING DRIVEN, HOW IS A LOGIC VALUE READ FROM THE PIN?

When a "1" is loaded into the output flip-flop, the (weak) pull-up can be easily over-powered by other logic drivers. Even if a pin does not have a pull-up (just the open-drain driver), it is sufficient to have a "1" written to it. The transistor will be off and the pin will float and can be driven by the external circuit.

25. WHAT IS DONE TO REDUCE THE TIME TAKEN BY THE I/O PIN TO CHANGE FROM LOW TO HIGH VOLTAGE VALUE?

To reduce the relatively long time to change from low to high voltage output, the manufacturers provide high-current drivers on the I/O pins that drive high (without pull-up) for two clock cycles. When using peripheral I/O devices, the pins are driven high, rather than just pulled up.

26. WHAT IS A "DOTTED-AND BUS"? WHY IS IT CALLED "DOTTED AND"?

The dotted-AND bus is a bus that utilizes a number of transistors pulling down line to ground using open collectors or open drain.

The bus is pulled-up with a number of transistors, controlled by a control signal, any of which can pull the line low. The bus will go low, when the transistors in the circuit are turned on and will be high, when the transistors are off, it is known as "dotted-AND".

27. WHAT ARE THE RULES FOLLOWED FOR INTERFACING I/O PIN TO EXTERNAL DEVICES?

The few rules that have to be followed are:

- i. Only use negatively active signals
- ii. If a pin is not actively outputting a signal, set it high.

28. WHAT IS THE PURPOSE OF A GATE BIT IN TIMER?

The gate is a secondary execution control bit. If the gate bit is reset, the timer is enabled to run at any time. If the bit is set, then only when appropriate-INTn bit is high, the timer will run.

29. WHEN ARE TIMER OVERFLOW BITS SET AND RESET?

The timer overflow bits are set when timer rolls over and reset either by the execution of an ret instruction or by software, manually clearing the bits. The bits are located in the TCON register along with timer run control (TRn) bits.

30. EXPLAIN THE MODE (0 AND1) OPERATION OF THE TIMER.

The operations are as follows:

- Timer mode 0 and 1 operations are similar for the 13 bit (mode) or 16 bit (mode 1) counter. When the timer reaches the limits of the count, the overflow flag is set and the counter is reset back to zero.
- The modes 0 and 1 can be used to time external events.
- They can be used as specific time delays by loading them with an initial value before allowing them to execute and overflow.

### 31. WHAT IS THE DIFFERENT MODES IN WHICH TIMER 2 CAN OPERATE?

The two different modes in which Timer 2 operates are.

#### i. Capture mode

Timer 2 operates as free running clocks, which saves the timers value on each high to low transition. It can be used for recording bit lengths when receiving Manchester-encoded data.

#### ii. Auto-reload mode:

When the timer overflows, value is written into TH2/TL2 registers from RCA P2H/RCA P2L registers. This feature is used to implement a system watch dog timer.

### 33. WHAT IS THE USE OF A WATCH DOG TIMER?

A watching timer is used to protect an application in case the controlling microcontroller begins to run amok and execute randomly rather than the preprogrammed instructions written for the application.

### 34. DEFINE INTERRUPT.

Interrupt is defined as request that can be refused. If not refused and when an interrupt request is acknowledged, a special set of routine or events are followed to handle the interrupt.

### 35. WHAT ARE THE STEPS FOLLOWED TO SERVICE AN INTERRUPT?

The steps followed are:

- I. Save the context register information.
- II. Reset the hardware requesting the interrupt.
- III. Reset the interrupt controller.
- IV. Process the interrupt.
- V. Restore the context information.
- VI. Return to the previously executing code.

### 36. HOW CAN 8051 BE INTERRUPTED?

There are five different ways to interrupt 8051. Two of these are from external electrical signals. The other three are caused by internal 8051 I/O hardware operations.

### 37. WHAT ARE THE TWO DIFFERENT ELECTRICAL SIGNALS THAT CAUSE AN INTERRUPT?

The two different electrical signals that cause an interrupt are:

- I. Logic – 0 to Logic – 1 change known as transition activated interrupt.
- II. Logic 0, Level activated interrupt.

### 38. GIVE THE FORMAT OF THE INTERRUPT ENABLE REGISTER.

The format of the interrupt enable register is,

EA    -        -        ES    ET1   EX1   ET0   EX0

The register is used to enable or disable all 8051 interrupts and to selectively enable or disable each of the five different interrupts.

EA: Disables all interrupts

Es: Enables or disable the serial port interrupt.

ET1: Enable or disable the timer 1 overflow interrupt.

EX1: Enable or disable external interrupt 1.

ET0: Enable or disable the timer 0 overflow interrupt.

EX0: Enable or disable external interrupt 0.

### 39. WHAT IS MEANT BY NESTING OF INTERRUPTS?

Nesting of interrupts means that interrupts are re-enabled inside an interrupt handler. If another interrupt request codes in, while the first interrupt handler is executing, processor execution will acknowledge the new interrupt and jump to its vector.

### 40. HOW IS THE 8051 SERIAL PORT DIFFERENT FROM OTHER MICRO CONTROLLERS?

The 8051 serial port is a very complex peripheral and able to send data synchronously and asynchronously in a variety of different transmission modes.

### 41. EXPLAIN SYNCHRONOUS DATA TRANSMISSION.

- In synchronous mode (mode 0), the instruction clock is used.
- Data transfer is initiated by writing to the serial data port address.
- Txd pin is used for clock output, while Rxd pin is for data transfer.
- When a character is received, the status of the data transfer is monitored by polling the RI-n bit in serial control register (SCON).

### 46. GIVE AN APPLICATION FOR SYNCHRONOUS SERIAL COMMUNICATION.

An application for synchronous serial communication is RS – 232.

### 47. WHEN IS AN EXTERNAL MEMORY ACCESS GENERATED IN 8051?

In 8051, during execution the data is fetched continuously. Most of the data is executed out of the 8051's built-in control store. When an address is outside the internal control store, an external memory access is generated.

## 48. WHAT IS AN EXTERNAL MEMORY?

External memory is the attachment of RAM or ROM memory to 8051's P0 and P2 ports, giving 8051 additional RAM or application space.

## 49. WHAT IS THE PURPOSE OF CONTROL STORE?

Control store allows external memory to be added to the device using standard byte-wide ROM, PROM and EPROM ports.

## 50. HOW IS THE CODE PROTECTED FROM THE OUTSIDERS?

To protect the code from others, the output data is XORed with the value in a 64-byte portion in EPROM that is used to scramble what is read back after programming.

## 52. WHAT ARE MACROS?

Macros are small routines that are used to replace strings in the program. They can have parameters passed to them, which enhances the functionality of the micro itself.

## 53. HOW ARE CONSTANTS DECLARED?

Constants are declared in the same way as variables, using the format:

Const – Label EQU 012h

When the constant's label is encountered, the constant numeric value is exchanged for the string.

## 54. WRITE AN ASSEMBLY LANGUAGE PROGRAM FOR A 16-BIT INCREMENT AND WILL NOT AFFECT THE CONTENTS OF THE ACCUMULATOR.

```
MACRO inc16 variable      ; Increment two bytes starting at "variable"
Local INC16 End
INC variable              ; Increment the low 8 bits
PUSH ACC
MOV A variable            ; Are the incremented low 8 bits = 0?
JNZ INC 16 End
INC variable + 1
Inc16 End                 ; Yes – increment the upper 8 bits
POP ACC
END MAC
```



55. WHAT WILL HAPPEN IF A LABEL WITHIN A MACRO IS NOT DECLARED LOCAL?

If a label within a macro is not declared local, then at assembly time, there will be two types of errors:

- I. The first will state that there are multiple labels in the source.
- II. The second will indicate that jump instructions don't know which one to use.

56. WRITE AN ASSEMBLY LANGUAGE PROGRAM TO LOAD THE ACCUMULATOR WITH A CONSTANT VALUE.

```
MACRO invert value
    if (value==0)
        MOV A, #1
    else
        clr A
    end if
END MAC.
```

56. WHERE CAN A SUBROUTINE BE LOCATED?

The subroutine can be located after the interrupt handlers or between variable initialization and the mainline code. The location of the subroutine is location of the subroutine is largely arbitrary.

57. WHAT ARE CONDITIONAL ASSEMBLY STATEMENTS?

Conditional assembly statements are "if / else / end if" statements that execute during assembly and depending on the conditions, they will not allow certain sections of code to be assembled.

58. WHAT IS THE PURPOSE OF INTERPRETERS AND COMPILERS?

Interpreters and compilers convert high-level language statements directly into processor instructions without the programmer being involved.

59. GIVE FEW APPLICATIONS OF 16 BIT MICROCONTROLLERS?

They are used in the field of:

- I. Closed – loop control.
- II. Modems
- III. Printers
- IV. Disk drives
- V. Medical instrumentation.

60. WHAT IS THE DIFFERENCE BETWEEN THE MICROPROCESSOR AND MICROCONTROLLER?

Microprocessor does not contain RAM, ROM and I/O ports on the chip. But a microcontroller contains RAM, ROM and I/O ports and a timer all on a single chip.

61. WHAT ARE ADDRESSING MODES?

The various ways of accessing data are called addressing modes.

62. LIST THE FIVE ADDRESSING MODES OF 8051 MICROCONTROLLER.

The five addressing modes are,

- I. Immediate addressing
- II. Register addressing
- III. Direct addressing
- IV. Register indirect addressing
  - a. Indexed addressing.

63. EXPLAIN THE IMMEDIATE ADDRESSING MODE.

In immediate addressing mode, the source operand is constant. In this mode, as the name implies, when the instruction is assembled, the operand comes immediately after the opcode.

MOV A, #25H ; load 25H into A

64. EXPLAIN THE REGISTER ADDRESSING MODE.

Register addressing mode involves the use of register to hold data to be manipulated.

Examples of register addressing mode is as follows:

MOV A, R0; Copy the contents of R0 into A.

MOV R2, A; Copy the contents of A into R2.

65. MOV R4, R7 IS INVALID. WHY?

The movement of data between the accumulator and Rn (for n = 0 to 7) is valid. But movement of data between Rn register is not allowed. That is why MOV R4, R7 is invalid.

66. WHAT IS SFR?

In the 8051 microcontroller registers A, B, PSW and DPTR are part of the group of registers commonly referred to as special function registers (SFR).

67. WHAT ARE THE TWO MAIN FEATURES OF SFR ADDRESSES?

The following two points should be noted SFR addresses.

I. The special function registers have addresses between 80H and FFH. These addresses are above 80H, since the addresses 00 to 7FH are addresses of RAM memory inside the 8051.

II. Not all the address space of 80 to FH is used by the SFR. The unused locations 80H to FFH are reserved and must not be used by the 8051 programmer.

68. WRITE CODE TO SEND 55H TO PORTS P1 AND P2 USING

I. THEIR NAMES

II. THEIR ADDRESSES.

```

I.  MOV A, #55H           ; A = 55H
    MOV P1, A             ; P1 = 55H
    MOV P2, A             ; P2 = 55H
II. P1 address = 80H     ; P2 address = A0H
    MOV A, #55H           ; A = 55H
    MOV 80H, A            ; P1 = 55H
    MOV 0A0H, A           ; P2 = 55H.

```

69. WHAT IS THE MAIN ADVANTAGE OF REGISTER INDIRECT ADDRESSING MODE?

The main advantage of register indirect addressing mode is that it makes addressing data dynamic rather than static as in the case of direct addressing mode.

70. WHAT IS THE DIFFERENCE BETWEEN DIRECT AND REGISTER INDIRECT ADDRESSING MODE?

Loop is most efficient and is possible only in register indirect addressing whereas looping is not direct addressing mode.

71. WHAT ARE UNSIGNED NUMBERS?

Unsigned numbers are defined as data in which all the bits are used to represent data, and no bit is set aside for the positive or negative sign.

72. LIST SOME LOGICAL INSTRUCTIONS.

The logical instructions are:

- a. AND
- b. OR
- c. XOR
- d. CPL A

## 73. LIST OUT SOME COMPARE INSTRUCTIONS.

The compare instructions are:

- a. CJNE
- b. CLR
- c. CPL

## 74. WRITE A PROGRAM TO SAVE THE ACCUMULATOR IN R7 OF BANK 2.

```
CLR PSW - 3
SETB PSW - 4
MOV R7, A.
```

## 75. WHAT ARE SINGLE BIT INSTRUCTIONS? GIVE EXAMPLE.

Instructions that are used for single bit operation are called single bit instructions.

Examples: SETB bit  
CLR bit  
CPL bit

## 76. WRITE A PROGRAM TO SAVE THE STATUS OF BITS P1.2 AND P1.3 ON RAM BIT LOCATIONS 6 AND 7 RESPECTIVELY.

```
MOV C, P1.2      ; save status of P1.2 on CY
MOV 06, C        ; save carry in RAM bit location 06
MOV C, p1.3      ; save status of p1.3 on CY
MOV 07, C        ; save carry in RAM bit location 07.
```

## 77. WRITE A PROGRAM TO SEE IF BITS 0 AND 5 OF REGISTER B R1. IF THEY ARE NOT, MAKE THEM SO AND SAVE IT IN R0.

```
JNB OF0H, NEXT - 1 ; JUMP if B.0 is low
SET BOFOH           ; Make bit B.0 high
NEXT - 1: JNB OF5H, NEXT - 2 ; JUMP if B.5 is low
SETB OF5H           ; Make B.5 high
NEXT - 2: MOV R0, B ; Save register B.
```

## 79. GIVE THE PRIORITY LEVEL OF THE INTERRUPT SOURCES.

Interrupt source      Priority within a level

IE0 (External INT0 )

TF0(Timer 0)

IE 1 (External INT 1)

TF 1 (Timer 1)

RI = TI (Serial port)      Highest

.

.

.

Lowest

80. DIFFERENTIATE BETWEEN EDGE -SENSITIVE AND LEVEL-SENSITIVE PROGRAMMING OF INTERRUPTS.

EDGE – SENSITIVE LEVEL – SENSITIVE

I. When the interrupts are programmed as edge-sensitive the flags are automatically cleared after the control is transferred to the respective vector.

II. The interrupts should remain high for atleast one machine cycle and low for atleast one machine cycle, for being sensed. I. When the interrupts are programmed as level-sensitive, the flags are controlled by the external internal interrupt sources themselves.

II. The interrupts should remain high for atleast two machine cycles for being sensed.

**Part B – (16 Marks)**

1. Draw & explain the architecture of 8085 microprocessor
  - Block Diagram
  - Registers Available
  - Function Of Accumulator
  - Explanation about all blocks in the block diagram
2. Draw the Pin Diagram of 8085 and explain the function of various signals.
  - Pin Diagram
  - Explanation about all signals
3. Explain the instruction classification & instruction sets
  - Data Transfer Instructions
  - Arithmetic Instructions
  - Logical Instructions
  - Branch Instructions
  - Machine Control Instructions
4. Write a program to sort the numbers in ascending and descending order.
  - Program
  - Result Verification
5. Draw the timing diagram of the following Instructions
  - PUSH
  - IN Port A
  - STA 5000
  - MVI A, 08
  - Explain the machine cycles needed for every Instructions and draw the timing diagram
6. Explain the 8085 based microcomputer system
7. With neat sketch explain the functions of 8255 PPI.
  - Block Diagram
  - Explanation about all the ports available.
  - Explanation about the modes of transfer
  - Explain the control Word Register
8. With neat sketch explain the functions of 8251.
  - Block Diagram
  - Types of data transfer
  - Explanation about all the blocks.
  - Explain the control Word Register, Status Register
9. With neat sketch explain the function of DMA controller.
  - Block Diagram
  - Explanation about all blocks in the block diagram

10. With neat sketch explain the function of Programmable Interrupt Controller.
  - Block Diagram
  - Explanation about all blocks in the block diagram
11. With neat sketch explain the function of Keyboard and display controller.
  - Block Diagram
  - Types of Display Available
  - Types of keys available
  - Explanation about all blocks in the block diagram
12. With neat sketch explain the function of A/D converter.
  - Fundamental steps
  - Figure
  - Explain the functions.
13. With neat sketch explain the function of D/A converter.
  - Fundamental steps
  - Figure
  - Explain the functions.
14. With neat sketch explain the architecture of 8051 microcontroller.
  - Block Diagram
  - Explanation about all blocks in the block diagram
15. Draw the Pin Diagram of 8051 and explain the function of various signals.
  - Pin Diagram
  - Explanation about all signals
16. List the various Instructions available in 8051 microcontroller.
  - Data Transfer Instructions
  - Arithmetic Instructions
  - Logical Instructions
  - Boolean variable Manipulation Instructions
  - Program and Machine Control Instructions