



COE/EE152: Basic Electronics

Lecture 6 Andrew Selasi Agbemenu

<https://sites.google.com/site/agbemenu/courses/ee-coe-152>



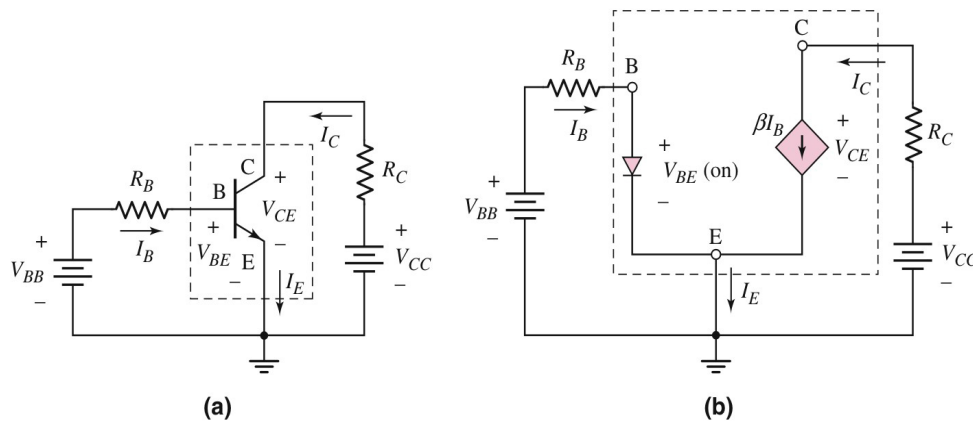
Outline

- Load Line Analysis and Operating Point Determination
- Small Signal Model



Load Line Analysis

- Consider the DC equivalent circuit for npn common emitter configuration shown



Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.



Load Line Analysis

- Input Load Line equation
 - Obtained by solving KVL for the input loop

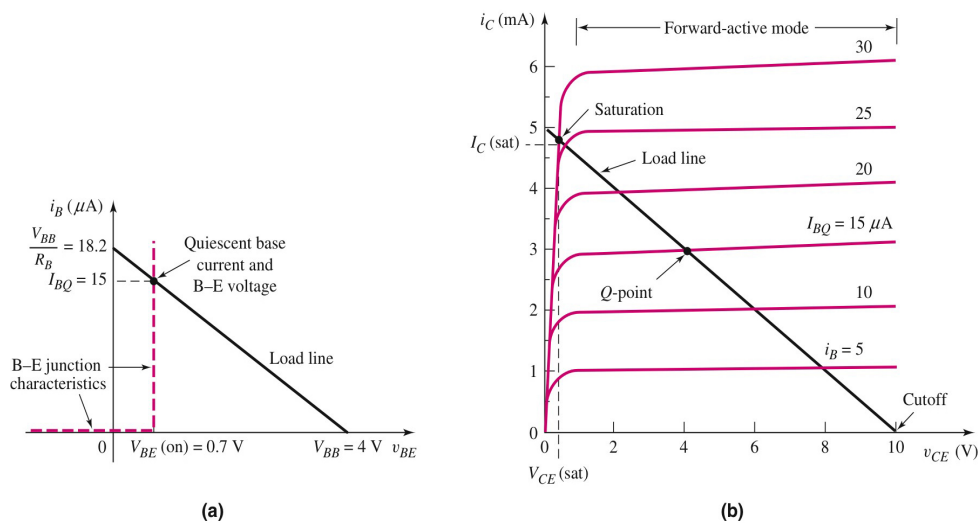
$$V_{BB} = i_B R_B + V_{BE}$$

- Output Load Line equation
 - Obtained by solving KVL for the output loop

$$V_{CC} = i_C R_C + V_{CE}$$



Load Line Analysis



Load line drawn on (a) input characteristics (b) output characteristics for CE configuration



Problem Solving Technique: BJT Biasing

- Determine the transistor operating mode which will be dependent on the application. e.g assume forward active mode
 - $V_{BE} = V_{BE(on)}$, $I_B > 0$, & $I_C = \beta I_B$
- Analyze 'linear' circuit.
 - The goal is to establish the Q-point which establishes initial operating region of the transistor
 - The Q-point controls the *diffusion capacitance*, *transconductance*, *input* and *output resistances*
 - *The Q-point is represented by (I_C, V_{CE}) for an npn transistor or (I_C, V_{EC}) for a pnp transistor.*

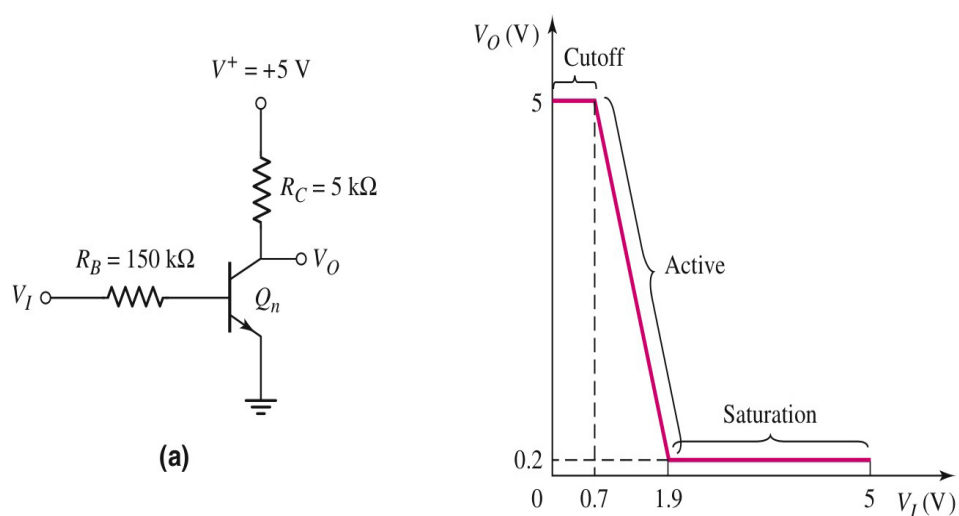


Problem Solving Technique: BJT Biasing

- Evaluate the resulting state of transistor.
 - If $V_{CE} > V_{CE}(\text{sat})$, assumption is correct
 - If $I_B < 0$, transistor likely in cutoff
 - If $V_{CE} < 0$, transistor likely in saturation
- If initial assumption is incorrect, make new assumption and return to Step 2.



Voltage Transfer Characteristics for npn circuit

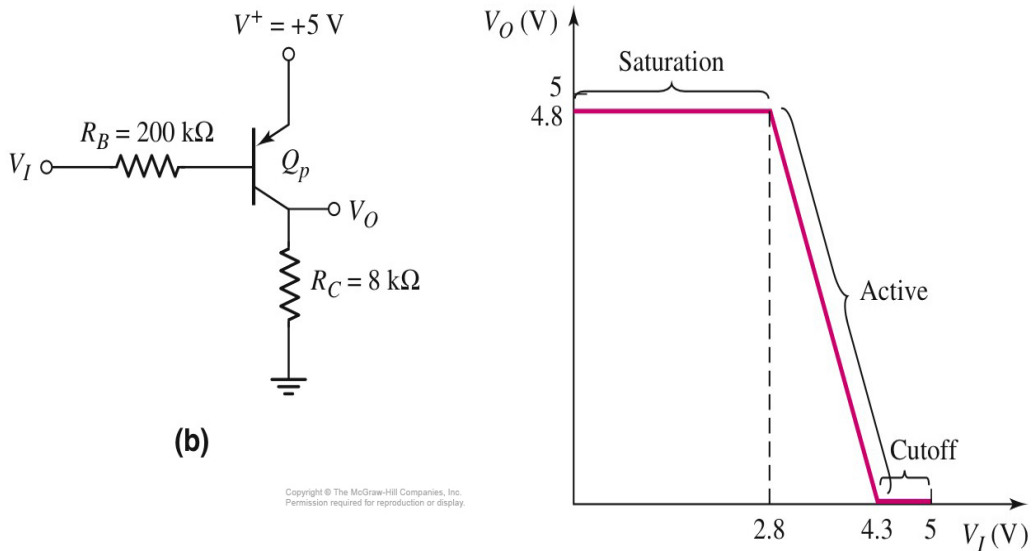


Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.

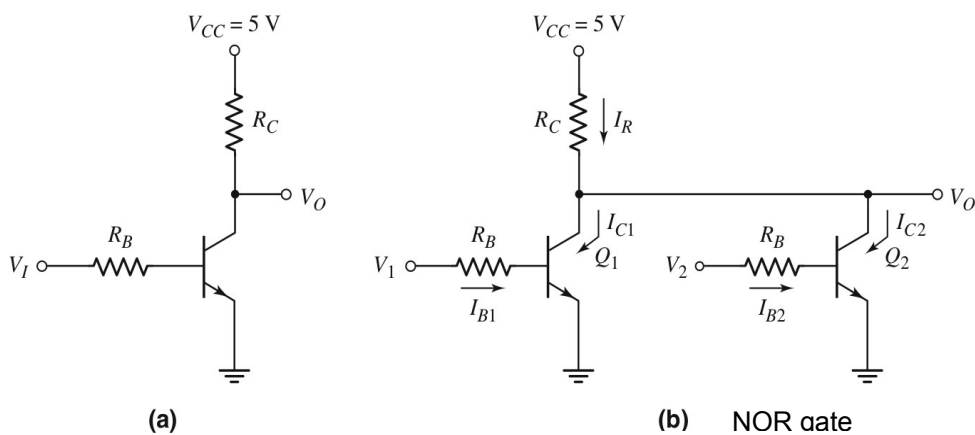
$$V_1 = I_B R_B + V_{BE}$$
$$V_0 = V_{CE} = V^+ - I_C R_C$$



Voltage Transfer Characteristics for pnp circuit



Digital Logic: Transistor biased to work in Cutoff and Saturation Regions



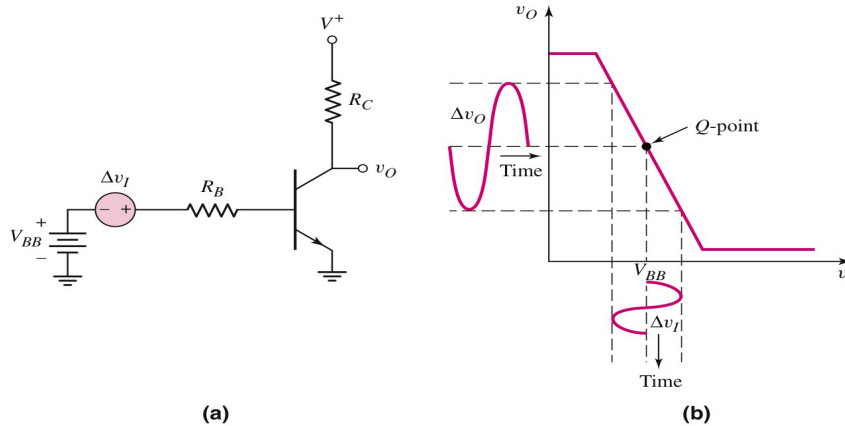
Copyright © The McGraw-Hill Companies, Inc. Permission required for reproduction or display.

V_1	V_0
ON	OFF
OFF	ON

V_1	V_2	V_0
ON	ON	OFF
ON	OFF	OFF
OFF	ON	OFF
OFF	OFF	ON



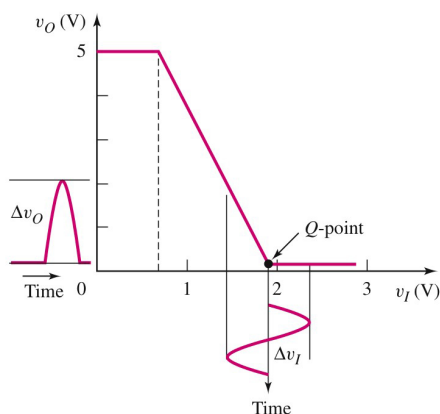
Amplifier: Transistor biased to work in the Forward Active Region



By choosing the right values of R_B and R_C , the Q-point is the middle as desired
The transistor amplifies the whole signal



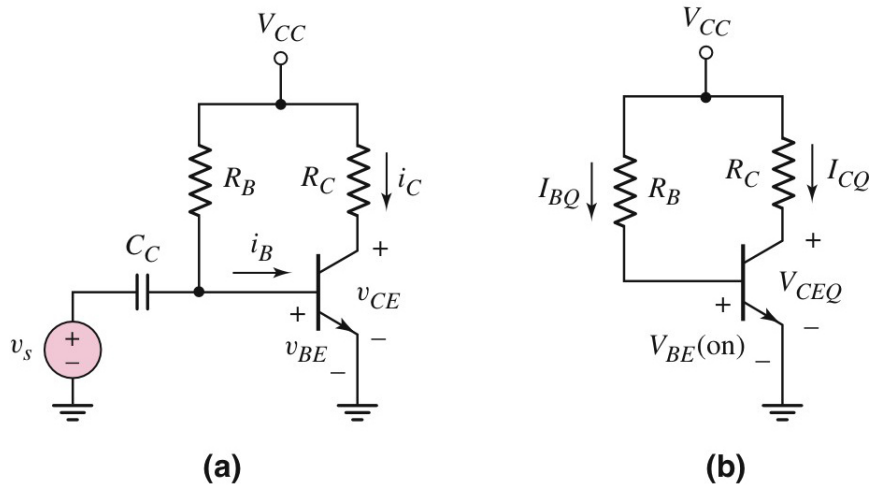
Effects of Improper Biasing



- The Q-point is not chosen in the middle of transfer characteristics
- Part of the signal moves into the cutoff or saturation regions where it is cut at zero or cut at V_{DD}



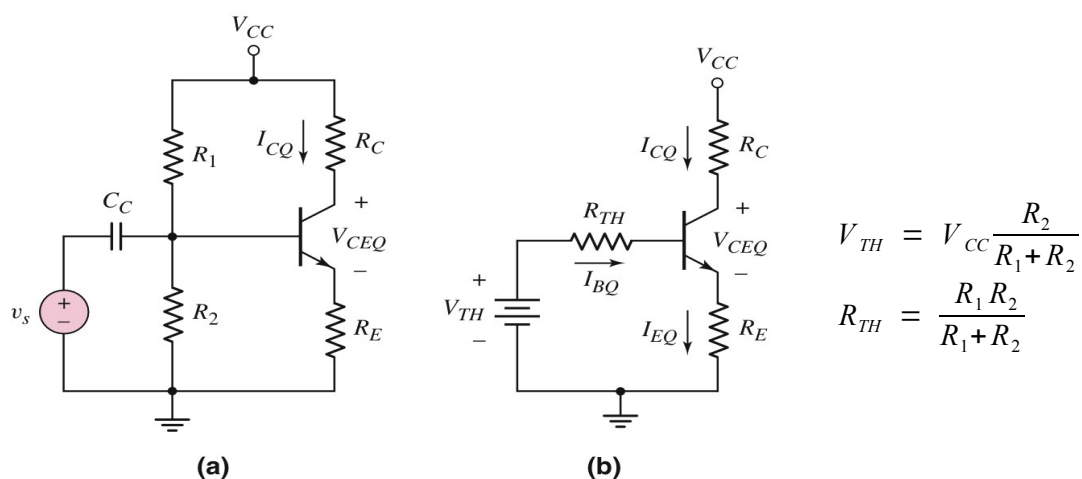
Single Base Resistor Biasing



Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.



Four Resistor or Voltage Divider Biasing

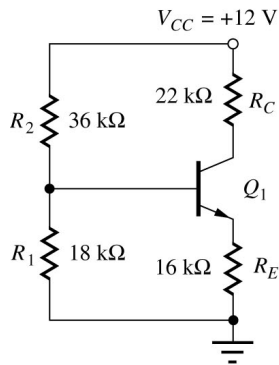


Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.

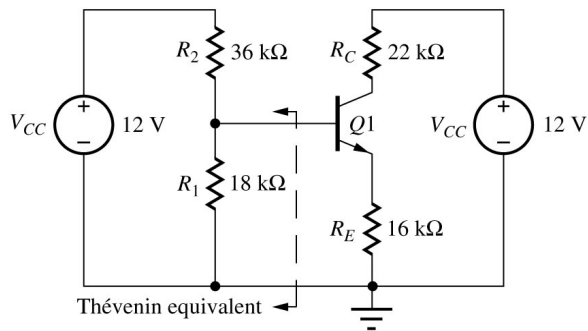


Example: Four-Resistor Bias Network

Copyright © The McGraw-Hill Companies, Inc. Permission required for reproduction or display.



(a)



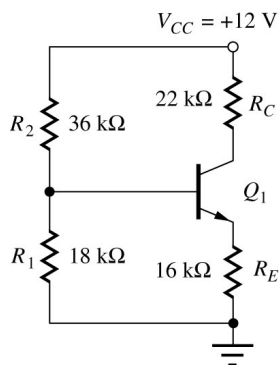
(b)

First find Thevenin Equivalent of the circuit

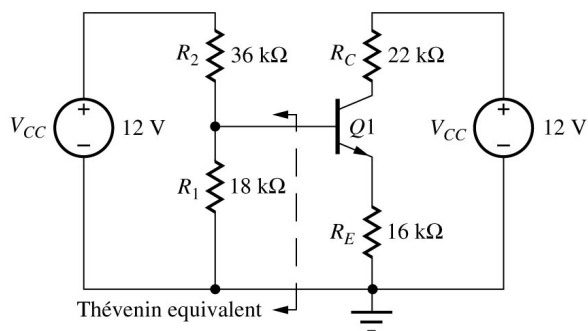


Example: Four-Resistor Bias Network

Copyright © The McGraw-Hill Companies, Inc. Permission required for reproduction or display.



(a)



(b)

First find Thevenin Equivalent of the circuit



Four-Resistor Bias Network

Thevenin Equivalent of Base Bias Network

$$V_{TH} = V_{CC} \frac{R_1}{R_1 + R_2}$$

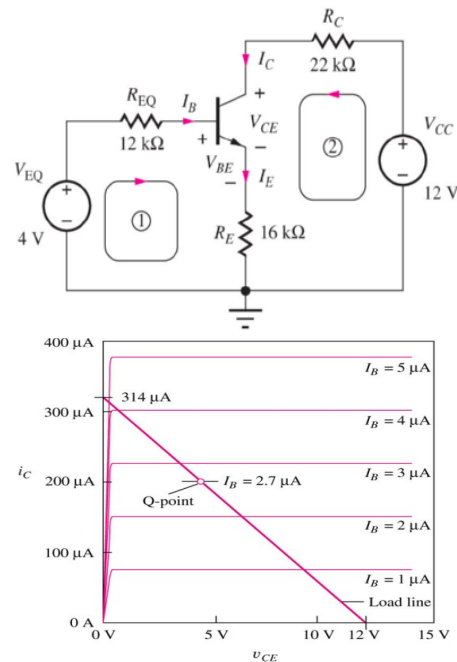
$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

Frm Diagram :

$$R_{TH} = R_{EQ}$$

$$V_{TH} = V_{EQ}$$

Now determine Load Line equation
And plot on characteristic curve



Four-Resistor Bias Network: Solution

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$

for $\beta = 75$

$$I_B = 2.29 \mu A$$

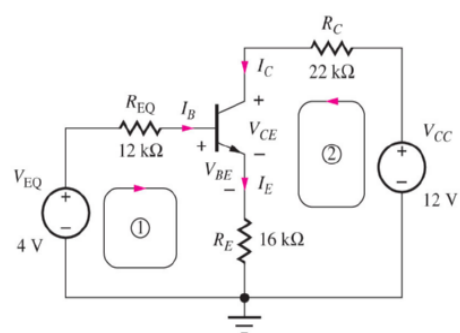
$$I_C = \beta I_B \approx 202 \mu A$$

$$I_E = (\beta + 1) I_B \approx 204 \mu A$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 4.29 V$$

Q point is (202 μA, 4.29 V)

⇒ Forward active region is correct





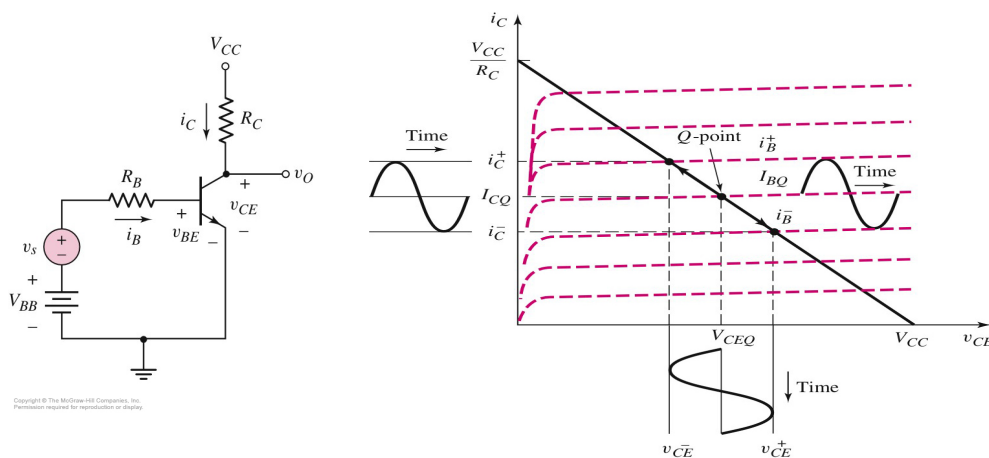
Four-Resistor Bias Network: Circuit Design

- **Problem:** Design 4-resistor bias circuit with given parameters.
- **Given data:** $I_C = 750 \mu\text{A}$, $\beta = 100$, $V_{CC} = 15 \text{ V}$, $V_{CE} = 5 \text{ V}$
- **Assumptions:** Forward-active operation region, $V_{BE} = 0.7 \text{ V}$
- **Analysis:** Divide $(V_{CC} - V_{CE})$ equally between R_E and R_C . Thus, $V_E = 5 \text{ V}$ and $V_C = 10 \text{ V}$; Choose nearest 5% resistor values.



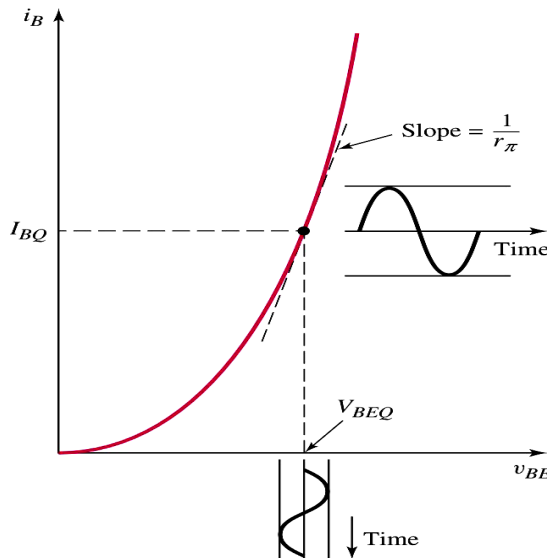
BJT Small Signal Model

- We want to investigate how a transistor circuit can amplify a small, time-varying signal.





I_B Versus V_{BE} Characteristic of Transistor with Small Signal



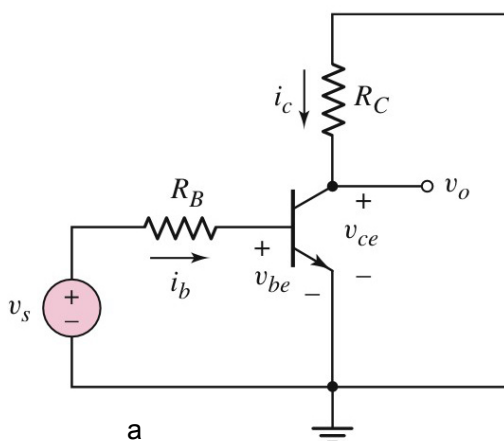
$$i_B \cong I_{BQ} \left(1 + \frac{v_{be}}{V_T}\right) = I_B + i_b$$

Base current varies around the Q-point current with small signal input to a well biased transistor

Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.



Small-Signal Equivalent Circuit



Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.

- After finding the DC operating point values
- Take out the DC sources as shown in (a) – the ac equivalent circuit



Small-Signal Hybrid π Model for npn BJT

Transconductance :

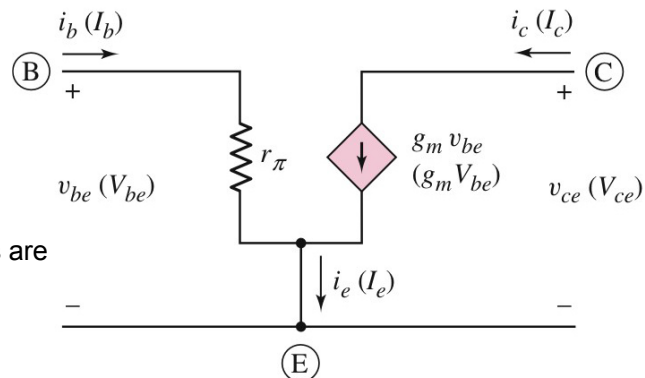
$$g_m = \frac{I_{CQ}}{V_T}, \text{ where } I_{CQ} \text{ is } Q\text{-point current}$$

Diffusion (emitter – base) resistance :

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m r_\pi = \beta$$

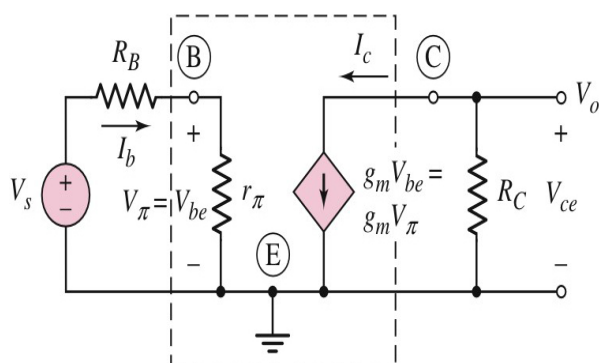
Phasor (magnitude and angle) signals are shown in parenthesis



Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.



Small-Signal Voltage Gain, A_v



Copyright © The McGraw-Hill Companies, Inc.
Permission required for reproduction or display.

From output portion of circuit :

$$V_o = V_{CE} = -(g_m V_\pi) R_C$$

From input portion of circuit :

$$V_s = \left(\frac{r_\pi + R_B}{r_\pi} \right) V_\pi$$

Small – Signal Voltage Gain :

$$A_v = \frac{V_o}{V_s} = -(g_m R_C) \cdot \left(\frac{r_\pi}{r_\pi + R_B} \right)$$






Problem-Solving Technique: BJT AC Analysis

- Analyze circuit with only dc sources to find Q point.
- Replace each element in circuit with small-signal model, including the hybrid π model for the transistor.
- Analyze the small-signal equivalent circuit after setting dc source components to zero.

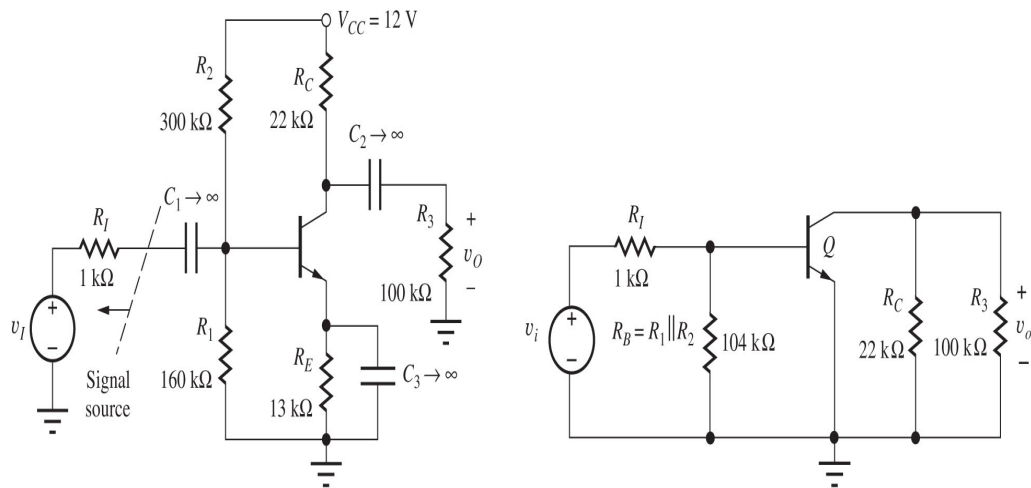


Element Transformation

Element	DC Model	AC Model
Resistor	R	R
Capacitor	Open	C
Inductor	Short	L
Diode	$+V_{\gamma}, r_f -$ 	$r_d = nV_T/I_D$
Independent Constant Voltage Source	$+ V_s -$ 	Short
Independent Constant Current Source	I_s 	Open



Example



“Everything should be made as simple as possible, but not simpler.”

Albert Einstein

