Transistor
DC Biasing Circuits

Pictures are redrawn (with some modifications) from
Introductory Electronic Devices and Circuits

Objectives

- State the purpose of dc biasing circuits.
- Plot the dc load line given the value of V_{CC} and the total collector-emitter circuit resistance.
- Describe the Q-point of an amplifier.
- Describe and analyze the operations of various bias circuits:
  - base-bias circuits
  - voltage-divider bias circuits
  - emitter-bias circuits
  - collector-feedback bias circuits
  - emitter-feedback bias circuits

Transistor Biasing

The basic function of transistor is amplification. The process of raising the strength of weak signal without any change in its general shape is referred as faithful amplification. For faithful amplification it is essential that:-

1. Emitter-Base junction is forward biased
2. Collector- Base junction is reversed biased
3. Proper zero signal collector current

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is called transistor biasing.

WHY BIASING?

If the transistor is not biased properly, it would work inefficiently and produce distortion in output signal.

HOW A TRANSISTOR CAN BE BIASED?

A transistor is biased either with the help of battery or associating a circuit with the transistor. The later method is more efficient and is frequently used. The circuit used for transistor biasing is called the biasing circuit.

BIAS STABILITY

❖ Through proper biasing, a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained. It is desired that once selected the operating point should remain stable. The maintenance of operating point stable is called Stabilisation.

❖ The selection of a proper quiescent point generally depends on the following factors:

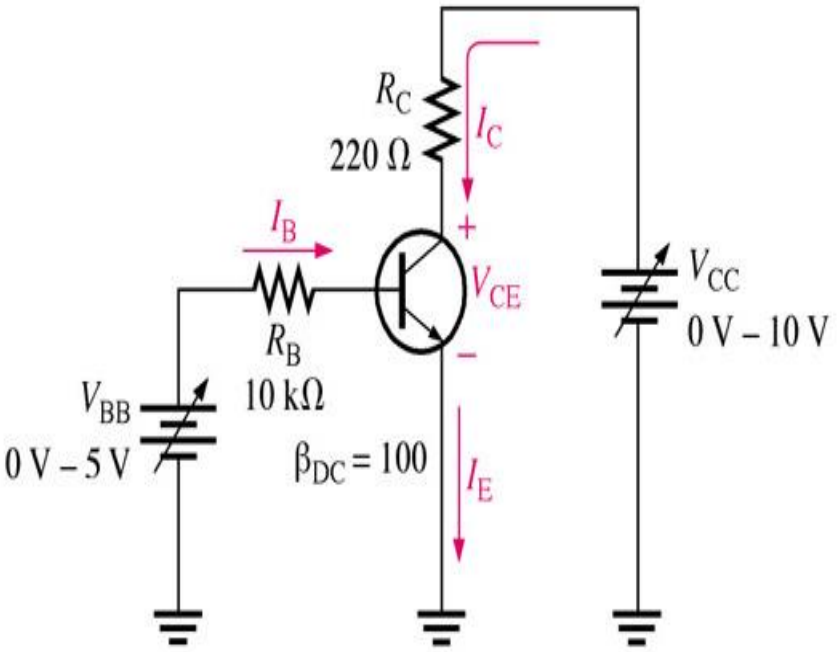
(a) The amplitude of the signal to be handled by the amplifier and distortion level in signal

(b) The load to which the amplifier is to work for a corresponding supply voltage

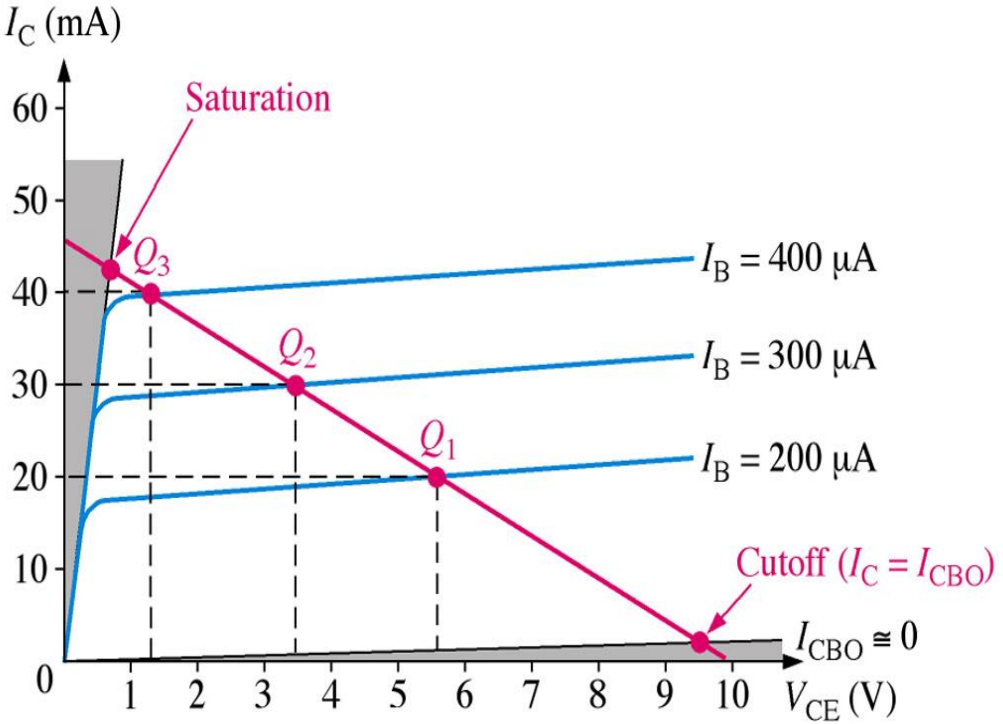
❖ The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters — *β, I_{CO} and V_{BE} (where the symbols carry their usual meaning)—are functions of* temperature.

The DC Operating Point

For a transistor circuit to amplify it must be properly biased with dc voltages. The dc operating point between saturation and cutoff is called the **Q-point.** The goal is to set the Q-point such that that it does not go into saturation or cutoff when an a ac signal is applied.



(a) DC biased circuit



Requirements of biasing network

- Ensuring proper zero signal collector current.
- Ensuring V_{CE} not falling below 0.5V for Ge transistor and 1V for Silicon transistor at any instant.
- Ensuring Stabilization of operating point. (zero signal I_C and V_{CE})

The Thermal Stability of Operating Point (S_{Ico})

❖**Stability Factor *S*:-** The stability factor *S, as the change of collector current with respect to the reverse saturation* current, keeping β *and VBE constant. This can be written as:*

The Thermal Stability Factor : S_{Ico}

$$S_{Ico} = \left.\frac{\partial I_c}{\partial I_{co}}\right|_{V_{be},\ \beta}$$

This equation signifies that I_c Changes S_{Ico} times as fast as I_{co}

Differentiating the equation of Collector Current $I_C = (1+\beta)Ico + \beta I_b$ & rearranging the terms we can write

$$S_{Ico} = \frac{1+\beta}{1-\beta\,(\partial I_b/\partial I_C)}$$

It may be noted that Lower is the value of S_{Ico} better is the stability

Various Biasing Circuits

- **Fixed Bias Circuit**
- **Fixed Bias with Emitter Resistor**
- **Collector to Base Bias Circuit**
- **Potential Divider Bias Circuit**

Fig 7.1 Typical amplifier operation.

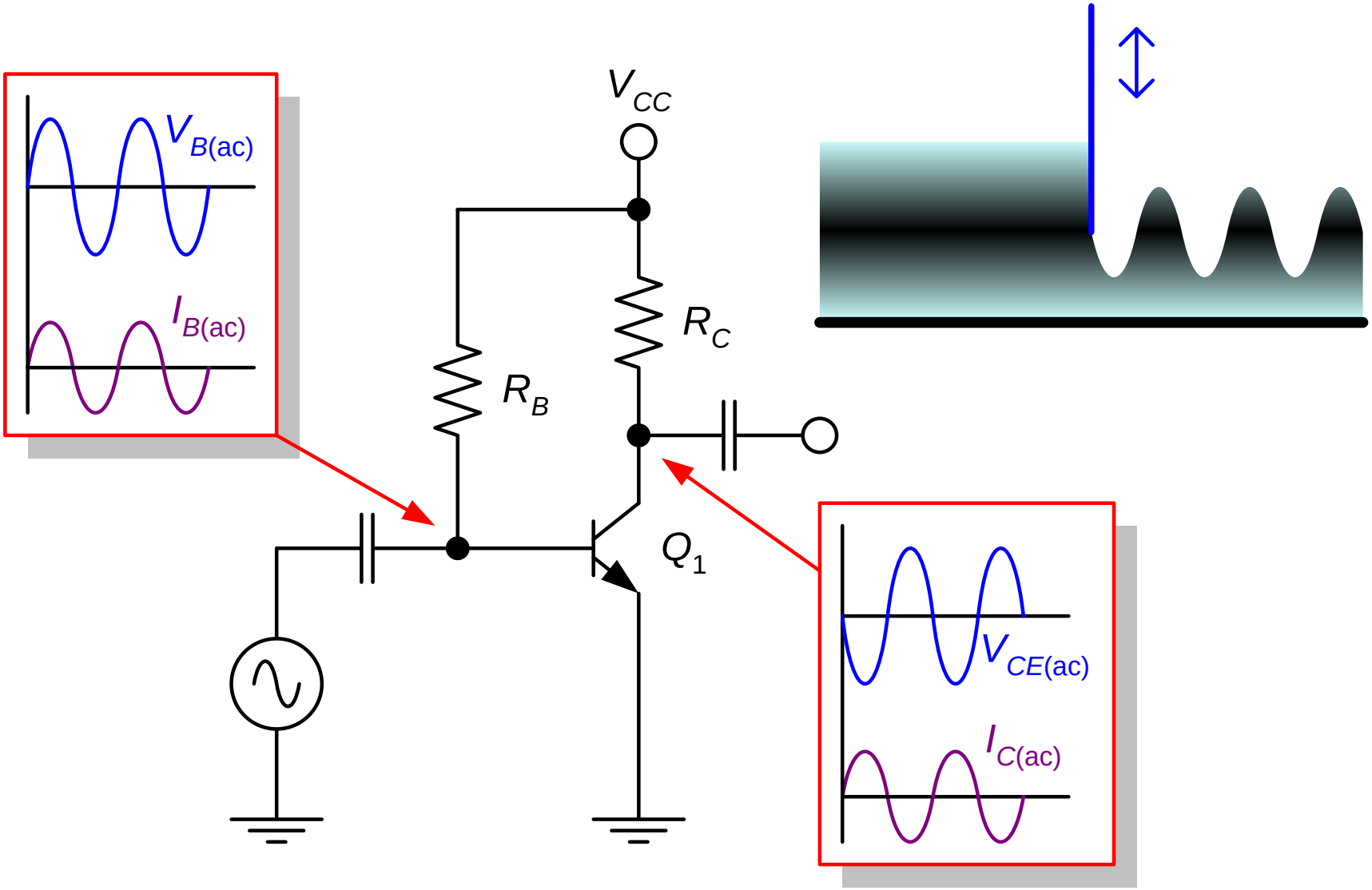


Fig 7.2 A generic dc load line.

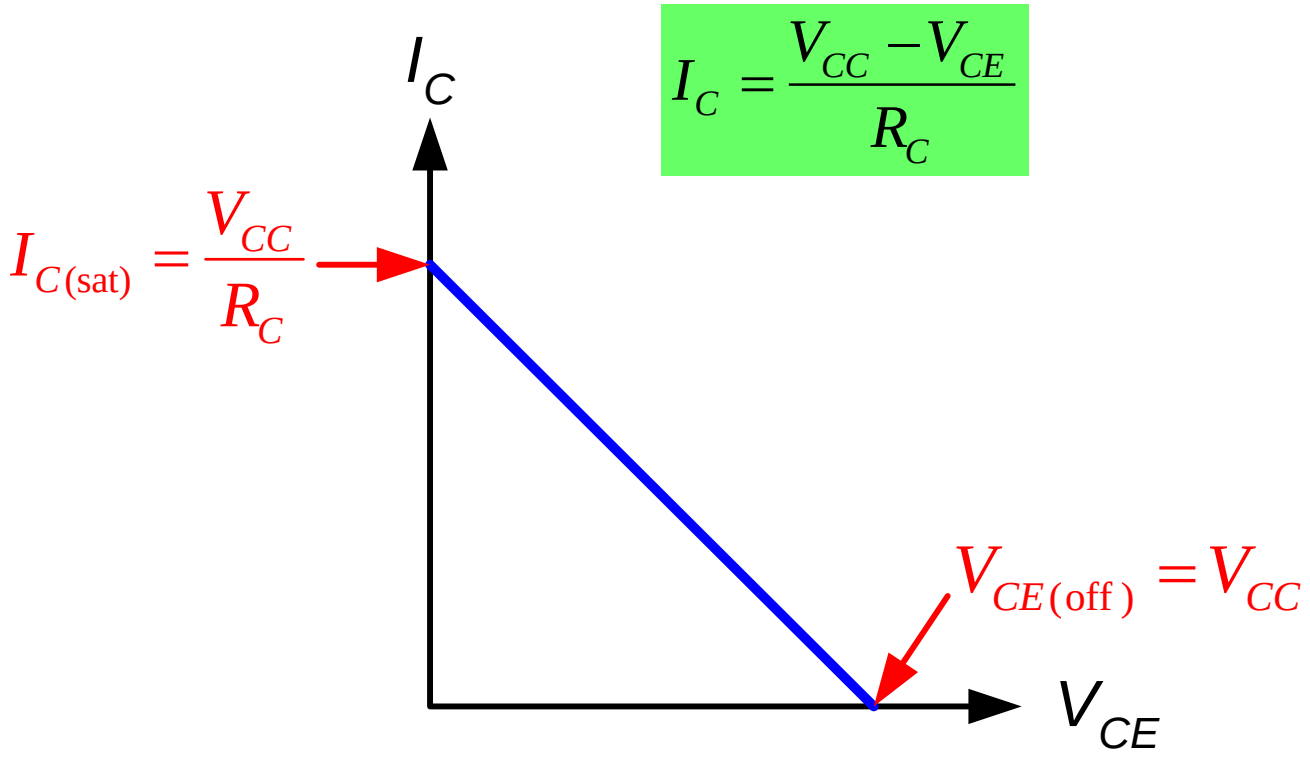
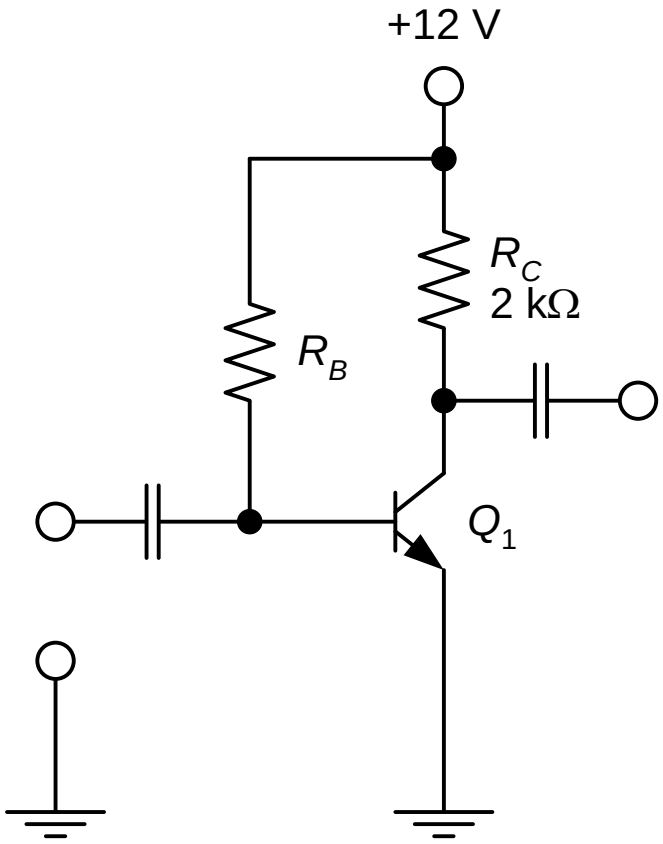


Fig 7.3 Example 7.1.

Plot the dc load line for the circuit shown in Fig. 7.3a.



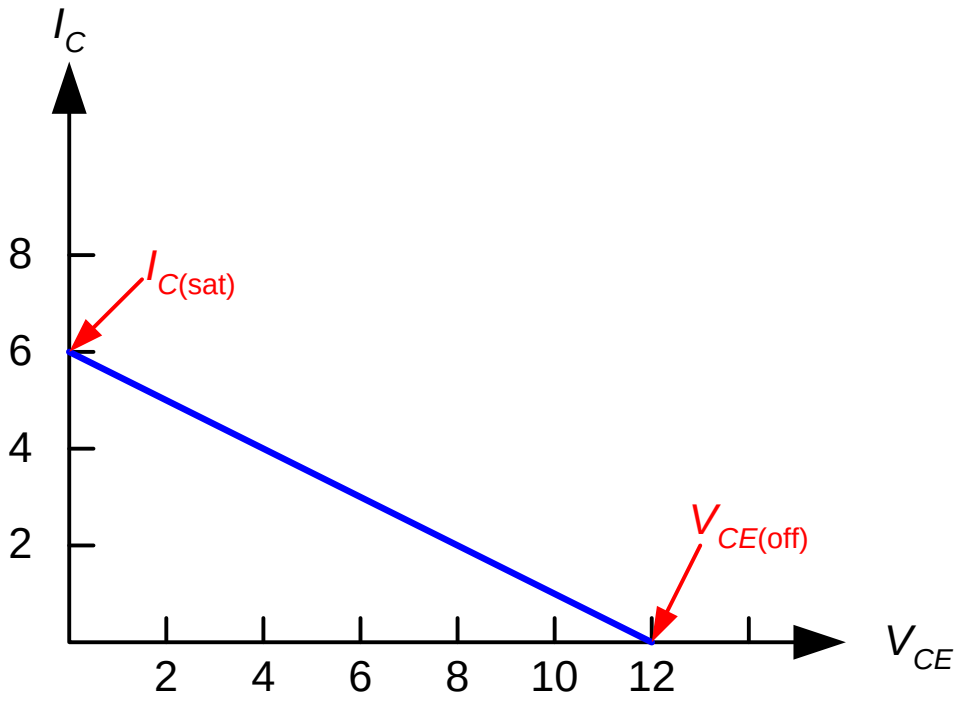
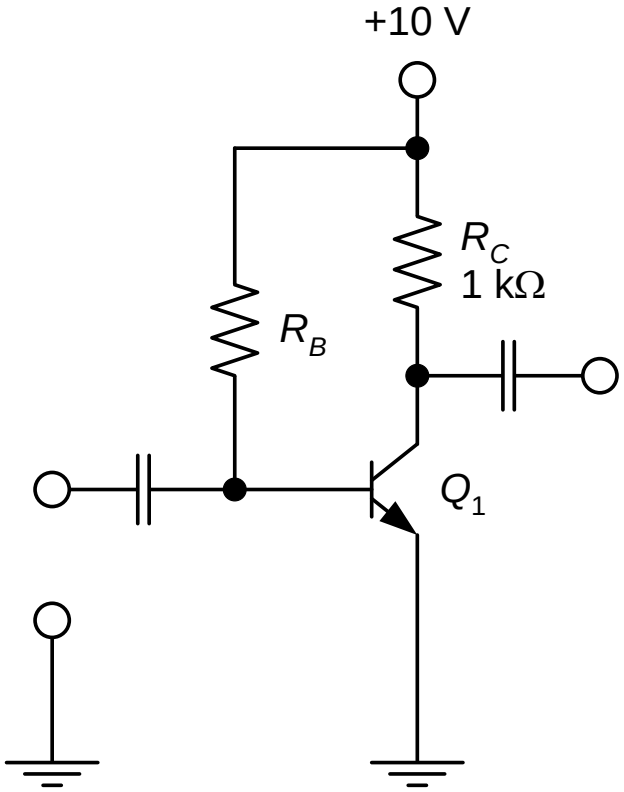
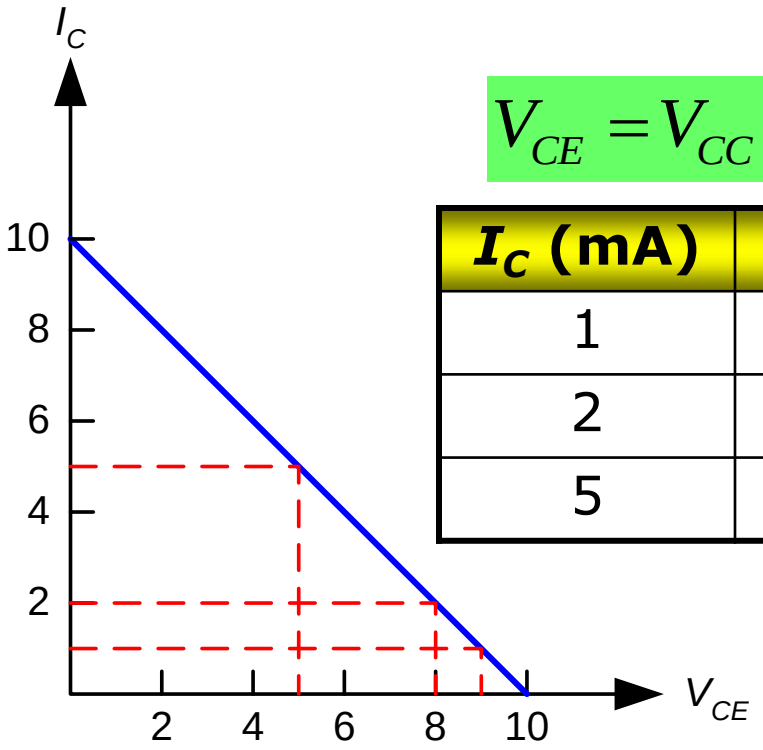


Fig 7.4 Example 7.2.

Plot the dc load line for the circuit shown in Fig. 7.4. Then, find the values of V_{CE} for I_C = 1, 2, 5 mA respectively.





$$V_{CE} = V_{CC} - I_C R_C$$

I_C (mA)	V_{CE} (V)
1	9
2	8
5	5

Fig 7.6-8 Optimum Q-point with amplifier operation.

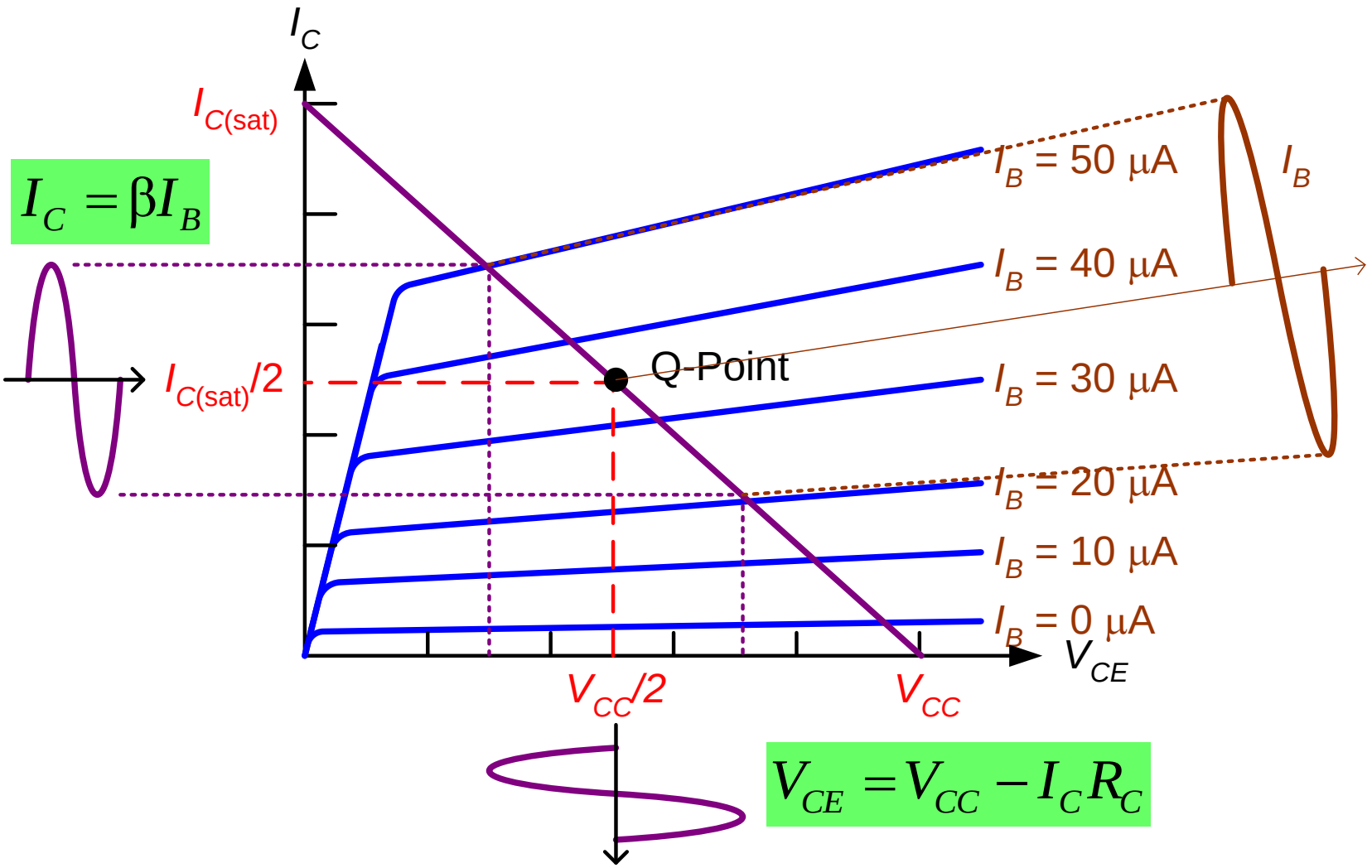
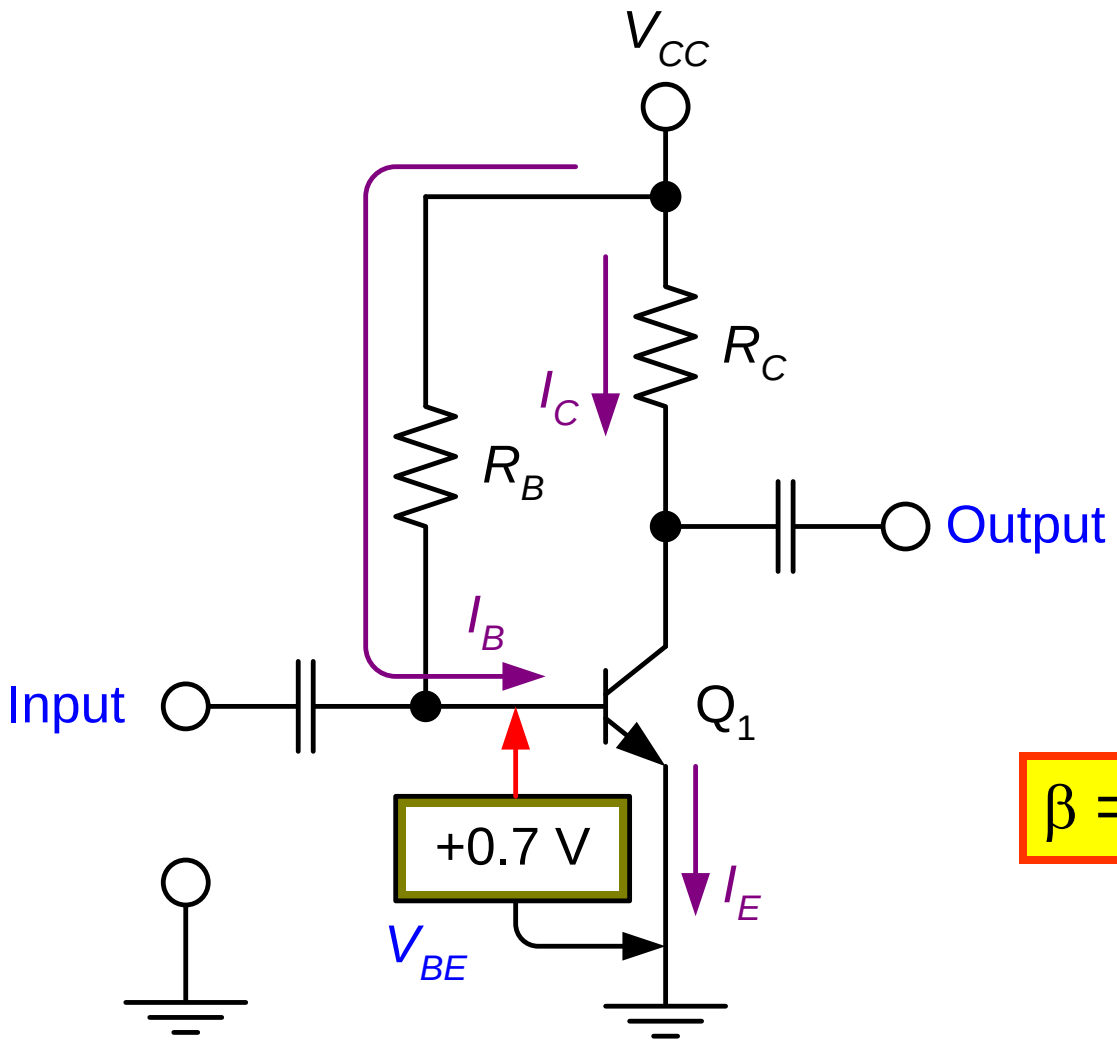


Fig 7.9 Base bias (fixed bias).



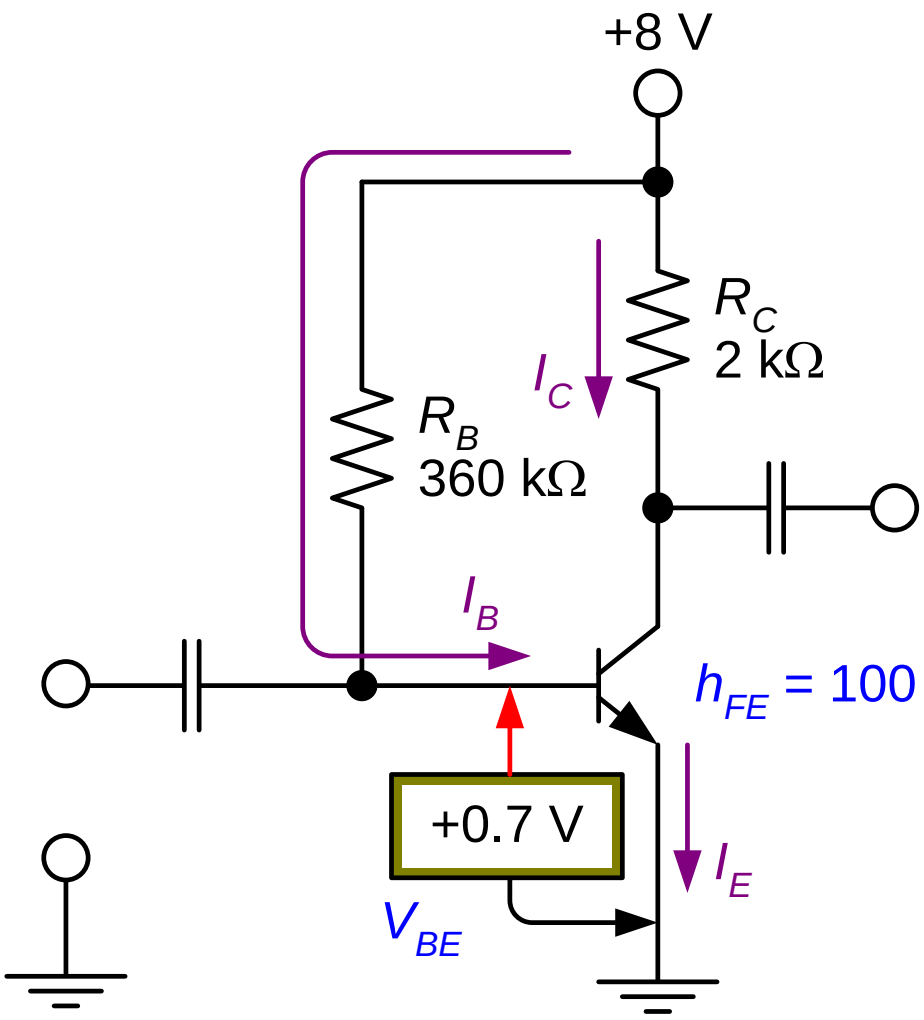
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

β = dc current gain = h_{FE}

Fig 7.10 Example 7.3.



$$I_B = \frac{V_{CC} - 0.7\text{V}}{R_B} = \frac{8\text{V} - 0.7\text{V}}{360\text{k}\Omega}$$
$$= 20.28\mu\text{A}$$

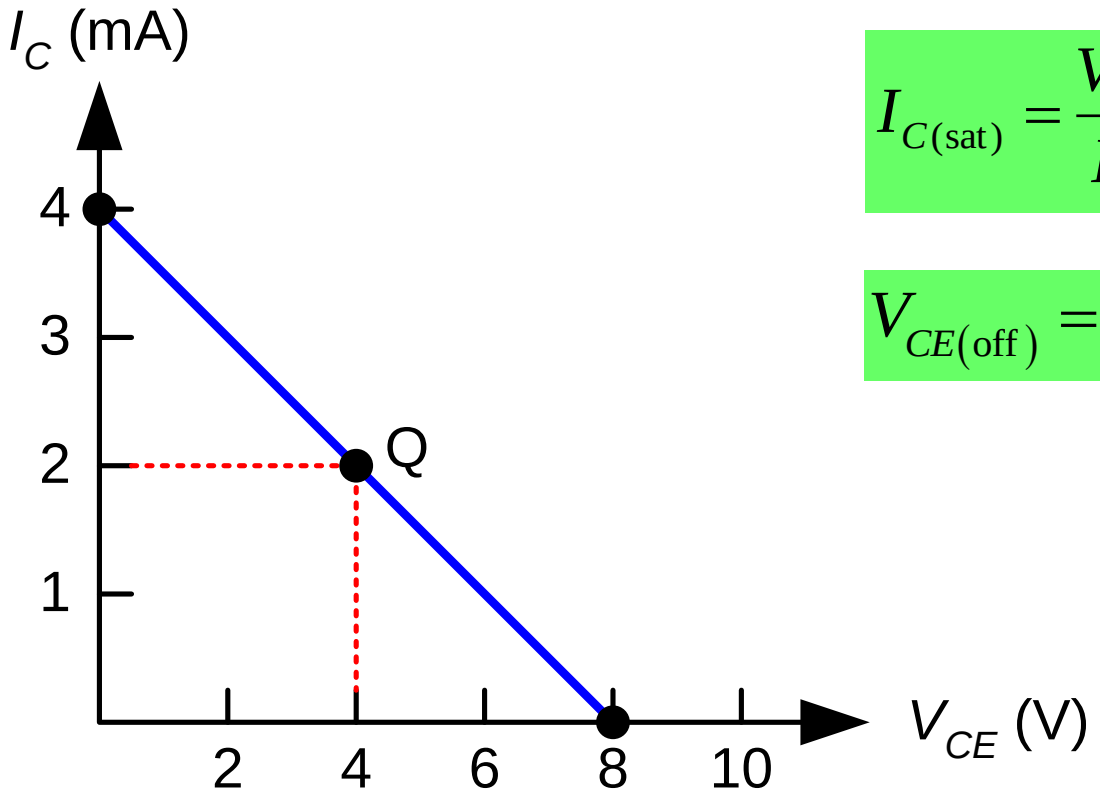
$$I_C = h_{FE} I_B = (100)(20.28\mu\text{A})$$
$$= 2.028\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 8\text{V} - (2.028\text{mA})(2\text{k}\Omega)$$
$$= 3.94\text{V}$$

The circuit is midpoint biased.

Fig 7.11 Example 7.4.

Construct the dc load line for the circuit shown in Fig. 7.10, and plot the Q-point from the values obtained in Example 7.3. Determine whether the circuit is midpoint biased.

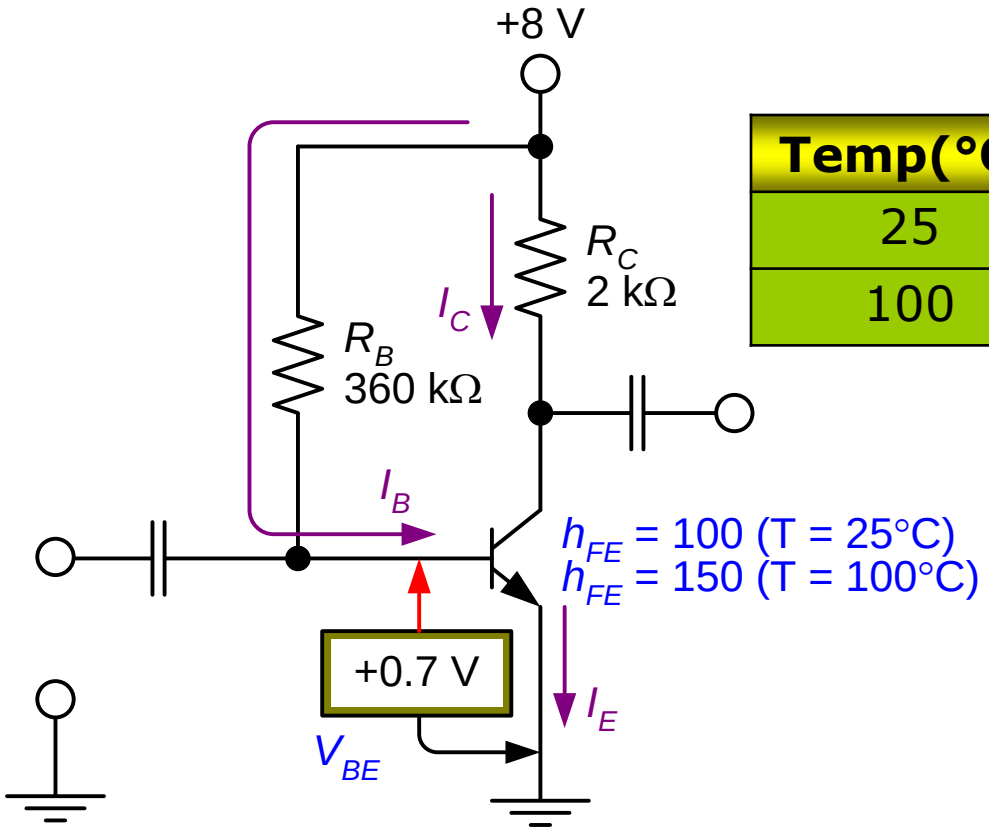


$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{8\text{V}}{2\text{k}\Omega} = 4\text{mA}$$

$$V_{CE(\text{off})} = V_{CC} = 8\text{V}$$

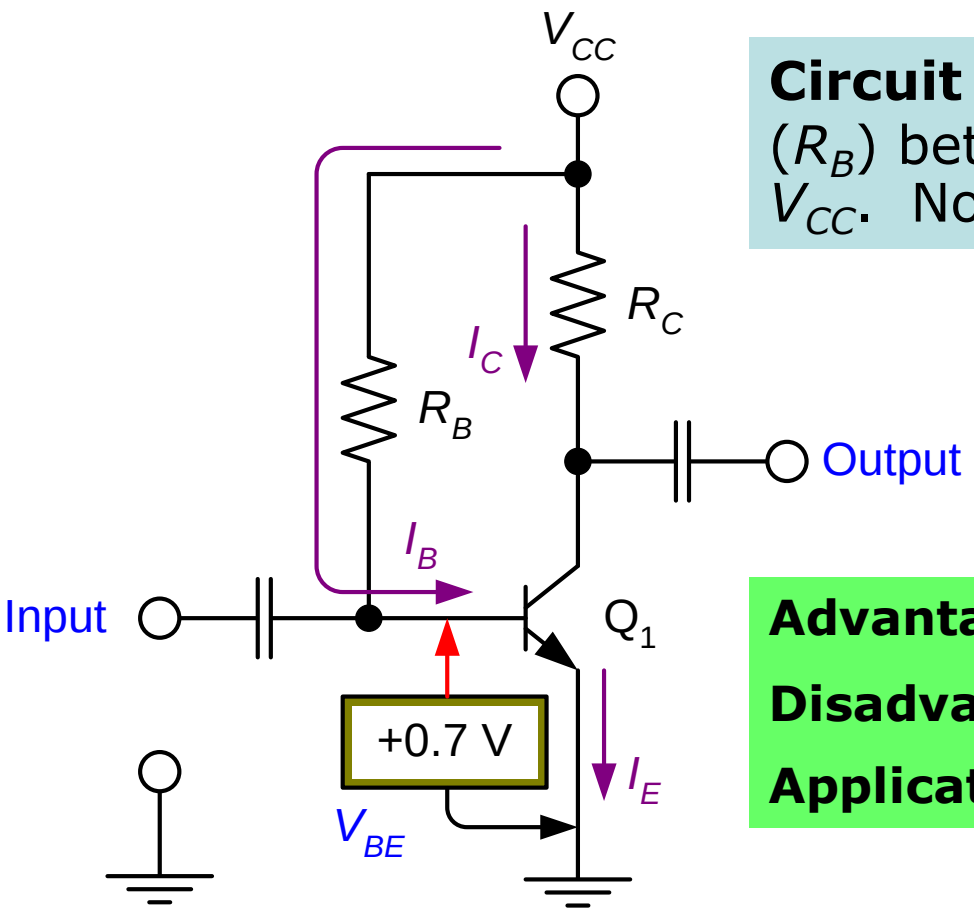
Fig 7.12 Example 7.6. (Q-point shift.)

The transistor in Fig. 7.12 has values of h_{FE} = 100 when T = 25 °C and h_{FE} = 150 when T = 100 °C. Determine the Q-point values of I_C and V_{CE} at both of these temperatures.



Temp(°C)	I_B (μA)	I_C (mA)	V_{CE} (V)
25	20.28	2.028	3.94
100	20.28	3.04	1.92

Fig 7.13 Base bias characteristics. (1)



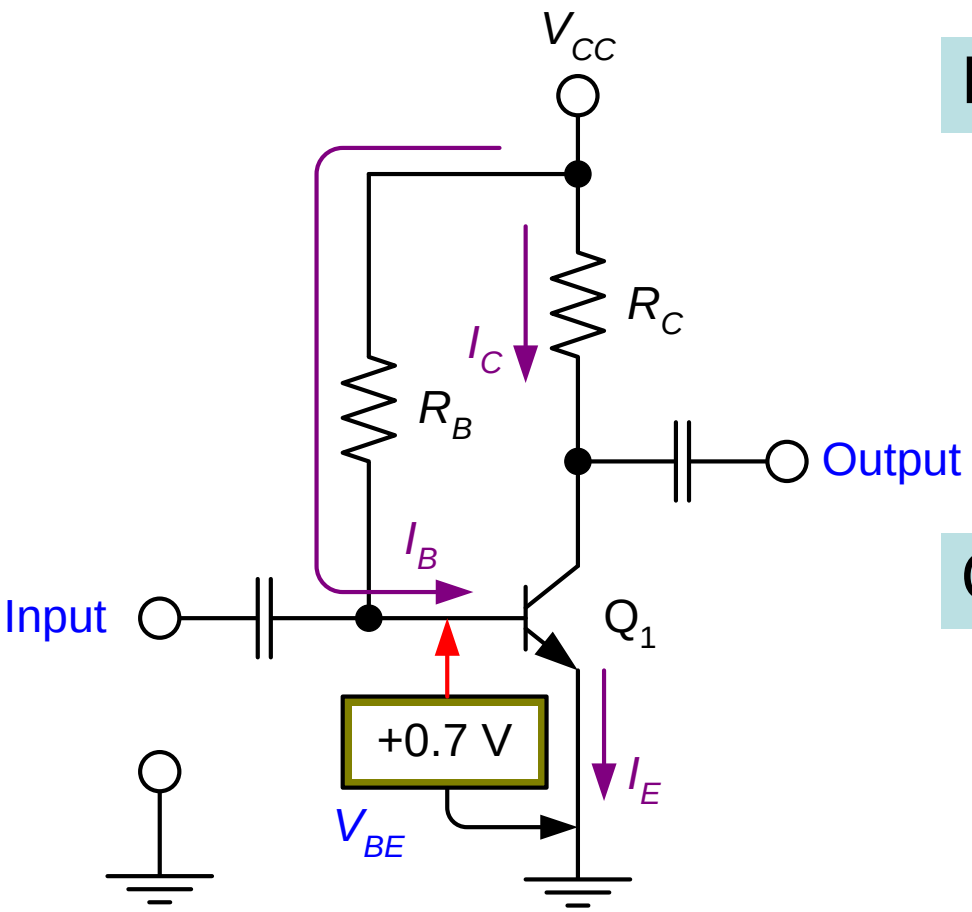
Circuit recognition: A single resistor (R_B) between the base terminal and V_{CC}. No emitter resistor.

Advantage: Circuit simplicity.

Disadvantage: Q-point shift with temp.

Applications: Switching circuits only.

Fig 7.13 Base bias characteristics. (2)



Load line equations:

$$I_{C(\text{sat})} \cong \frac{V_{CC}}{R_C}$$

$$V_{CE(\text{off})} = V_{CC}$$

Q-point equations:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = h_{FE} I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (RB).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

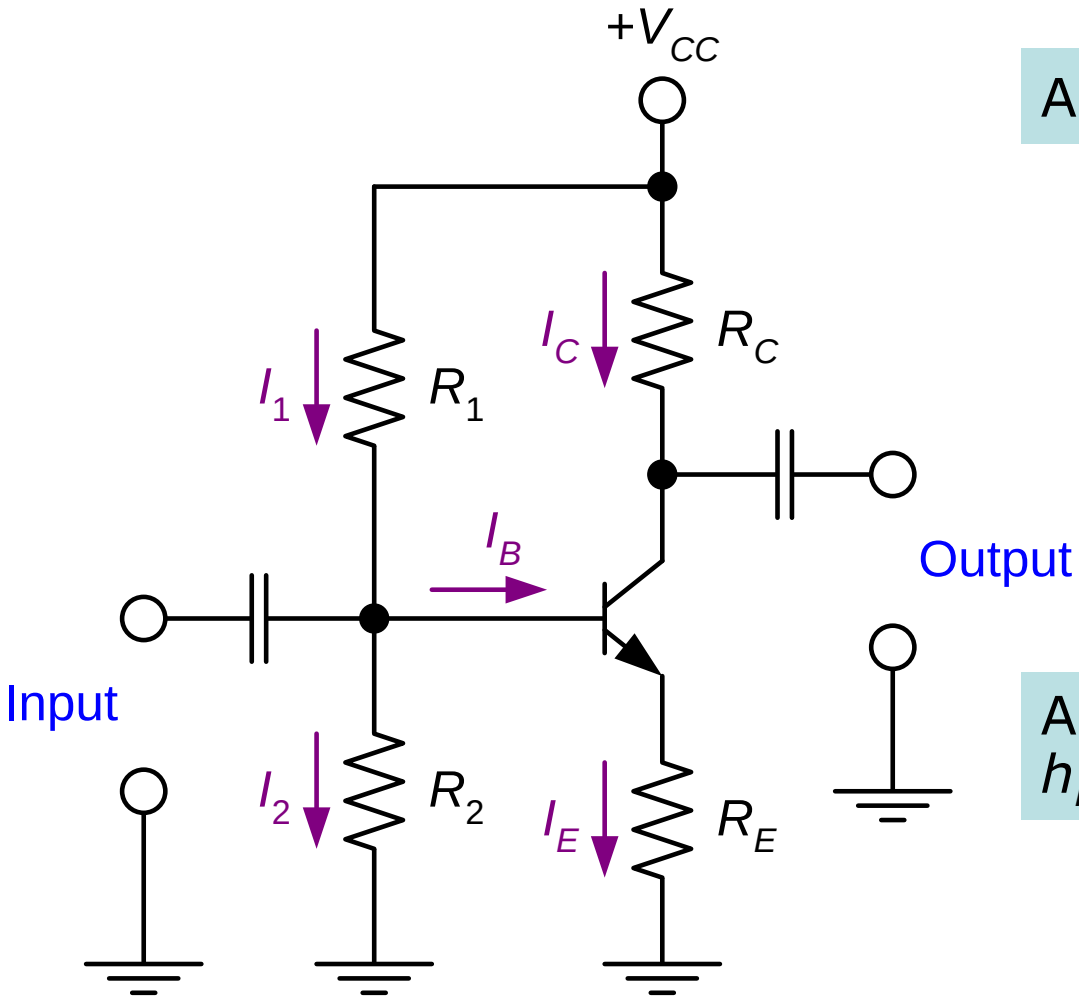
Usage:

- Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

The Potential Divider Bias Circuit

This is the most commonly used arrangement for biasing as it provide good bias stability. In this arrangement the emitter resistance 'R_E' provides stabilization. The resistance 'R_E' cause a voltage drop in a direction so as to reverse bias the emitter junction. Since the emitter-base junction is to be forward biased, the base voltage is obtained from R_1-R_2 network. The net forward bias across the emitter base junction is equal to V_B- dc voltage drop across 'R_E'. The base voltage is set by Vcc and R_1 and R_2. The dc bias circuit is independent of transistor current gain. In case of amplifier, to avoid the loss of ac signal, a capacitor of large capacitance is connected across R_E. The capacitor offers a very small reactance to ac signal and so it passes through the condensor.

Fig 7.14 Voltage divider bias. (1)



Assume that $I_2 > 10I_B$.

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$V_E = V_B - 0.7\text{V}$$

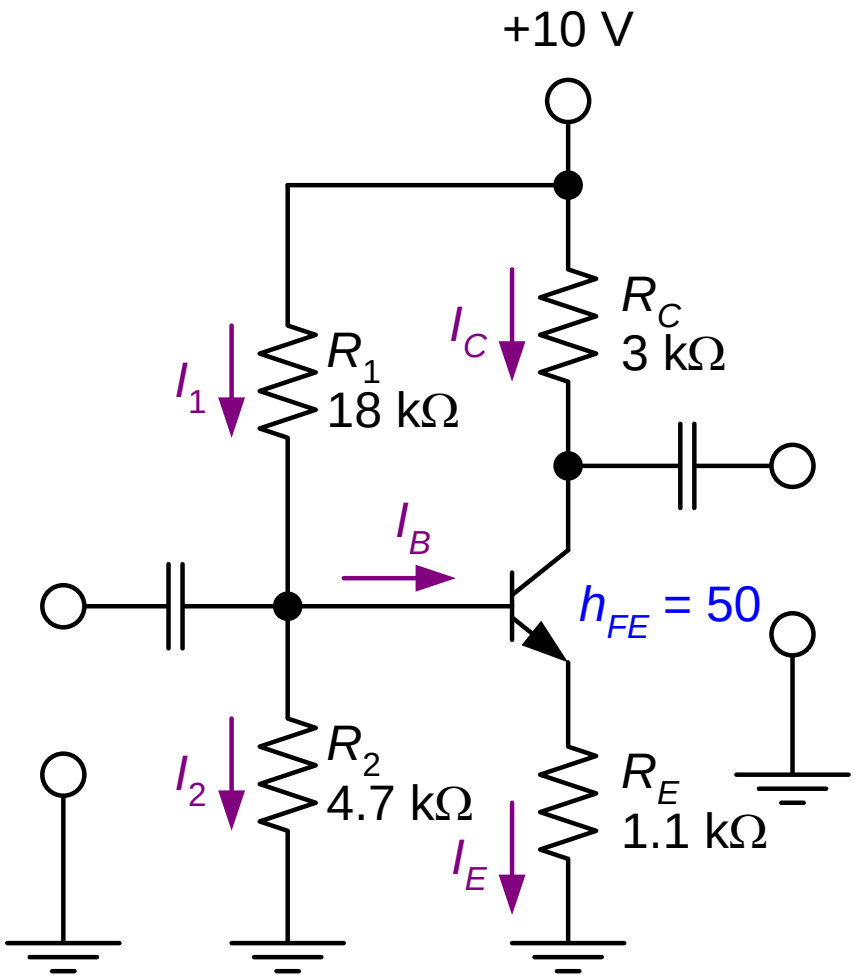
$$I_E = \frac{V_E}{R_E}$$

Assume that $I_{CQ} \cong I_E$ (or $h_{FE} >> 1$). Then

$$V_{CEQ} = V_{CC} - I_{CQ}\left(R_C + R_E\right)$$

Fig 7.15 Example 7.7. (1)

Determine the values of I_{CQ} and V_{CEQ} for the circuit shown in Fig. 7.15.



$$V_B = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$= (10\text{V})\frac{4.7\text{k}\Omega}{22.7\text{k}\Omega} = 2.07\text{V}$$

$$V_E = V_B - 0.7\text{V}$$

$$= 2.07\text{V} - 0.7\text{V} = 1.37\text{V}$$

Because $I_{CQ} \cong I_E$ (or $h_{FE} >> 1$),

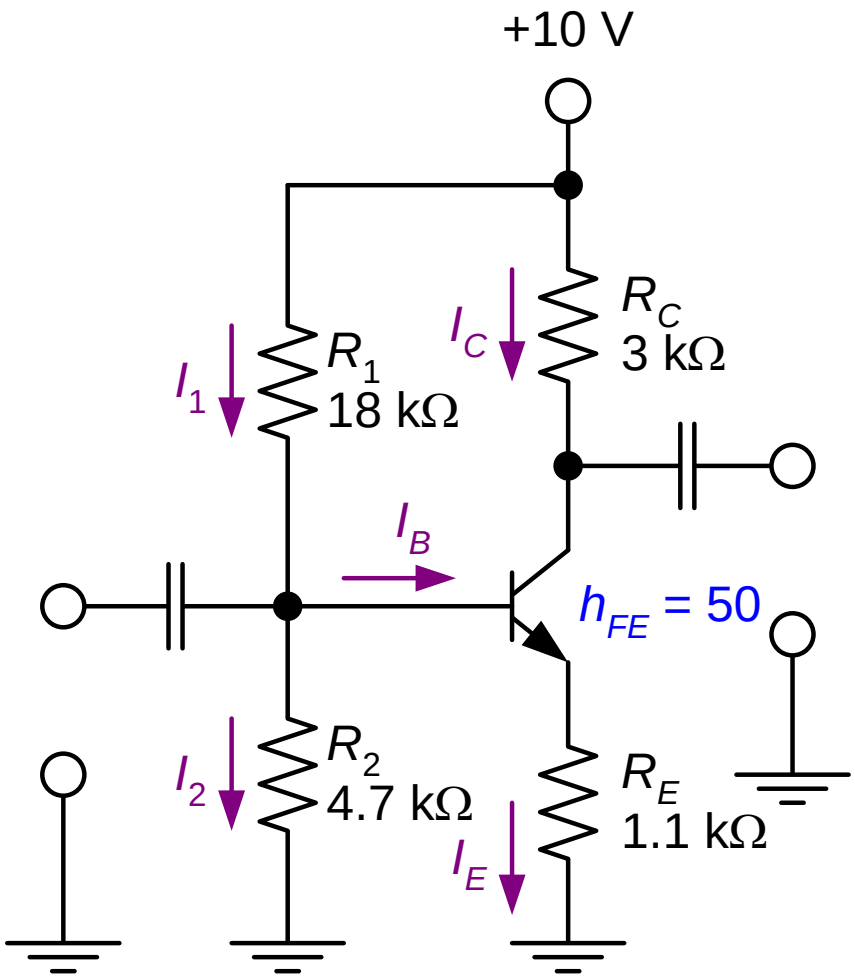
$$I_{CQ} \cong \frac{V_E}{R_E} = \frac{1.37\text{V}}{1.1\text{k}\Omega} = 1.25\text{mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$

$$= 10\text{V} - (1.25\text{mA})(4.1\text{k}\Omega) = 4.87\text{V}$$

Fig 7.15 Example 7.7. (2)

Verify that $I_2 > 10\ I_B$.



$$I_2 = \frac{V_B}{R_2} = \frac{2.07\text{V}}{4.7\text{k}\Omega} = 440.4\mu\text{A}$$

$$I_B = \frac{I_E}{h_{FE}+1} = \frac{1.25\text{mA}}{50+1} = 24.51\mu\text{A}$$

$$\therefore I_2 > 10 I_B$$

Which value of h_{FE} do I use?

Transistor specification sheet may list any combination of the following h_{FE}: max. h_{FE}, min. h_{FE}, or typ. h_{FE}. Use typical value if there is one. Otherwise, use

$$h_{FE(\text{ave})} = \sqrt{h_{FE(\text{min})} \times h_{FE(\text{max})}}$$

Example 7.9

A voltage-divider bias circuit has the following values: R_1 = 1.5 kΩ, R_2 = 680 Ω, R_C = 260 Ω, R_E = 240 Ω and V_{CC} = 10 V. Assuming the transistor is a 2N3904, determine the value of I_B for the circuit.

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2} = (10\text{V})\frac{680\Omega}{2180\Omega} = 3.12\text{V}$$

$$V_E = V_B - 0.7\text{V} = 3.12\text{V} - 0.7\text{V} = 2.42\text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{2.42\text{V}}{240\Omega} = 10\text{mA}$$

$$h_{FE(ave)} = \sqrt{h_{FE(\min)} \times h_{FE(\max)}} = \sqrt{100 \times 300} = 173$$

$$I_B = \frac{I_E}{h_{FE(\text{ave})} + 1} = \frac{10\text{mA}}{174} = 57.5\mu\text{A}$$

Stability of Voltage Divider Bias Circuit

The Q-point of voltage divider bias circuit is less dependent on h_{FE} than that of the base bias (fixed bias).

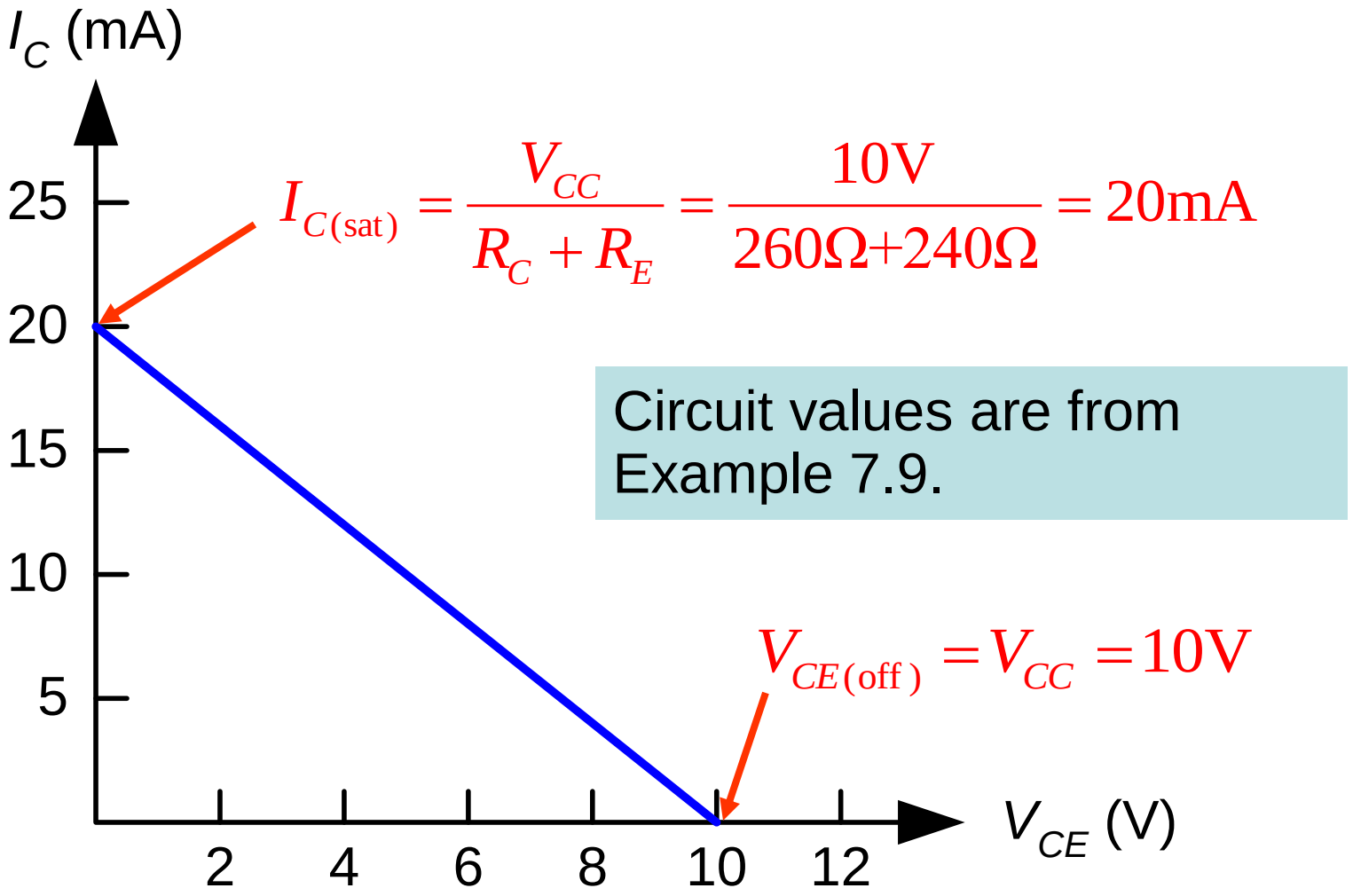
For example, if I_E is exactly 10 mA, the range of h_{FE} is 100 to 300. Then

$$\text{At } h_{FE} = 100,\ I_B = \frac{I_E}{h_{FE}+1} = \frac{10\text{mA}}{101} \cong 100\mu\text{A and } I_{CQ} = I_E - I_B \cong 9.90\text{mA}$$

$$\text{At } h_{FE} = 300,\ I_B = \frac{I_E}{h_{FE}+1} = \frac{10\text{mA}}{301} \cong 33\mu\text{A and } I_{CQ} = I_E - I_B \cong 9.97\text{mA}$$

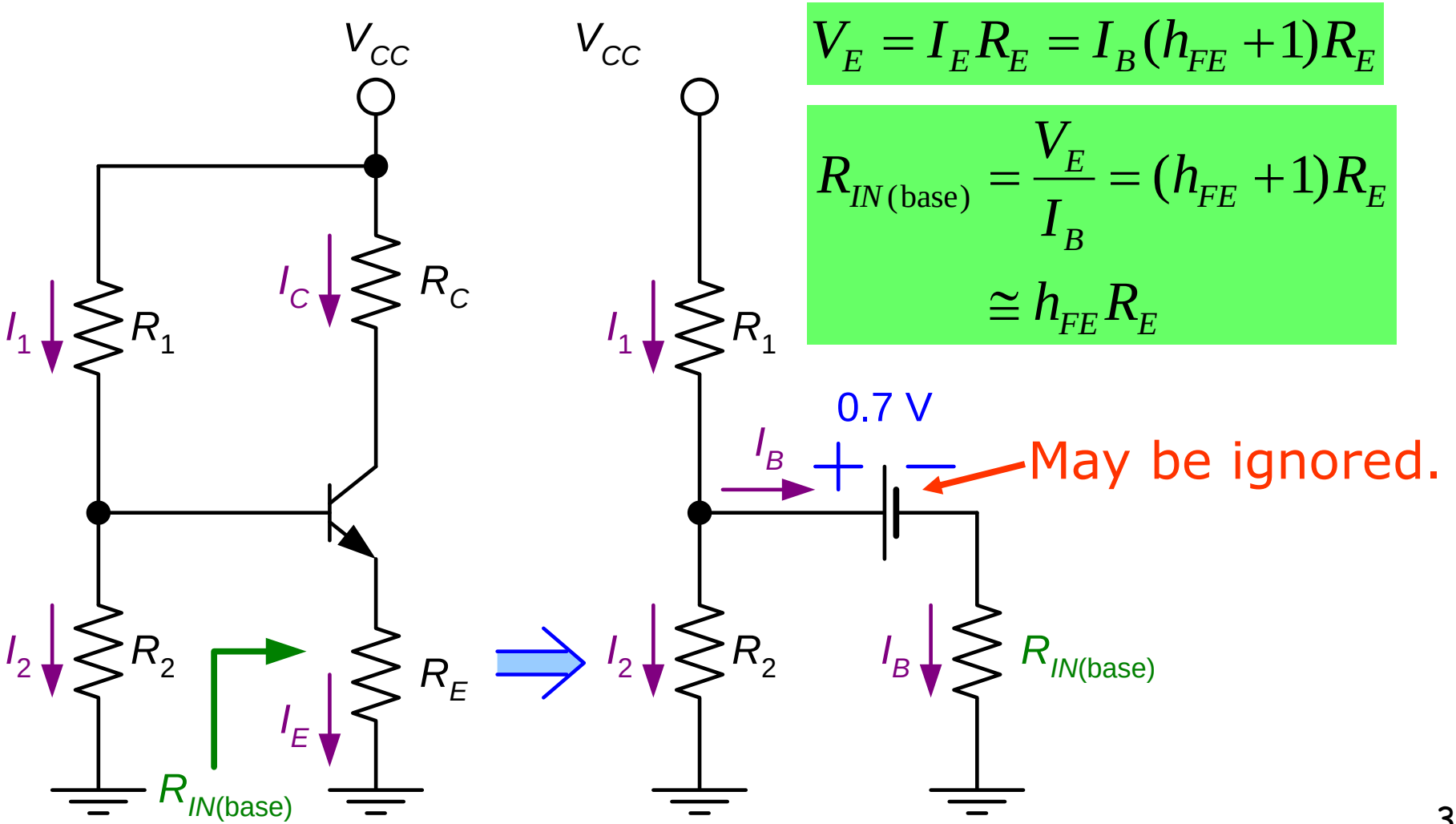
I_{CQ} hardly changes over the entire range of h_{FE}.

Fig 7.18 Load line for voltage divider bias circuit.



Circuit values are from Example 7.9.

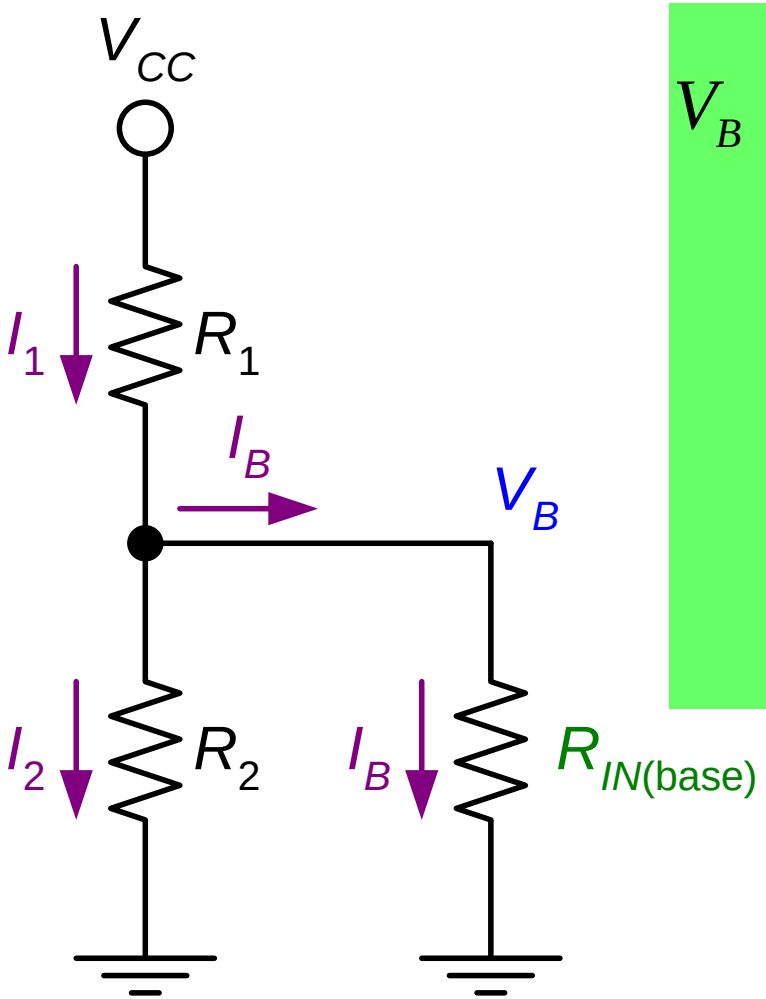
Fig 7.19-20 Base input resistance. (1)



$$V_E = I_E R_E = I_B (h_{FE} + 1) R_E$$

$$R_{IN\,(\text{base})} = \frac{V_E}{I_B} = (h_{FE} + 1) R_E \cong h_{FE} R_E$$

Fig 7.19-20 Base input resistance. (2)

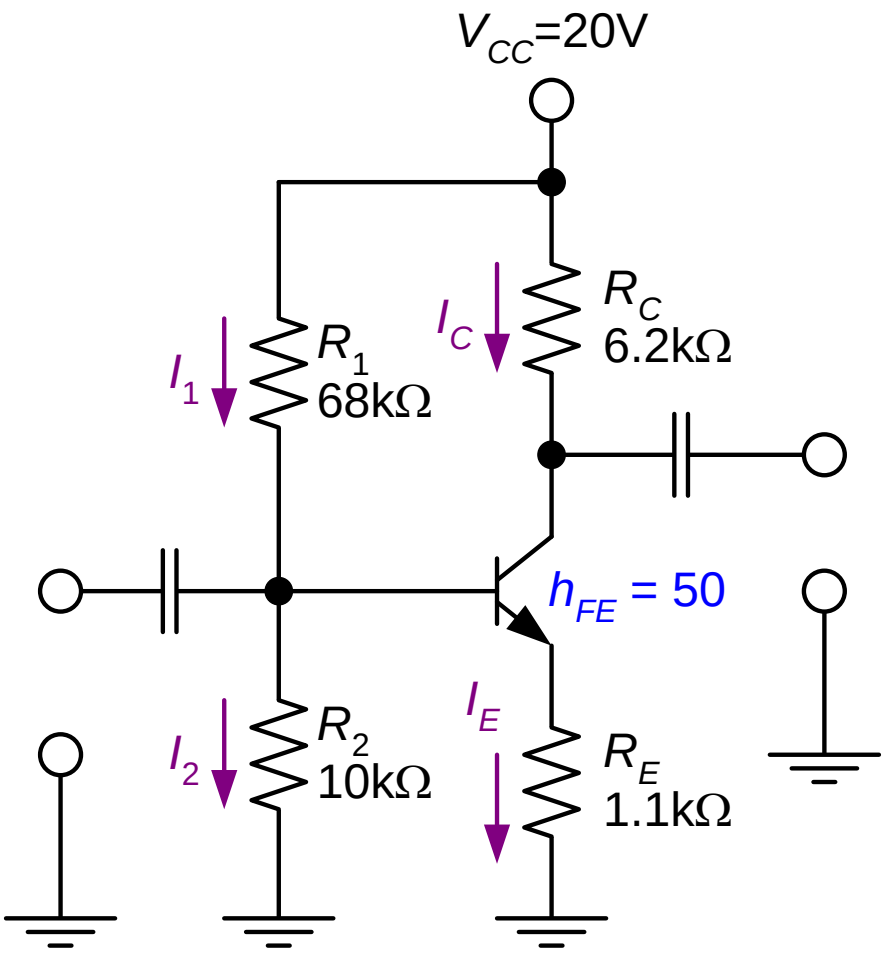


$$V_B = \frac{R_2 \,//\, R_{IN\,(\text{base})}}{R_1 + R_2 \,//\, R_{IN\,(\text{base})}} V_{CC}$$

$$= \frac{R_2 \,//\, \left(h_{FE} R_E\right)}{R_1 + R_2 \,//\, \left(h_{FE} R_E\right)} V_{CC}$$

$$= \frac{R_{EQ}}{R_1 + R_{EQ}} V_{CC} \Bigg| R_{EQ} = R_2 \,//\, \left(h_{FE} R_E\right)$$

Fig 7.21 Example 7.11.



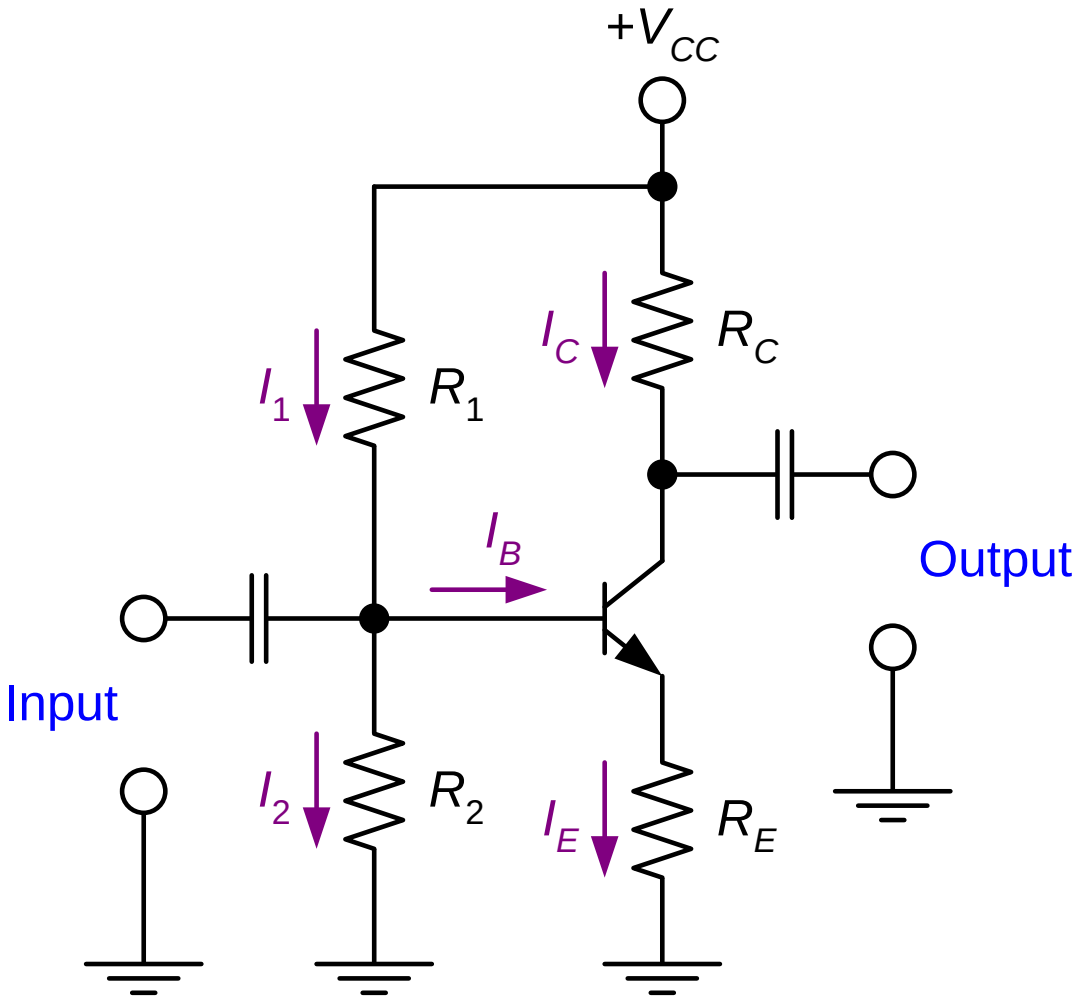
$$R_{EQ} = R_2 \,//\, (h_{FE} R_E)$$
$$= 10\text{k}\Omega // (50 \times 1.1\text{k}\Omega) = 8.46\text{k}\Omega$$

$$V_B \cong V_{CC} \frac{R_{EQ}}{R_1 + R_{EQ}}$$
$$= (20\text{V}) \frac{8.46\text{k}\Omega}{68\text{k}\Omega + 8.46\text{k}\Omega} = 2.21\text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7\text{V}}{R_E}$$
$$= \frac{2.21\text{V} - 0.7\text{V}}{1.1\text{k}\Omega} = 1.37\text{mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$
$$= 20\text{V} - (1.37\text{mA})(7.3\text{k}\Omega) = 9.99\text{V}$$

Fig 7.24 Voltage-divider bias characteristics. (1)



Circuit recognition: The voltage divider in the base circuit.

Advantages: The circuit Q-point values are stable against changes in h_{FE}.

Disadvantages: Requires more components than most other biasing circuits.

Applications: Used primarily to bias linear amplifier.

Merits:

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

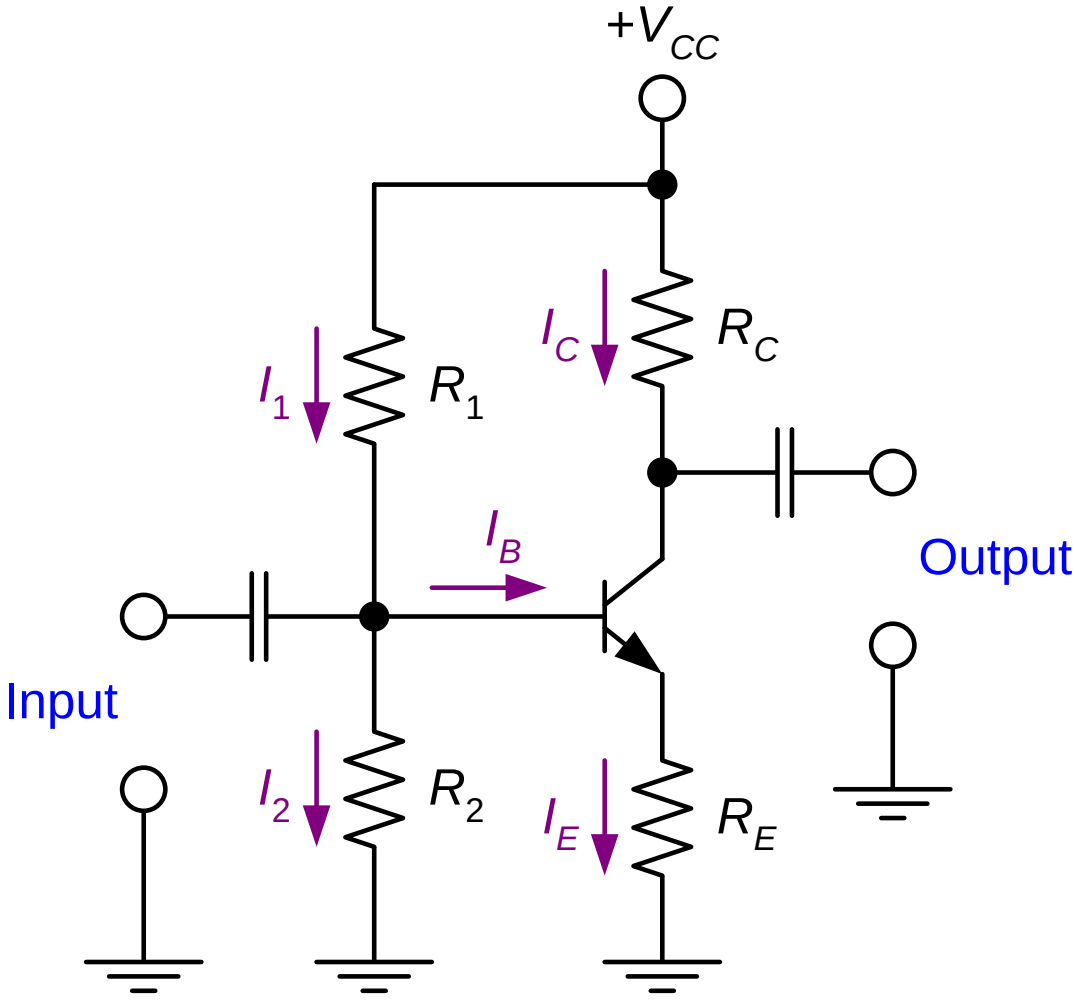
- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making R1||R2 very low.
  - If R_E is of large value, high V_{CC} is necessary. This increases cost as well

  as precautions necessary while handling.
  - If R1 || R2 is low, either R1 is low, or R2 is low, or both are low. A low R1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R2 lowers Vbe, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
  - AC as well as DC feedback is caused by RE, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage:

The circuit's stability and merits as above make it widely used for linear circuits.

Fig 7.24 Voltage-divider bias characteristics. (2)



Load line equations:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE(\text{off})} = V_{CC}$$

Q-point equations (assume that $h_{FE}R_E > 10R_2$):

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$V_E = V_B - 0.7\text{V}$$

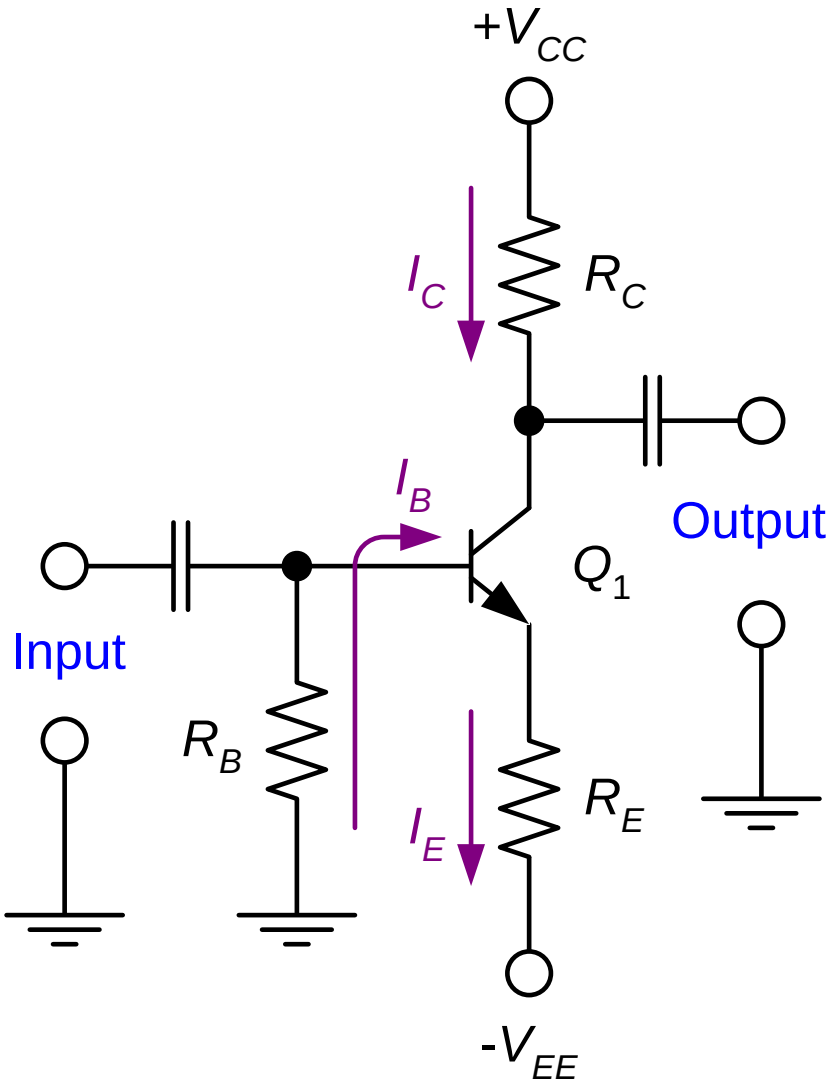
$$I_{CQ} \cong I_E = \frac{V_E}{R_E}$$

$$V_{CEQ} = V_{CC} - I_{CQ}\left(R_C + R_E\right)$$

Other Transistor Biasing Circuits

- Emitter-bias circuits
- Feedback-bias circuits
  - Collector-feedback bias
  - Emitter-feedback bias

Fig 7.25-6 Emitter bias.



Assume that the transistor operation is in active region.

$$I_B = \frac{V_{EE} - 0.7\text{V}}{R_B + (h_{FE} + 1)R_E}$$

$$I_C = h_{FE} I_B$$

$$I_E = (h_{FE} + 1) I_B$$

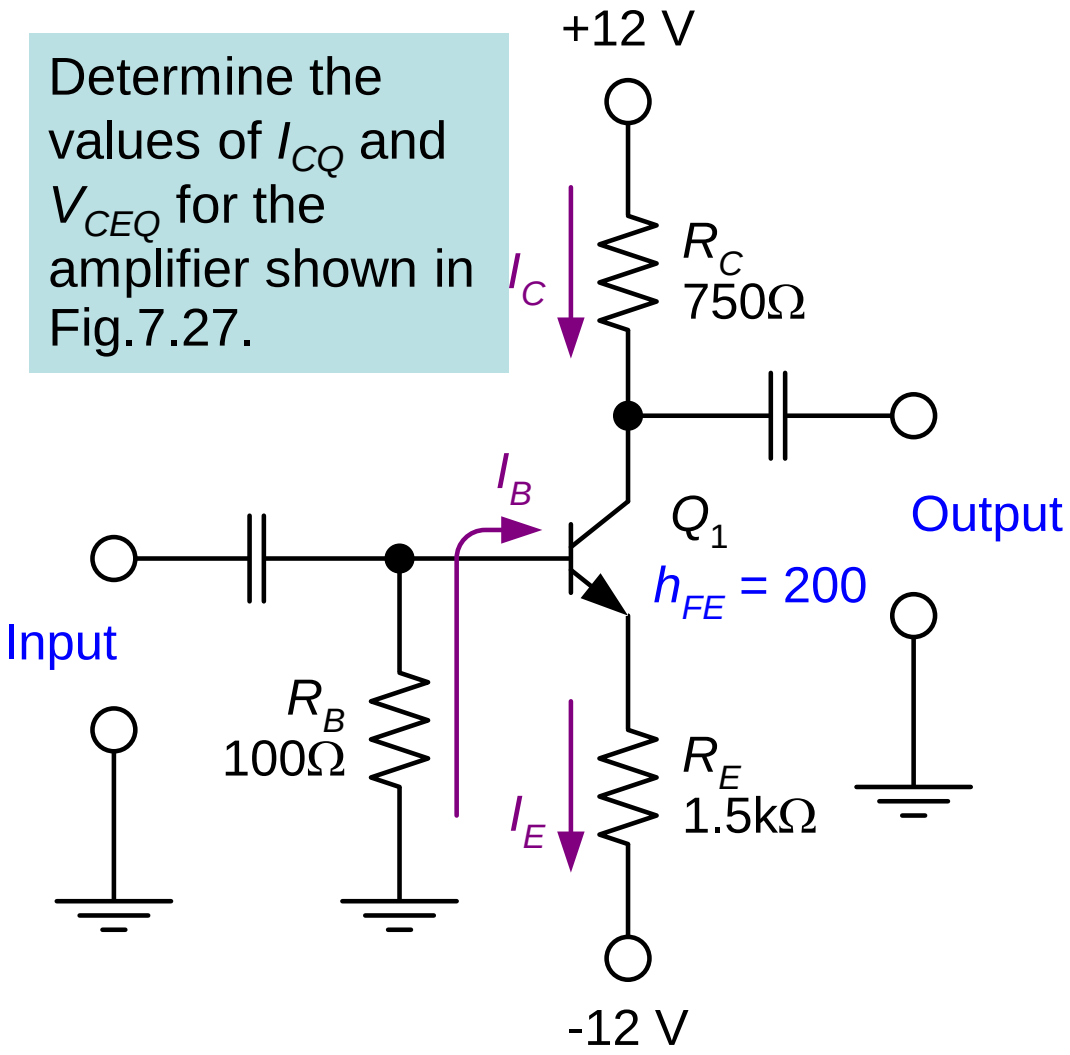
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E + V_{EE}$$

Assume that $h_{FE} >> 1$.

$$V_{CE} \cong V_{CC} - I_C (R_C + R_E) + V_{EE}$$

Fig 7.27 Example 7.12.

Determine the values of I_{CQ} and V_{CEQ} for the amplifier shown in Fig.7.27.



$$I_B = \frac{12\text{V} - 0.7\text{V}}{R_B + (h_{FE} + 1)R_E}$$

$$= \frac{11.3\text{V}}{100\Omega + 201 \times 1.5\text{k}\Omega} = 37.47\mu\text{A}$$

$$I_{CQ} = h_{FE} I_B = 200 \times 37.47\mu\text{A}$$

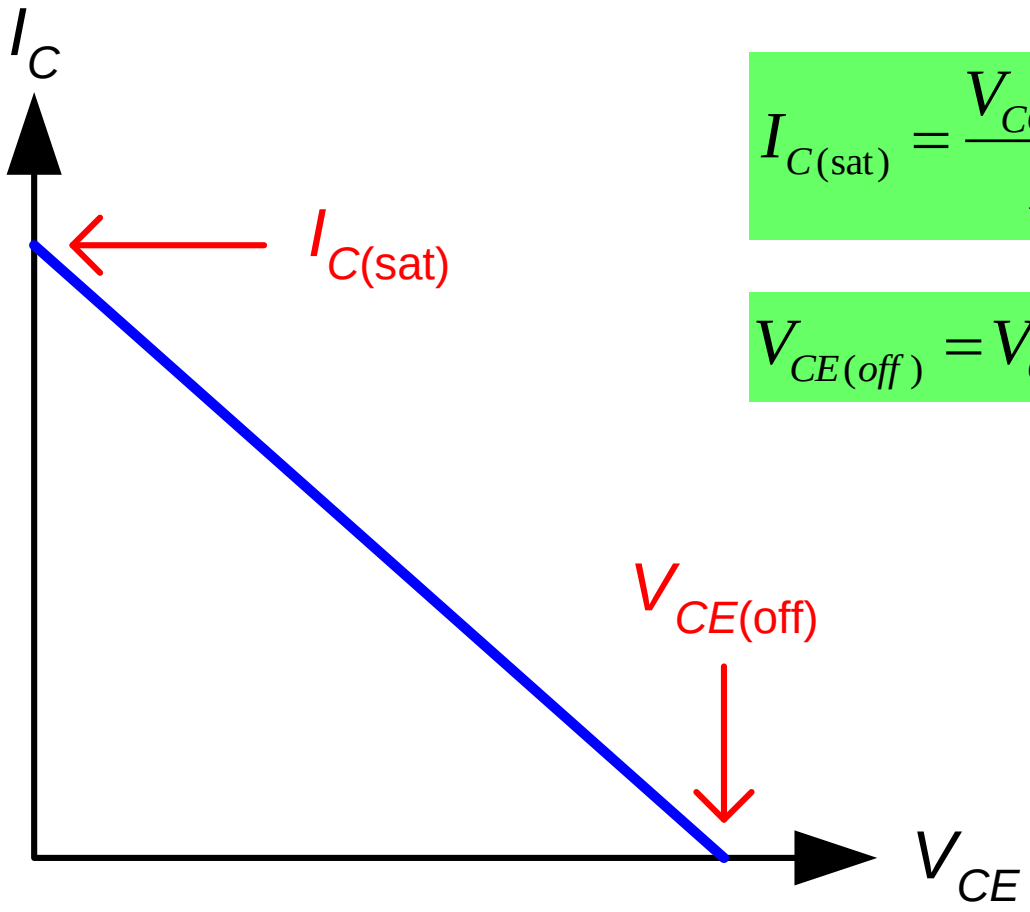
$$= 7.49\text{mA}$$

$$V_{CEQ} \cong V_{CC} - I_C\left(R_C + R_E\right) - (-V_{EE})$$

$$= 24\text{V} - 7.49\text{mA}\left(750\Omega + 1.5\text{k}\Omega\right)$$

$$= 7.14\text{V}$$

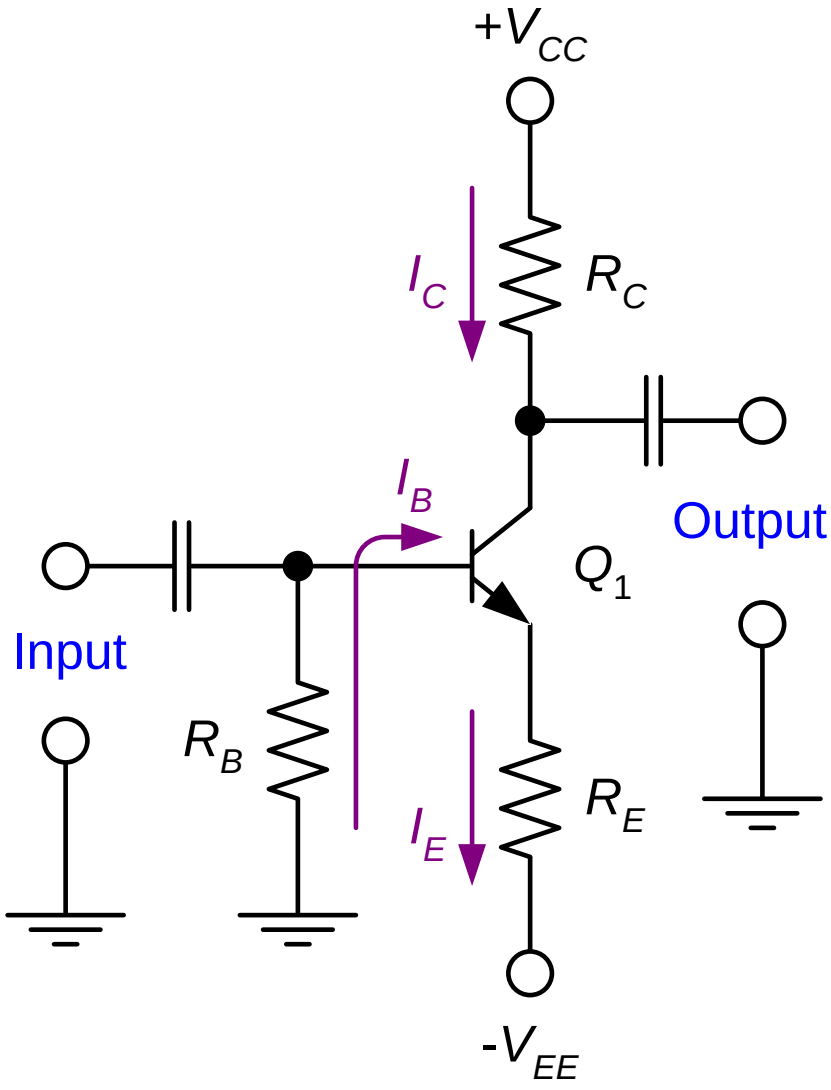
Load Line for Emitter-Bias Circuit



$$I_{C(\text{sat})} = \frac{V_{CC} - (-V_{EE})}{R_C + R_E} = \frac{V_{CC} + V_{EE}}{R_C + R_E}$$

$$V_{CE(off)} = V_{CC} - (-V_{EE}) = V_{CC} + V_{EE}$$

Fig 7.28 Emitter-bias characteristics. (1)



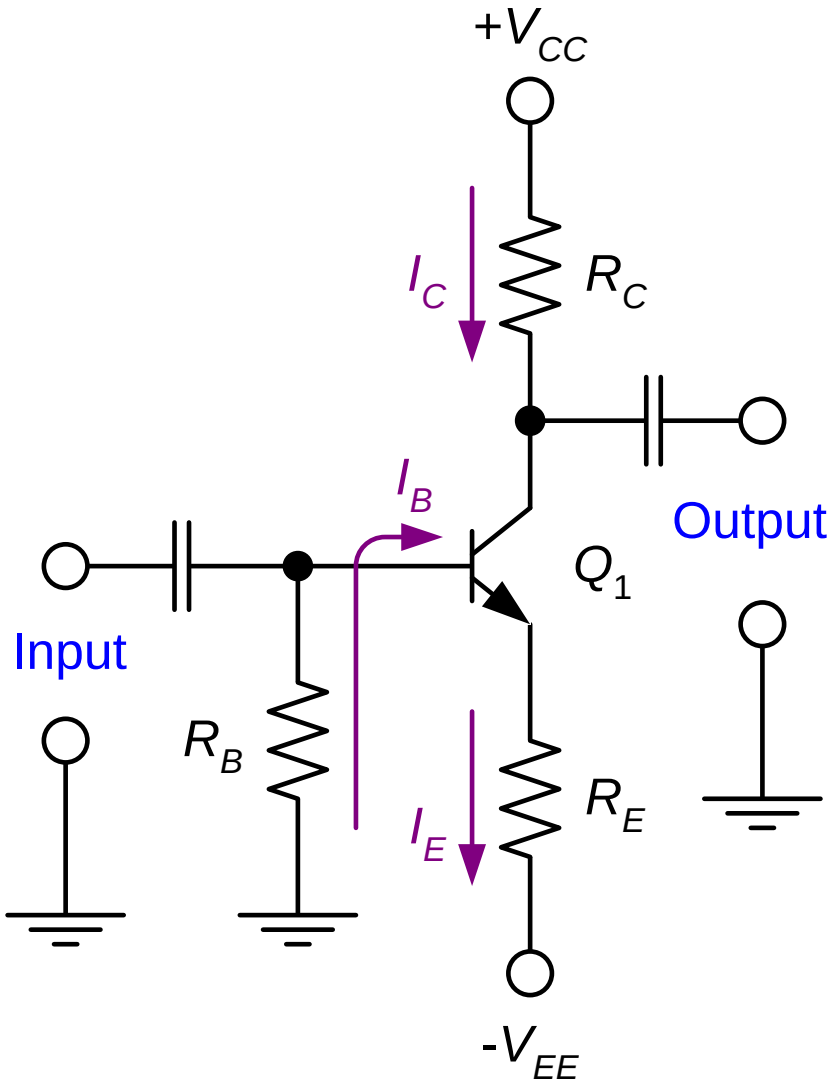
Circuit recognition: A split (dual-polairty) power supply and the base resistor is connected to ground.

Advantage: The circuit Q-point values are stable against changes in h_{FE}.

Disadvantage: Requires the use of dual-polarity power supply.

Applications: Used primarily to bias linear amplifiers.

Fig 7.28 Emitter-bias characteristics. (2)



Load line equations:

$$I_{C(\text{sat})} = \frac{V_{CC} + V_{EE}}{R_C + R_E}$$

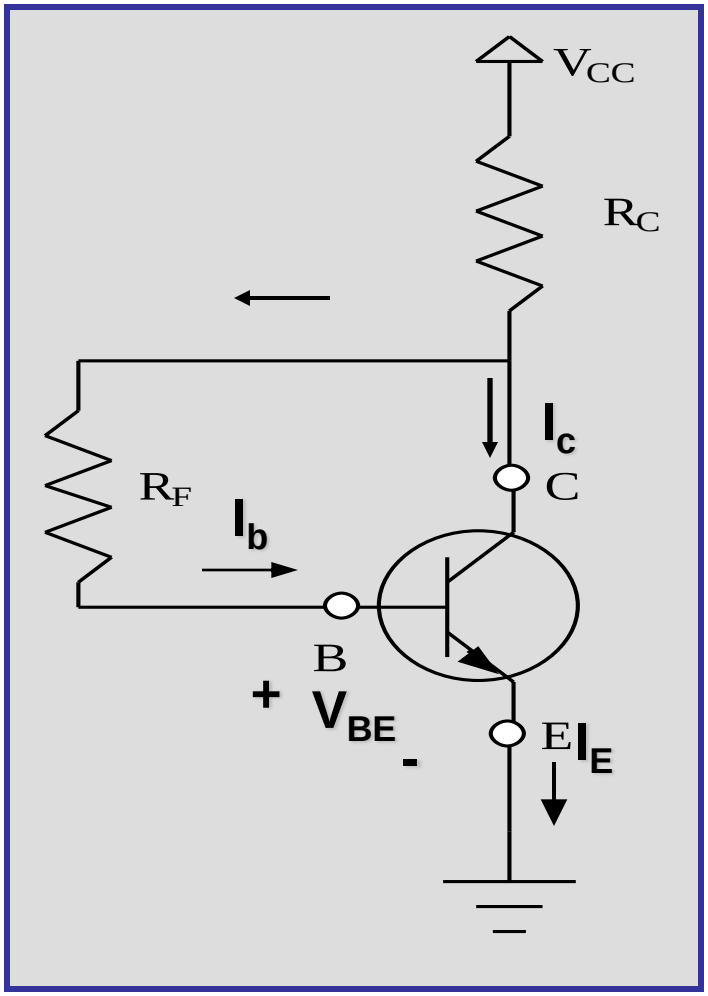
$$V_{CE(\text{off})} = V_{CC} + V_{EE}$$

Q-point equations:

$$I_{CQ} = (h_{FE}) \frac{-V_{BE} + V_{EE}}{R_B + (h_{FE} + 1) R_E}$$

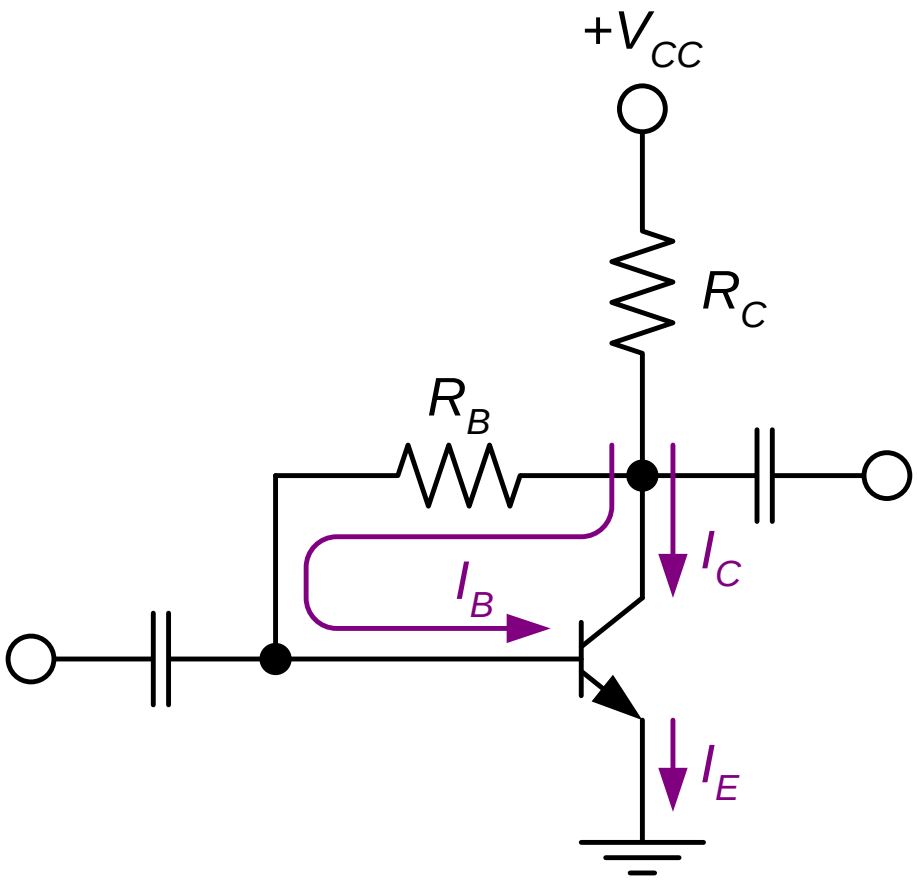
$$V_{CEQ} \cong V_{CC} - I_{CQ}(R_C + R_E) + V_{EE}$$

The Collector to Base Bias Circuit



This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_F is connected to the collector instead of connecting it to the DC source V_{CC}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

Fig 7.29 Collector-feedback bias.



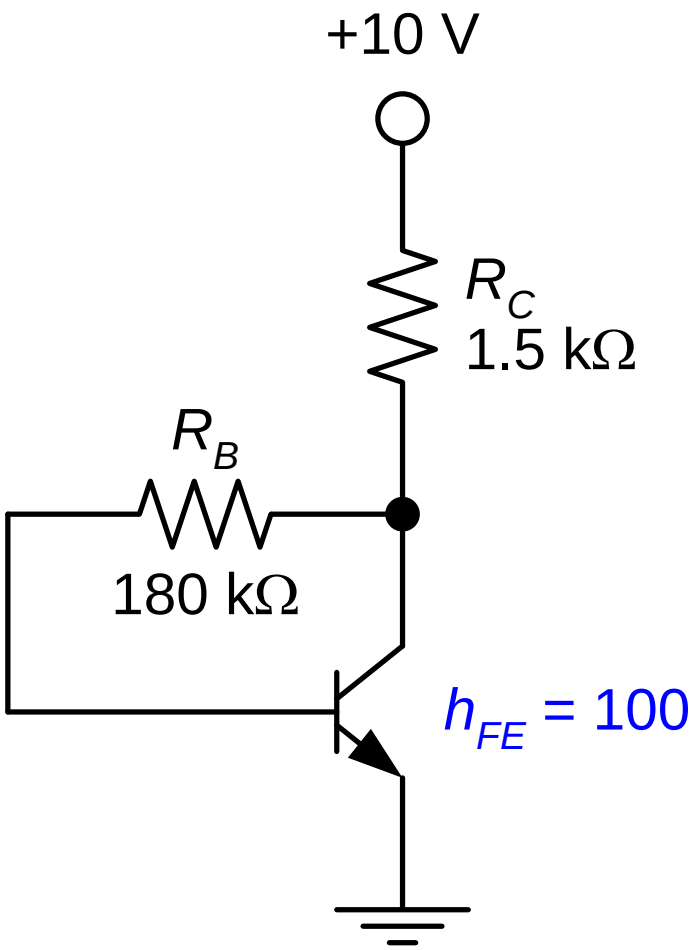
$$V_{CC} = \left(I_C + I_B\right)R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{(h_{FE} + 1)R_C + R_B}$$

$$I_{CQ} = h_{FE} I_B$$

$$V_{CEQ} = V_{CC} - \left(h_{FE} + 1\right) I_B R_C$$
$$\cong V_{CC} - I_{CQ} R_C$$

Fig 7.30 Example 7.14.



Determine the values of I_{CQ} and V_{CEQ} for the amplifier shown in Fig. 7.30.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (h_{FE} + 1)R_C}$$

$$= \frac{10\text{V} - 0.7\text{V}}{180\text{k}\Omega + 101 \times 1.5\text{k}\Omega} = 28.05\mu\text{A}$$

$$I_{CQ} = h_{FE} I_B = 100 \times 28.05\mu\text{A}$$

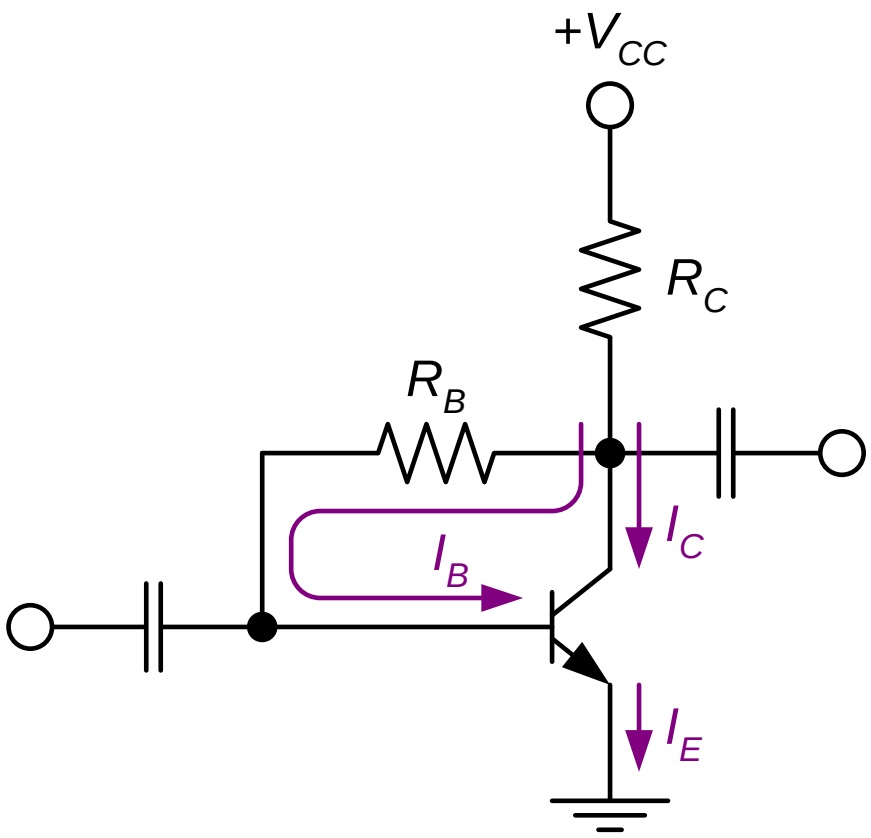
$$= 2.805\text{mA}$$

$$V_{CEQ} = V_{CC} - (h_{FE} + 1) I_B R_C$$

$$= 10\text{V} - 101 \times 28.05\mu\text{A} \times 1.5\text{k}\Omega$$

$$= 5.75\text{V}$$

Circuit Stability of Collector-Feedback Bias



h_{FE} increases

↓

I_C increases (if I_B is the same)

↓

V_{CE} decreases

↓

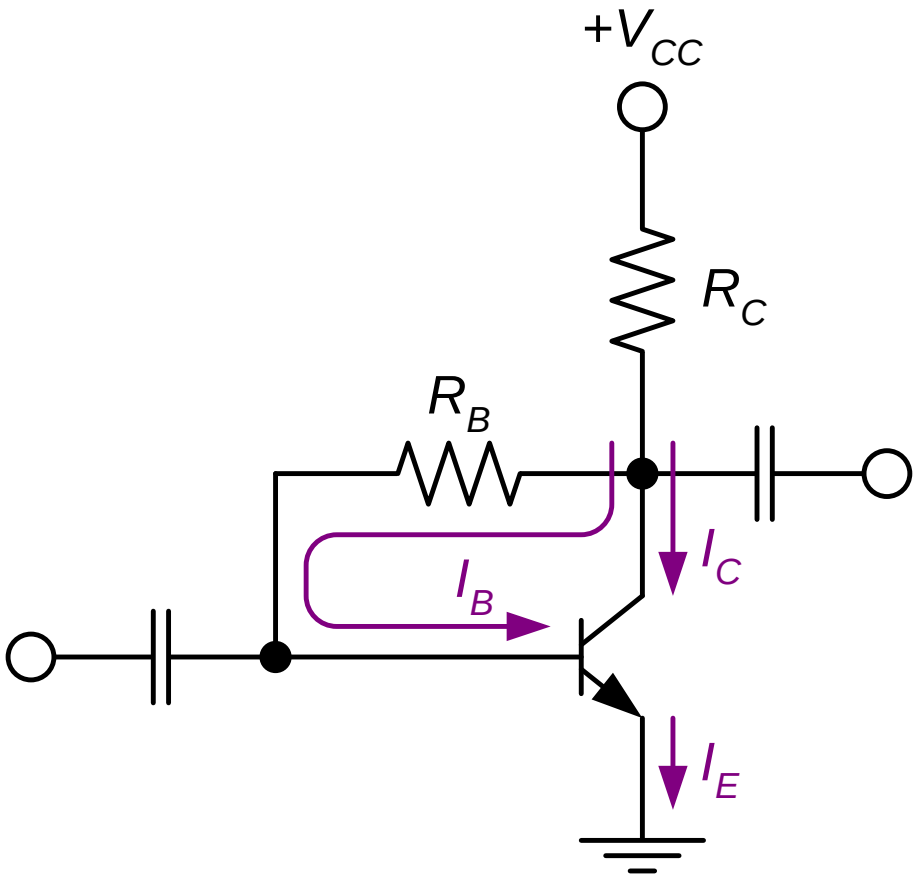
I_B decreases

↓

I_C does not increase that much.

Good Stability. Less dependent on h_{FE} and temperature.

Collector-Feedback Characteristics (1)



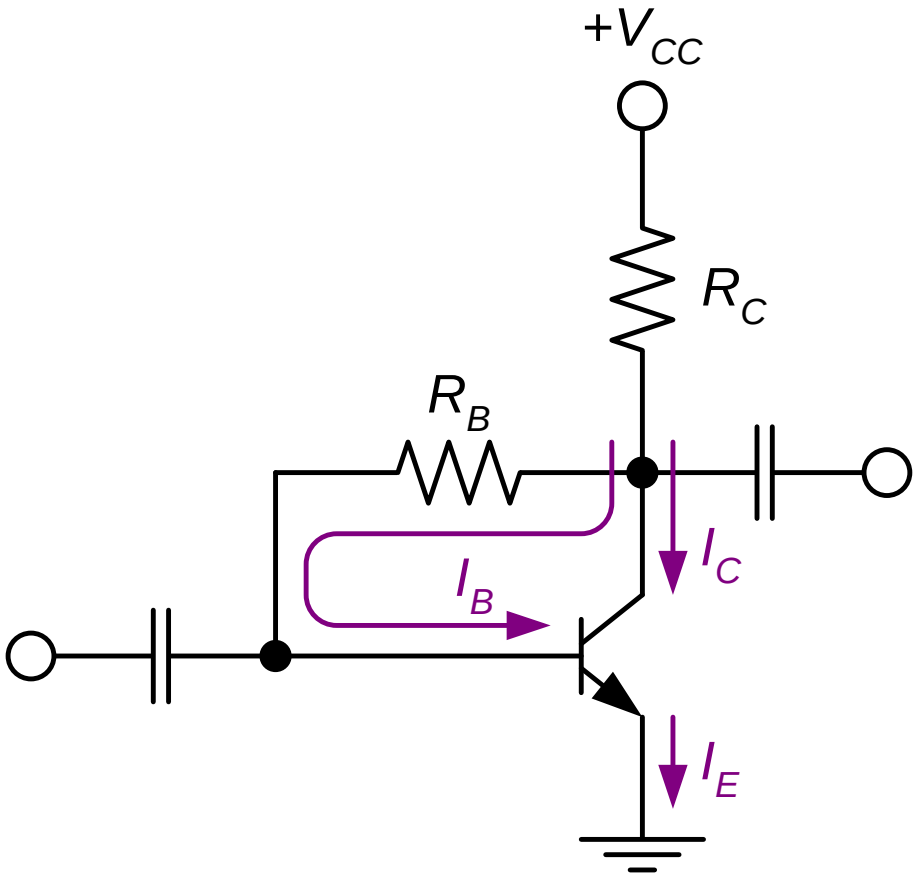
Circuit recognition: The base resistor is connected between the base and the collector terminals of the transistor.

Advantage: A simple circuit with relatively stable Q-point.

Disadvantage: Relatively poor ac characteristics.

Applications: Used primarily to bias linear amplifiers.

Collector-Feedback Characteristics (2)



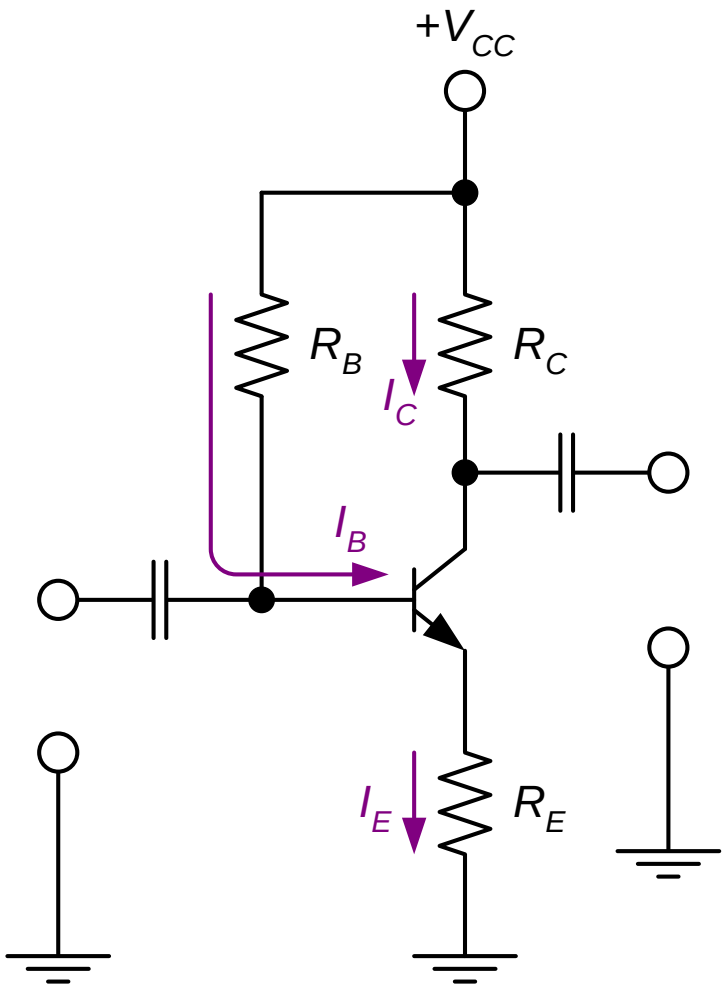
Q-point relationships:

$$I_B = \frac{V_{CC} - V_{BE}}{(h_{FE} + 1)R_C + R_B}$$

$$I_{CQ} = h_{FE} I_B$$

$$V_{CEQ} \cong V_{CC} - I_{CQ} R_C$$

Fig 7.31 Emitter-feedback bias.



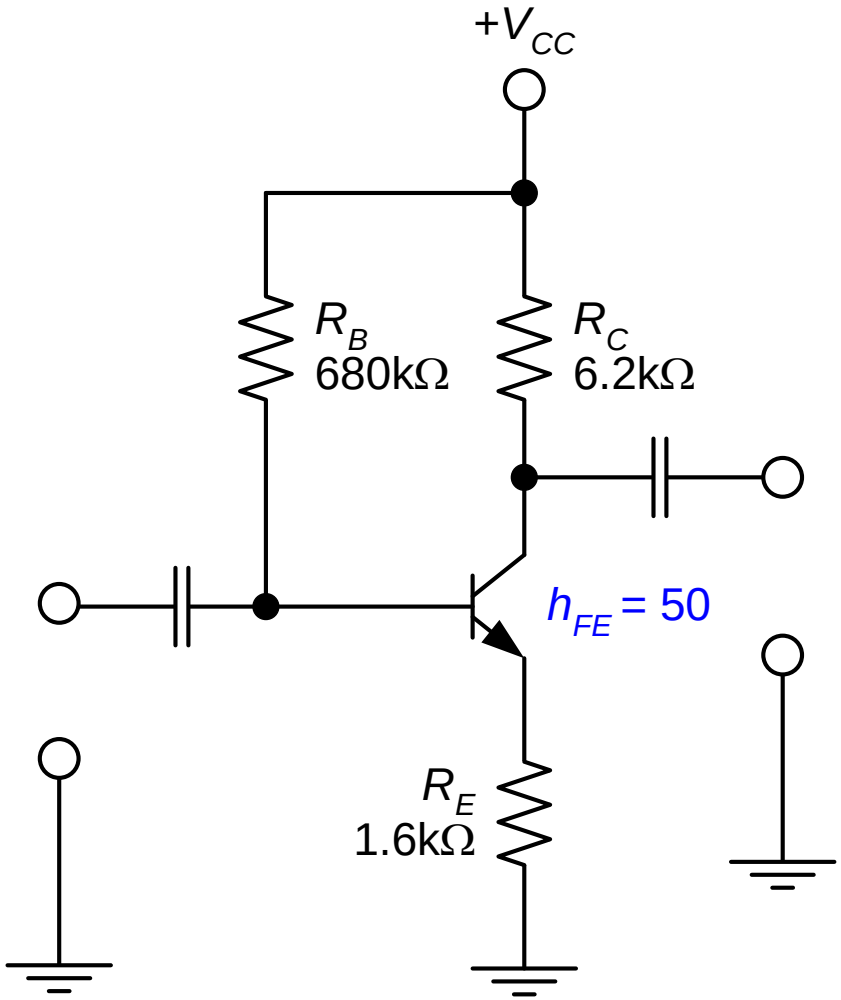
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (h_{FE} + 1) R_E}$$

$$I_{CQ} = h_{FE} I_B$$

$$I_E = (h_{FE} + 1) I_B$$

$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$
$$\cong V_{CC} - I_{CQ} (R_C + R_E)$$

Fig 7.32 Example 7.15.

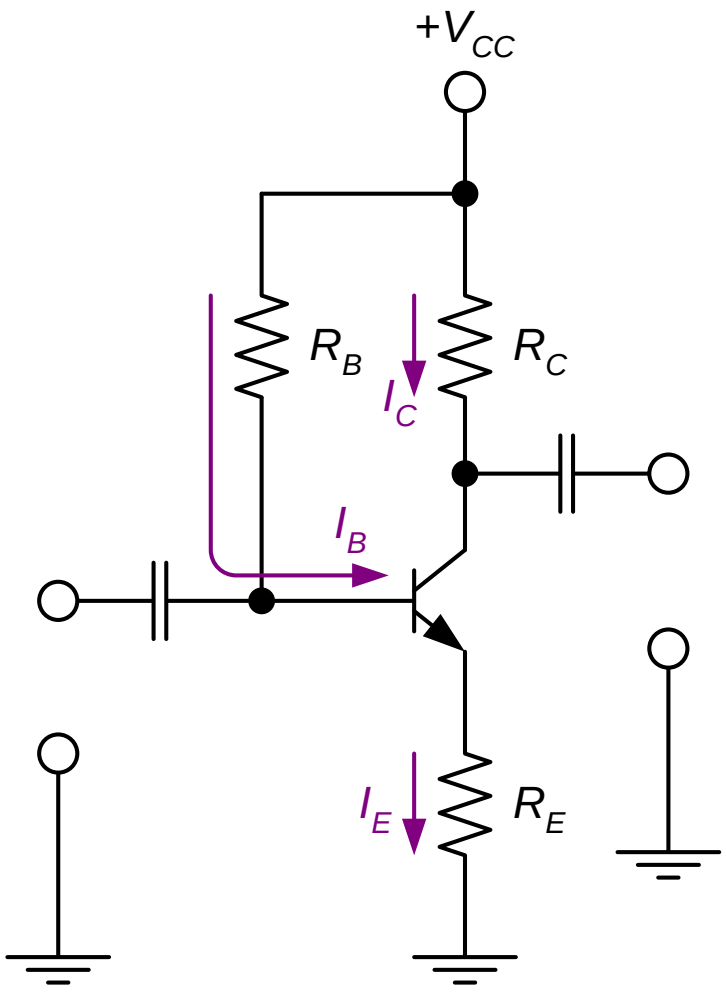


$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (h_{FE} + 1)R_E} = \frac{16\text{V} - 0.7\text{V}}{680\text{k}\Omega + 51 \times 1.6\text{k}\Omega}$$
$$= 20.09\mu\text{A}$$

$$I_{CQ} = h_{FE} I_B = 50 \times 20.09\mu\text{A} = 1\text{mA}$$

$$V_{CEQ} \cong V_{CC} - I_{CQ}(R_C + R_E)$$
$$= 16\text{V} - (1\text{mA})(7.8\text{k}\Omega) = 8.2\text{V}$$

Circuit Stability of Emitter-Feedback Bias



h_{FE} increases

↓

I_C increases (if I_B is the same)

↓

V_E increases

↓

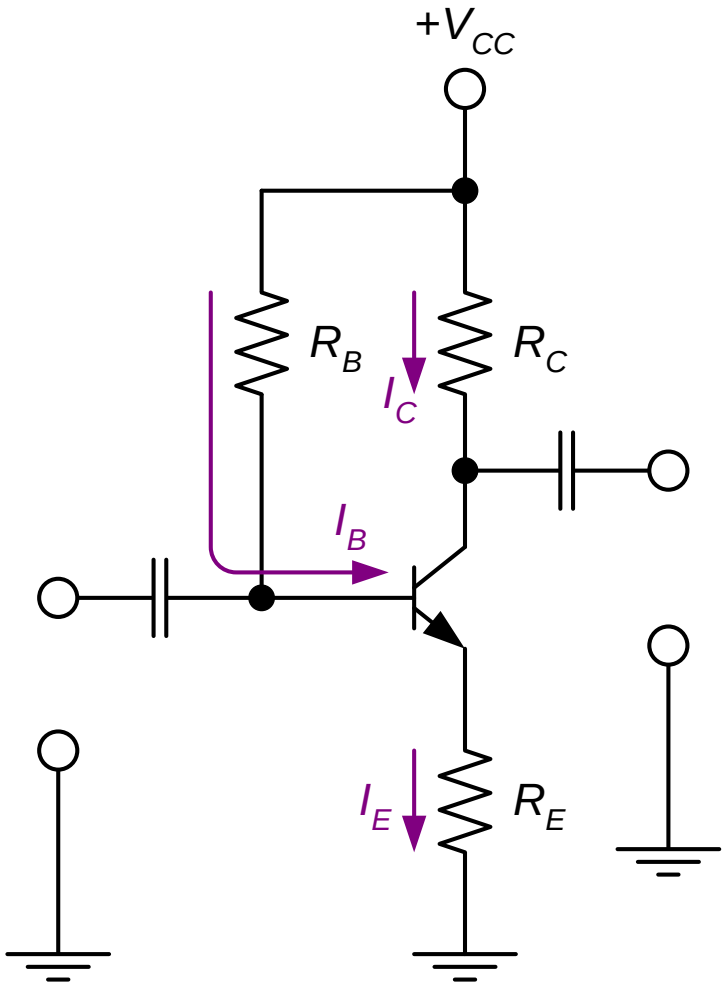
I_B decreases

↓

I_C does not increase that much.

I_C is less dependent on h_{FE} and temperature.

Emitter-Feedback Characteristics (1)



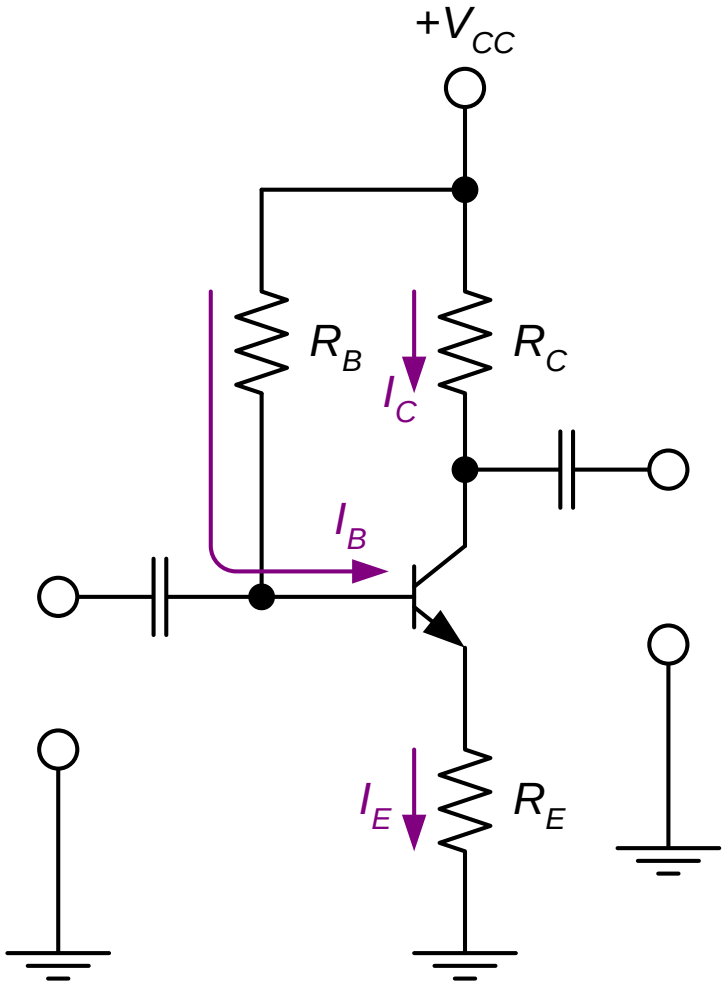
Circuit recognition: Similar to voltage divider bias with R_2 missing (or base bias with R_E added).

Advantage: A simple circuit with relatively stable Q-point.

Disadvantage: Requires more components than collector-feedback bias.

Applications: Used primarily to bias linear amplifiers.

Emitter-Feedback Characteristics (2)



Q-point relationships:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (h_{FE} + 1)R_E}$$

$$I_{CQ} = h_{FE} I_B$$

$$V_{CEQ} \cong V_{CC} - I_{CQ}\left(R_C + R_E\right)$$

Summary

- DC Biasing and the dc load line
- Base bias circuits
- Voltage-divider bias circuits
- Emitter-bias circuits
- Feedback-bias circuits
  - Collector-feedback bias circuits
  - Emitter-feedback bias circuits