Lecture 26 - Design Problems & 6.012 Wrap-Up

May 15, 2003

Contents:

1. Design process
2. Design project pitfalls
3. Lessons learned from design project
4. 6.012 Wrap-Up

Annoucements:

- Pick up your design projects after lecture today.
- Final review session Wednesday, May 21, 7-9pm.
- Final Exam: May 23, 1:30-4:30 PM; open book, calculator required; entire subject under examination but emphasis on lectures #18-26.

Key questions

- What is design all about?
- How do we approach a design problem?
- How can we use simulation tools to help?
- What were some pitfalls and lessons learned from the 6.012 design project?

- What did we learn in 6.012, and where do I go from here?

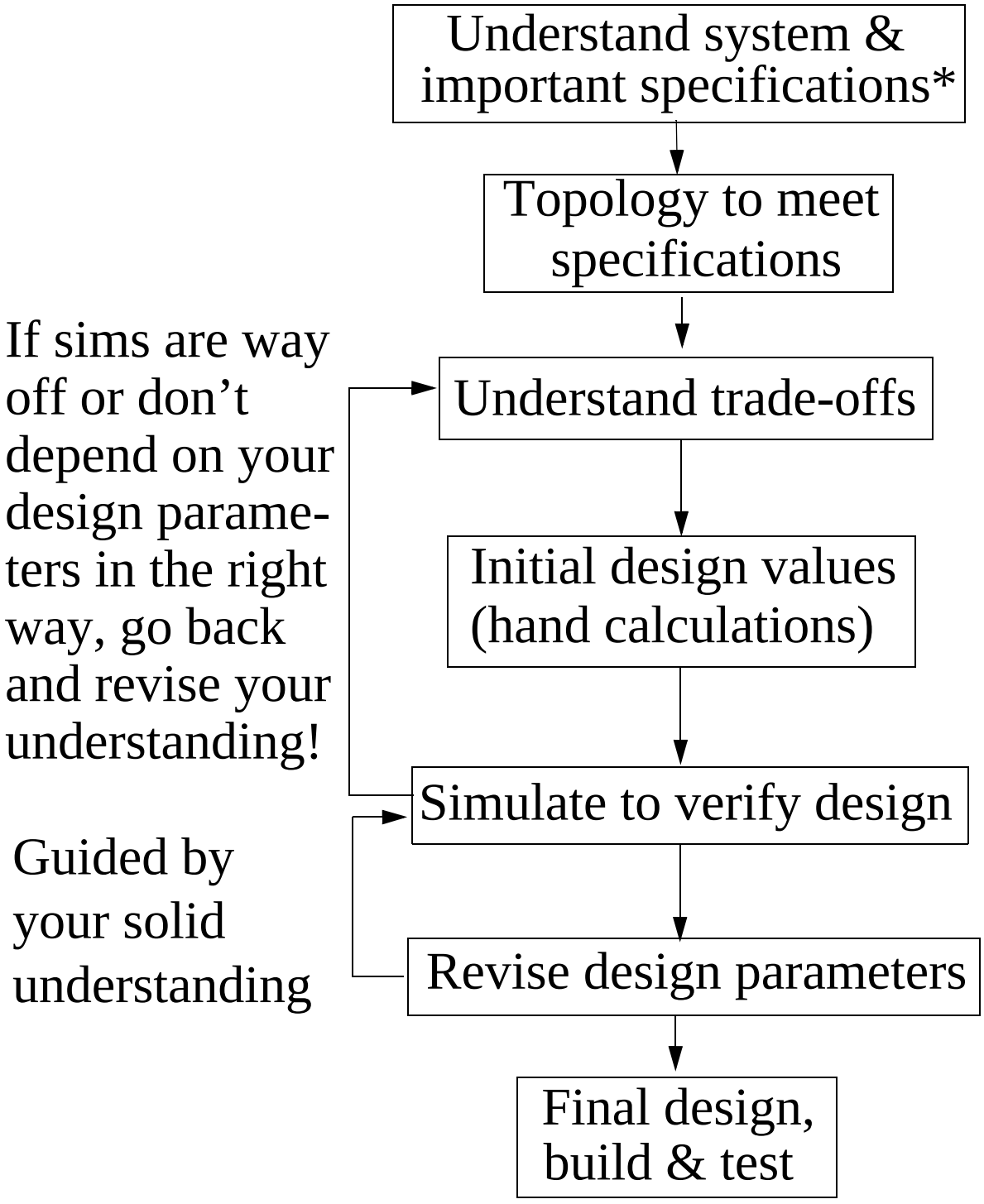
1. Design Problems

Design a circuit or system to meet real-world specifications.

A few modern-day examples:

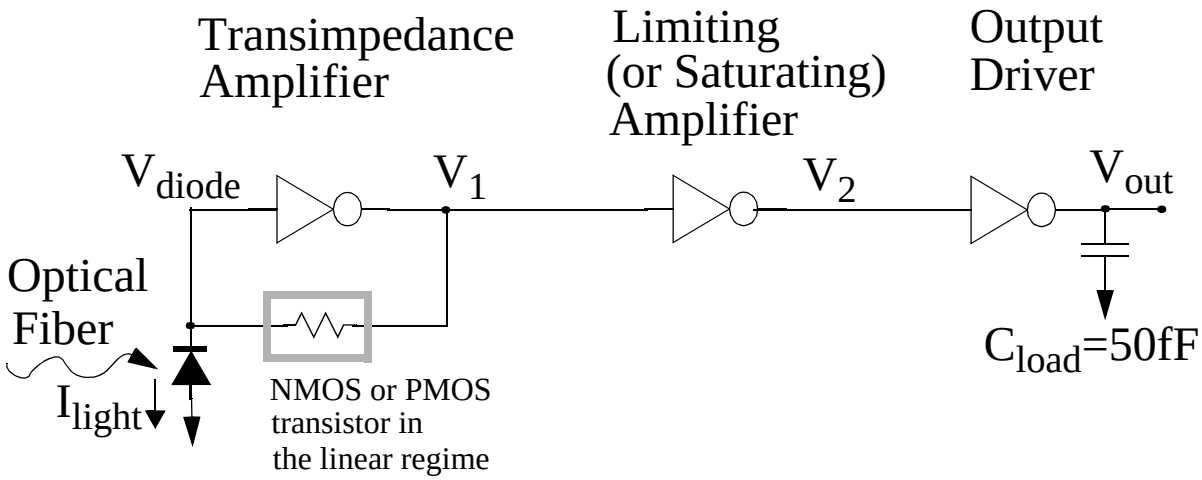
- Optical receiver for communications (6.012)
- Imagers for digital cameras (Pablo)
- Circuits for cell phones (Susan)
- Amplifier for ultrasound systems
- TV tuner, cable modem
- Microprocessors

Generic Design Process



* Engineering principle: You can't have every-thing! Must understand what's *most* important and then make trade-offs in your design.

2. Optical Receiver Design Project



Key Specs:

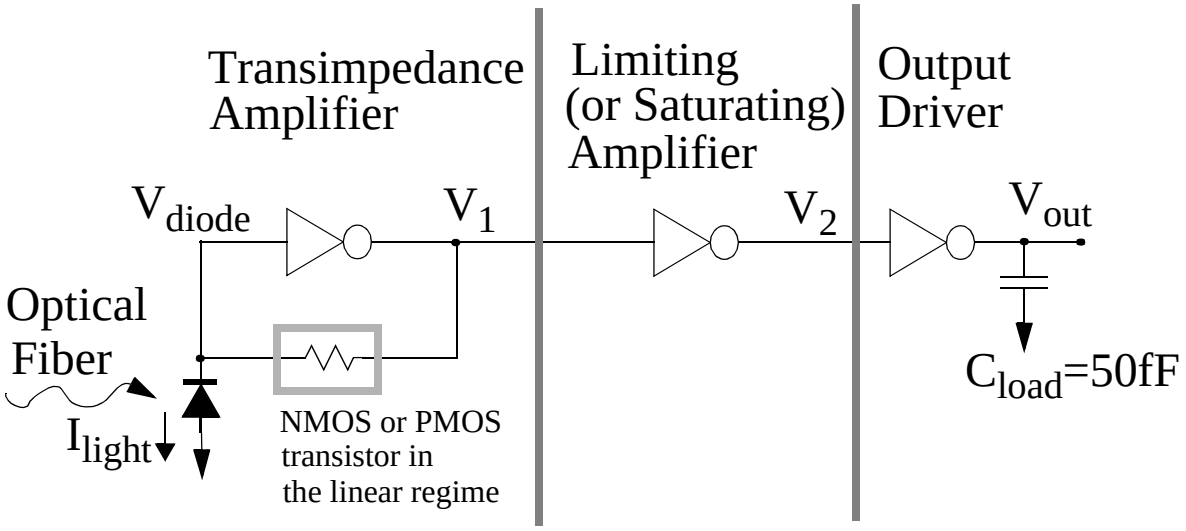
- V_1 large swing
- V_{diode} small swing
- A_v large
- V_M
- t_p low
- NM high

- Minimize power & area where possible.

There are 28 W's and L's in this problem, and at least 6 key specs.

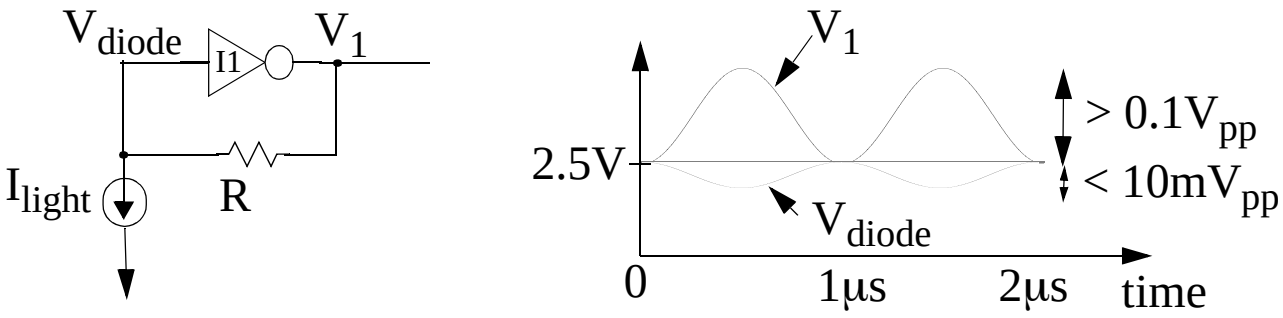
How do we get started??

Getting Started

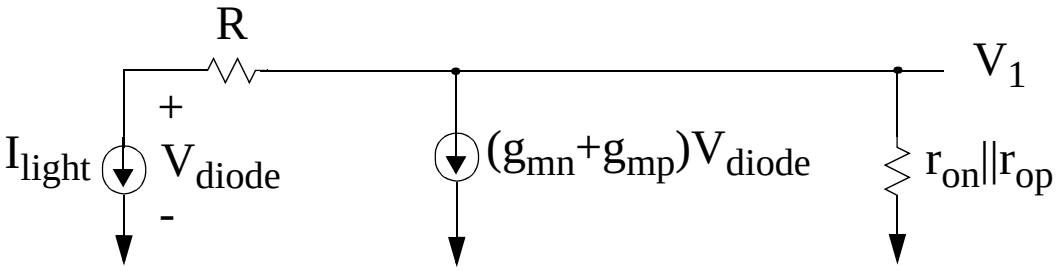


- Define boundaries between the stages.
- As long as we use a realistic input driving source and output load, we can design each stage independent of the others.
- Analyze each stage and understand how the specifications change with the W's and L's.
- Design the W's and L's to meet the specifications.
- Put the stages back together and verify the complete design.

Transimpedance Amplifier

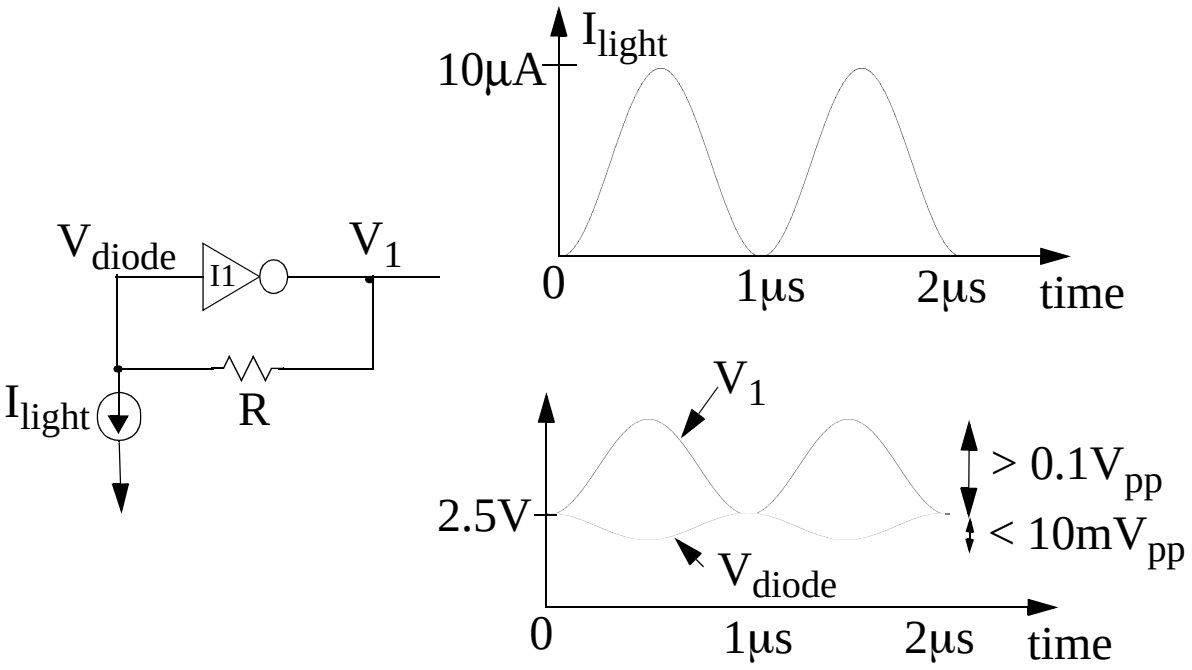


- Since V_1 and V_{diode} have small swing, the small signal model is a good/bad model for the transimpedance amplifier.

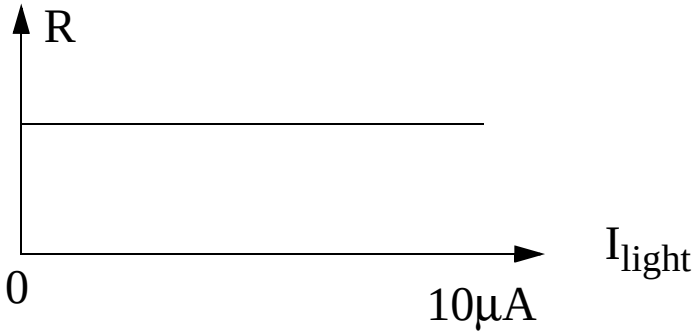


- Does $V_1=A_vV_{diode}$, $V_{diode}=V_1/A_v$ where $A_v=-(g_{mn}+g_{mp})r_{on}||r_{op}$?
- This says for V_{diode} small, A_v means
- This is true for an open-loop inverter, but is this true for a transimpedance amplifier??
- Need to consider closed loop system:

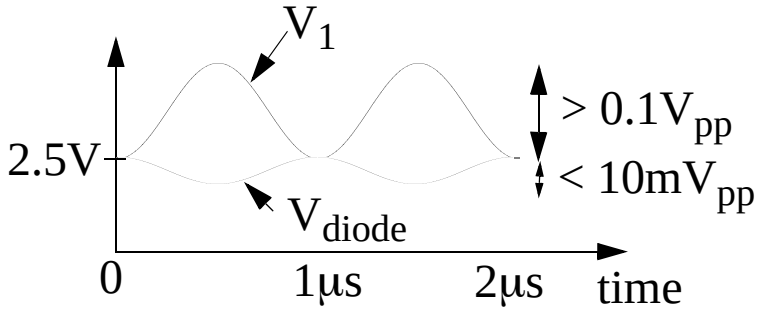
How do we implement the resistor?

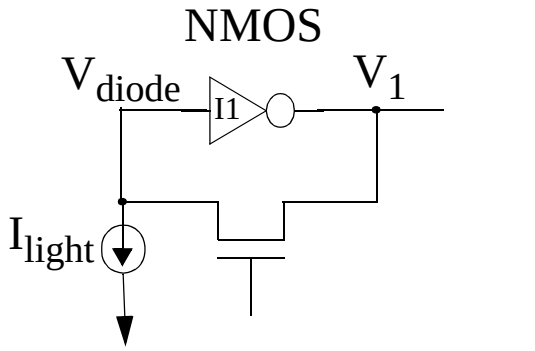


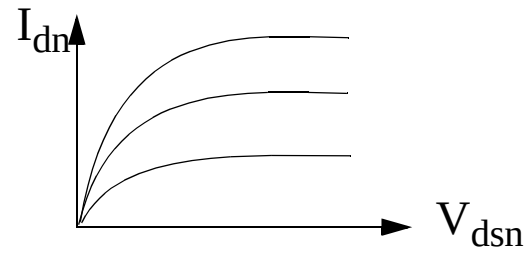
- Want R as constant as possible over the range of I_{light} values, i.e. R as linear as possible.

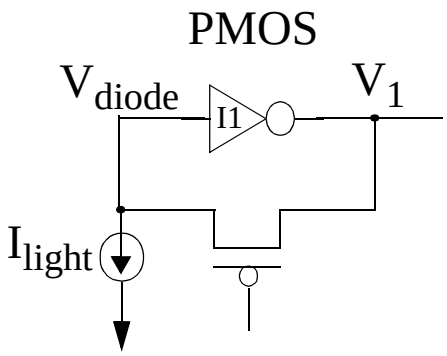


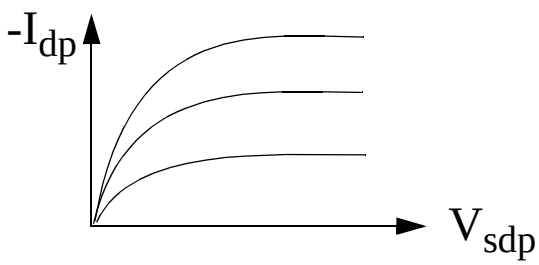
NMOS vs. PMOS











Where do the transistors look most like resistors?

V_{ds} $V_{gs}-V_{tn}$

$V_{gs}-V_{tn}$ =

$I_{light}=0$

$I_{light}=10\mu A$

V_{dsmax}=

V_{sd} $V_{sg}+V_{tp}$

$V_{sg}+V_{tp}$ =

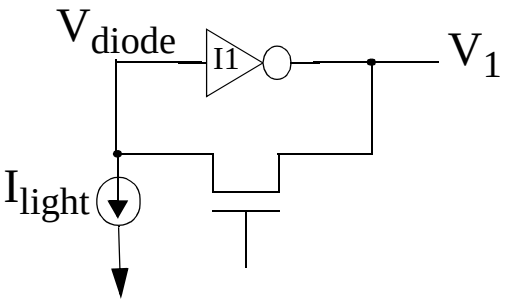
$I_{light}=0$

$I_{light}=10\mu A$

V_{sdmax}=

Are we in danger of going out of the linear regime?

NMOS



In the linear regime,

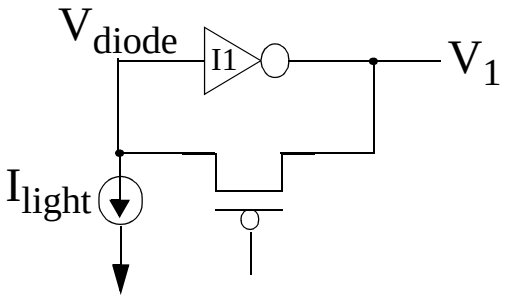
$$I_{dn} = \frac{W}{L}\mu_n C_{ox}\left(V_{gs} - V_{tn} - \frac{V_{ds}}{2}\right)V_{ds}$$

$$\frac{1}{R} = \frac{dI_{dn}}{dV_{ds}} = \frac{W}{L}\mu_n C_{ox}(V_{gs} - V_{tn} - V_{ds})$$

$$R = \frac{1}{\frac{W}{L}\mu_n C_{ox}(V_{gs} - V_{tn} - V_{ds})}$$

$$R = \frac{1}{\frac{W}{L}\mu_n C_{ox}(V_{gd} - V_{tn})}$$

PMOS



In the linear regime,

$$-I_{dp} = \frac{W}{L}\mu_p C_{ox}\left(V_{sg} + V_{tp} - \frac{V_{sd}}{2}\right)V_{sd}$$

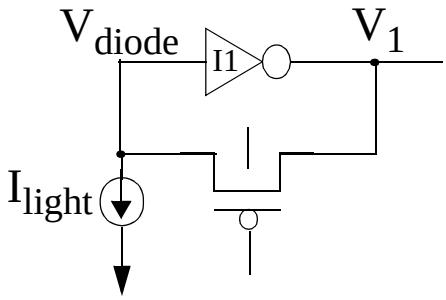
$$\frac{1}{R} = \frac{-dI_{dp}}{dV_{sd}} = \frac{W}{L}\mu_p C_{ox}(V_{sg} + V_{tp} - V_{sd})$$

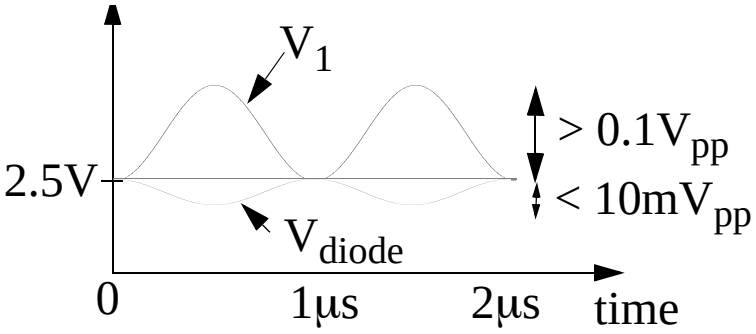
$$R = \frac{1}{\frac{W}{L}\mu_p C_{ox}(V_{sg} + V_{tp} - V_{sd})}$$

$$R = \frac{1}{\frac{W}{L}\mu_p C_{ox}(V_{dg} + V_{tp})}$$

What makes R non-linear?

What about the bulk connection?





Choices: G D S V_{dd} Ground

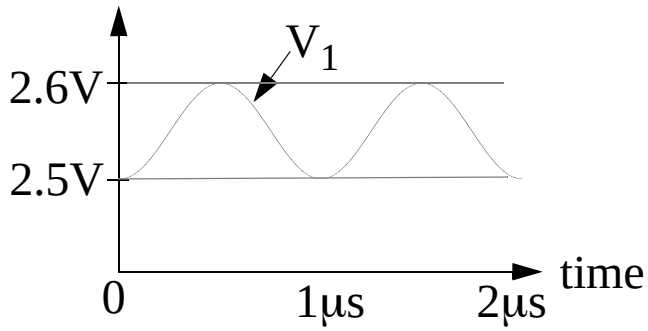
If we choose V_{tp}

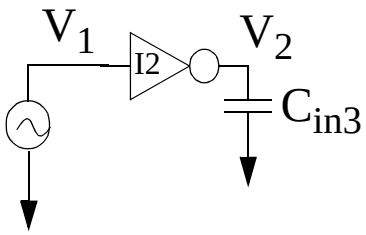
V_{tp} with $|V_{sb}|$

$$V_{tp} = V_{tpo} - \gamma\sqrt{2\phi_n + |V_{sb}|} - \sqrt{2\phi_n}$$

$$R = \frac{1}{\frac{W}{L}\mu_p C_{ox}(V_{dg} - \gamma\sqrt{2\phi_n + |V_{sb}|} + V_{tpo} - \sqrt{2\phi_n})}$$

High Gain Stage





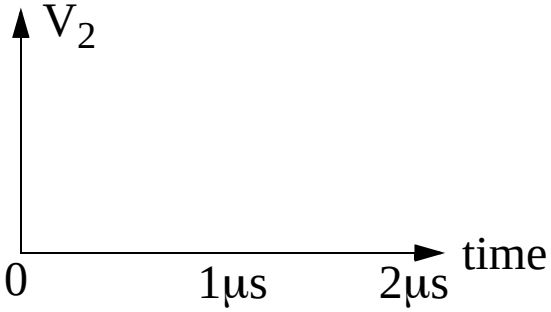
Key specs: V_M, A_v

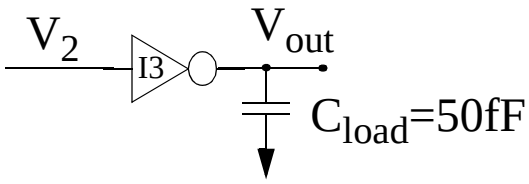
V_M:

$A_v=-(g_{mn}+g_{mp})r_{on}\|r_{op}$

How does A_v depend on W and L?

Output Driver



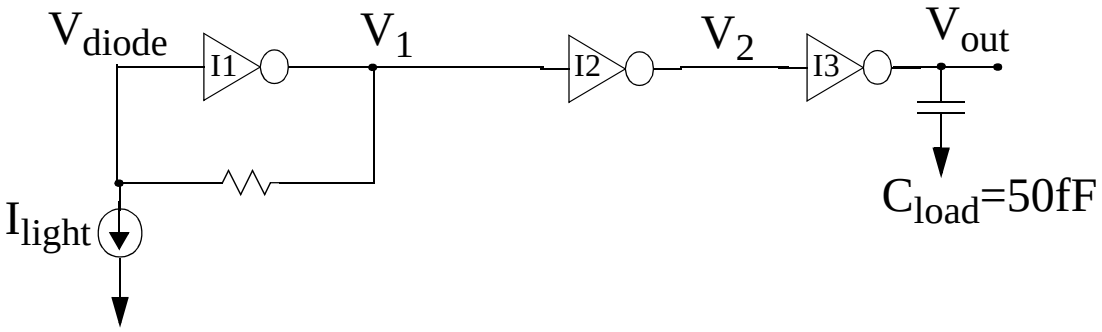


Key specs: NM, t_p

NM:

How does t_p depend on W/L?

Power Dissipation



A. Dynamic Power

- Dynamic power dissipated by charging and discharging capacitors over time.
- Dynamic Power: $P = C V_{sw}^2 f$

	V_{diode}	V_1	V_2	V_3
V_{sw}				

B. Static Power

- Static power is current flowing all the time.
- $P=V_{DD}*I$

Which stage has constant current?

Going back

After we've done the first pass design, go back and try to minimize power and area.

Minimum area:

Minimum static power:

Minimum dynamic power:

Using HSPICE to verify the design

Simulators:

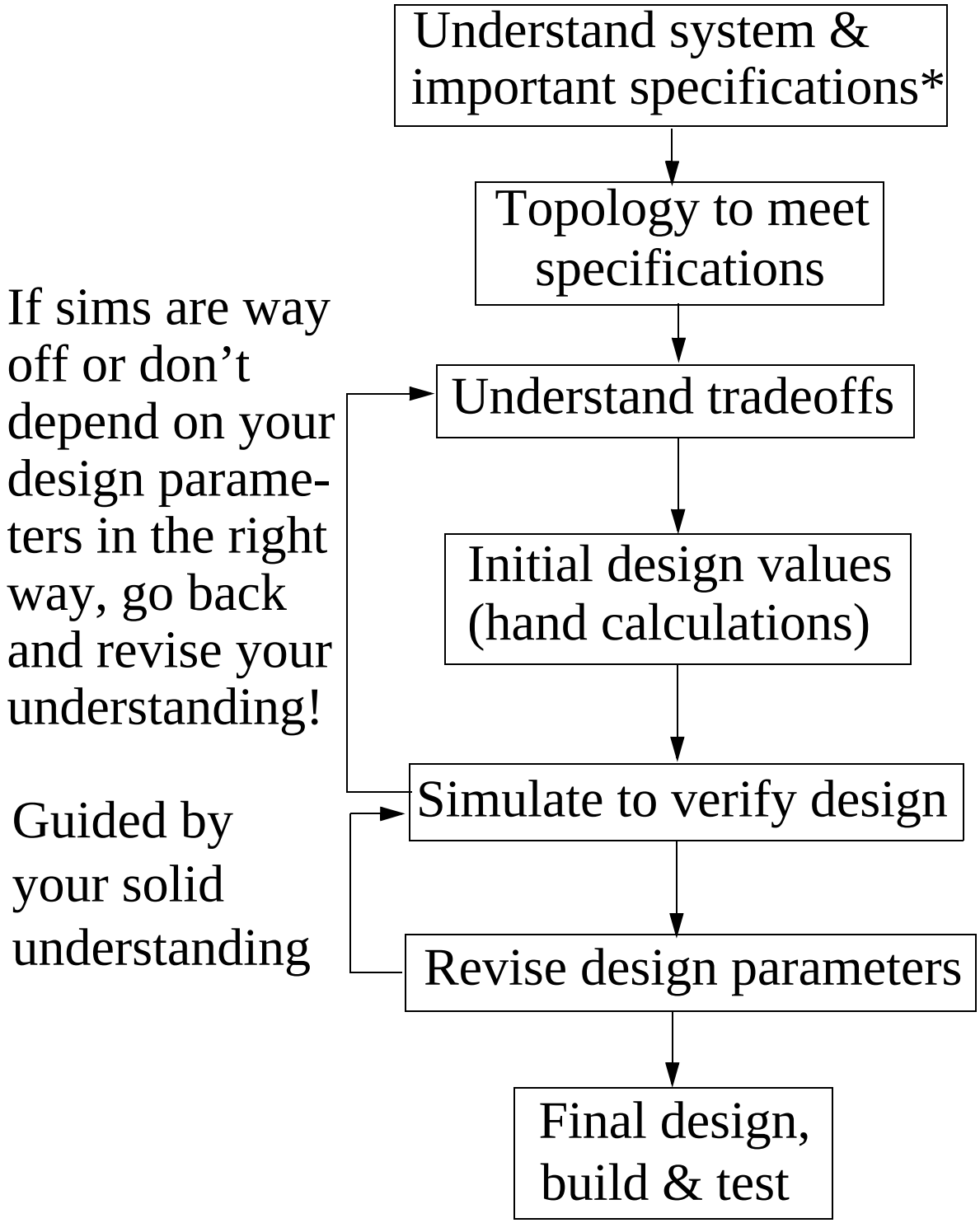
- Model 2nd and 3rd order effects, all the things that are hard to calculate by hand.
- Allow final tweaking of parameters to ensure the specs are met.
- Verify the design before we spend lots of $$ to implement it.

Build *margin* into the design for inadequacies in device modeling, process variations, temperature variations, etc.

Simulators do not:

- Replace our understanding of the circuit! If the simulator doesn't show the dependency we expect, we need to revise our understanding.

Design Process



3. Lessons learned from 6.012 design project

- Break large problems into smaller pieces.
- You can’t have everything - need to understand the trade-offs in your design.
- Simulators are an essential tool to verify your design *and* your understanding.
- Design problems have many issues to think about, it’s important to get an early start.
- State-of-the art tools have bugs, the networks will crash, customers will change specs, etc. Things will always come up...
- There’s no procrastinating in this business!

4. Wrap up of 6.012

□ *The amazing properties of Si*

- two types of carriers: electrons and holes [although can make good electronic devices with just one, *i.e.* MESFET; but can't do CMOS without two]
- carrier concentrations can be controlled over many orders of magnitude and in short length scales by addition of dopants
- carrier concentrations can be controlled electrostatically
- carriers are fast:
  - electrons can cross $L = 0.1\ \mu m$ in about:

$$\tau = \frac{L}{v_e} = \frac{0.1\ \mu m}{10^7\ cm/s} = 1\ ps$$

  - high current density:

$$J_e = qnv_e = 1.6 \times 10^{-19}\ C \times 10^{17}\ cm^{-3} \times 10^7\ cm/s$$
$$= 1.6 \times 10^5\ A/cm^2$$

    $\Rightarrow$ high current drivability to capacitance ratio
- extraordinary physical and chemical properties

□ *The amazing properties of Si MOSFET*

- ideal properties of Si/SiO_2 interface: can drive surface all the way from accumulation to inversion [not possible in GaAs, for example]
- performance improves as MOSFET scales down in size; as $L,\ W \downarrow$:
  - current:
$$I_D = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_T)^2 \ unchanged$$
  - capacitance:
$$C_{gs} = WLC_{ox} \downarrow\downarrow$$
  - figure of merit for device switching delay:
$$\frac{C_{gs}V_{DD}}{I_D} = L^2\frac{2V_{DD}}{\mu(V_{GS} - V_T)^2} \downarrow\downarrow$$
- No gate current.
- V_T can be engineered.
- MOSFETs come in two types: NMOS and PMOS.
- Easy to integrate.

□ *The amazing properties of Si CMOS*

- Rail-to-rail logic: logic levels are 0 and V_{DD}.
- No power consumption while idling in any logic state.
- Scales well.

  As $L,\ W \downarrow$:

  – Power consumption (all dynamic):

$$P_{diss} = fC_L V_{DD}^2 \propto fWLC_{ox}V_{DD}^2 \downarrow\downarrow$$

  – Propagation delay:

$$t_P \propto \frac{C_L V_{DD}}{\frac{W}{L}\mu C_{ox}(V_{DD} - V_T)^2} \downarrow\downarrow$$

  – Logic density:

$$Density \propto \frac{1}{A} = \frac{1}{WL} \uparrow\uparrow$$

□ All this is enabling the *electronics revolution*:

- *exponential growth* in complexity and functionality of integrated circuits [Moore's Law]
- *exponential decrease* in power per function and cost per function of integrated circuits
- profound penetration of IC technology into all aspects of human society

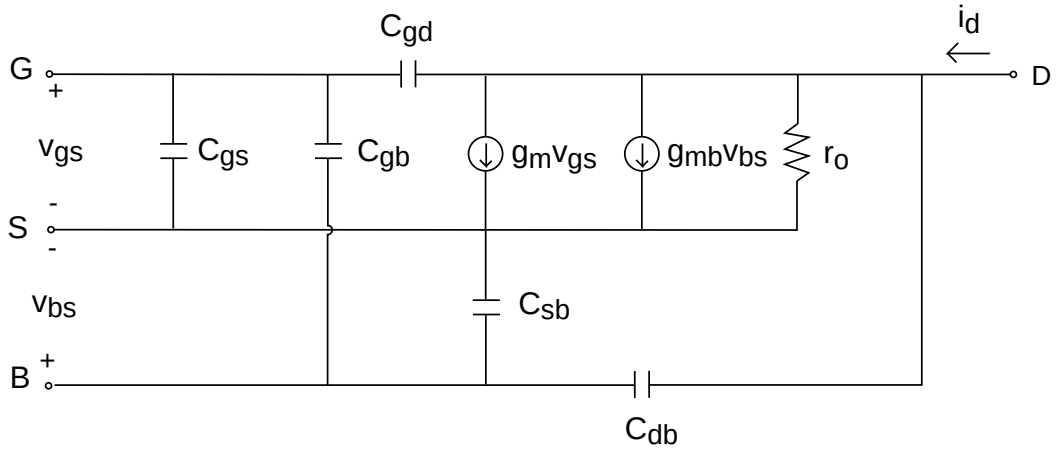
□ Circuit design lessons from 6.012:

1. Importance of optimum level of abstraction:

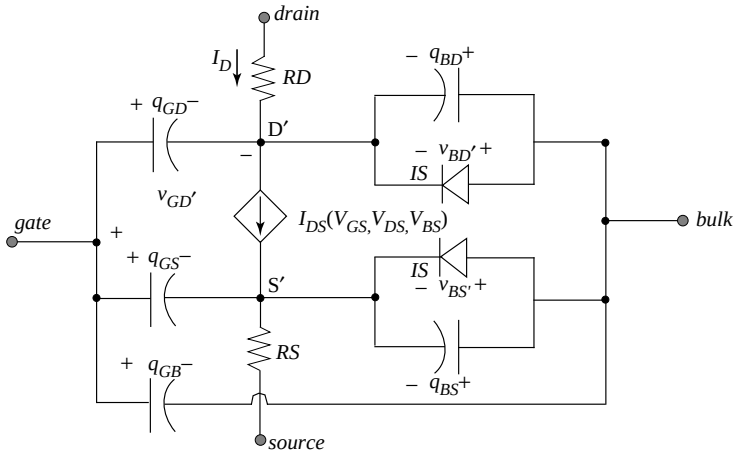
- device physics equations, *i.e.*:

$$I_D = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_T)^2, \ etc.$$

- device equivalent circuit models, *i.e.*:



- device SPICE models, *i.e.*:



2. Many considerations in circuit design:

   - multiple performance specs:
     - in analog systems: gain, bandwidth, power consumption, swing, noise, etc.
     - in digital systems: propagation delay, power, ease of logic synthesis, noise, etc.
   - need to be immune to temperature variations and device parameter variations (*i.e.*: differential amplifier)
   - must choose suitable technology: CMOS, BJT, CBJT, BiCMOS, etc.
   - must avoid costly components (*i.e.:* resistors, capacitors)

3. Trade-offs:

   - gain-bandwidth trade-off in amplifiers (*i.e.*: Miller effect)
   - performance-power trade-off (*i.e.*: delay in logic circuits, gain in amplifiers)
   - performance-cost trade-off (cost=design complexity, Si area, more aggressive technology)
   - accuracy-complexity trade-off in modeling

□ Exciting times ahead in Si IC technology:

- *analog electronics* (since $\sim 50's$): amplifiers, mixers, oscillators, DAC, ADC, etc.
- *digital electronics* (since $\sim 60's$): computers, microcontrollers, random logic, DSP
- *solid-state memory* (since $\sim 60's$): dynamic random-access memory, non-volatile RAM
- *energy conversion* (since $\sim 70's$): solar cells, photodetectors
- *power control* (since $\sim 70's$): "smart" power
- *communications* (since $\sim 80's$): VHF, UHF, RF front ends, modems, fiber-optic systems
- *sensing, imaging* (since $\sim 80's$): CCD cameras, CMOS cameras, many kinds of sensors
- *micro-electro-mechanical systems* (since $\sim 90's$): accelerometers, movable mirror displays
- *biochip* (from ~ 2000): DNA sequencing, μfluidics
- *vacuum microelectronics* (from ~ 2000?): field-emitter displays
- *???????* (microreactors, microturbines, etc.)

□ Exciting times ahead in circuit design too:

- Numbers of transistors available outstrips ability to design by 3 to 1!
- Operational frequency of logic, analog, and communications circuits increasing very fast.
- Operational voltage shrinking quickly.
- New device technologies: GaAs HEMT, InP HBT, etc.

More subjects in microelectronics at MIT

- *6.152J - Microelectronics Processing Technology.* Theory and practice of IC technology. Carried out in clean rooms of Microsystems Technology Laboratories. Fulfills Institute or EECS Lab requirement. Fall and Spring.
- *6.301 - Solid-State Circuits.* Analog circuit design. Design project. Spring.
- *6.334 - Power Electronics.* Power electronics devices and circuits. Spring. H-level.
- *6.374 - Analysis and Design of Digital Integrated Circuits.* Digital circuit design. Design projects. Fall. H-level.
- *6.720J - Integrated Microelectronic Devices.* Microelectronic device physics and design. Emphasis on MOSFET. Design project. Fall. H-level.
- *6.775 - Design of Analog MOS LSI.* Analog circuit design based on MOSFETs. Design project. Fall. H-level.