Lecture 14 - Digital Circuits (III)

CMOS

April 1, 2003

Contents:

1. Complementary MOS (CMOS) inverter: introduction

2. CMOS inverter: noise margins

3. CMOS inverter: propagation delay

Reading assignment:

Howe and Sodini, Ch. 5, §5.4

Announcements:

- Final exam: May 23, 1:30-4:30 (Walker)

- HSPICE tutorial by Susan Luschas: April 1, 7:30-9:30 (Rm. 3-133)

- Webcast of Lecture 13 available (see course website)

Key questions

- How does CMOS work?

- What is special about CMOS as a logic technology?

- What are the key design parameters of a CMOS inverter?

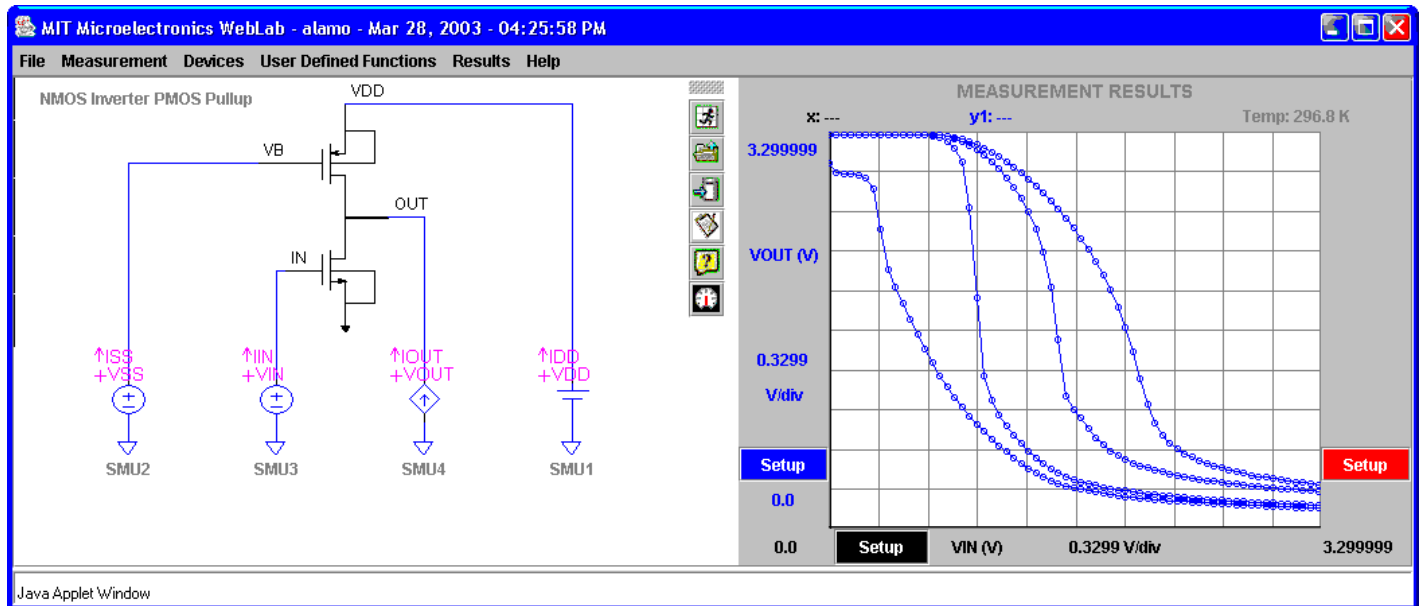- How can one estimate the propagation delay of a CMOS inverter?

Screen shots of NMOS inverters (currently in WebLab):

□ NMOS inverter with resistor pull-up
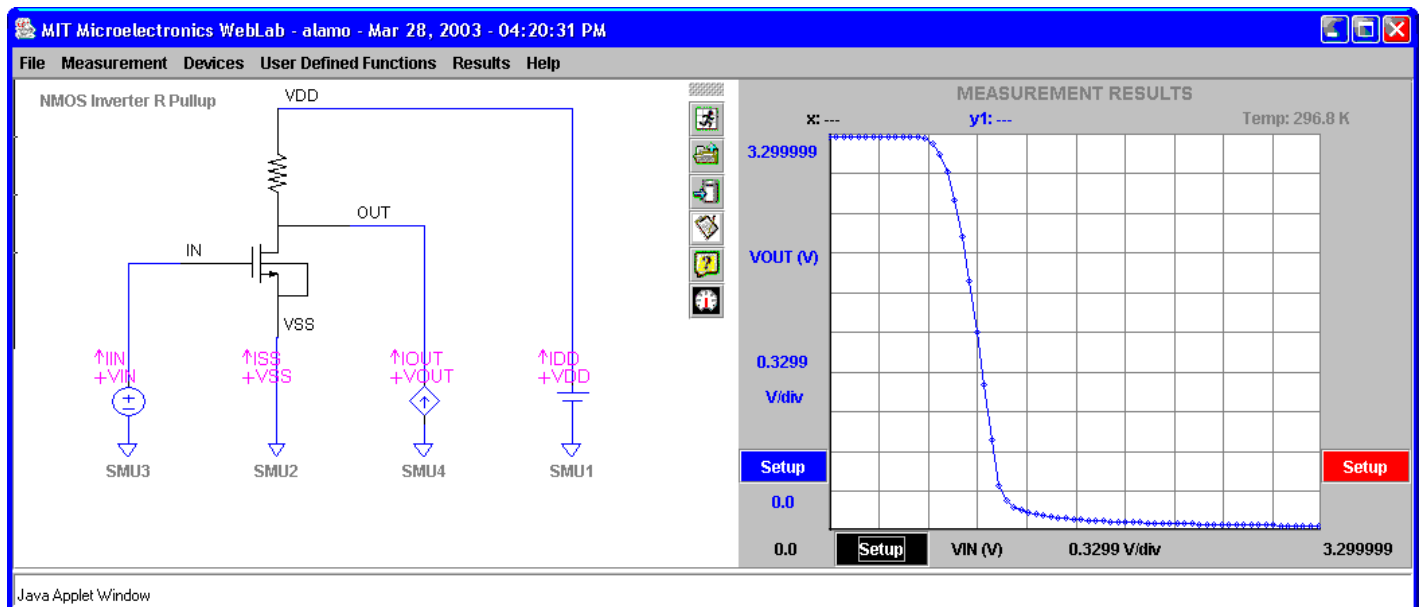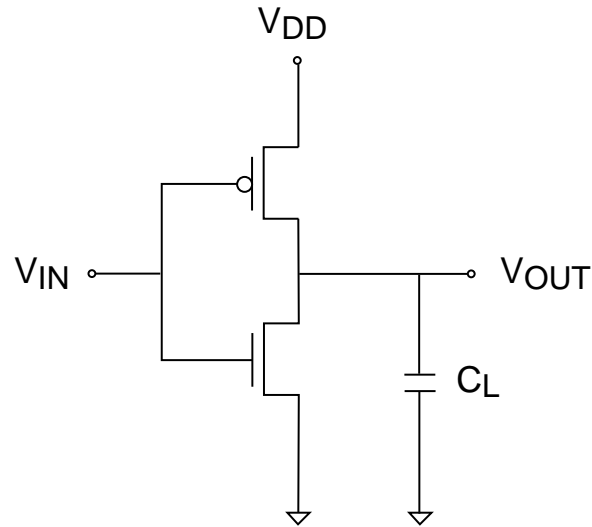

Main problem: slow pull up

□ NMOS inverter with current source pull-up

Main problem: DC current in one logic state

1. Complementary MOS (CMOS) Inverter

Circuit schematic:

Basic operation:

• $V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD}$

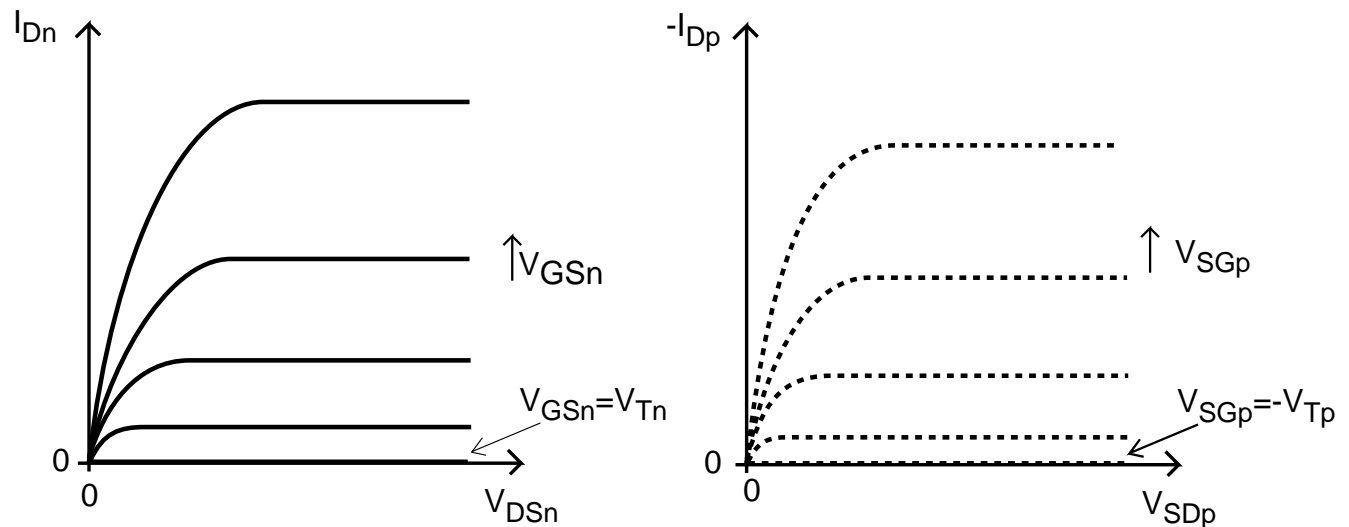$\qquad V_{GSn} = 0 < V_{Tn} \Rightarrow$ NMOS OFF

$\qquad V_{SGp} = V_{DD} > -V_{Tp} \Rightarrow$ PMOS ON

• $V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0$

$\qquad V_{GSn} = V_{DD} > V_{Tn} \Rightarrow$ NMOS ON

$\qquad V_{SGp} = 0 < -V_{Tp} \Rightarrow$ PMOS OFF
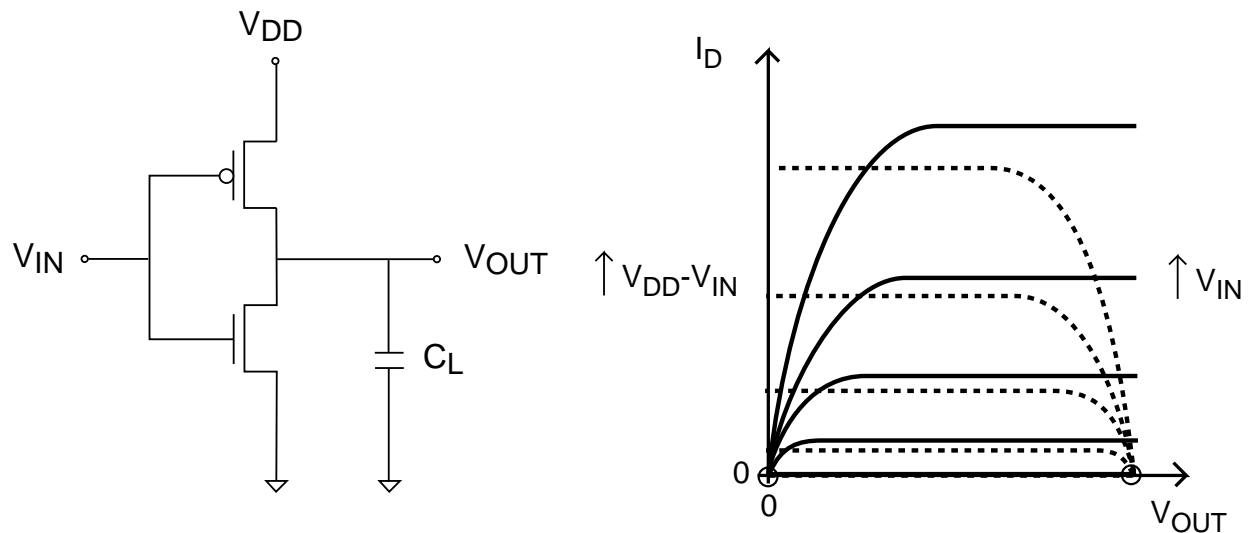
Output characteristics of both transistors:

Note:

$$V_{IN} = V_{GSn} = V_{DD} - V_{SGp} \Rightarrow V_{SGp} = V_{DD} - V_{IN}$$

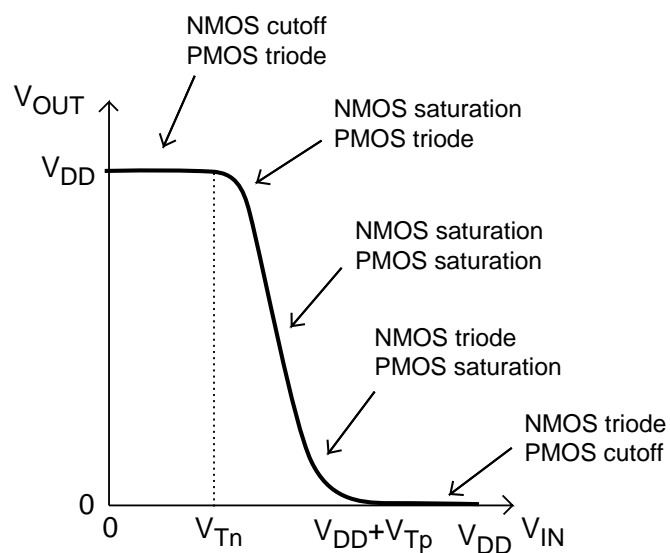$$V_{OUT} = V_{DSn} = V_{DD} - V_{SDp} \Rightarrow V_{SDp} = V_{DD} - V_{OUT}$$

$$I_{Dn} = -I_{Dp}$$

Combine into single diagram of I_D vs. V_{OUT} with V_{IN} as parameter.

$\star$ *no current while idling in any logic state.*
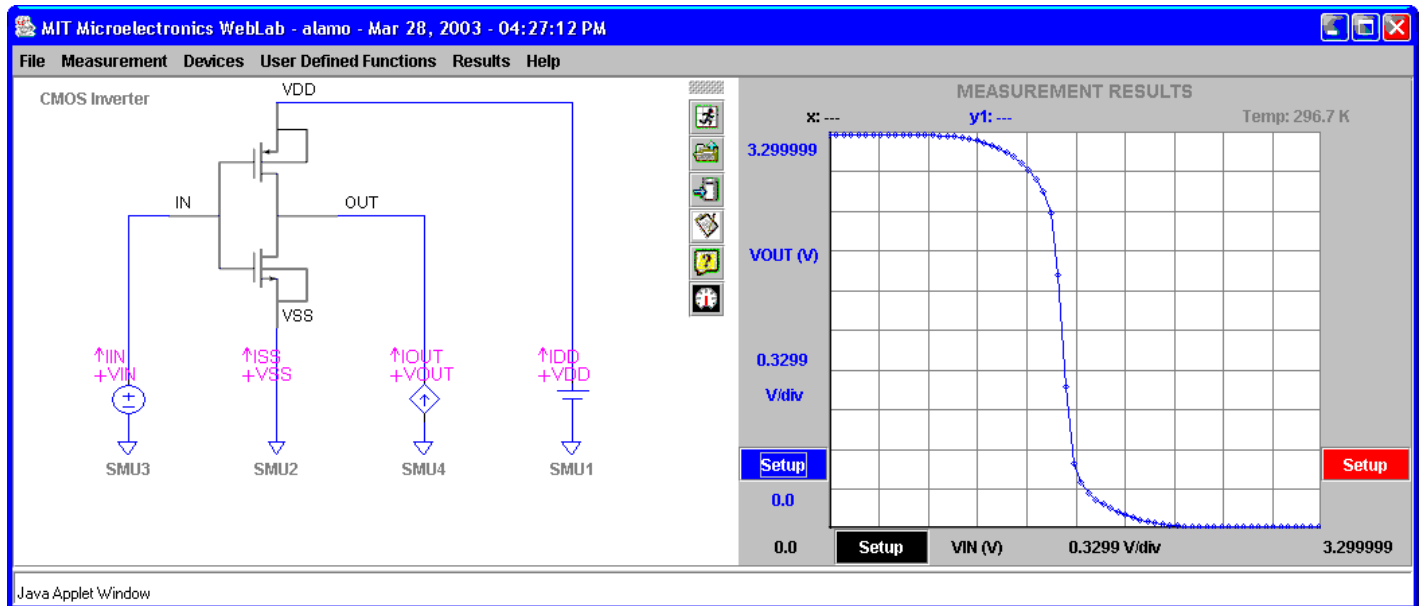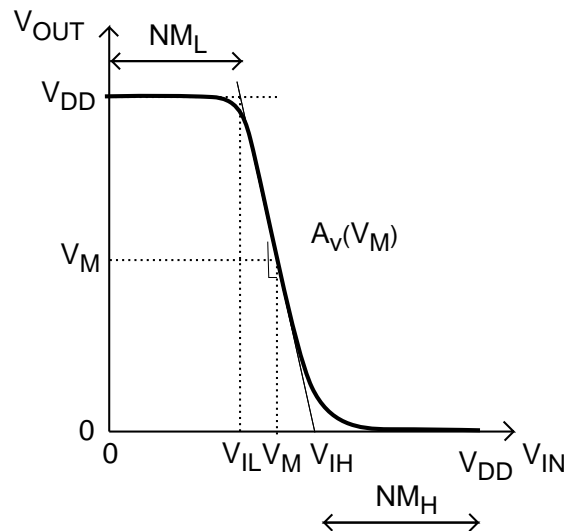
Transfer function:

$\star$ *"rail-to-rail" logic: logic levels are* 0 *and* V_{DD}

$\star$ *high* $|A_v|$ *around logic threshold* $\Rightarrow$ good noise margins

Transfer characteristics of CMOS inverter in WebLab:

2. CMOS inverter: noise margins

- Calculate V_M
- Calculate $A_v(V_M)$
- Calculate NM_L and NM_H

□ **Calculate** V_M $(V_M = V_{IN} = V_{OUT})$

At V_M both transistors saturated:

$$I_{Dn} = \frac{1}{2}\frac{W_n}{L_n}\mu_n C_{ox}(V_M - V_{Tn})^2$$

$$-I_{Dp} = \frac{1}{2}\frac{W_p}{L_p}\mu_p C_{ox}(V_{DD} - V_M + V_{Tp})^2$$

Define:

$$k_n = \frac{W_n}{L_n}\mu_n C_{ox}, \quad k_p = \frac{W_p}{L_p}\mu_p C_{ox}$$

Since:

$$I_{Dn} = -I_{Dp}$$

Then:

$$\frac{1}{2}k_n(V_M - V_{Tn})^2 = \frac{1}{2}k_p(V_{DD} - V_M + V_{Tp})^2$$

Solve for V_M:

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

Usually, V_{Tn} and V_{Tp} fixed and $V_{Tn} = -V_{Tp}$

$$\Rightarrow V_M \text{ engineered through } k_p/k_n \text{ ratio}$$

- Symmetric case: $k_n = k_p$

$$V_M = \frac{V_{DD}}{2}$$

This implies:

$$\frac{k_p}{k_n} = 1 = \frac{\frac{W_p}{L_p}\mu_p C_{ox}}{\frac{W_n}{L_n}\mu_n C_{ox}} \simeq \frac{\frac{W_p}{L_p}\mu_p}{\frac{W_n}{L_n}2\mu_p} \Rightarrow \frac{W_p}{L_p} \simeq 2\frac{W_n}{L_n}$$

Since usually $L_p \simeq L_n \Rightarrow W_p \simeq 2W_n$.

- Asymmetric case: $k_n \gg k_p$, or $\frac{W_n}{L_n} \gg \frac{W_p}{L_p}$

$$V_M \simeq V_{Tn}$$

NMOS turns on as soon as V_{IN} goes above V_{Tn}.

- Asymmetric case: $k_n \ll k_p$, or $\frac{W_n}{L_n} \ll \frac{W_p}{L_p}$
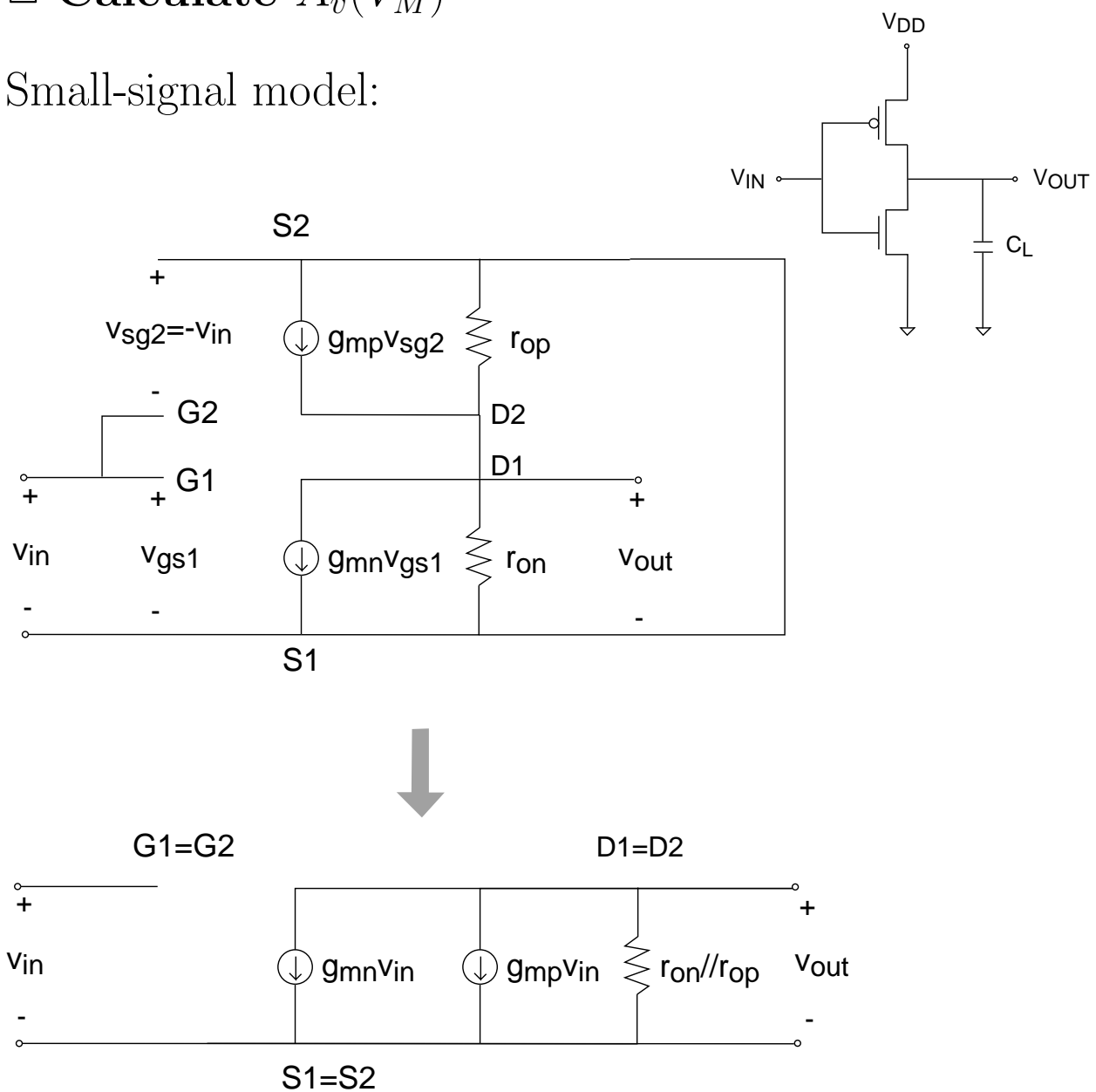
$$V_M \simeq V_{DD} + V_{Tp}$$

PMOS turns on as soon as V_{IN} goes below $V_{DD} + V_{Tp}$.

Can engineer V_M anywhere between V_{Tn} and $V_{DD} + V_{Tp}$.
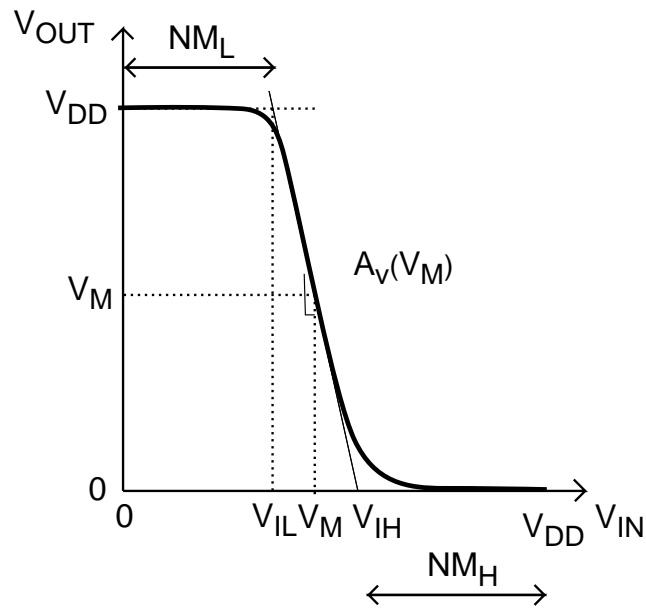
☐ **Calculate** $A_v(V_M)$

Small-signal model:

$$A_v = -(g_{mn} + g_{mp})(r_{on}//r_{op})$$

This can be rather large.

□ **Noise margins**

- Noise-margin-low:
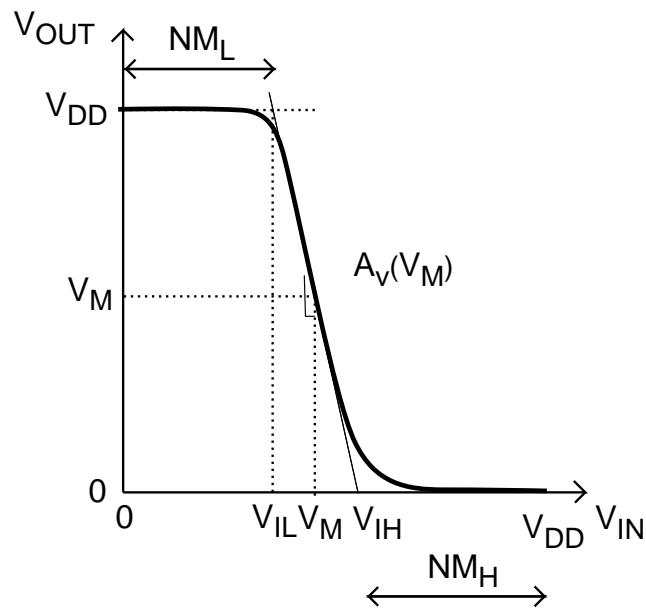
$$V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

Therefore:

$$NM_L = V_{IL} - V_{OL} = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

In the limit of $|A_v| \to \infty$:

$$NM_L \to V_M$$

- Noise-margin-high:

$$V_{IH} = V_M(1 + \frac{1}{|A_v|})$$

and

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_M(1 + \frac{1}{|A_v|})$$

In the limit of $|A_v| \to \infty$:
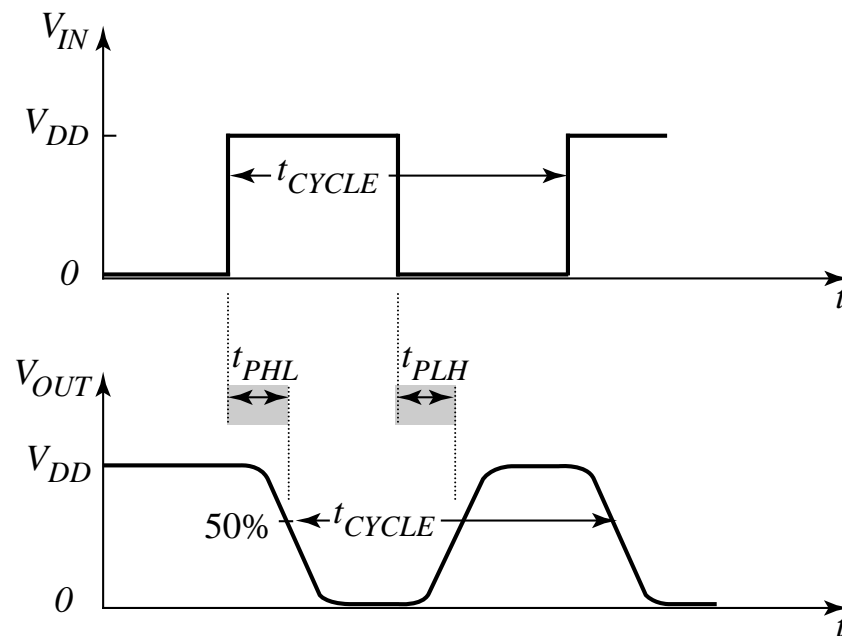
$$NM_H \to V_{DD} - V_M$$

3. CMOS inverter: propagation delay

Inverter propagation delay: time delay between input and output signals; key figure of merit of logic speed.

Typical propagation delays: $< 1 \ ns$.

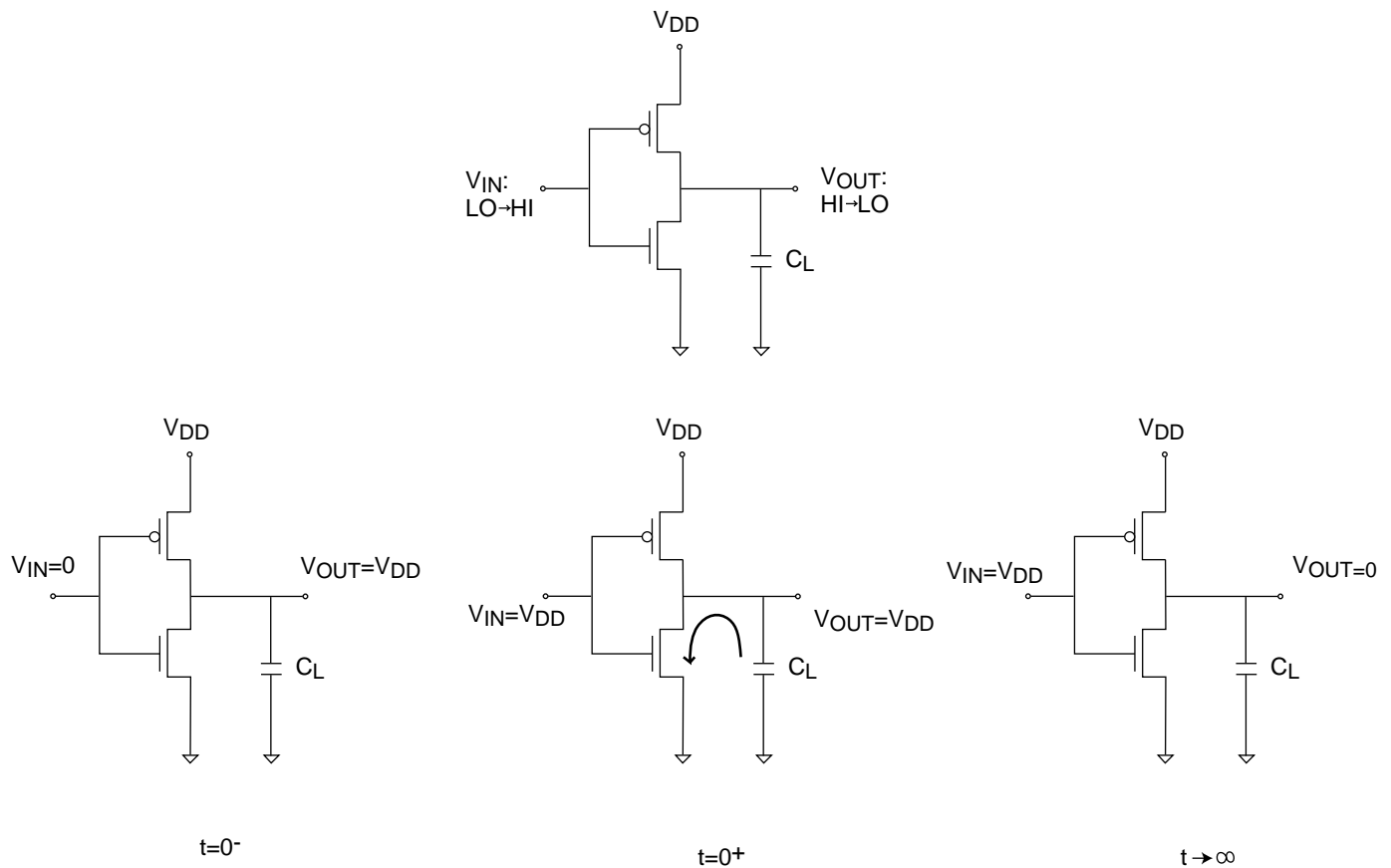Complex logic system has 20-50 propagation delays per clock cycle.

Estimation of t_p: use square-wave at input

Average propagation delay:

$$t_p = \frac{1}{2}(t_{PHL} + t_{PLH})$$

□ Propagation delay high-to-low:

VDD

V$_{IN}$:
LO→HI

V$_{OUT}$:
HI→LO

C$_L$

VDD

V$_{IN}$=0

V$_{OUT}$=V$_{DD}$

C$_L$

t=0$^-$

VDD

V$_{IN}$=V$_{DD}$

V$_{OUT}$=V$_{DD}$

C$_L$

t=0$^+$

VDD

V$_{IN}$=V$_{DD}$

V$_{OUT}$=0

C$_L$

t→∞

During early phases of discharge, NMOS is saturated and PMOS is cut-off.

Time to discharge *half* of C_L:

$$t_{PHL} \simeq \frac{\frac{1}{2}\text{charge of } C_L @ t = 0^-}{\text{discharge current}}$$
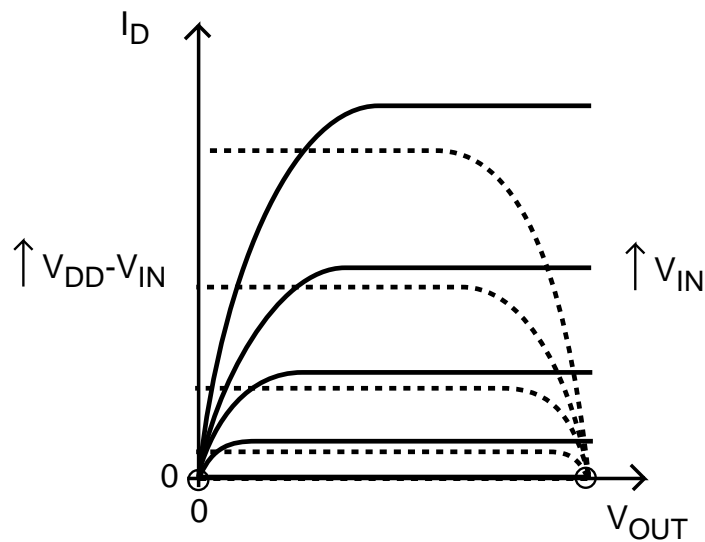
Charge in C_L at $t = 0^-$:

$$Q_L(t = 0^-) = C_L V_{DD}$$

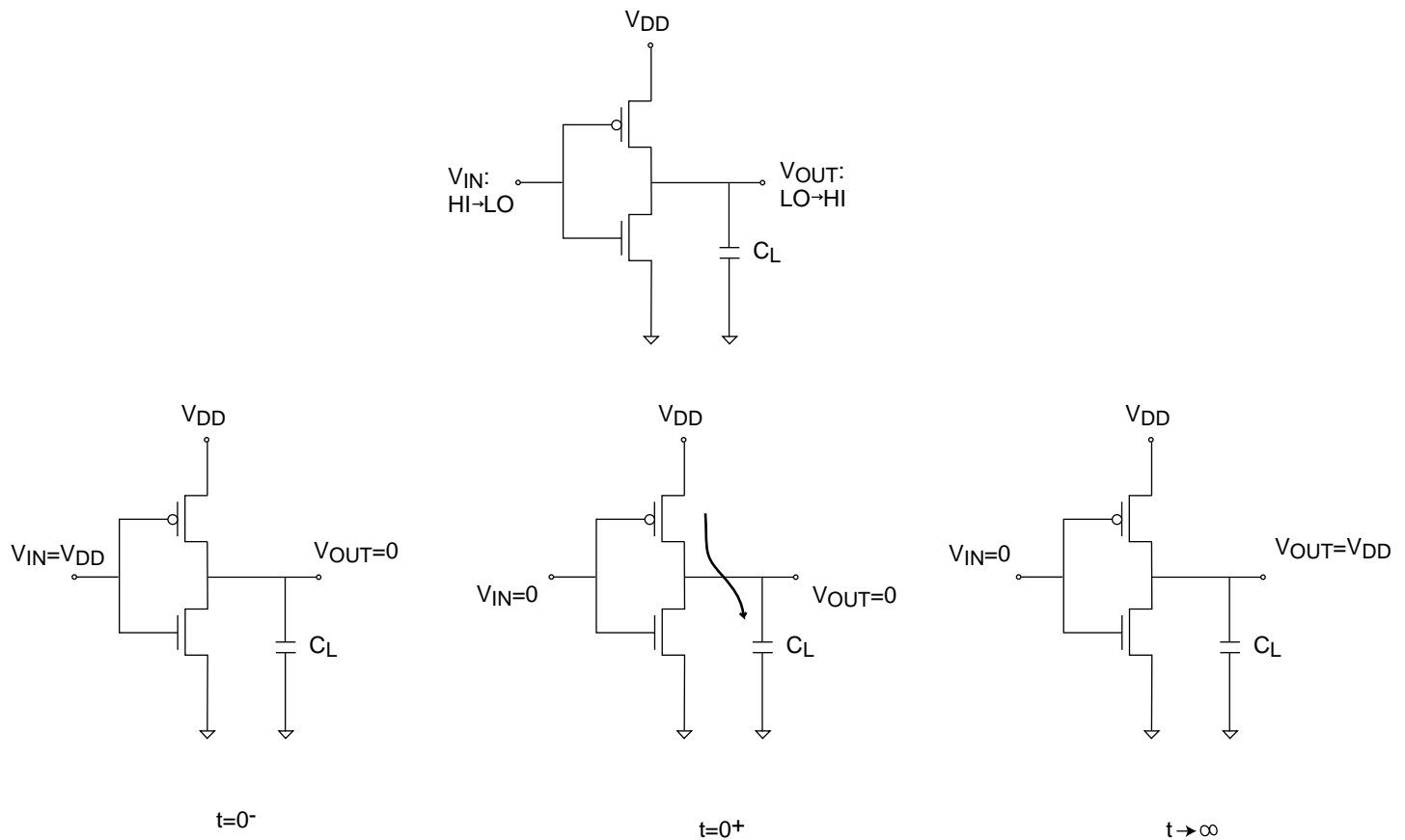Discharge current (NMOS in saturation):

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}(V_{DD} - V_{Tn})^2$$

Then:

$$t_{PHL} \simeq \frac{C_L V_{DD}}{\frac{W_n}{L_n}\mu_n C_{ox}(V_{DD} - V_{Tn})^2}$$

□ Propagation delay low-to-high:

During early phases of charge, PMOS is saturated and NMOS is cut-off.

Time to charge *half* of C_L:

$$t_{PLH} \simeq \frac{\frac{1}{2}\text{charge of } C_L @ t = \infty}{\text{charge current}}$$
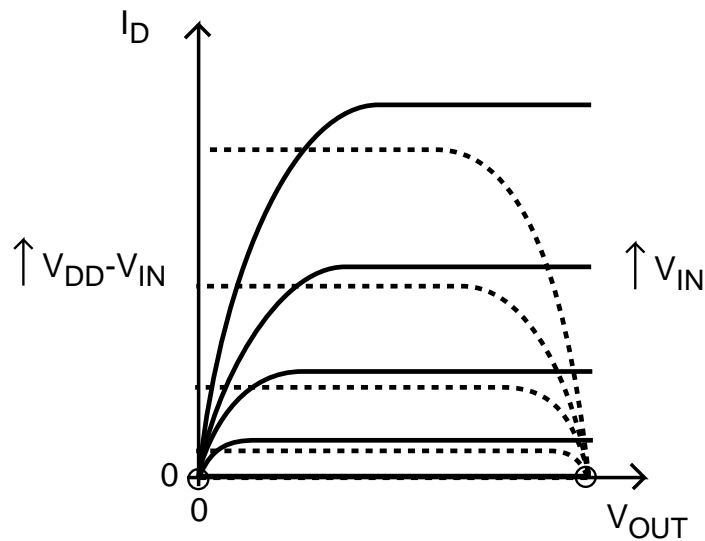
Charge in C_L at $t = \infty$:

$$Q_L(t = \infty) = C_L V_{DD}$$

Charge current (PMOS in saturation):

$$-I_{Dp} = \frac{W_p}{2L_p} \mu_p C_{ox} (V_{DD} + V_{Tp})^2$$

Then:

$$t_{PLH} \simeq \frac{C_L V_{DD}}{\frac{W_p}{L_p} \mu_p C_{ox} (V_{DD} + V_{Tp})^2}$$

Key dependencies of propagation delays:

- $V_{DD} \uparrow \Rightarrow t_p \downarrow$

  Reason: $V_{DD} \uparrow \Rightarrow Q(C_L) \uparrow$, but also $I_D \uparrow\uparrow$

  Trade-off: $V_{DD} \uparrow$, more power usage.
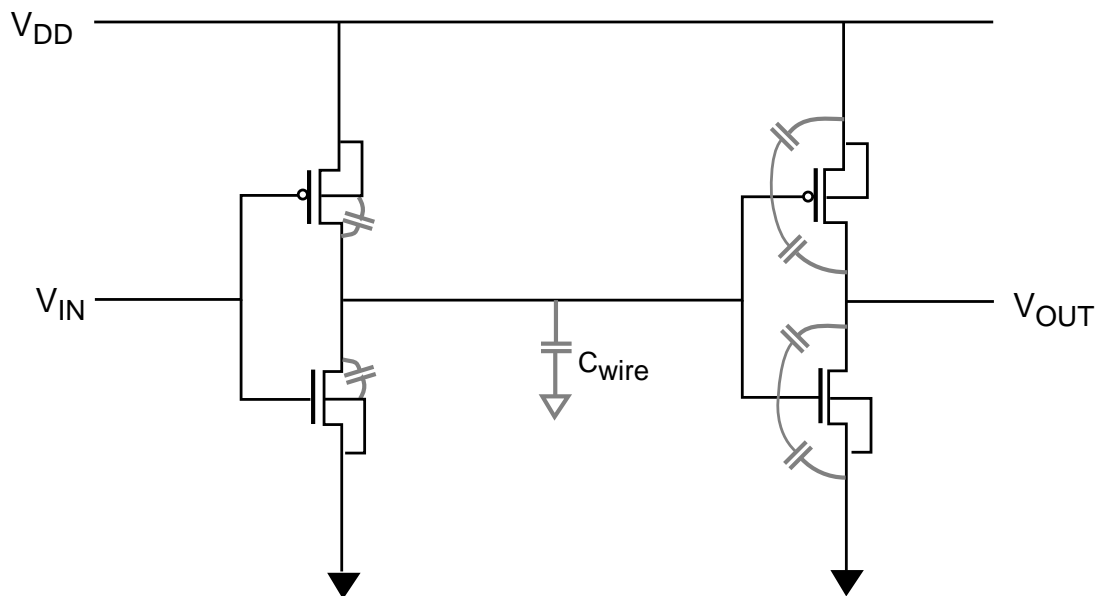
- $L \downarrow \Rightarrow t_p \downarrow$

  Reason: $L \downarrow \Rightarrow I_D \uparrow$

  Trade-off: manufacturing costs!

Components of load capacitance C_L:

- *following logic gates*: must add capacitance presented by each gate of every transistor the output is connected to

- *interconnect wire* that connects output to input of following logic gates

- *own drain-to-body capacitances*

$$C_L = C_G + C_{wire} + C_{DBn} + C_{DBp}$$

[See details in Howe & Sodini §5.4.3]

Key conclusions

- Key features of CMOS inverter:

  - no current while idling in any logic state
  - "rail-to-rail" logic: logic levels are 0 and V_{DD}
  - high $|A_v|$ around logic threshold $\Rightarrow$ good noise margins

- CMOS inverter logic threshold and noise margins engineered through W_n/L_n and W_p/L_p.

- Key dependences of propagation delay:

  - $V_{DD} \uparrow \Rightarrow t_p \downarrow$
  - $L \downarrow \Rightarrow t_p \downarrow$