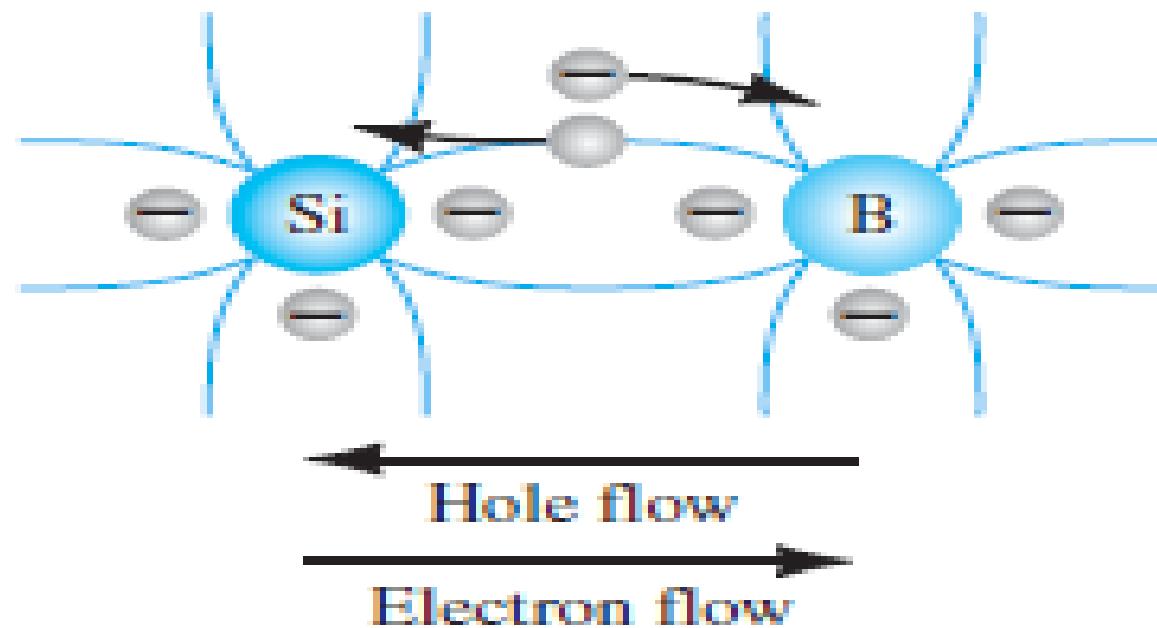


# SEMICONDUCTOR DEVICES

## DEPARTMENT OF COMPUTER ENGINEERING

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AND TECHNOLOGY, KUMASI, GHANA



Dipl.-Ing. B. Kommey

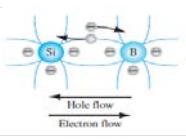
[bkommey.coe@knust.edu.gh](mailto:bkommey.coe@knust.edu.gh)

[nni\\_kommey@msn.com](mailto:nni_kommey@msn.com)

Tel: 050 770 3286

Whatsup: 0507703286





## SEMICONDUCTOR DEVICES DEPARTMENT OF COMPUTER ENGINEERING

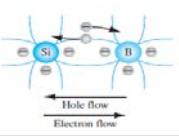
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**“Education is what remains after one has forgotten everything he learned in school”**

**Albert Einstein**





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# Overview

Course Info

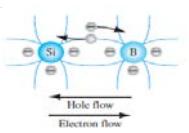
Course  
Outline

Reference  
Books

Intro to  
Semi-  
Conductors

Semi-  
Conductor  
Devices





# Course Information

## COE 271 Semiconductor Devices



2hrs Teaching



2 Credit Hours

## Requirements



Basic Knowledge in Electronics

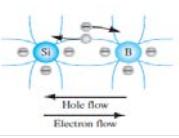


Basic Knowledge in Physics of  
Semiconductors



Basic Knowledge in Mathematics  
and Physics





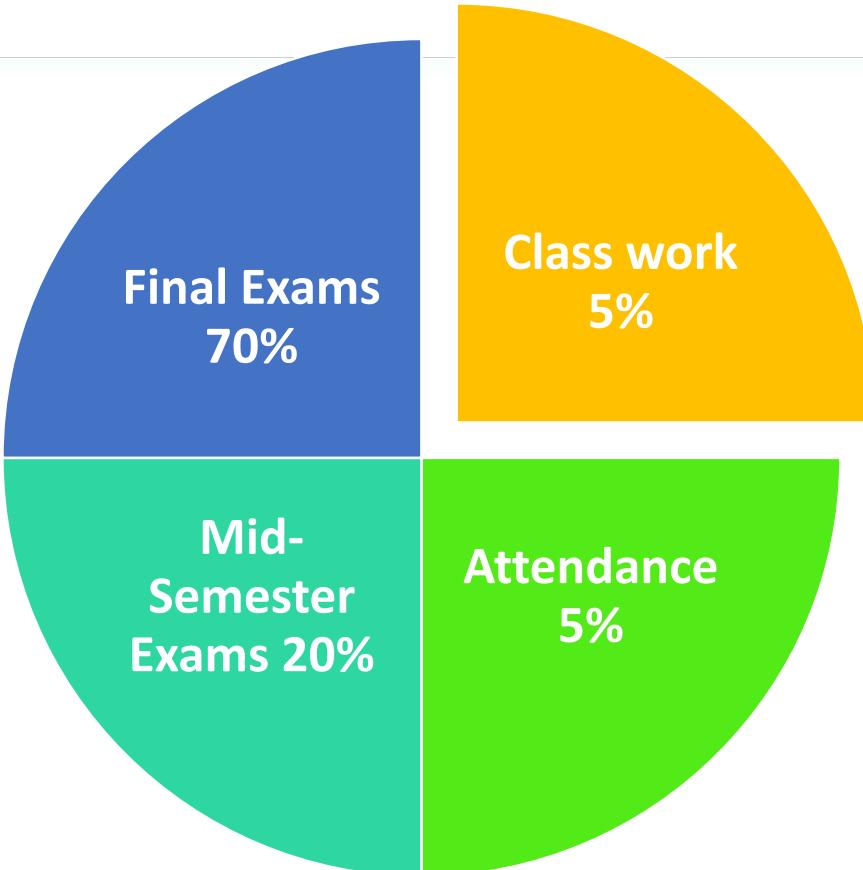
# SEMICONDUCTOR DEVICES

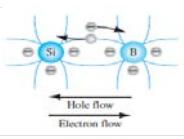
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# Course Grading





# Course Outline

**Introduction to Semiconductors – Week 1**

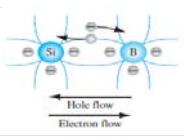
**Physics of Semiconductors – Week 2**

**Diode Models and Circuits – Week 3**

**Bipolar Transistors – Week 4**

**Bipolar Amplifiers – Week 5**





# Course Outline

**Field-Effect Transistors FET -JFET– Week 6**

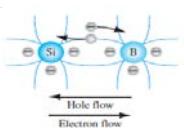
**Field-Effect Transistors FET - MOSFET – Week 7**

**Operational Amplifiers – Week 8**

**Other Two Terminal Devices (Schottsky Barrier, Solar Cells, Photodiodes) – Week 9**

**PNP Devices – Week 10**





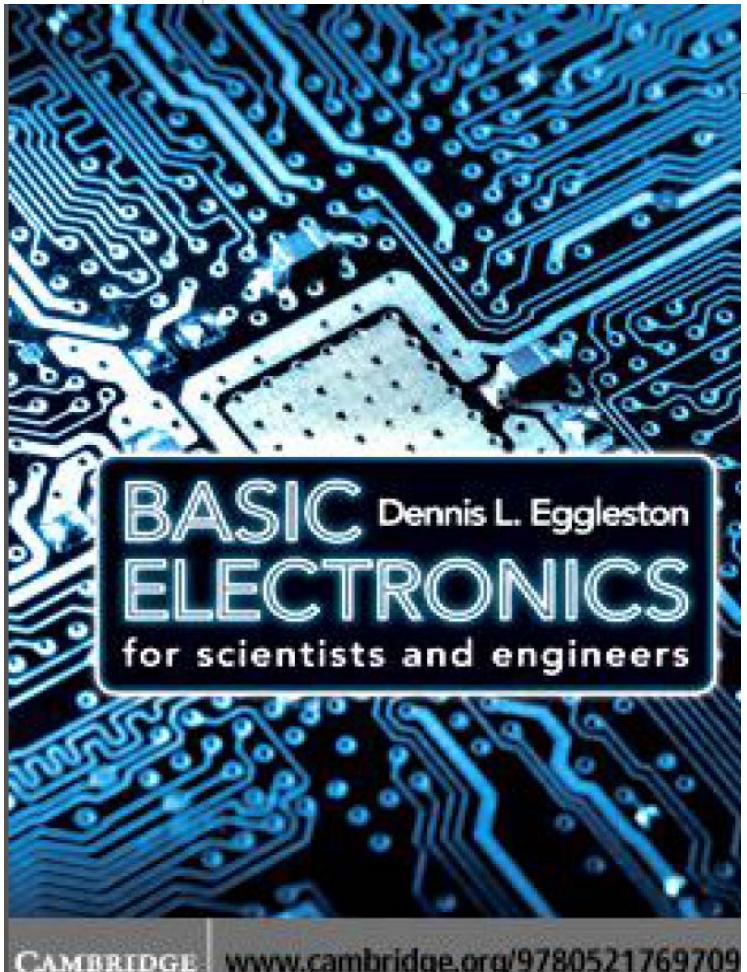
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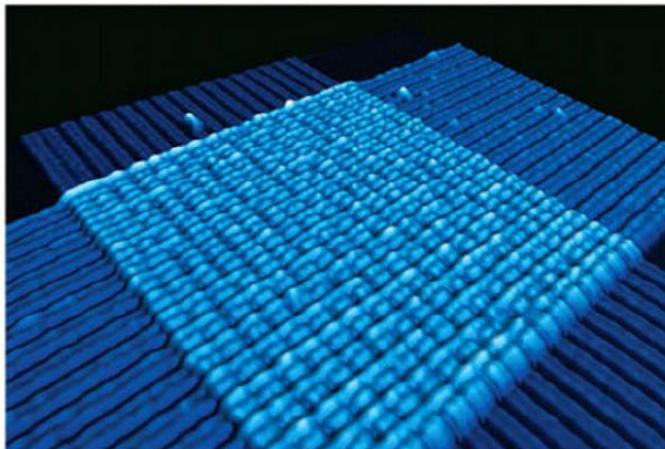


# References Books



electronic devices  
and circuit theory

ROBERT L. BOYLESTAD | LOUIS NASHELSKY

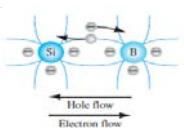


B. Jayant Baliga

Fundamentals  
of Power  
Semiconductor  
Devices

Springer





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# Reference Books

BEHZAD RAZAVI | Fundamentals of Microelectronics



SECOND EDITION

WILEY

Physics and Technology of  
Semiconductor Devices

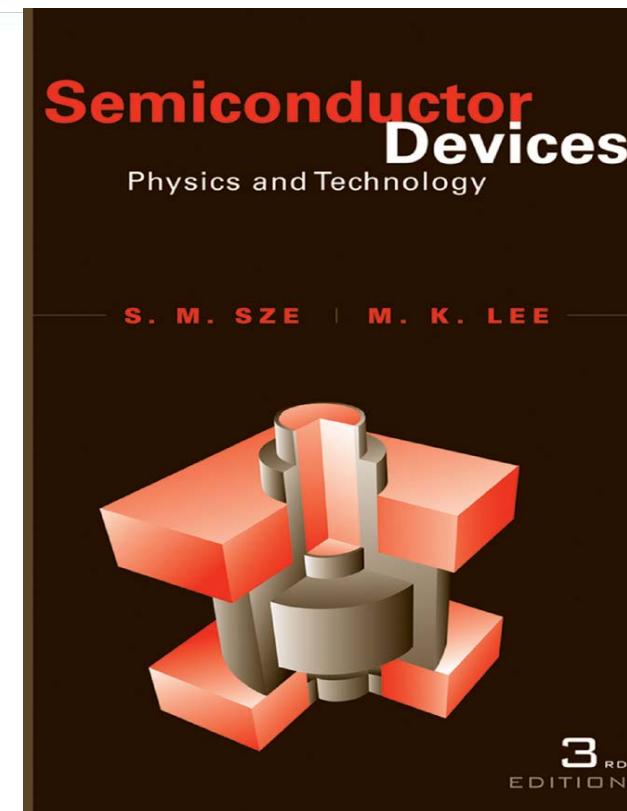
A. S. GROVE

Intel Corporation, Mountain View  
University of California, Berkeley

JOHN WILEY & SONS  
New York • Chichester • Brisbane • Toronto • Singapore

“The book is well written and clearly organized. It is a valuable addition to the literature on semiconductor devices. I highly recommend it to anyone interested in the field.”  
—Prof. Dr. H. J. Hwang, Institute of Microelectronics, A\*STAR, Singapore

“This book is a must for anyone who wants to understand the physics and technology of semiconductor devices. It is a comprehensive and well-written book that covers all the important topics in the field.”  
—Prof. Dr. M. K. Lee, Department of Electrical Engineering, University of California, Berkeley



Semiconductor Physics and Devices

*Basic Principles*

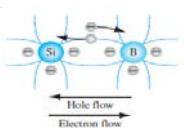
Third Edition

Donald A. Neamen  
*University of New Mexico*



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Bangkok Bogota Caracas Kuala Lumpur Lisbon London Madrid Mexico City  
Milan Montreal New Delhi Santiago Seoul Singapore Sydney Taipei Toronto





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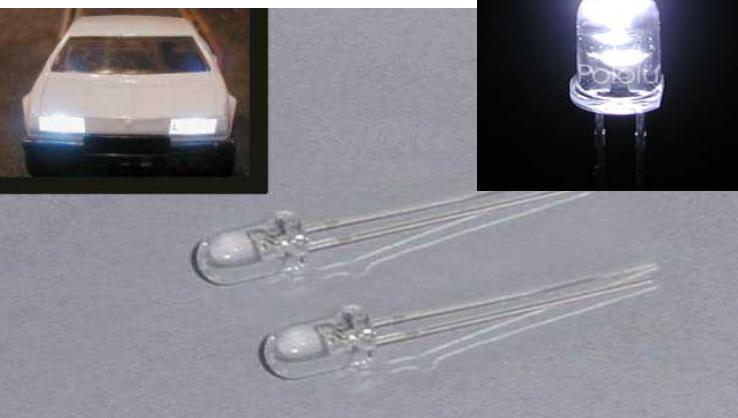
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# Semiconductor Device Applications



Red LED



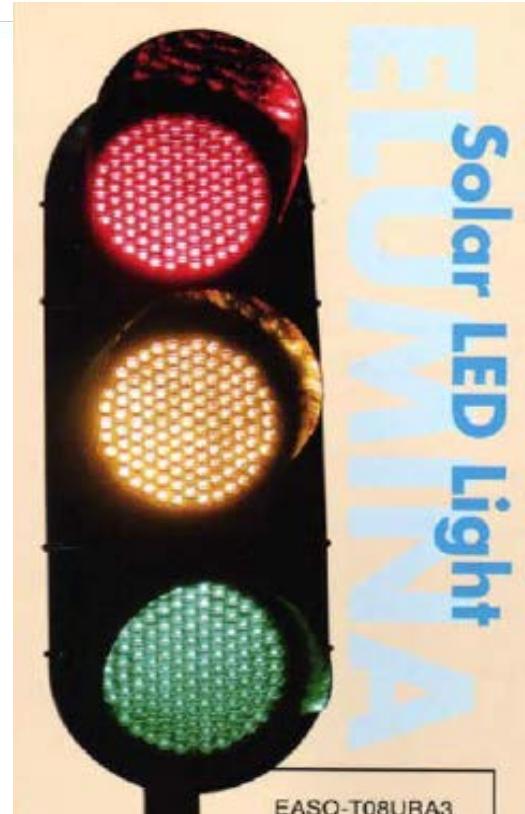
White LED



LED for displays



Blue LED

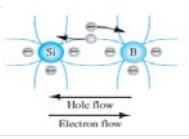


LED for traffic light



LEDs





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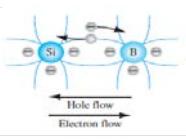
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# Semiconductor Device Applications

Diode lasers have been used for cutting, surgery, communication (optical fiber), CD writing and reading etc.



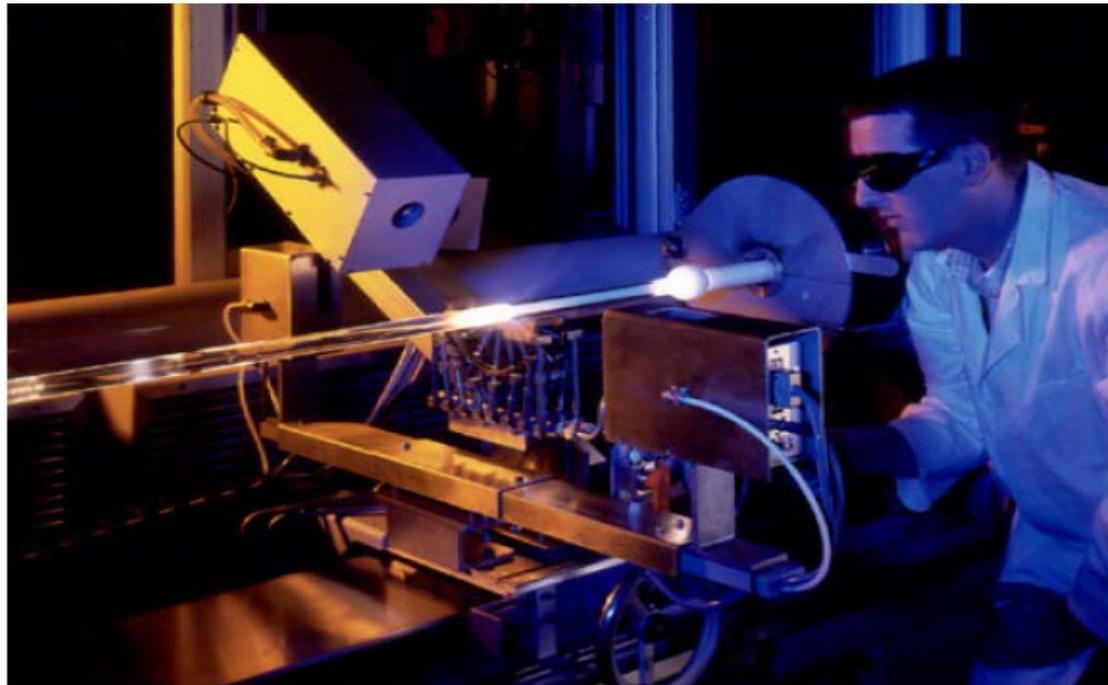


## SEMICONDUCTOR DEVICES DEPARTMENT OF COMPUTER ENGINEERING

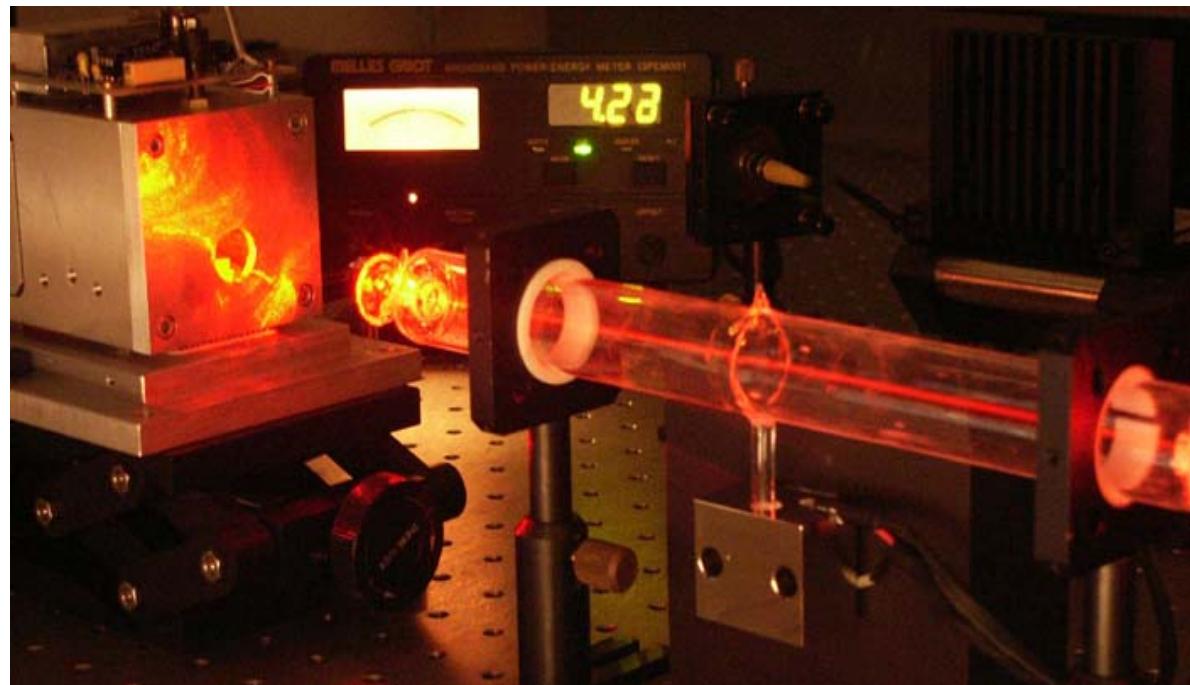
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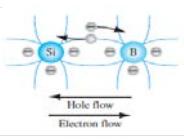


# Semiconductor Device Applications



Producing laser in the labs



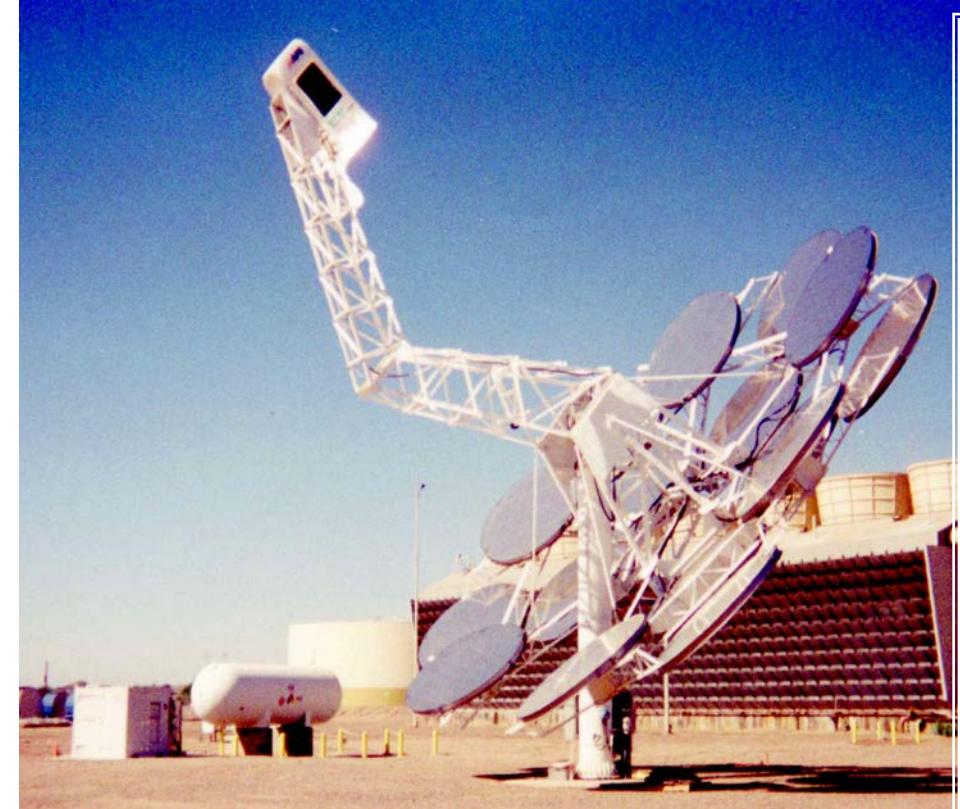


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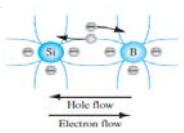


# Semiconductor Device Applications



Solar cells applications





# SEMICONDUCTOR DEVICES

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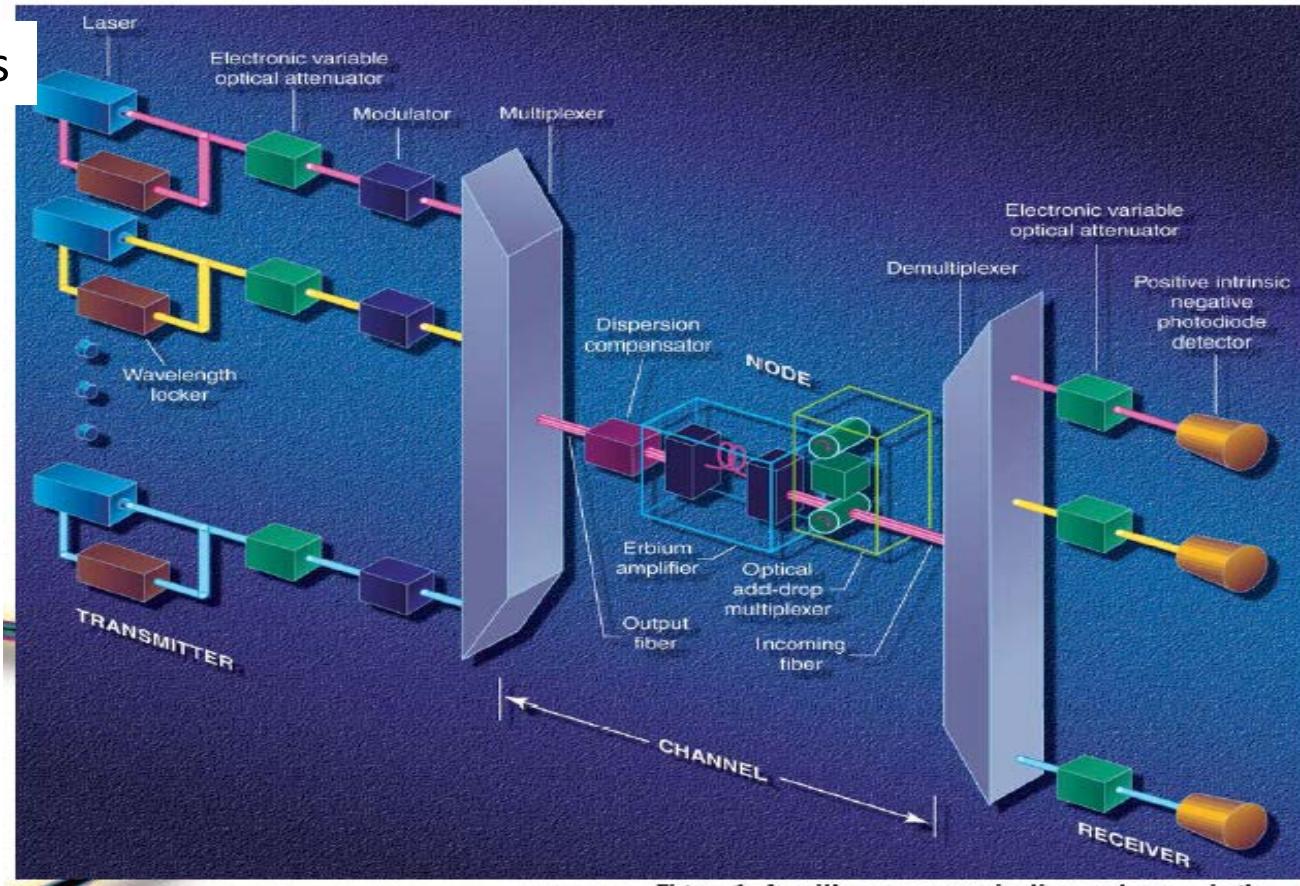


# Semiconductor Device Applications

## FIBRE OPTICS COMMUNICATION

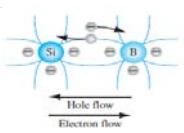
TRANSMITTER → CHANNEL → RECEIVER

IR - Lasers



IR- Photodetector





# SEMICONDUCTOR DEVICES

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# Overview

## Semiconductor Devices

### Semiconductors

### Insulators

### Conductors

Carrier Concentration

Intrinsic Semi-Conductors

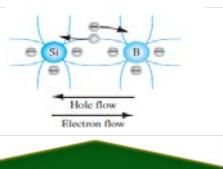
Extrinsic Semi-Conductors

Energy Band Gap

Thermal Equilibrium

Doping





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# Introduction to Semiconductors

## Electronic Devices

Most electronic devices are made out of semiconductors, insulators, and conductors.

## Semiconductors

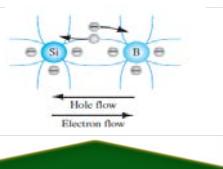
Old Days – Germanium (Ge)

Now – Silicon (Si)

Now – Gallium Arsenide (GaAs) used for high speed and optical devices.

New – Silicon Carbide (SiC) – High voltage Schottky diodes.





# Introduction to Semiconductors

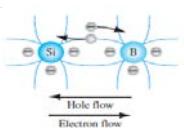
Elements in the periodic table are grouped by the number of electrons in their valence shell (most outer shell).

Conductors – Valence shell is mostly empty (1 electron)

Insulators – Valence shell is mostly full

Semiconductors – Valence shell is half full (Or is it half empty?)

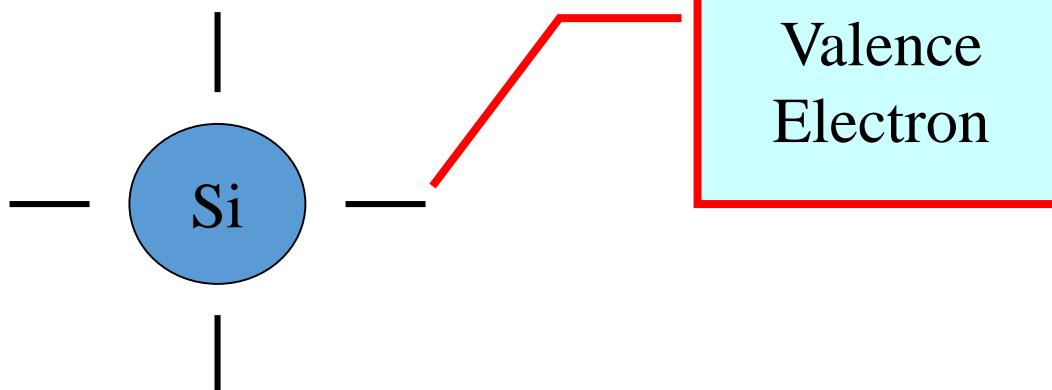


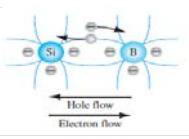


# Introduction to Semiconductors

	III	IV	V	VI
II	B 5	C 6	N 7	O 8
	Al 13	Si 14	P 15	S 16
Zn 30	Ga 31	Ge 32	As 33	Se 34
Cd 48	In 49	Sn 50	Sb 51	Te 52
Hg 80	Tl 81	Pb 82	Bi 83	Po 84

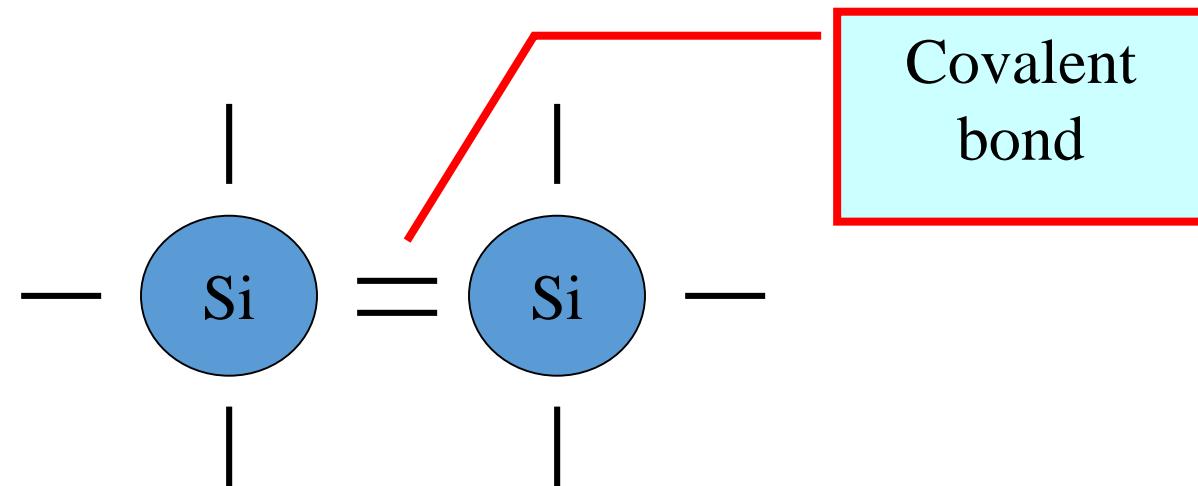
Silicon and Germanium are group 4 elements  
– they have 4 electrons in their valence shell.

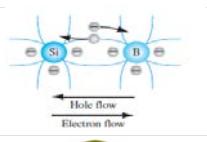




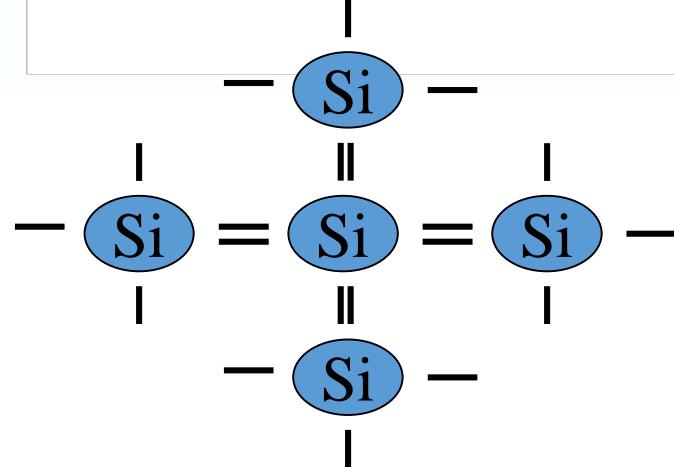
# Introduction to Semiconductors

When two silicon atoms are placed close to one another, the valence electrons are shared between the two atoms, forming a covalent bond.





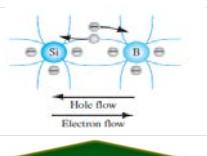
# Introduction to Semiconductors



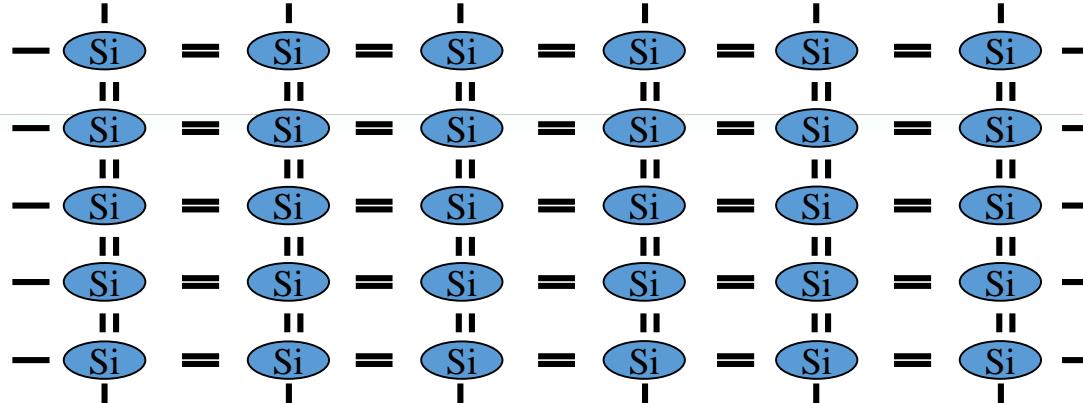
## 5-atom Silicon Structure

An important property of the 5-atom silicon lattice structure is that valence electrons are available on the outer edge of the silicon crystal so that other silicon atoms can be added to form a large single silicon crystal.





# Introduction to Semiconductors

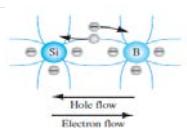


At 0 °K, each electron is in its lowest energy state so each covalent bond position is filled.

If a small electric field is applied to the material, no electrons will move because they are bound to their individual atoms.

=> At 0 °K, silicon is an insulator.





# Introduction to Semiconductors

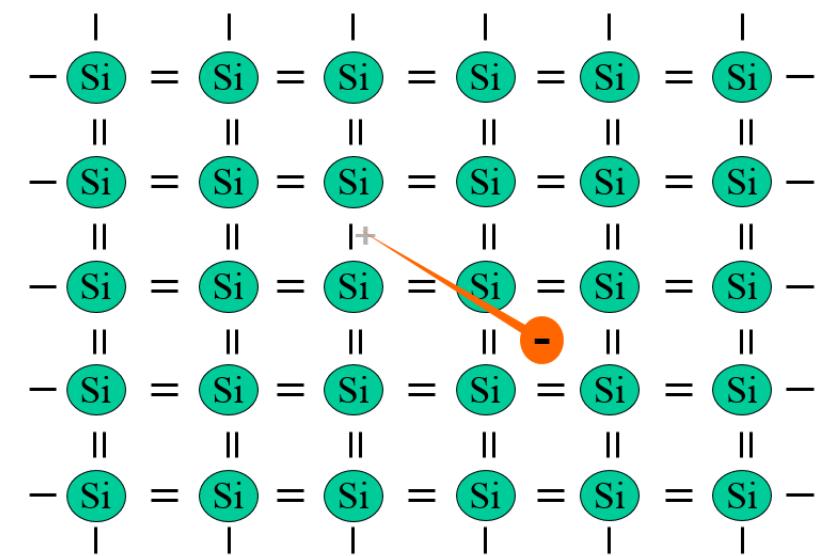
## Silicon

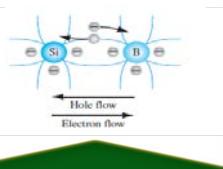
As temperature increases, the valence electrons gain thermal energy.

If a valence electron gains enough energy, it may break its covalent bond and move away from its original position.

This electron is free to move within the crystal.

Since the net charge of a crystal is zero, if a negatively (-) charged electron breaks its bond and moves away from its original position, a positively charged “empty state” is left in its original position.





# Introduction to Semiconductors

As temperature increases, more bonds are broken creating more negative free electrons and more positively charged empty states.

(Number of free electrons is a function of temperature.)

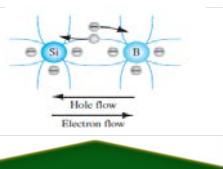
To break a covalent bond, a valence electron must gain a minimum energy  $E_g$ , called the energy band gap.

(Number of free electrons is a function of  $E_g$ .)

Elements that have a large energy band gap of 3 to 6 eV are **insulators** because at room temperature, essentially no free electrons exist.

An electron volt eV is the amount of energy an electron will gain if it is accelerated through a 1 volt potential.





# Introduction to Semiconductors

Elements that have a small energy band gap are **conductors**.

These elements have a large number of free electrons at room temperature because the electrons need very little energy to escape from their covalent bonds.

**Semiconductors** have a band gap energy of about 1 eV

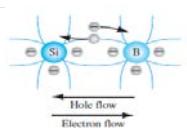
Silicon = 1.1 eV

GaAs = 1.4 eV

Ge = 0.66 eV

An electron that has sufficient energy and is adjacent to an empty state may move into the empty state, leaving an empty state behind.





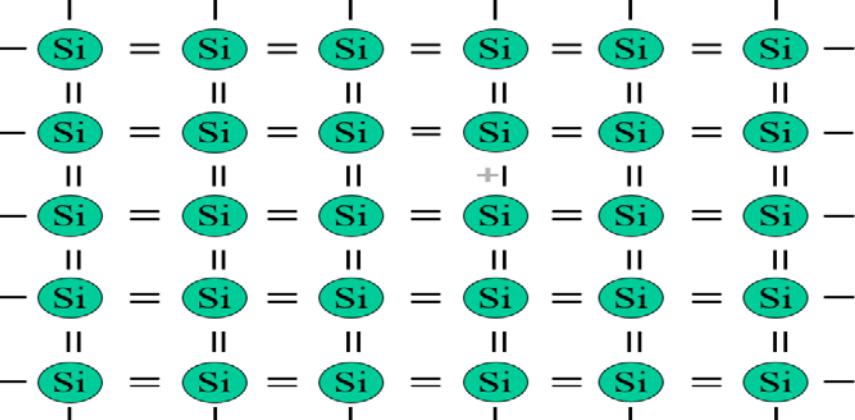
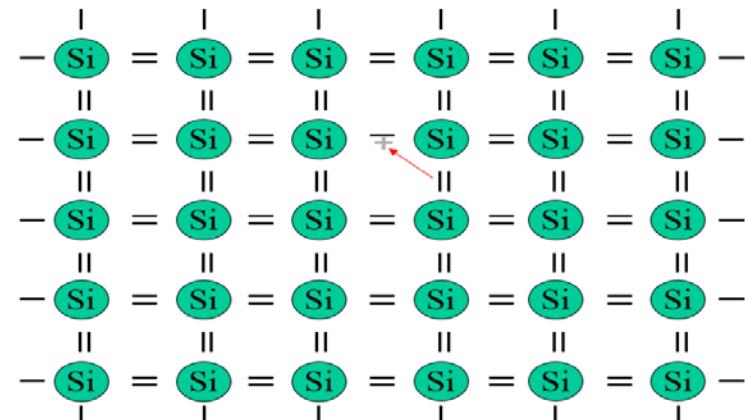
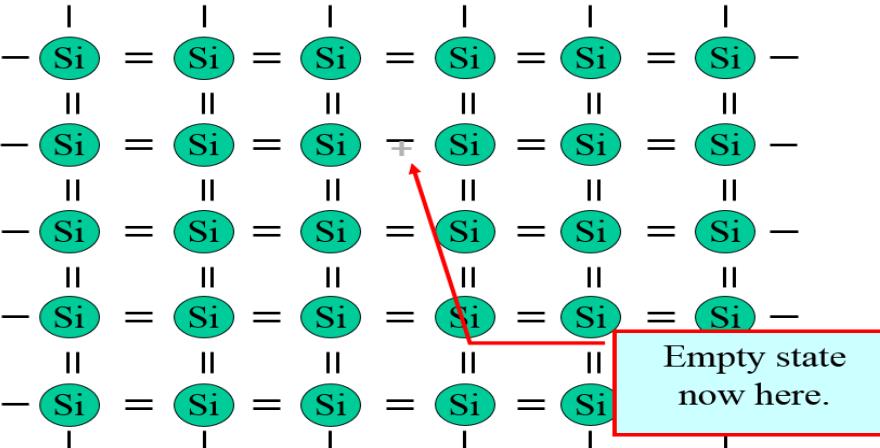
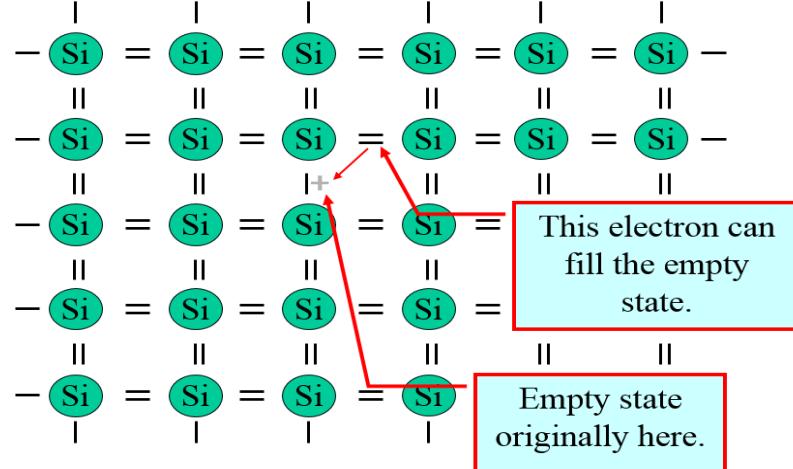
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# Introduction to Semiconductors

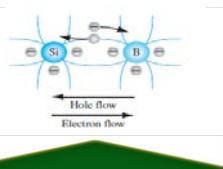


Moving empty states can give the appearance that positive charges move through the material.

This moving empty state is modeled as a positively charged particle called a **hole**.

In semiconductors, two types of “particles” contribute to the current: **positively charged holes** and **negatively charged electrons**





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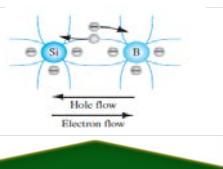
# Carrier Concentrations

The concentrations of holes and free electrons are important quantities in the behavior of semiconductors.

Carrier concentration is given as the number of particles per unit volume, or

$$\text{Carrier concentration} = \#/cm^3$$





# Intrinsic Semiconductors

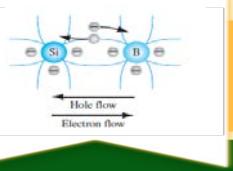
An **intrinsic semiconductor** is a single crystal semiconductor with no other types of atoms in the crystal.

Pure silicon

Pure germanium

Pure gallium arsenide.





# Intrinsic Semiconductors

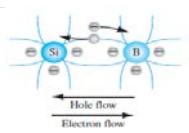
In an **intrinsic semiconductor**, the number of holes and free electrons are the same because they are thermally generated.

If an electron breaks its covalent bond we have one free electron and one hole.

In an **intrinsic semiconductor**, the concentration of holes and free electrons are the same.

- $n_i$  = the concentration of free electrons in an intrinsic semiconductor.  
 $n_i$  = the concentration of holes in an intrinsic semiconductor.





# Intrinsic Semiconductors

$$n_i = BT^{3/2} \exp\left(\frac{-E_g}{2KT}\right)$$

B and  $E_g$  are determined by the properties of the semiconductor.

$E_g$  = band gap energy (eV)

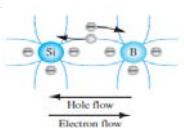
B = material constant

T = temperature ( $^{\circ}$ K)

K = Boltzmann's constant =  $86.2 \times 10^{-6}$  eV/ $^{\circ}$ K

$$\left( \frac{\#}{(cm^3) \cdot ({}^{\circ}K)^{3/2}} \right)$$





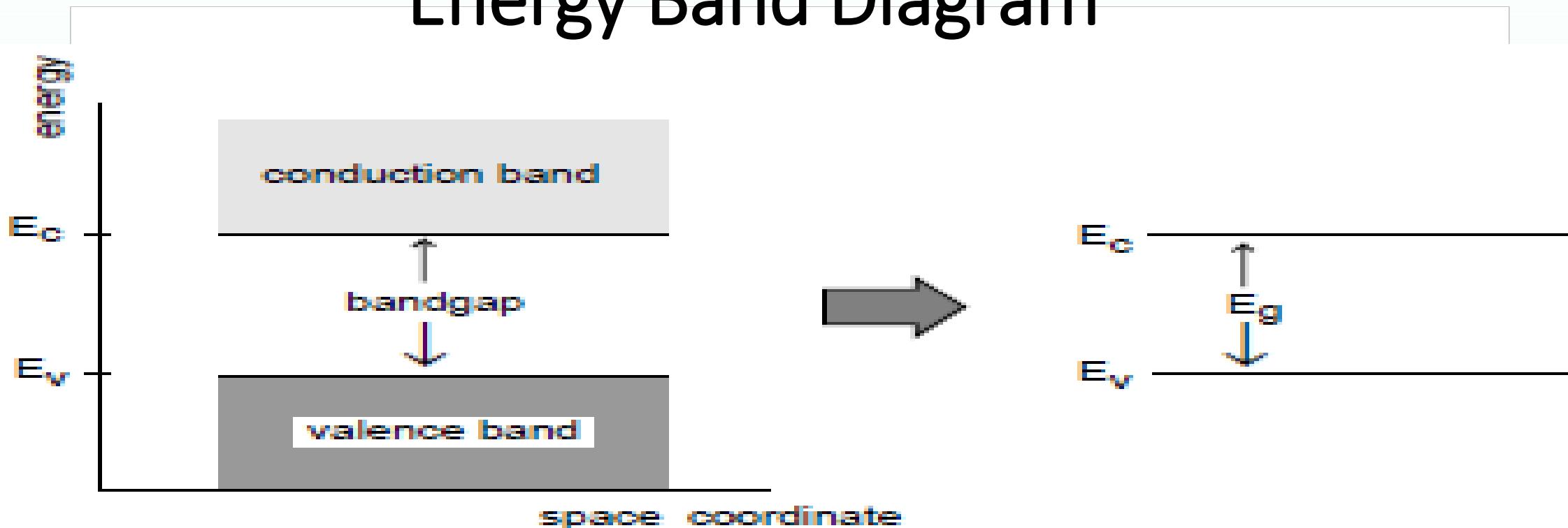
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# Energy Band Diagram

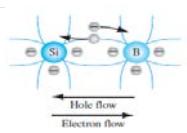


Bonding electrons occupy states in valence band

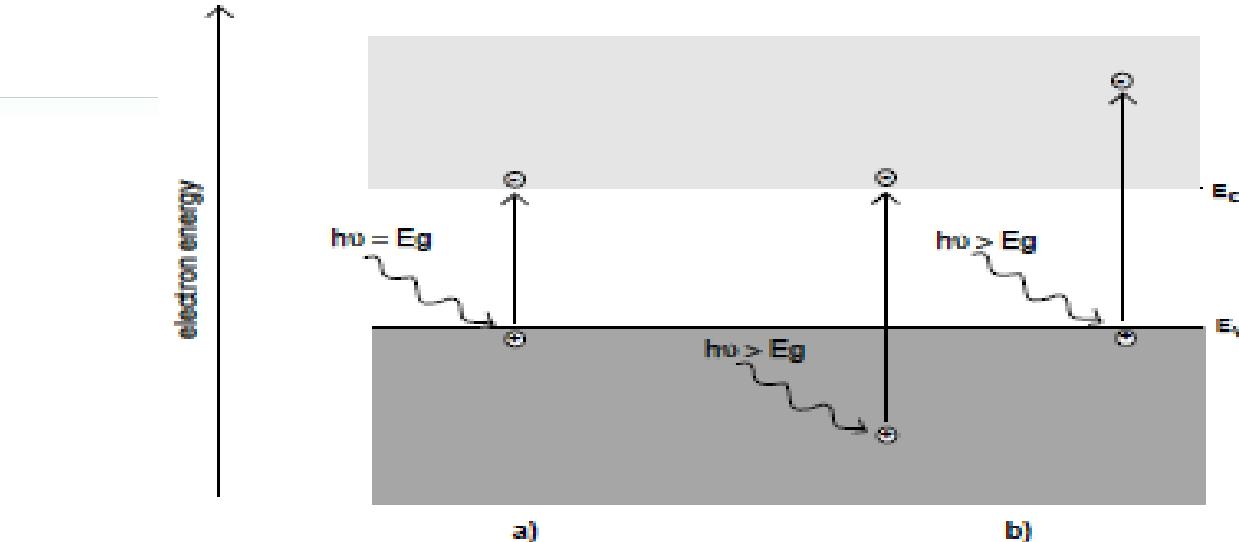
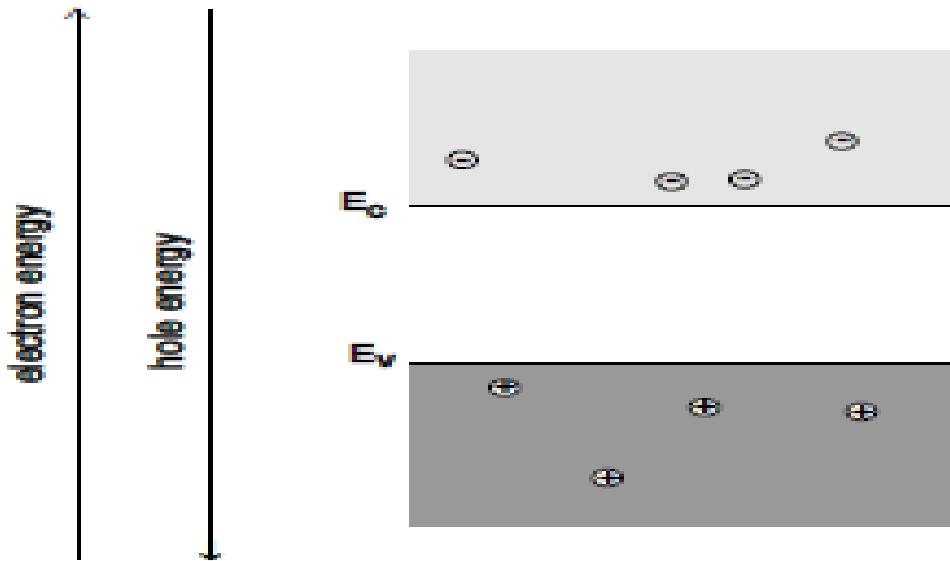
Free electrons occupy states in conduction band

Holes empty states in valence band





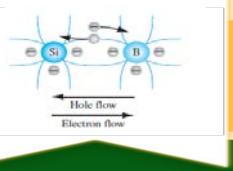
# Energy Band Diagram



Elements of energy band diagrams:

- At edges of the bands, kinetic energy of carriers is zero
- Electron energies increase upwards
- Hole energies increase downwards





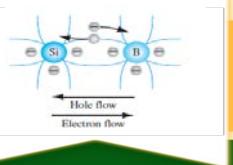
# Extrinsic Semiconductors

Since the concentrations of free electrons and holes is small in an intrinsic semiconductor, only small currents are possible.

Impurities can be added to the semiconductor to increase the concentration of free electrons and holes

An impurity would have one less or one more electron in the valance shell than silicon.





## Extrinsic Semiconductors

Impurities for group 4 type atoms (silicon) would come from group 3 or group 5 elements

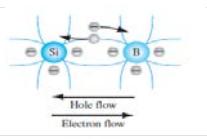
The most common group 5 elements are phosphorous and arsenic.

Group 5 elements have 5 electrons in the valence shell.

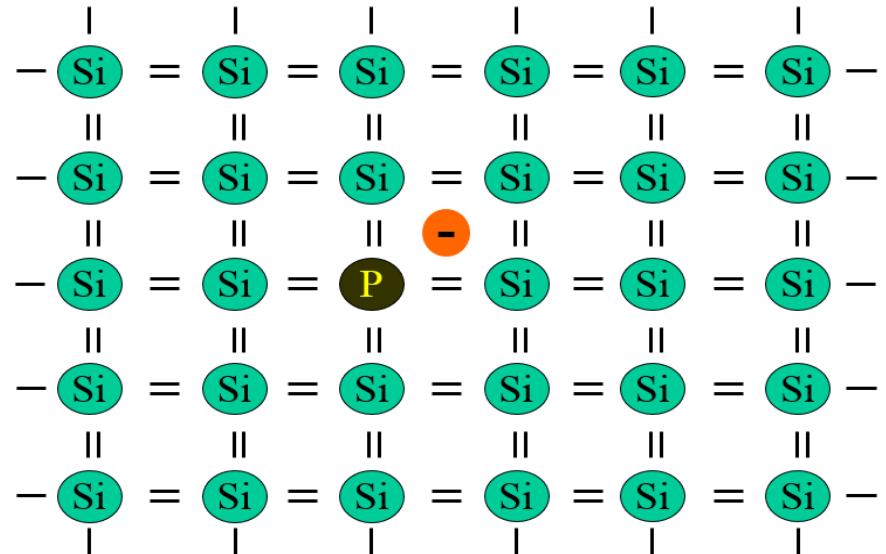
Four of the electrons fill the covalent bonds in the silicon crystal structure.

The 5<sup>th</sup> electron is loosely bound to the impurity atom and is a free electron at room temperature





# Extrinsic Semiconductors

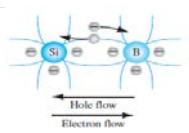


The group 5 atom is called a **donor** impurity since it donates a free electron.

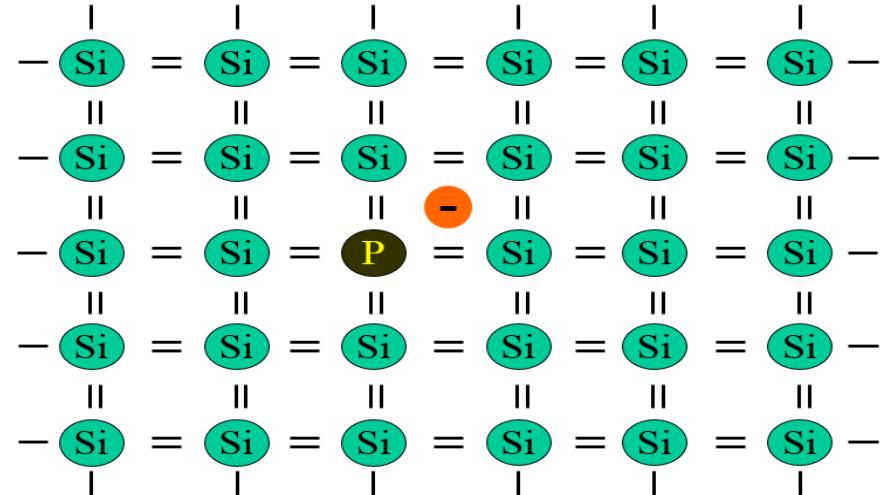
The group 5 atom has a net positive charge that is fixed in the crystal lattice and cannot move.

With a donor impurity, free electrons are created without adding holes.





# Extrinsic Semiconductors



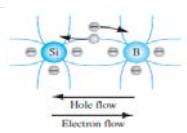
Adding impurities is called **doping**.

A semiconductor doped with donor impurities has excess free electron and is called an **n-type** semiconductor

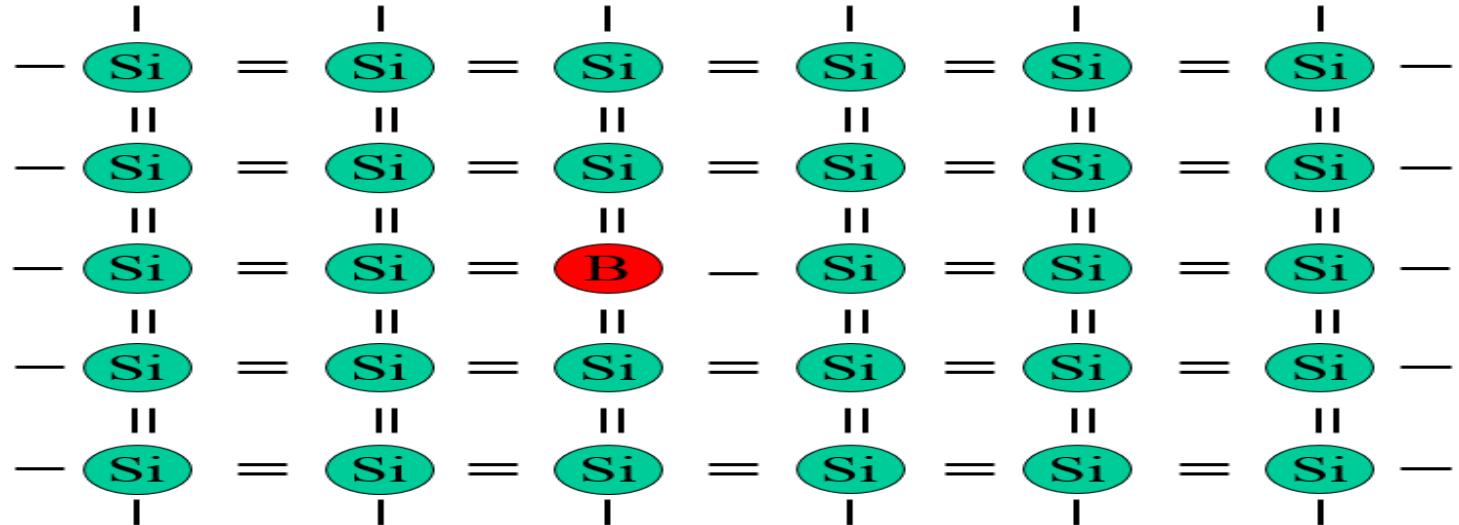
The most common group 3 impurity is boron which has 3 valence electrons.

Since boron has only 3 valence electrons, the boron atom can only bond with three of its neighbors leaving one open bond position.





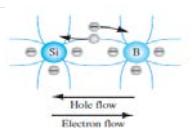
# Extrinsic Semiconductors



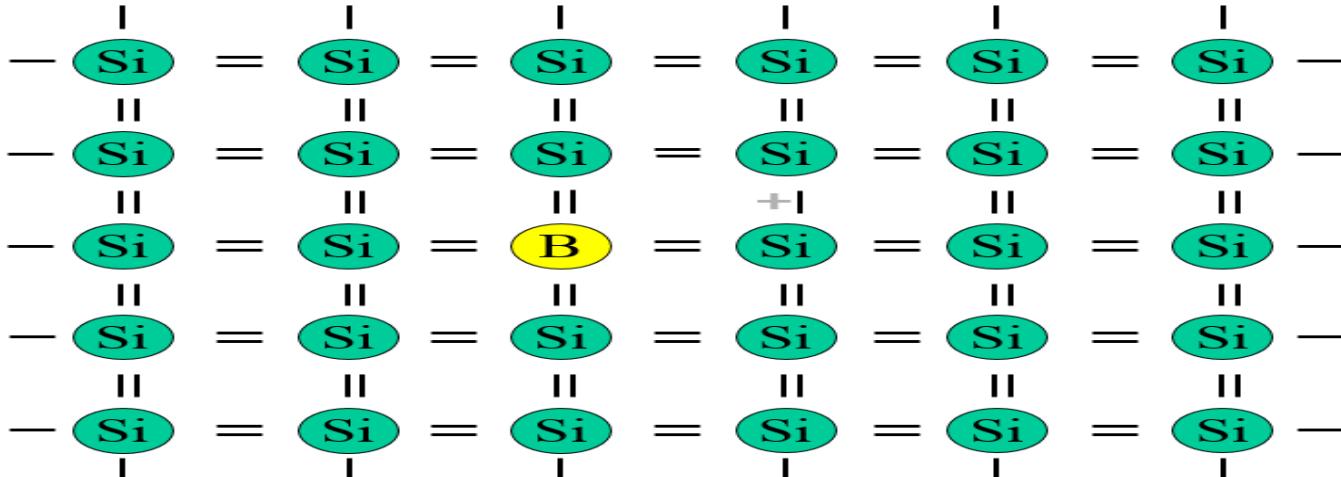
At room temperature, silicon has free electrons that will fill the open bond position, creating a hole in the silicon atom from where it came.

The boron atom has a net negative charge because of the extra electron, but the boron atom cannot move





# Extrinsic Semiconductors

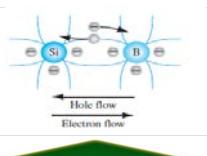


Since boron accepts a valence electron, it is called an **acceptor impurity**.

Acceptor impurities create excess holes but do not create free electrons.

A semiconductor doped with an acceptor impurity has extra holes and is called a **p-type** semiconductor.





# Extrinsic Carrier Concentrations

For any semiconductor in thermal equilibrium

$$n_o p_o = n_i^2,$$

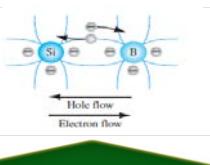
where

$n_o$  = the concentration of free electrons.

$p_o$  = the concentration of holes.

$n_i$  = the intrinsic carrier concentration





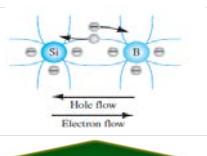
# Extrinsic Carrier Concentrations

$$n_i = BT^{3/2} \exp\left(\frac{-Eg}{2KT}\right)$$

For an n-type semiconductor with donor impurities, the concentration of donor impurities is  $N_d$  with units #/cm<sup>3</sup>.

If  $N_d \gg n_i$ , then the concentration of free electrons in the n-type semiconductor is approximately  $n_o \approx N_d$ .





# Extrinsic Carrier Concentrations

Since  $n_o p_o = n_i^2$  for any semiconductor in thermal equilibrium, and

For an n-type semiconductor,  $n_o \approx N_d$

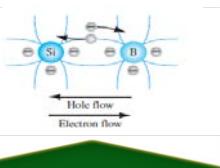
$$p_o = \frac{n_i^2}{N_d}$$

Where  $p_o$  is the concentration of holes in the n-type semiconductor

For a p-type semiconductor with acceptor impurities, the concentration of acceptor impurities is  $N_a$  with units #/cm<sup>3</sup>.

If  $N_a \gg n_i$ , then the concentration of holes in the p-type semiconductor is approximately  $p_o \approx N_a$





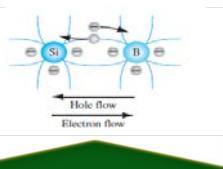
# Extrinsic Carrier Concentrations

Since  $n_o p_o = n_i^2$  for any semiconductor in thermal equilibrium,  
and for a p-type semiconductor,  $p_o \approx N_a$

$$n_o = \frac{n_i^2}{N_a}$$

Where  $n_o$  is the concentration of free electrons in  
the p-type semiconductor





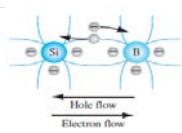
# Currents in Semiconductors

The two processes that cause free electrons and holes to move in a semiconductor are **drift** and **diffusion**.

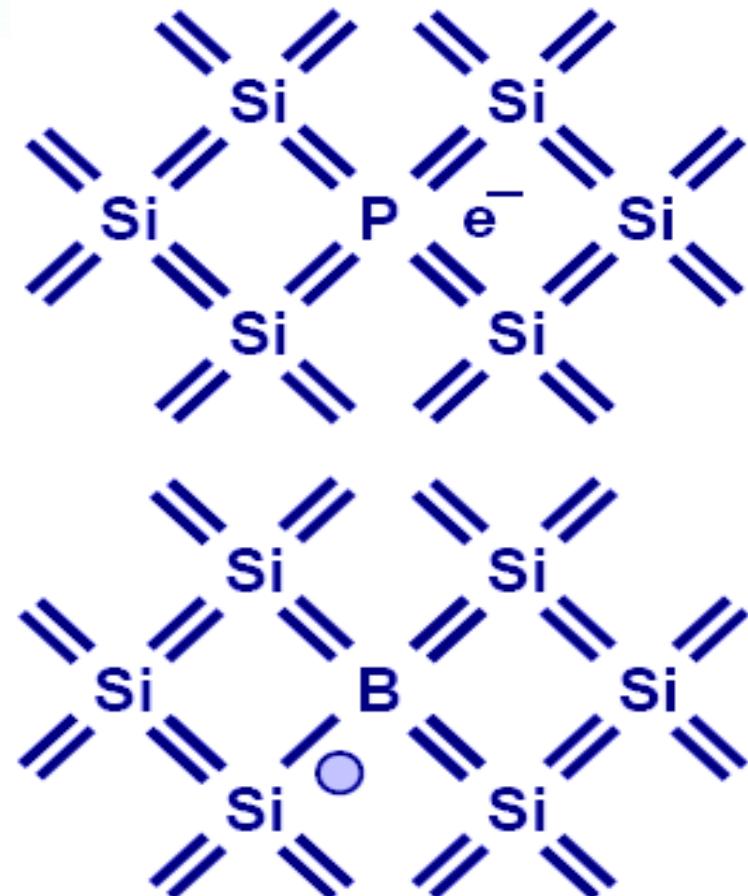
Drift – the movement of holes and electrons due to an electric field

Diffusion – the movement of holes and electrons due to variations in concentrations.





# Doping in Semiconductors

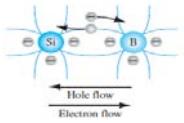


Pure Si can be doped with other elements to change its electrical properties.

For example, if Si is doped with P (phosphorous), then it has more electrons, or becomes type N (electron).

If Si is doped with B (boron), then it has more holes, or becomes type P.





# SEMICONDUCTOR DEVICES

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# Thank You

Dipl.-Ing. B. Kommey

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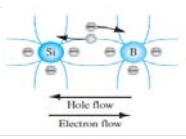
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

050 770 32 86

Whatsup: 0507703286

Skype\_id: calculus.affairs





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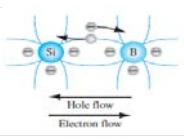
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“When you are courting a nice girl an hour seems like a second.  
When you sit on a red-hot cinder a second seems like an hour.  
That’s relativity”

**Albert Einstein**





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# Overview

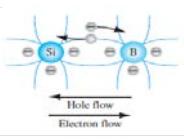
## Semiconductor Physics

Drift Current

Diffusion Current

PN Junction





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# Overview

## Drift Current

Electrons

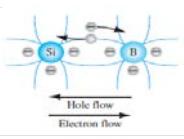
Density

Holes

Ohm's Law

Conductivity





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# Overview

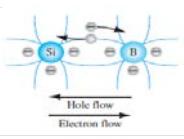
## Diffusion Current

Linear

Nonlinear

Einstein's  
Relation





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# Overview

## PN Junction

Structure

Bias  
Conditions

Forward

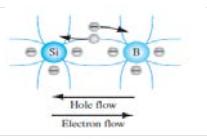
Reverse

Equilibrium

Zener

Avalanche

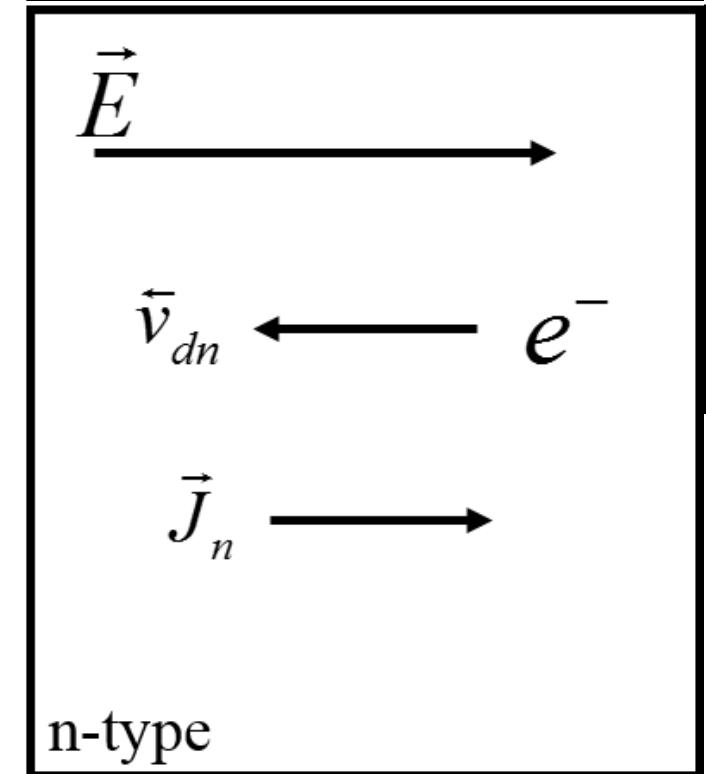




# Physics of Semiconductors

Assume that an electric field is applied to a semiconductor.

This field acts on holes and electrons

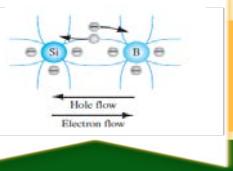


Electrons – The Electric field creates a force in the opposite direction of the electric field – Attractive.

$v_{dn}$  is the drift velocity of electrons.

$J_n$  is the current density due to electrons.





# Drift Current-Electrons

The electrons acquire a drift velocity of  $\vec{v}_{dn} = -\mu_n \vec{E}$

Where  $\mu_n$  is the mobility of electrons with units of  $\text{cm}^2/(\text{volt}\cdot\text{sec})$ .

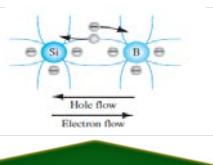
The units of  $v_{dn}$  are  $\text{cm/sec}$ .

For low-doped silicon, a typical number is  $\mu_n = 1350 \text{ cm}^2/\text{volt}\cdot\text{sec}$ .

$$\vec{v}_{dn} = -\mu_n \vec{E}$$

The minus sign (-) indicates that the electrons move in the opposite direction of the applied electric field.





# Drift Current Density Electrons

Current = charge per unit time (coul/sec).

Current density = current flowing through a specific area =  
amps/unit area = coul/(sec-cm<sup>2</sup>)

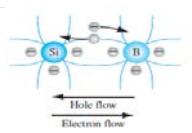
$$J_n = -env_{dn} = en\mu_n E$$

e = the charge on an electron =  $1.602 \times 10^{-19}$  coulombs.

n=concentration of electrons = #/cm<sup>3</sup>.

$$\rightarrow en = \text{charge}/\text{cm}^3. \quad env_{dn} = \frac{\text{charge}}{\text{cm}^3} \frac{\text{cm}}{\text{sec}} = \frac{\text{charge}}{\text{sec} \cdot \text{cm}^2} = \frac{\text{amp}}{\text{cm}^2}$$





## Drift Current Holes

$$\vec{E}$$
  
$$h^+ \longrightarrow \vec{v}_{dp}$$
  
$$\vec{J}_p \longrightarrow$$
  
p-type

Holes – The Electric field creates a force in the same direction of the electric field.

$v_{dp}$  is the drift velocity of holes.

$J_p$  is the current density due to holes.

The holes acquire a drift velocity of

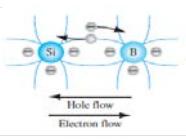
$$\vec{v}_{dp} = \mu_p \vec{E}$$

Where  $\mu_p$  is the mobility of holes with units of  $\text{cm}^2/(\text{volt}\cdot\text{sec})$ .

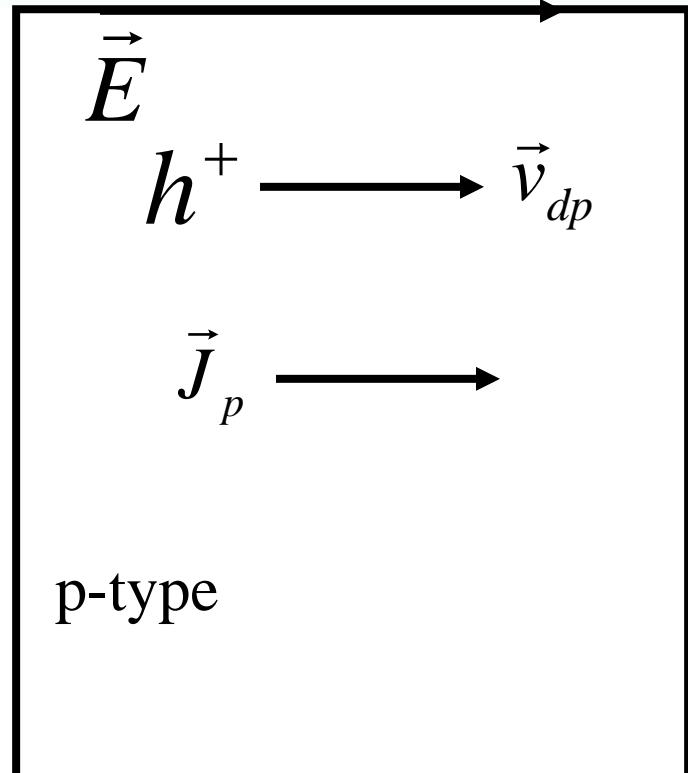
The units of  $v_{dp}$  are  $\text{cm/sec}$ .

For low-doped silicon, a typical number is  $\mu_{dp}=480 \text{ cm}^2/\text{volt}\cdot\text{sec}$





# Drift Current Holes



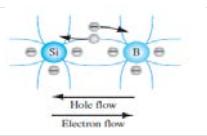
Note that  $\mu_n > \mu_p$ .

Electrons are faster than holes.

P-type and n-type devices operate the same.

However, n-type devices are faster





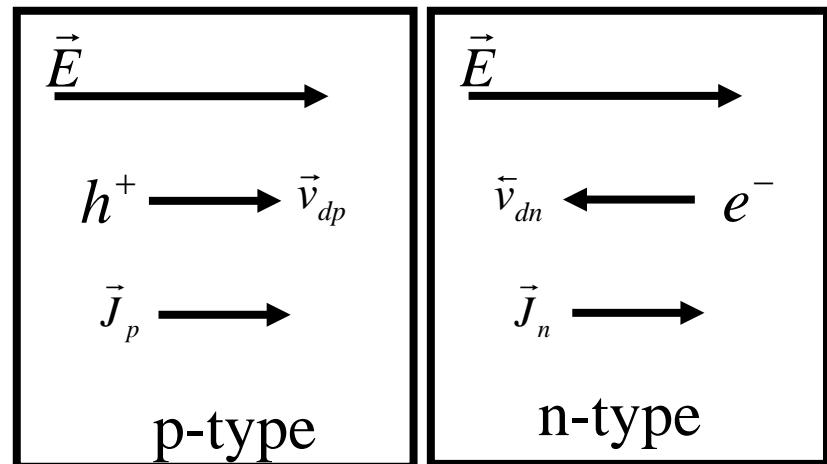
# Drift Current Density Holes

$$J_p = epv_{dp} = ep\mu_p E$$

e = the charge on an electron =  $1.602 \times 10^{-19}$  coulombs.

p = concentration of holes = #/cm<sup>3</sup>.

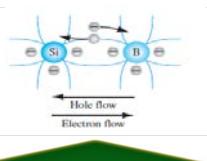
→ ep = charge/cm<sup>3</sup>



$$env_{dp} = \frac{\text{charge}}{\text{cm}^3} \frac{\text{cm}}{\text{sec}} = \frac{\text{charge}}{\text{sec} \cdot \text{cm}^2} = \frac{\text{amp}}{\text{cm}^2}$$

Drift current due to holes and electrons is in the same direction.





# Total Drift Current

Since the hole current and the electron current are in the same direction, the currents add.

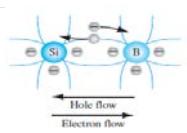
The total drift current is:  $\vec{J} = en\mu_n \vec{E} + ep\mu_p \vec{E}$

$\vec{J} = \sigma \vec{E}$  another form of Ohm's law  
 $\sigma$  is the conductivity of the material.

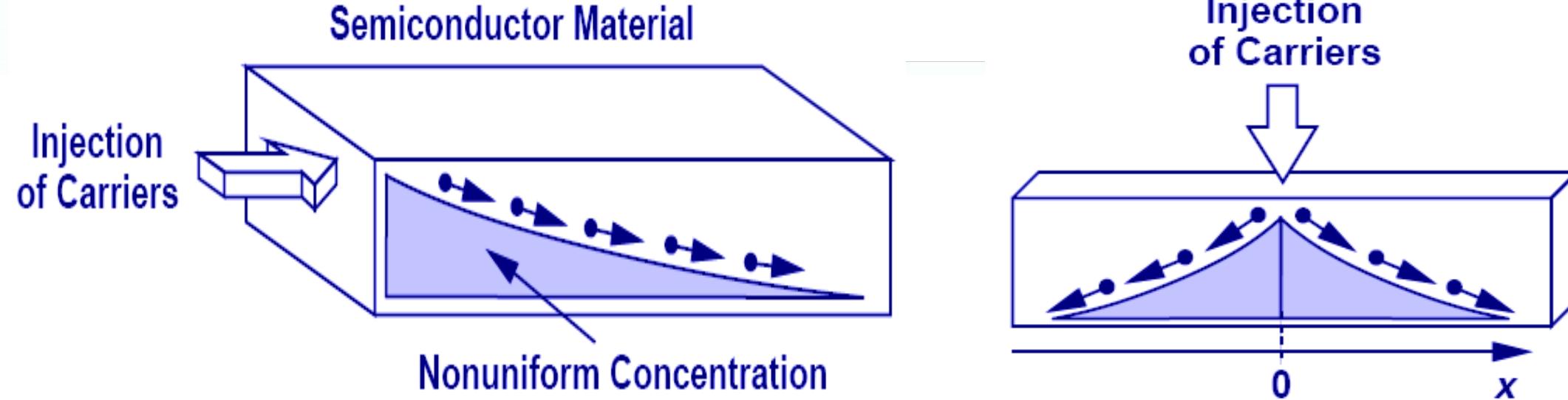
We can find the conductivity of a semiconductor as

$$\sigma = en\mu_n + ep\mu_p$$





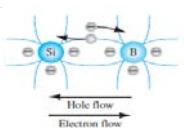
# Diffusion Current



Charge particles move from a region of high concentration to a region of low concentration.

It is analogous to an every day example of an ink droplet in water.





# Diffusion Current

$$I_d = AqD_n \frac{dn}{dx}$$

$$J_p = -qD_p \frac{dp}{dx}$$

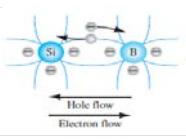
$$J_n = qD_n \frac{dn}{dx}$$

$$J_{\text{tot}} = q(D_n \frac{dn}{dx} - D_p \frac{dp}{dx})$$

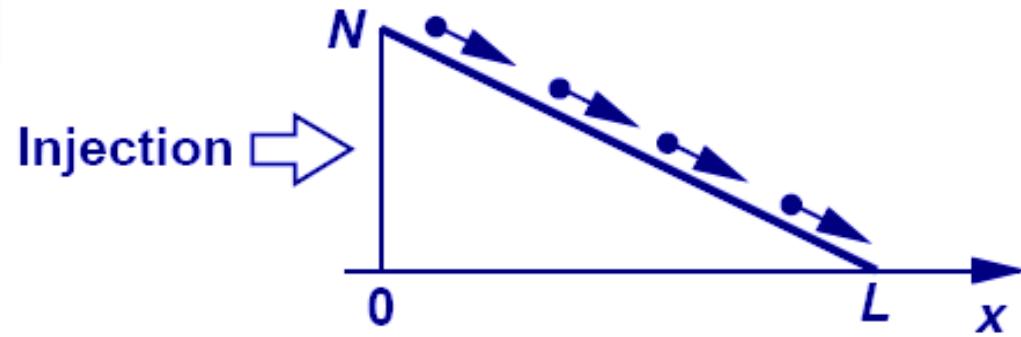
Diffusion current is proportional to the gradient of charge ( $dn/dx$ ) along the direction of current flow.

Its total current density consists of both electrons and holes.

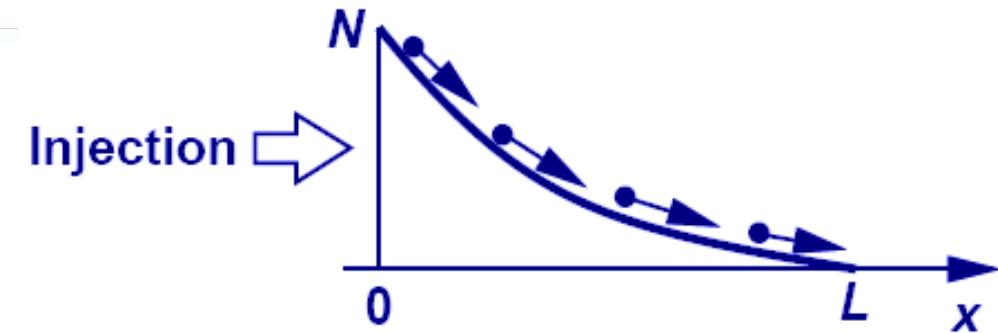




# Linear and Nonlinear Charge Density Profile



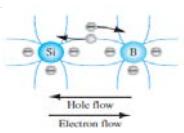
$$J_n = qD_n \frac{dn}{dx} = -qD_n \cdot \frac{N}{L}$$



$$J_n = qD \frac{dn}{dx} = \frac{-qD_n N}{L_d} \exp \frac{-x}{L_d}$$

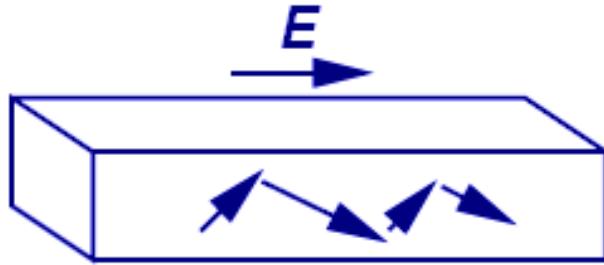
Linear charge density profile means constant diffusion current, whereas nonlinear charge density profile means varying diffusion current.





# Einstein's Relation

Drift Current



$$J_n = q \mu_n E$$

$$J_p = q \mu_p$$

Diffusion Current



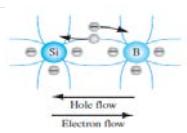
$$J_n = q D_n \frac{dn}{dx}$$

$$J_p = -q D_p \frac{dp}{dx}$$

$$\frac{D}{\mu} = \frac{kT}{q}$$

While the underlying physics behind drift and diffusion currents are totally different, Einstein's relation provides a mysterious link between the two.





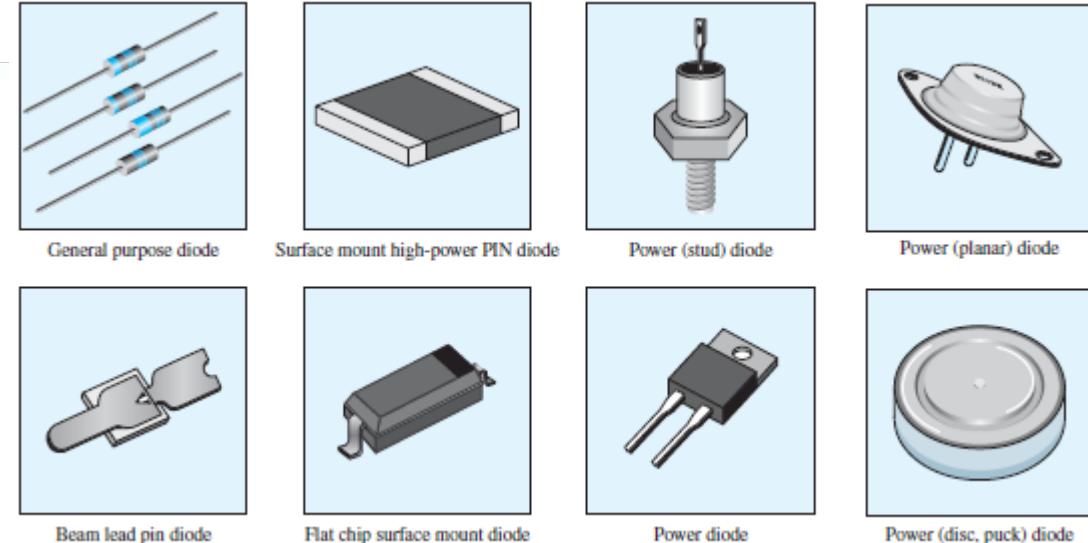
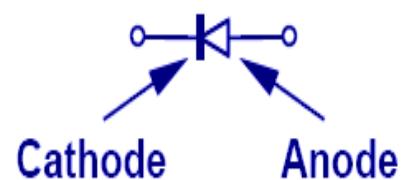
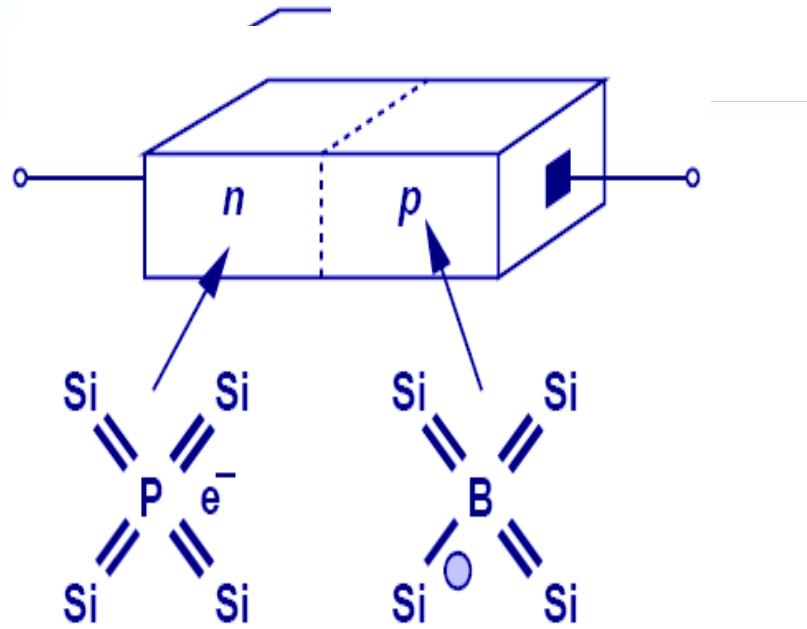
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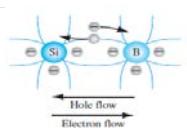
# PN Junction (Diode)



Different diodes

When N-type and P-type dopants are introduced side-by-side in a semiconductor, a PN junction or a diode is formed.





# Diode's Three Operation Regions

Diode Operation Regions

PN Junction in  
Equilibrium

PN Junction under  
Reverse Bias

PN Junction under  
Forward Bias

Depletion Region

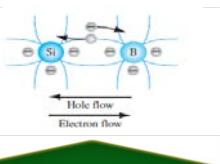
Built-in Potential

Junction Capacitance

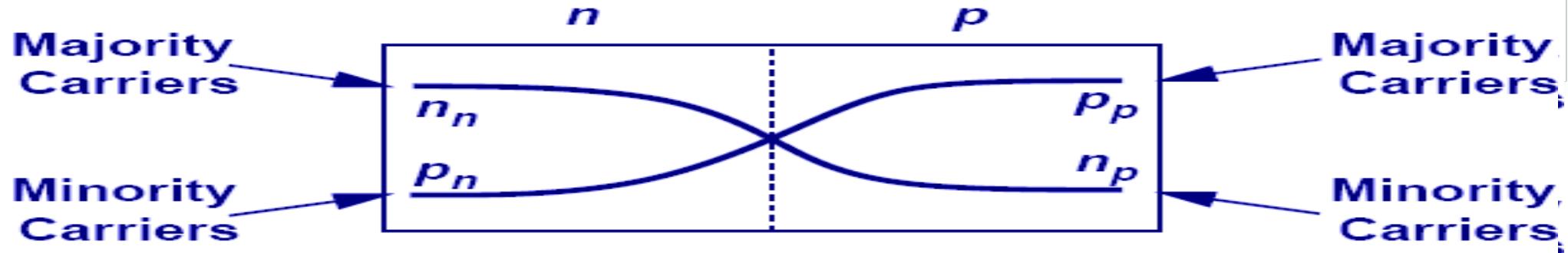
I/V Characteristics

In order to understand the operation of a diode, it is necessary to study its three operation regions: equilibrium, reverse bias, and forward bias.





# Current Flow Across Junction: Diffusion



$n_n$  : Concentration of electrons on n side

$p_n$  : Concentration of holes on n side

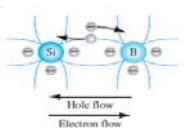
$p_p$  : Concentration of holes on p side

$n_p$  : Concentration of electrons on p side

Because each side of the junction contains an excess of holes or electrons compared to the other side, there exists a large concentration gradient.

Therefore, a diffusion current flows across the junction from each side.





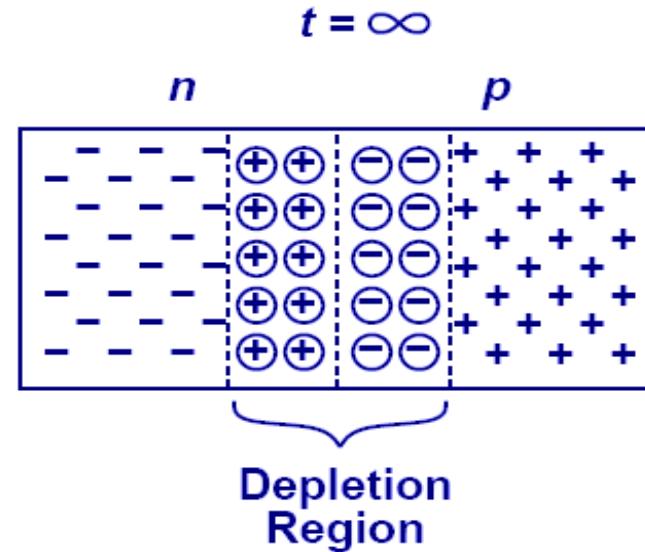
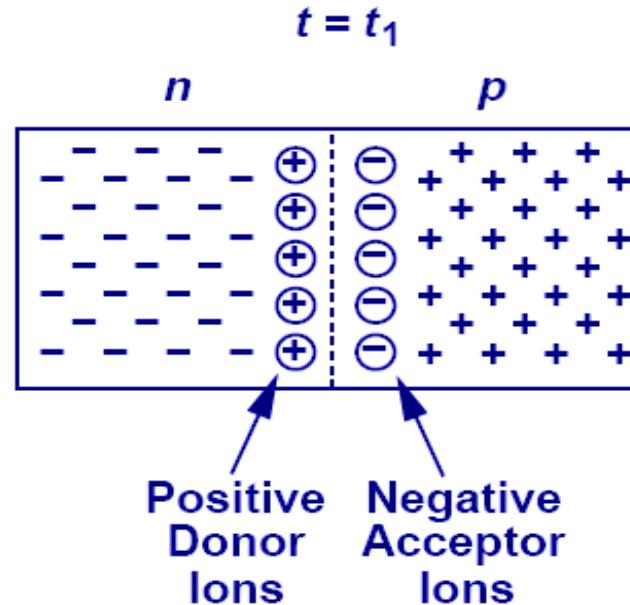
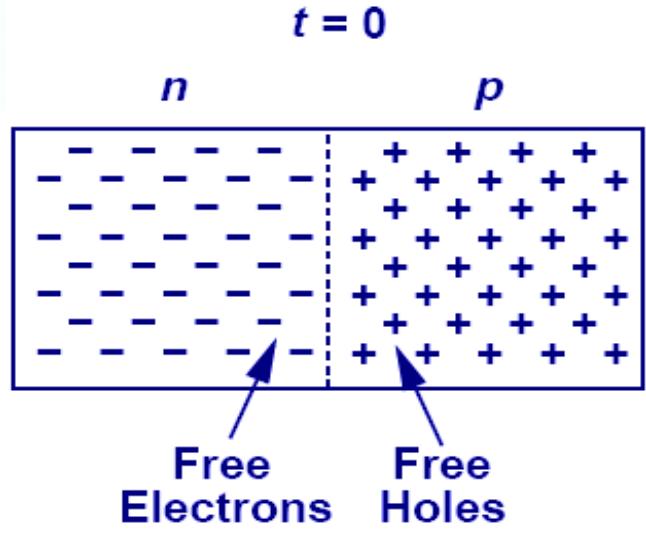
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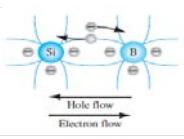
# Depletion Region



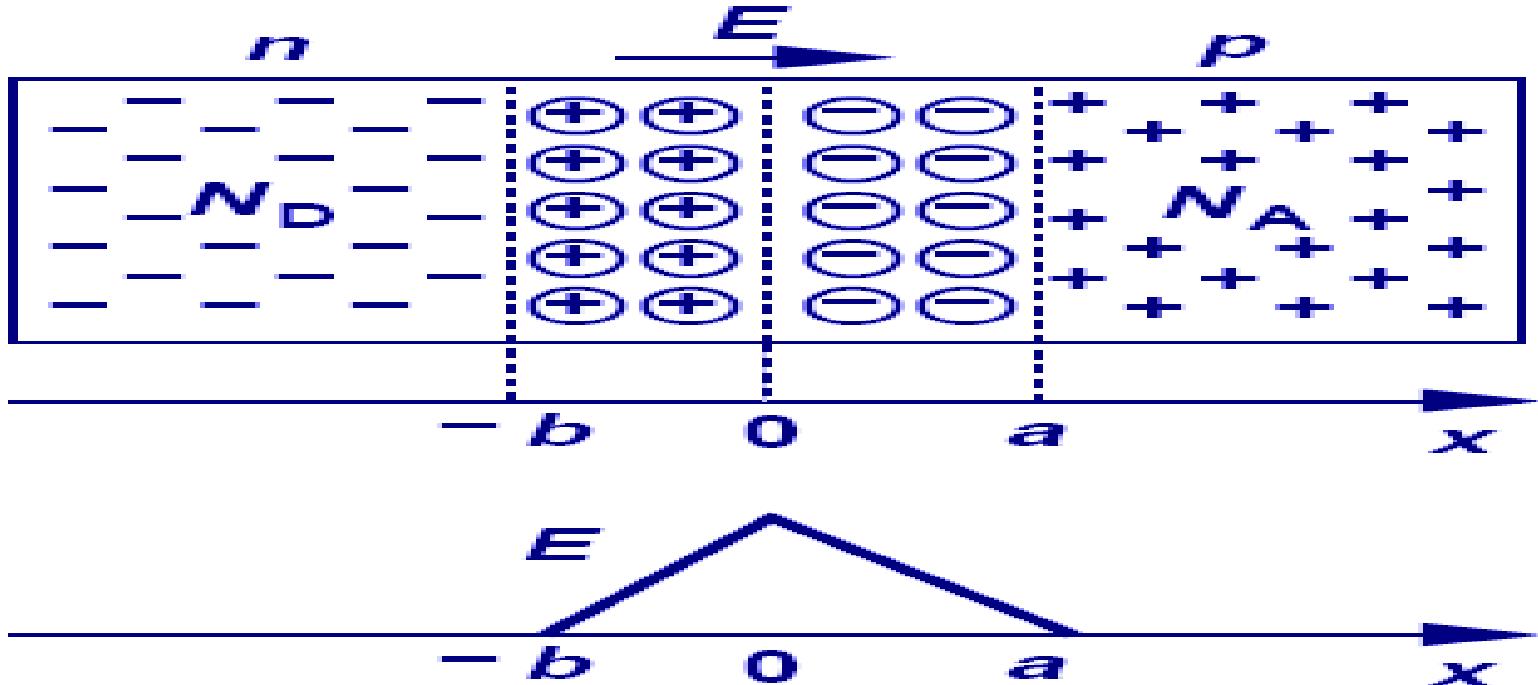
As free electrons and holes diffuse across the junction, a region of fixed ions is left behind.

This region is known as the “depletion region.”



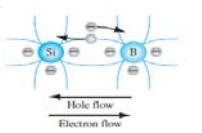


# Current Flow Across Junction: Drift

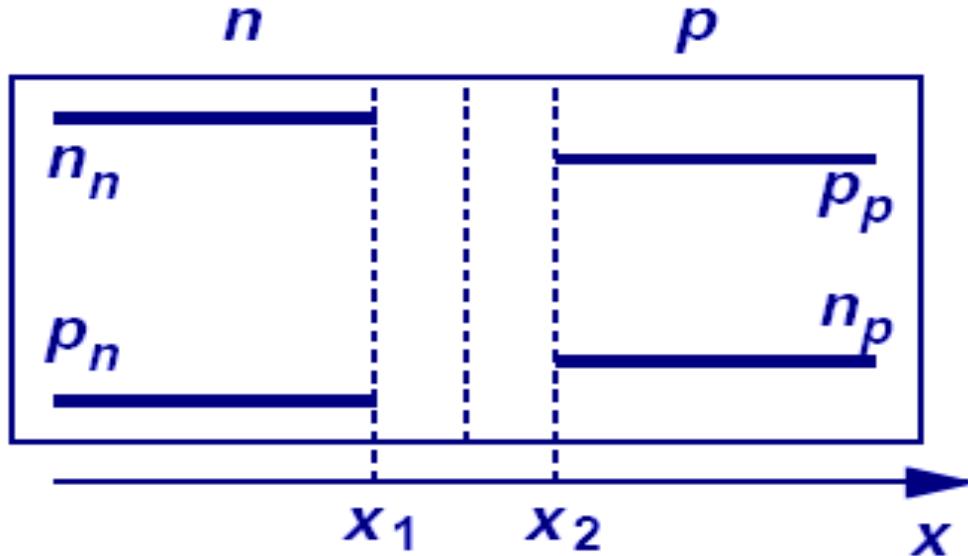


The fixed ions in depletion region create an electric field that results in a drift current.





# Current Flow Across Junction: Equilibrium

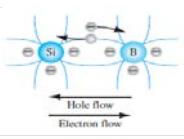


$$I_{drift,p} = I_{diff,p}$$
$$I_{drift,n} = I_{diff,n}$$

At equilibrium, the drift current flowing in one direction cancels out the diffusion current flowing in the opposite direction, creating a net current of zero.

The figure shows the charge profile of the PN junction.





# Built-in Potential

$$q\mu_p pE = -qD_p \frac{dp}{dx} \quad -\mu_p p \frac{dV}{dx} = -D_p \frac{dp}{dx}$$

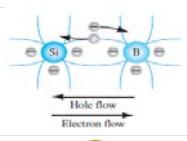
$$\mu_p \int_{x_1}^{x_2} dV = D_p \int_{p_p}^{p_n} \frac{dp}{p} \quad V(x_2) - V(x_1) = \frac{D_p}{\mu_p} \ln \frac{p_p}{p_n}$$

$$V_0 = \frac{kT}{q} \ln \frac{p_p}{p_n}, V_0 = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

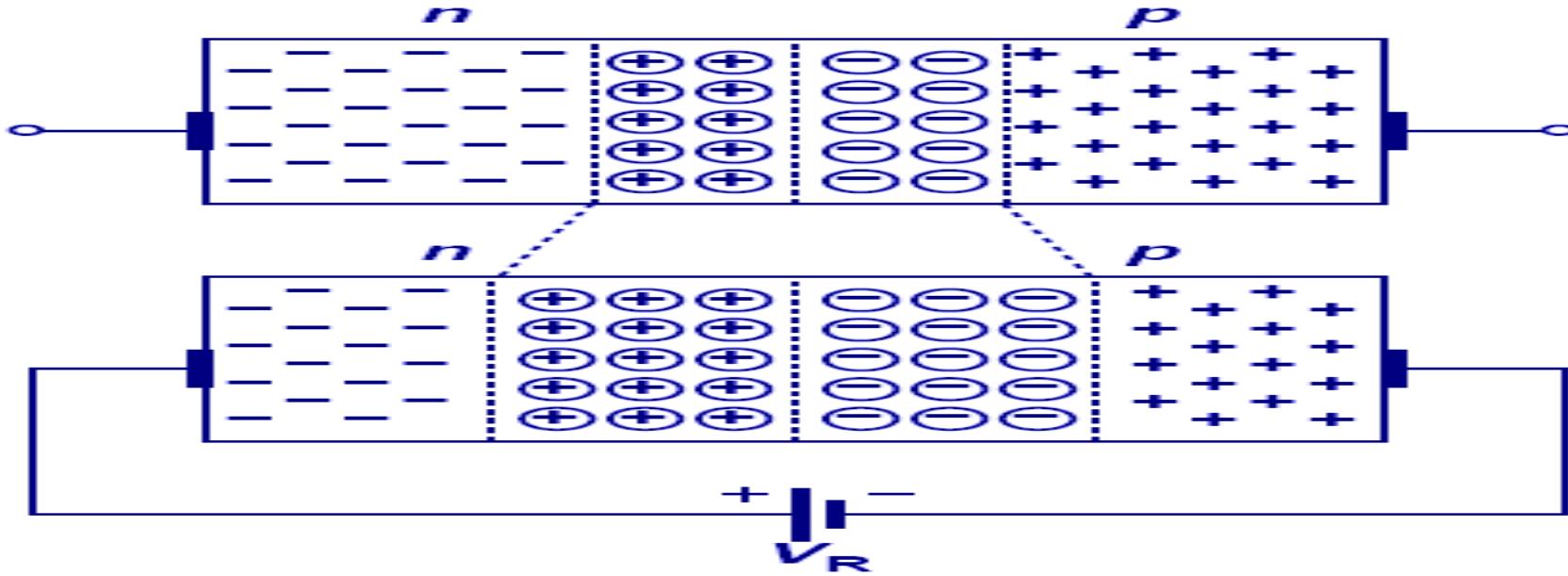
Because of the electric field across the junction, there exists a built-in potential.

Its derivation is shown above.



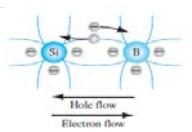


# Diode in Reverse Bias



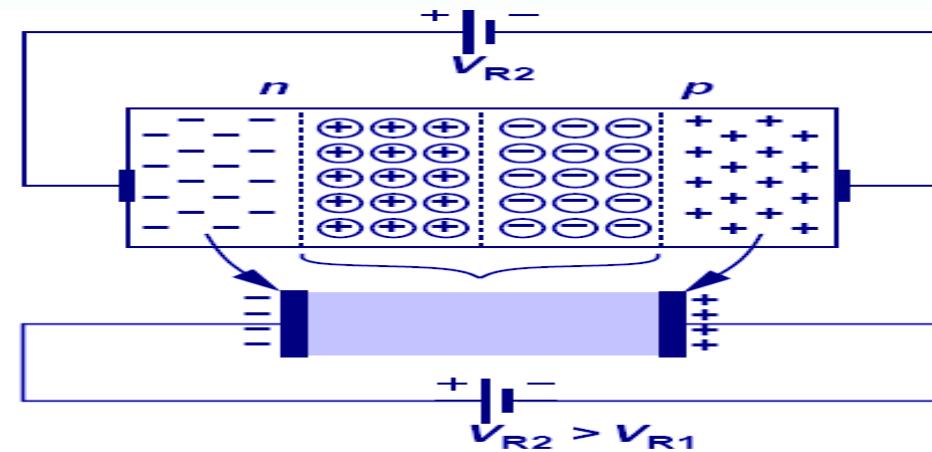
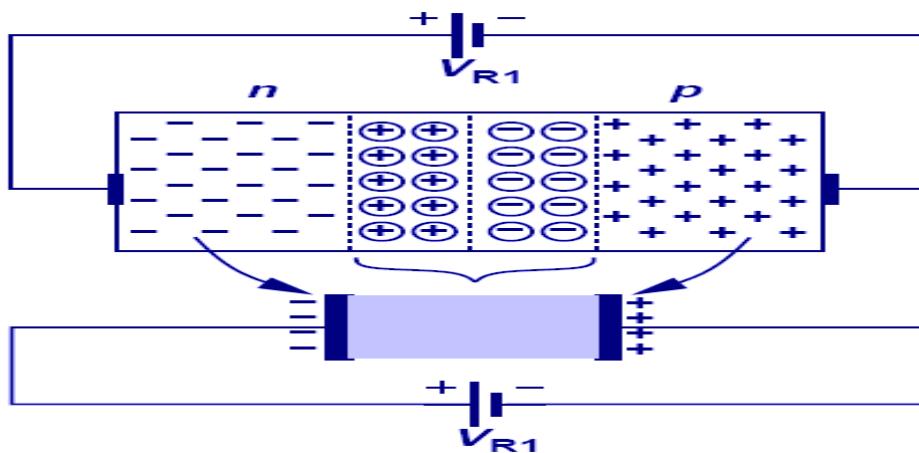
When the N-type region of a diode is connected to a higher potential than the P-type region, the diode is under reverse bias, which results in wider depletion region and larger built-in electric field across the junction.





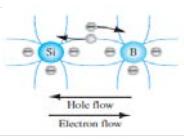
# Reverse Biased Diode's Application

## Voltage-Dependent Capacitor



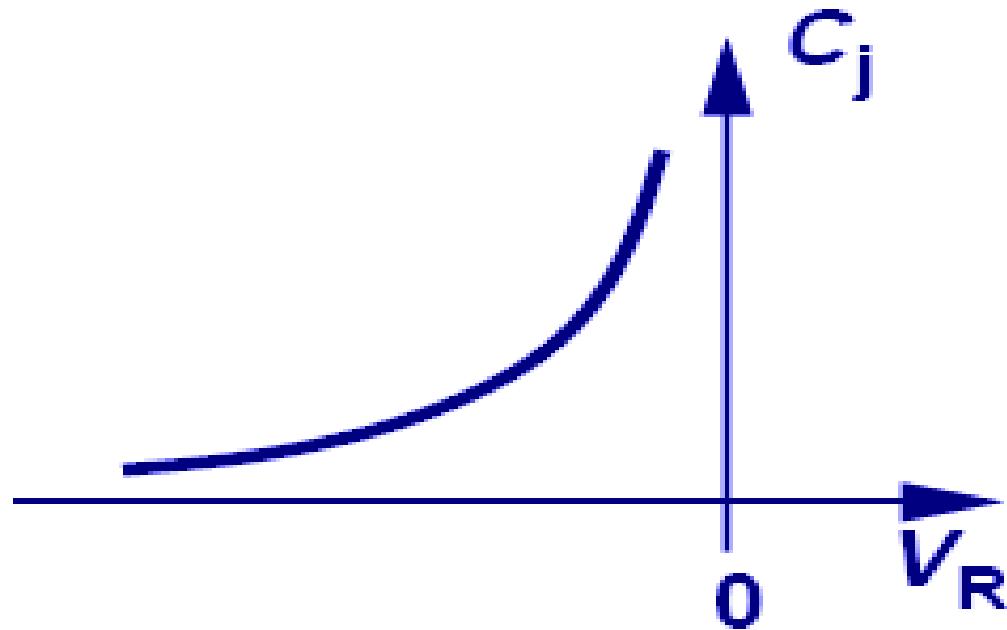
The PN junction can be viewed as a capacitor.  
By varying  $V_R$ , the depletion width changes, changing its capacitance value;  
therefore, the PN junction is actually a voltage-dependent capacitor.





# Voltage-Dependent Capacitance

Equations that describe the voltage-dependent capacitance

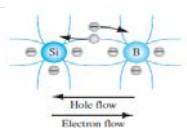


Voltage-dependent capacitance curve

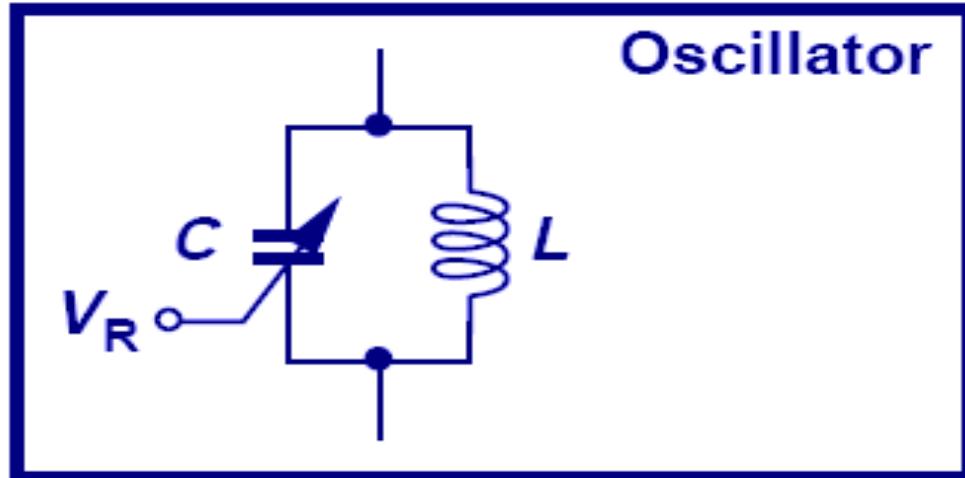
$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}}$$

$$C_{j0} = \sqrt{\frac{\epsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{V_0}}$$





# Voltage-Controlled Oscillator

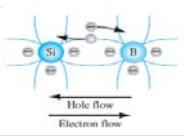


$$f_{res} = \frac{1}{2\pi} \frac{1}{\sqrt{LC}}$$

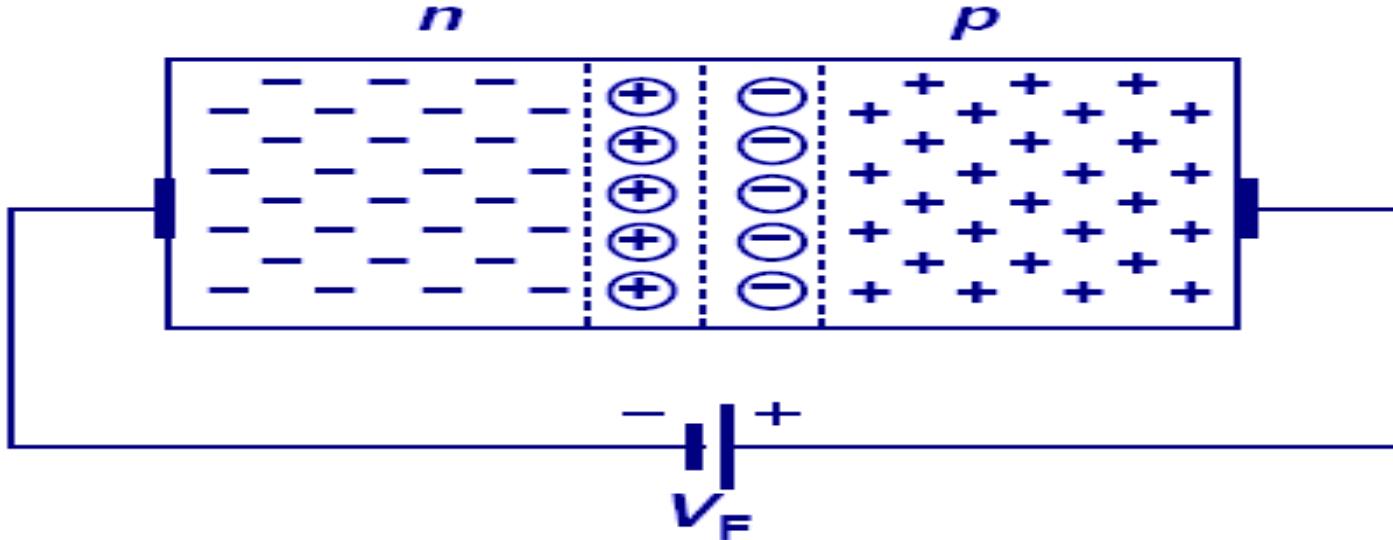
A very important application of a reverse-biased PN junction is VCO, in which an LC tank is used in an oscillator.

By changing  $V_R$ , we can change C, which also changes the oscillation frequency.





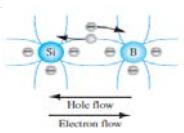
# Diode in Forward Bias



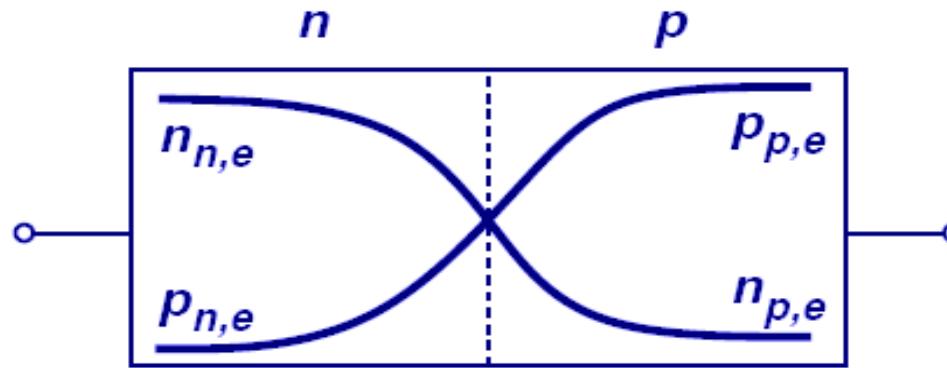
When the N-type region of a diode is at a lower potential than the P-type region, the diode is in forward bias.

The depletion width is shortened and the built-in electric field decreased.

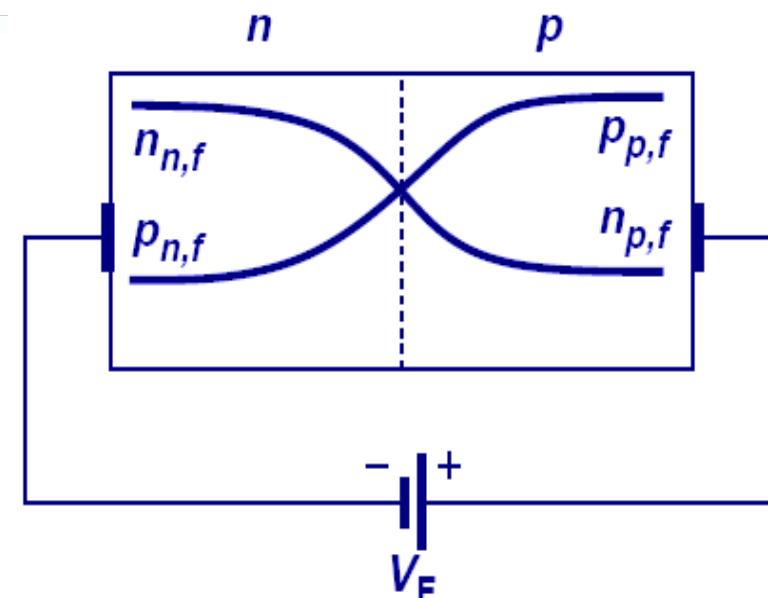




# Minority Carrier Profile in Forward Bias



$$P_{n,e} = \frac{p_{p,e}}{\exp \frac{V_o}{V_T}}$$

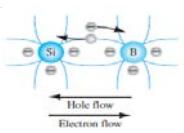


$$p_{n,f} = \frac{p_{p,f}}{\exp \frac{V_0 - V_F}{V_T}}$$

Under forward bias, minority carriers in each region increase due to the lowering of built-in field/potential.

Therefore, diffusion currents increase to supply these minority carriers.





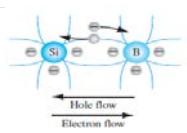
# Diffusion Current in Forward Bias

$$\Delta n_p \approx \frac{N_D}{\exp \frac{V_0}{V_T}} \left( \exp \frac{V_F}{V_T} - 1 \right) \quad \Delta p_n \approx \frac{N_A}{\exp \frac{V_0}{V_T}} \left( \exp \frac{V_F}{V_T} - 1 \right)$$
$$I_{tot} \propto \frac{N_A}{\exp \frac{V_0}{V_T}} \left( \exp \frac{V_F}{V_T} - 1 \right) + \frac{N_D}{\exp \frac{V_0}{V_T}} \left( \exp \frac{V_F}{V_T} - 1 \right)$$
$$I_{tot} = I_s \left( \exp \frac{V_F}{V_T} - 1 \right) \quad I_s = A q n_i^2 \left( \frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p} \right)$$

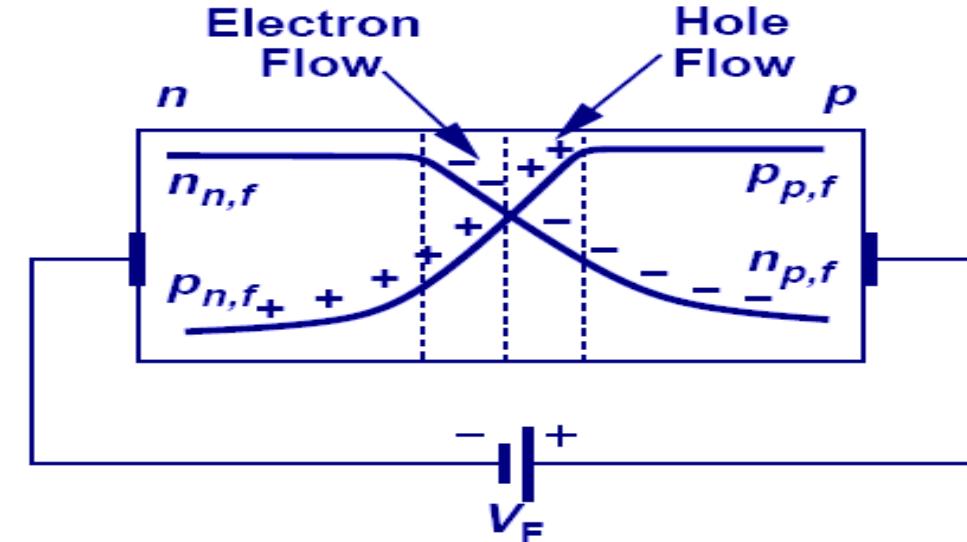
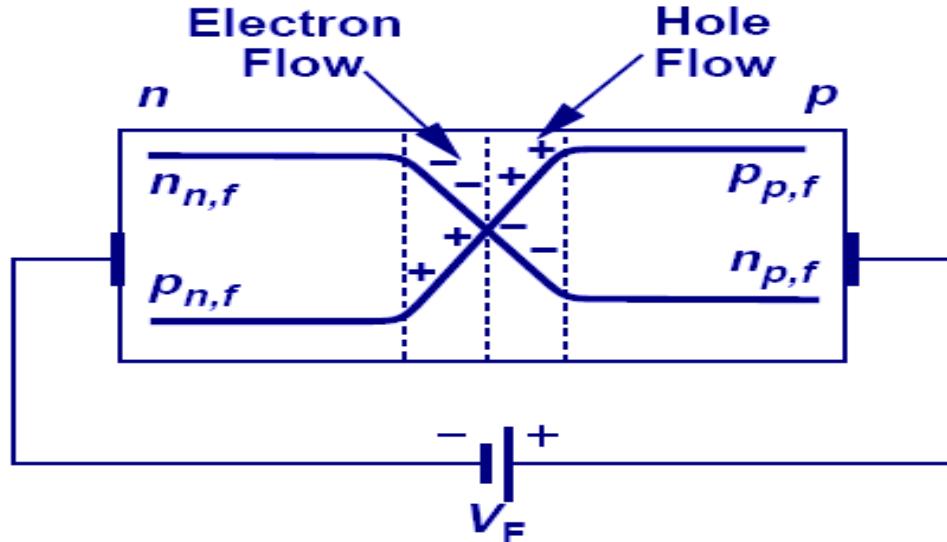
Diffusion current will increase in order to supply the increase in minority carriers.

The mathematics are shown above.





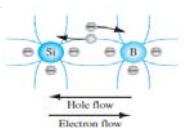
# Minority Charge Gradient



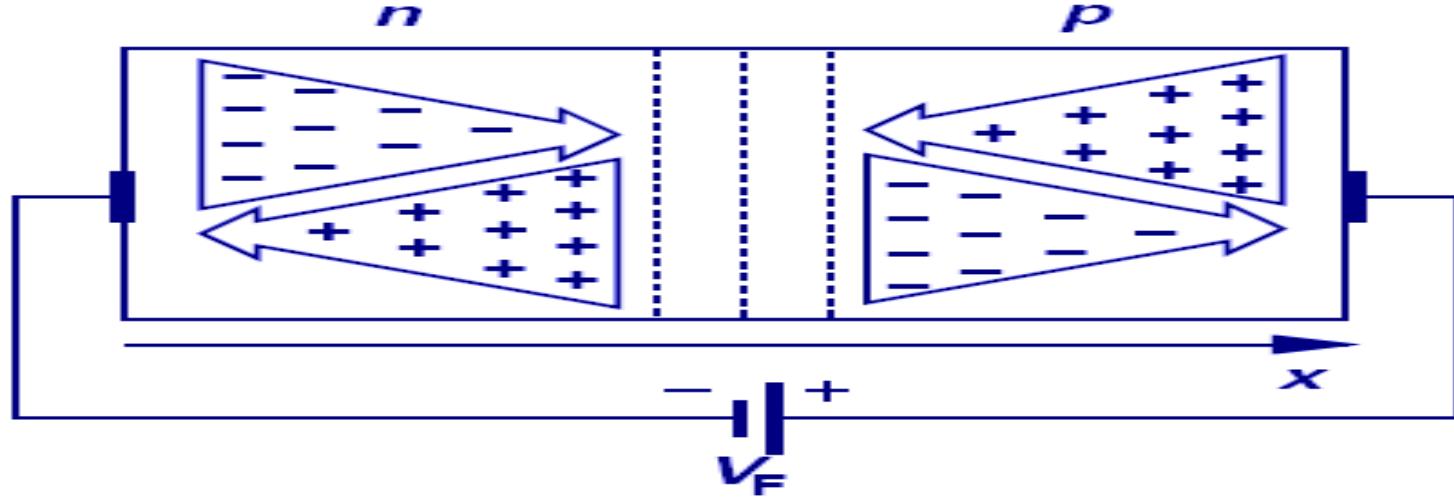
Minority charge profile should not be constant along the x-axis; otherwise, there is no concentration gradient and no diffusion current.

Recombination of the minority carriers with the majority carriers accounts for the dropping of minority carriers as they go deep into the P or N region.





# Forward Bias Condition: Summary

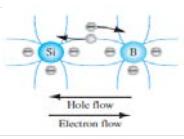


In forward bias, there are large diffusion currents of minority carriers through the junction.

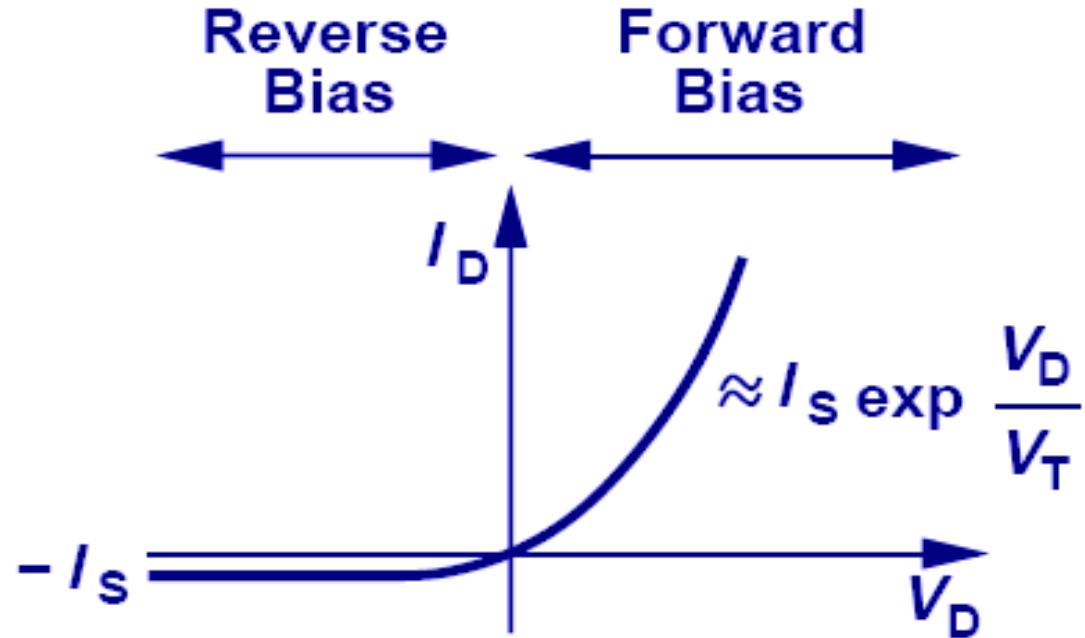
However, as we go deep into the P and N regions, recombination currents from the majority carriers dominate.

These two currents add up to a constant value.





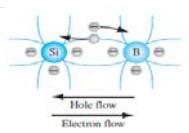
# IV Characteristic of PN Junction



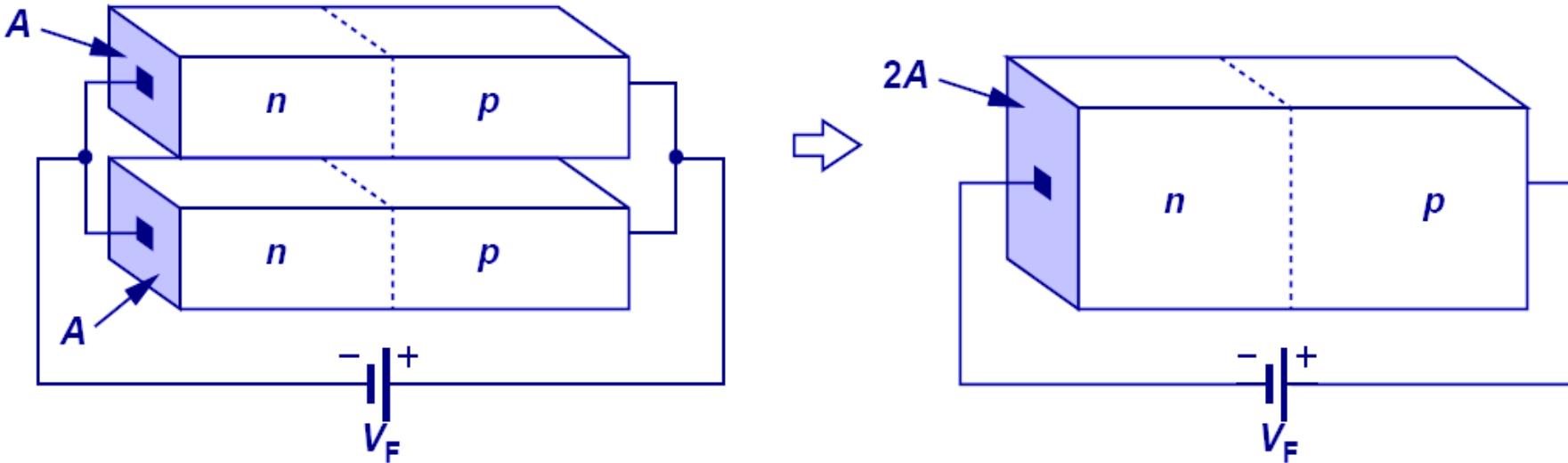
$$I_D = I_s \left( \exp \frac{V_D}{V_T} - 1 \right)$$

The current and voltage relationship of a PN junction is exponential in forward bias region, and relatively constant in reverse bias region.





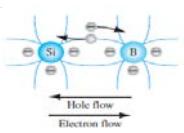
# Parallel PN Junctions



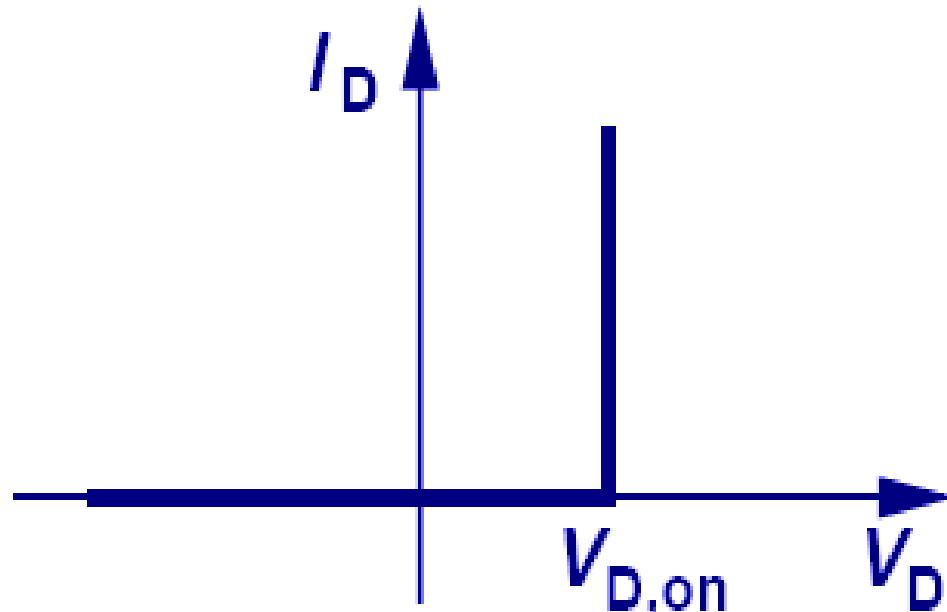
Since junction currents are proportional to the junction's cross-section area.

Two PN junctions put in parallel are effectively one PN junction with twice the cross-section area, and hence twice the current.





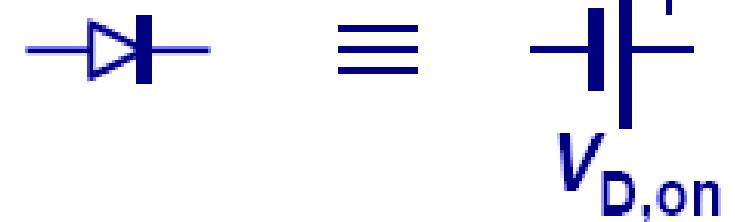
# Constant-Voltage Diode Model



$$V_D < V_{D,\text{on}}$$

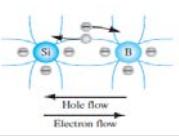


$$V_D > V_{D,\text{on}}$$

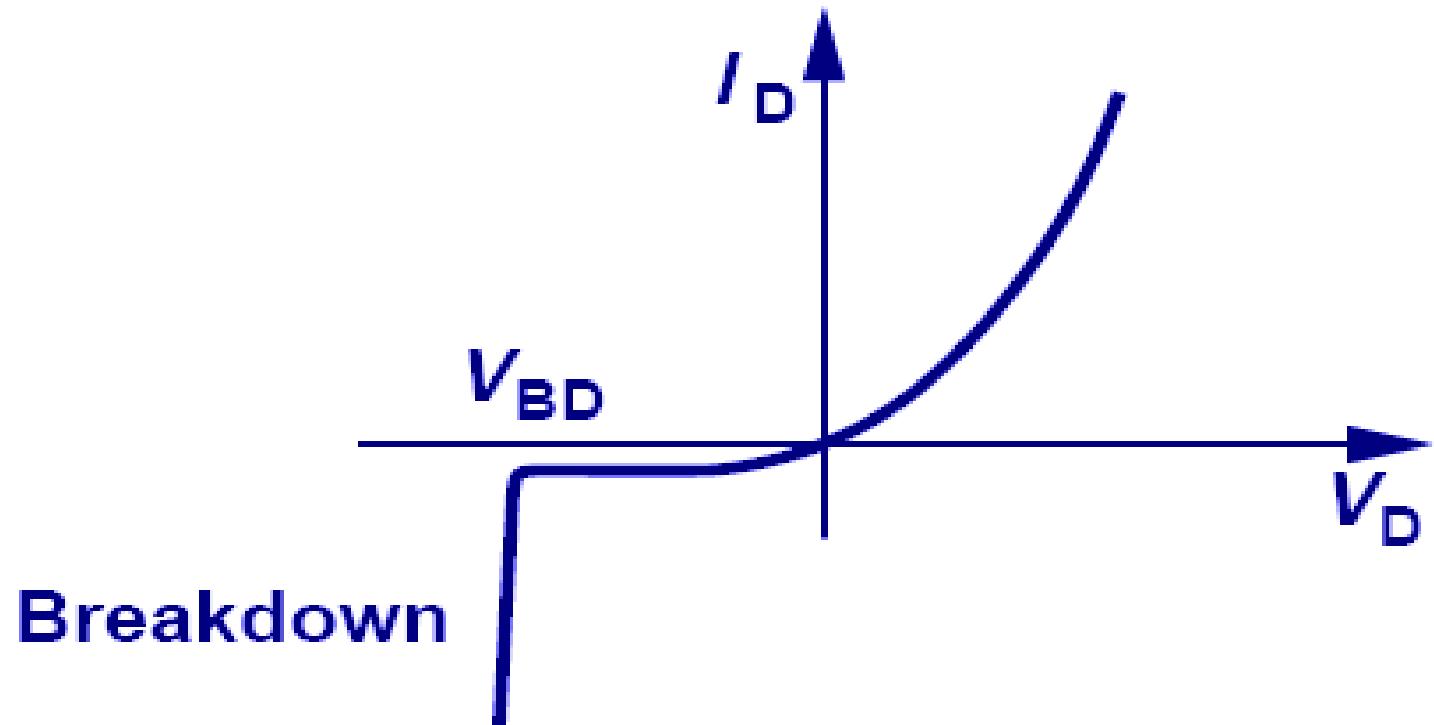


Diode operates as an open circuit if  $V_D < V_{D,\text{on}}$  and a constant voltage source of  $V_{D,\text{on}}$  if  $V_D$  tends to exceed  $V_{D,\text{on}}$ .



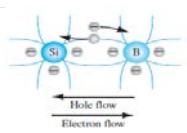


# Reverse Breakdown

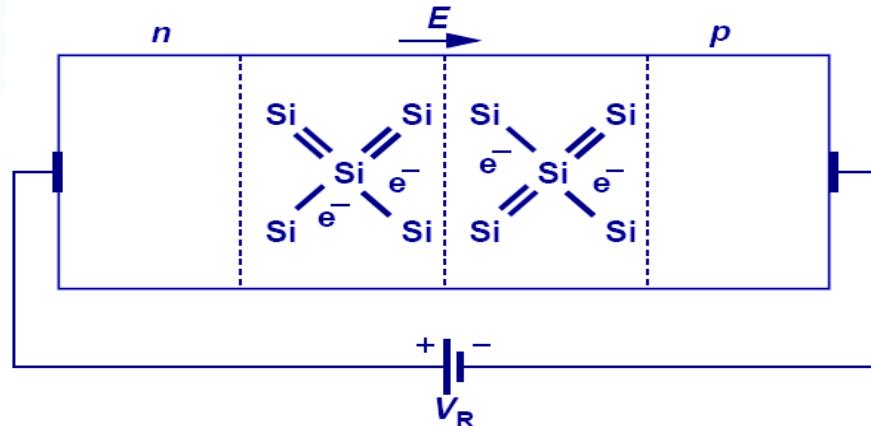


When a large reverse bias voltage is applied, breakdown occurs and an enormous current flows through the diode.



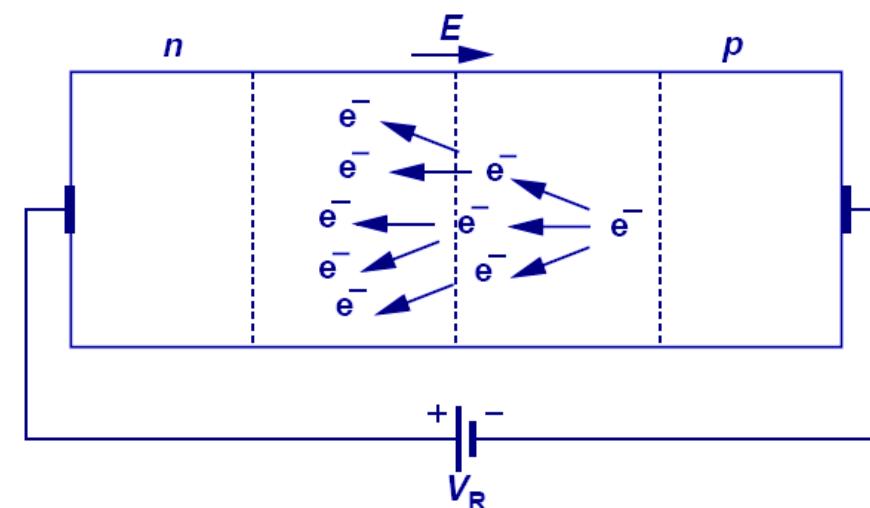


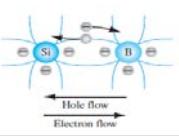
# Zener vs. Avalanche Breakdown



**Zener breakdown** is a result of the large electric field inside the depletion region that breaks electrons or holes off their covalent bonds.

**Avalanche breakdown** is a result of electrons or holes colliding with the fixed ions inside the depletion region.





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# Types of Diodes

## Diode Types

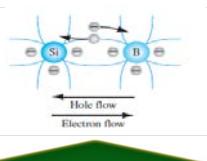
**Schottky  
Diode**

**Zener Diode**

**Light  
Emitting  
Diode LED**

**Standard  
Junction  
Diodes**





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# Schottky Diode

Schottky diodes are manufactured by bonding a metal conductor to an N-type semiconductor

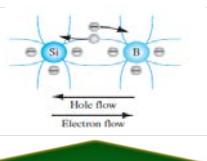
Electron from the N-type material migrate into the metal

This creates a potential barrier across the boundary, which then behaves in a similar fashion to a PN Junction

Schottky diodes are used in applications requiring high speed and low capacitance

Diodes are commonly rated by their switching speed, maximum power dissipation, maximum forward current, maximum forward voltage at a specified forward current, and reverse breakdown voltage





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# Zener Diode

Zener diodes are manufactured with controlled reverse-breakdown properties.

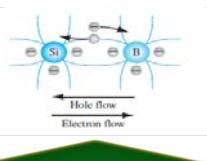
Their forward characteristics are similar to those of junction diodes; however, Zener diodes are used in reverse-biased mode.

Zener diodes are designed to operate at and around their reverse-breakdown('Zener') voltage.

The Zener voltage is determined during the manufacturing process by adjusting the semiconductor doping.

Typical Zener voltages range from 3.3 to 75 volts.





# Light-Emitting Diode -LED

LEDs are junction diodes typically made from gallium arsenide phosphide (GaAsP).

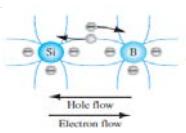
LEDs act very much like silicon junction diodes except that they emit light when conducting forward current

LEDs have forward voltage drops about twice as large as silicon diodes.

## LED Types

Infrared, red, orange, yellow, green, and blue





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# Thank You Very Much

Dipl.-Ing. B. Kommey

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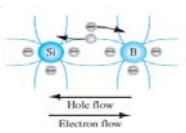
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

050 770 32 86

Whatsup: 0507703286

Skype\_id: calculus.affairs

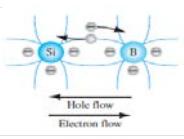




“Men marry women with the hope they  
will never change.  
Women marry men with the hope they  
will change.  
Invariably they are both disappointed.”

**Albert Einstein**





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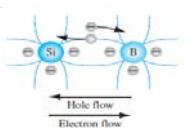
# Overview

## Diode Circuits

Diode as Circuit Element

Diode Applications





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# Overview

## Diode Circuits

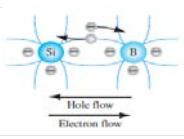
### Diode as Circuit Element

Ideal Diode

Circuit  
Characteristics

Real Diode





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# Overview

## Diode Circuits

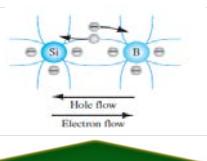
## Diode Applications

Rectifiers

Regulators

Limiting and Clamping  
Circuits





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# Diode - Recap

The diode is a two terminal non-linear device

Its I-V characteristics besides exhibiting non-linear behavior is also polarity dependent

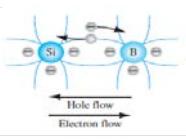
Meaning that the behavior of a diode depends on the relative polarity of its terminals

Depending on the polarity of the voltage  $v_d$  the diode is said to be:

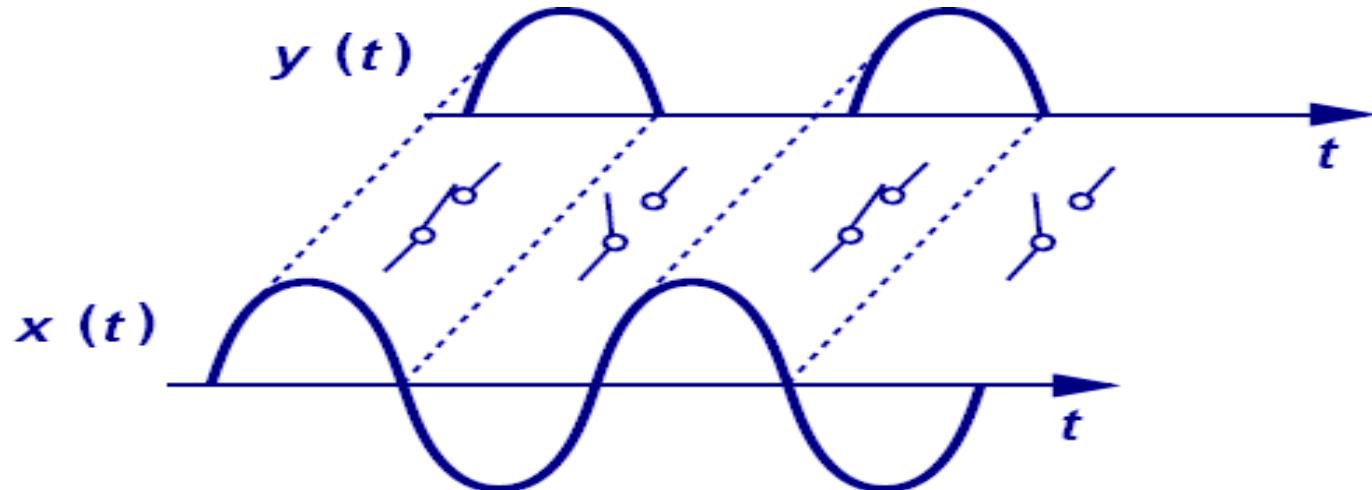
Forward bias  $v_d > 0$ ; Anode voltage > cathode voltage

Reverse bias  $v_d < 0$ ; Cathode voltage > anode voltage



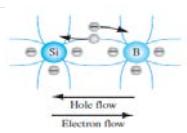


# Ideal Diode



The diode behaves as a short circuit during the positive half cycle (voltage across it tends to exceed zero), and an open circuit during the negative half cycle (voltage across it is less than zero).





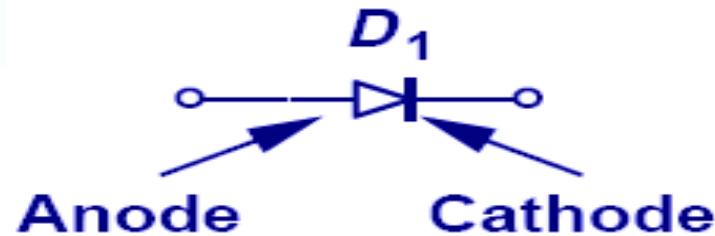
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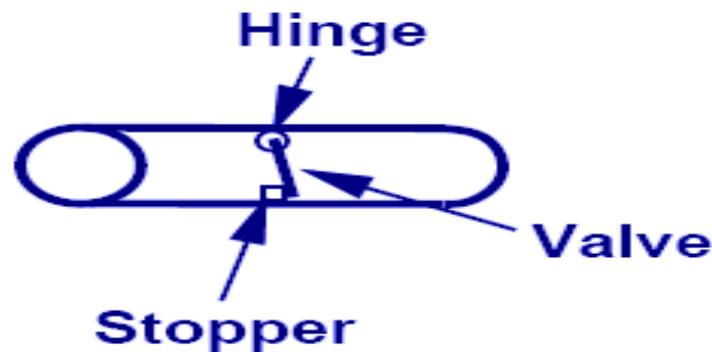
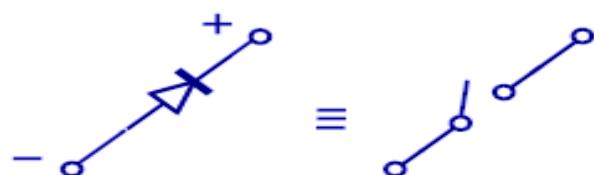
# Ideal Diode



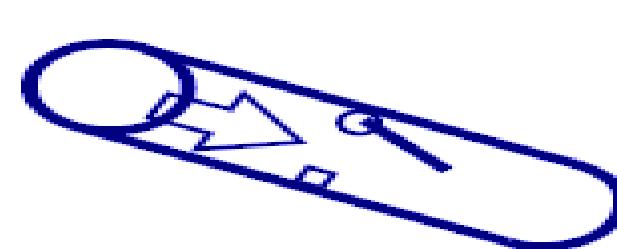
**Forward Bias**  
 $V_{\text{anode}} > V_{\text{cathode}}$



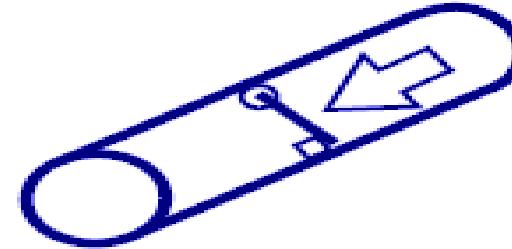
**Reverse Bias**  
 $V_{\text{anode}} < V_{\text{cathode}}$



**Forward Bias**

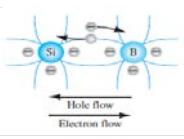


**Reverse Bias**



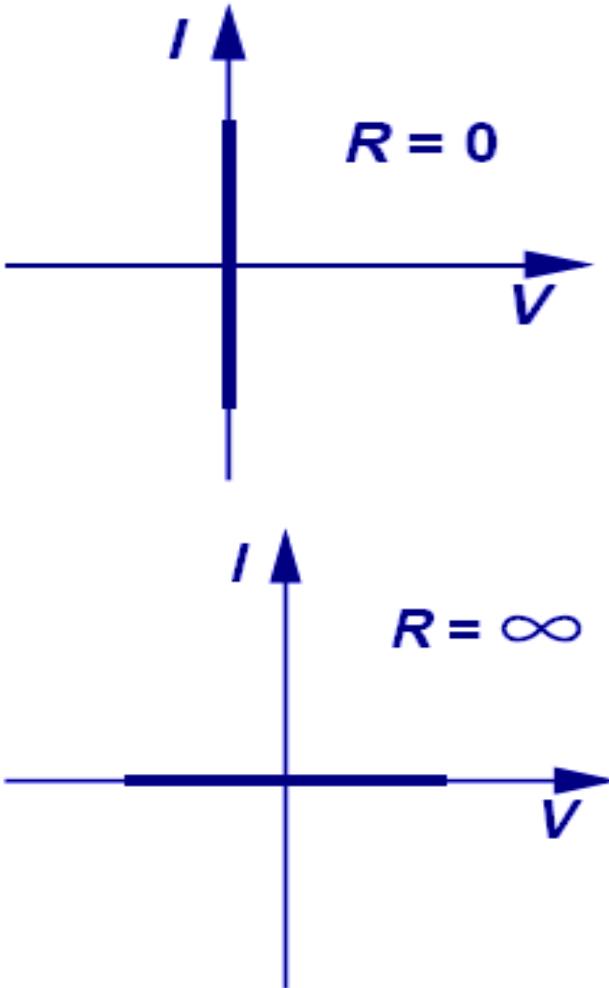
In an ideal diode, if the voltage across it tends to exceed zero, current flows. It is analogous to a water pipe that allows water to flow in only one direction.



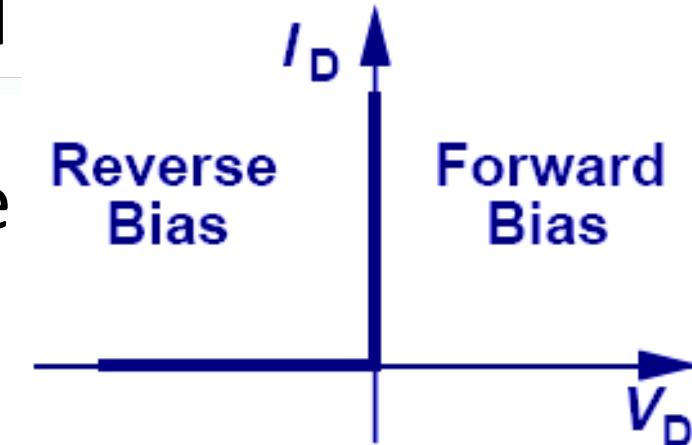


## IV Characteristics of an Ideal Diode

If the voltage across anode and cathode is greater than zero, the resistance of an ideal diode is zero and current becomes infinite.



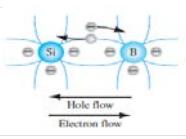
However, if the voltage is less than zero, the resistance becomes infinite and current is zero.



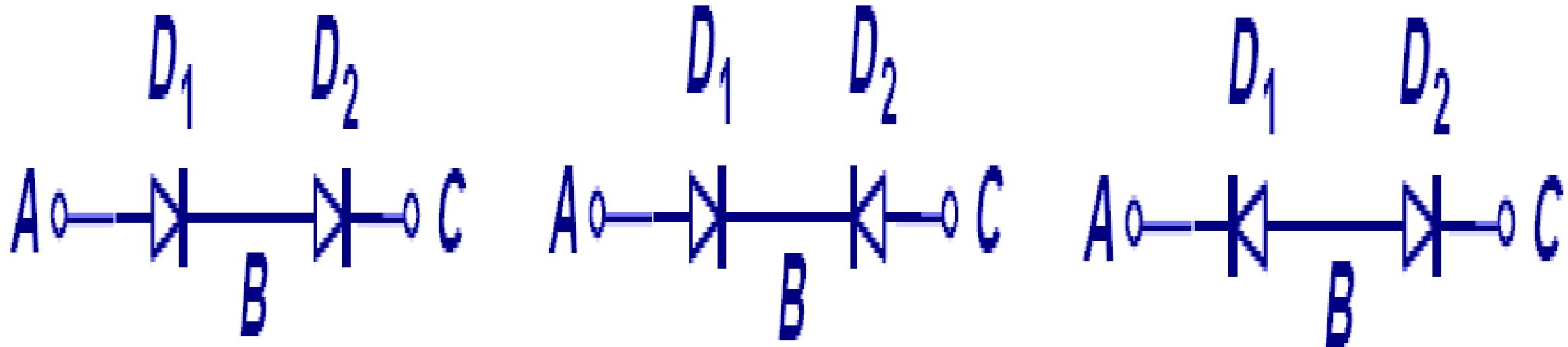
$$R = 0 \Rightarrow I = \frac{V}{R} = \infty$$

$$R = \infty \Rightarrow I = \frac{V}{R} = 0$$





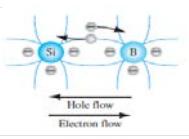
# Diodes in Series



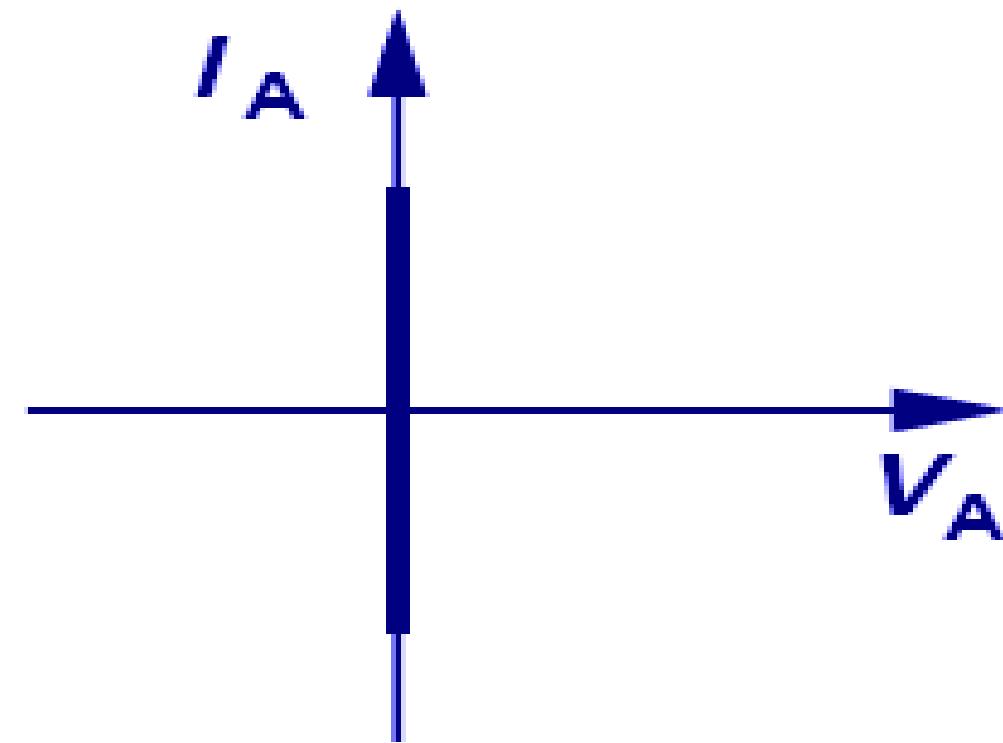
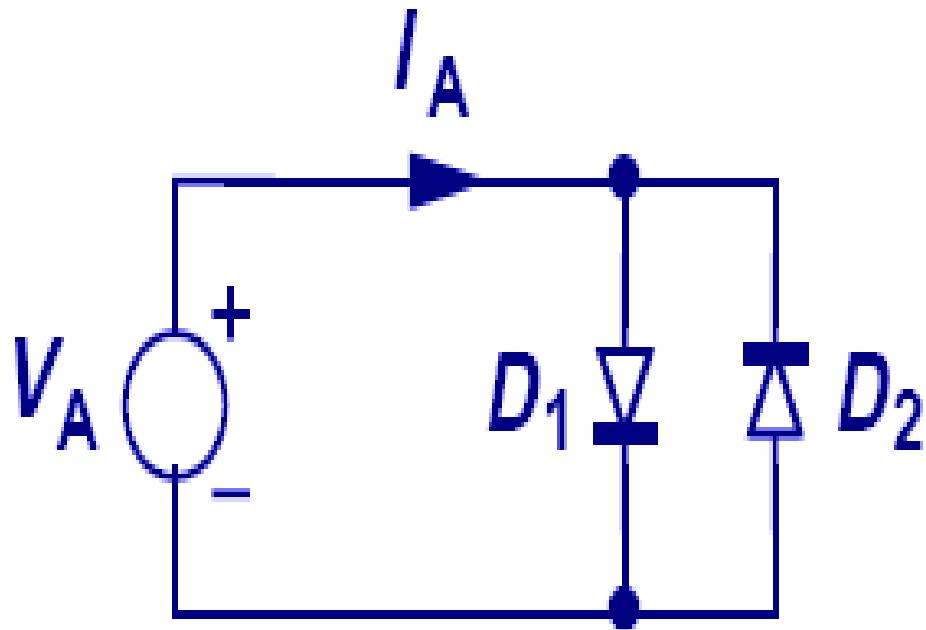
Diodes cannot be connected in series randomly.

For the circuits above, only a) can conduct current from A to C.



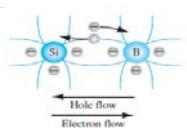


# Anti-Parallel Ideal Diodes

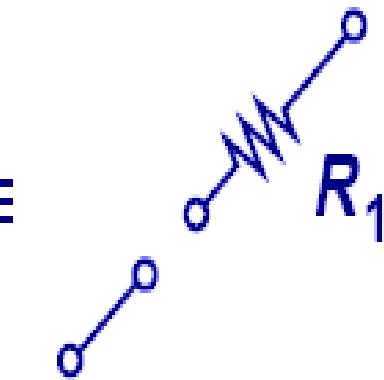
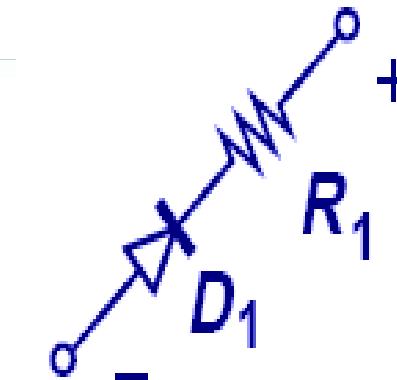
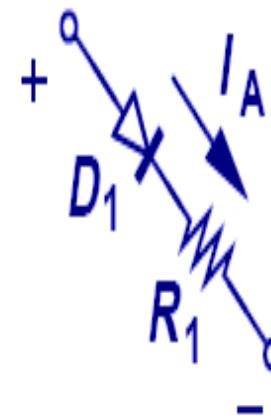
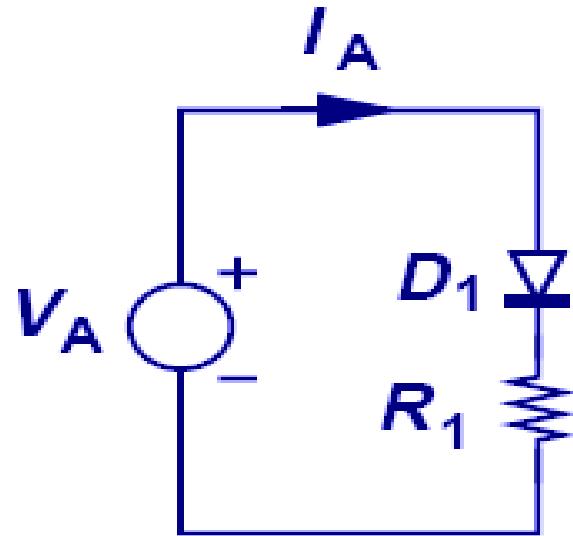


If two diodes are connected in anti-parallel, it acts as a short for all voltages.

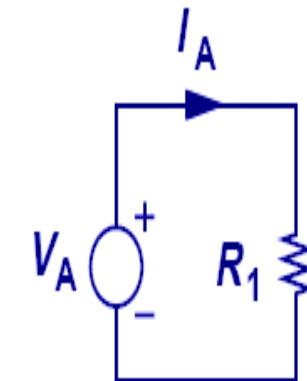
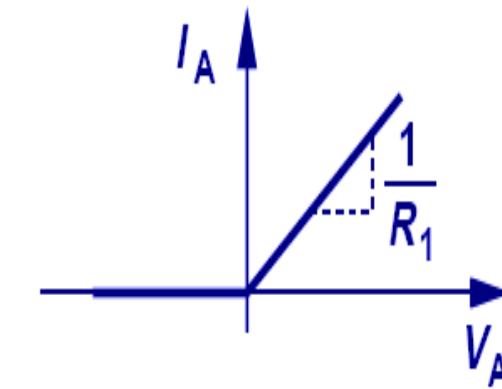


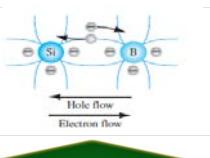


# Diode-Resistor Combination

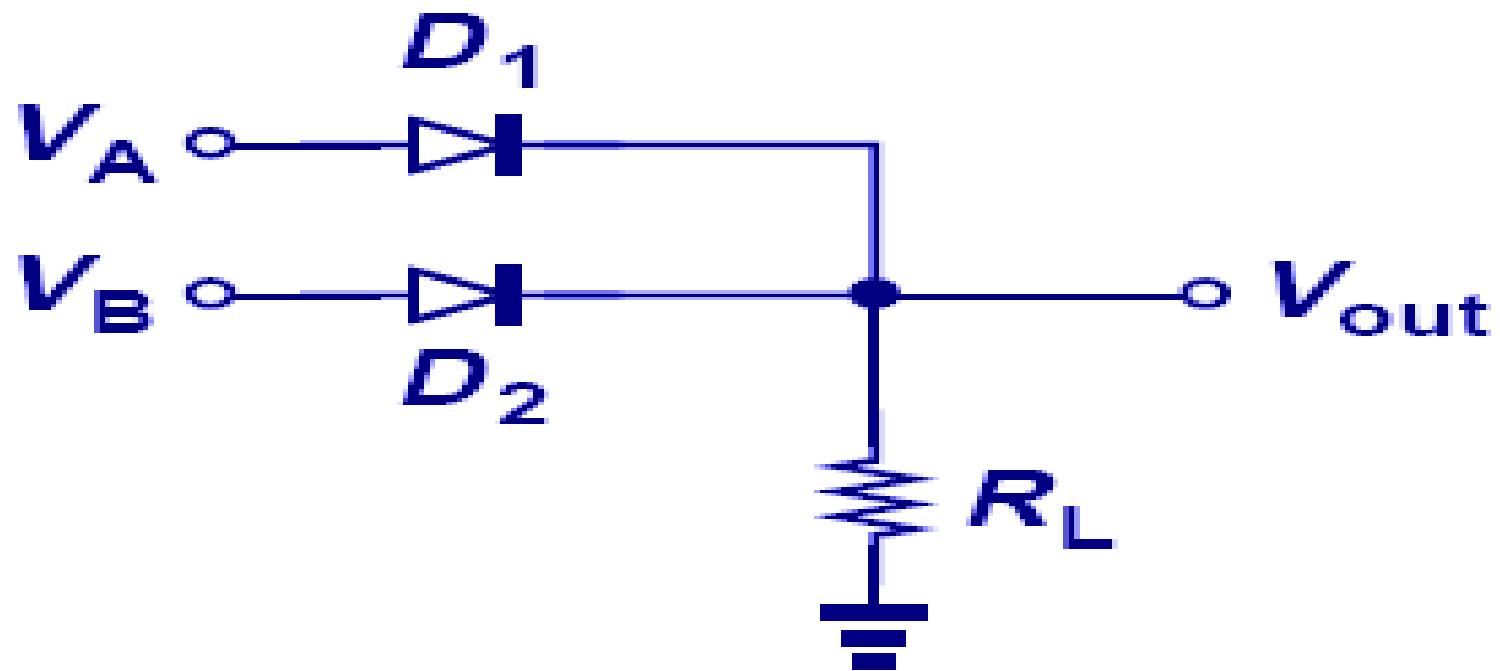


The IV characteristic of this diode-resistor combination is zero for negative voltages and Ohm's law for positive voltages.



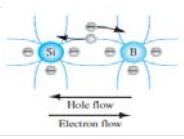


# Diode Implementation of OR Gate

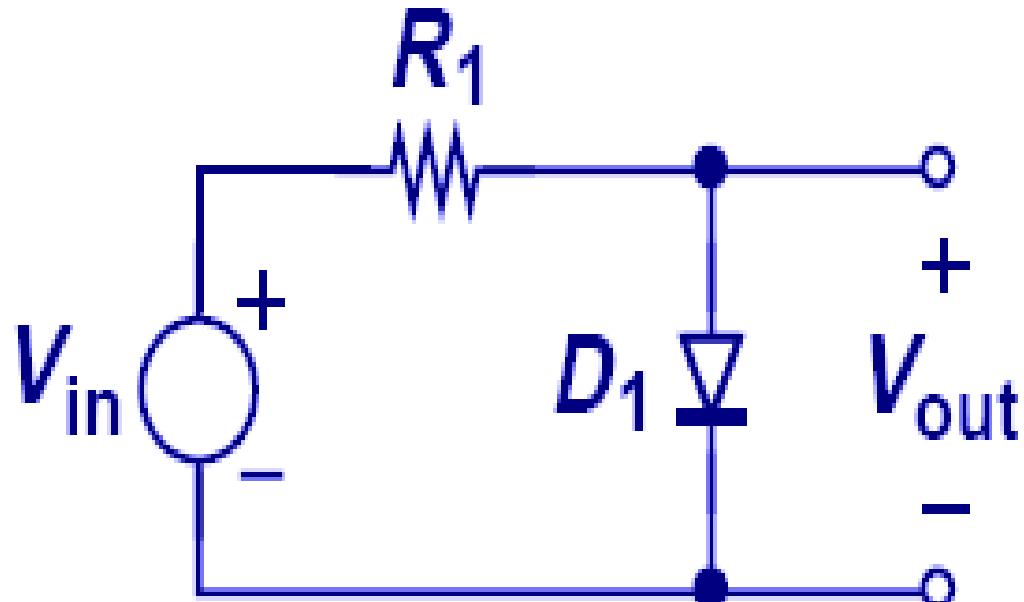


The circuit shows an example of diode-implemented as OR gate.  
 $V_{out}$  can only be either  $V_A$  or  $V_B$ , not both.

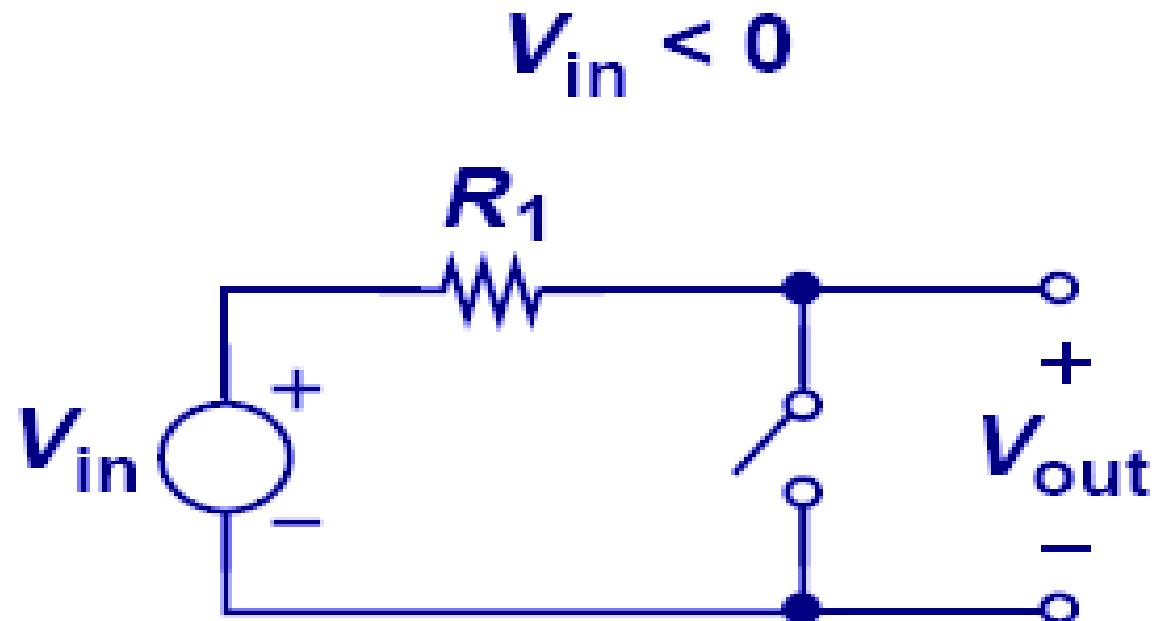


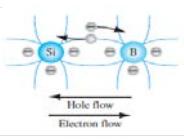


# Input / Output Characteristics



When  $V_{in}$  is less than zero, the diode opens, so  $V_{out} = V_{in}$ .

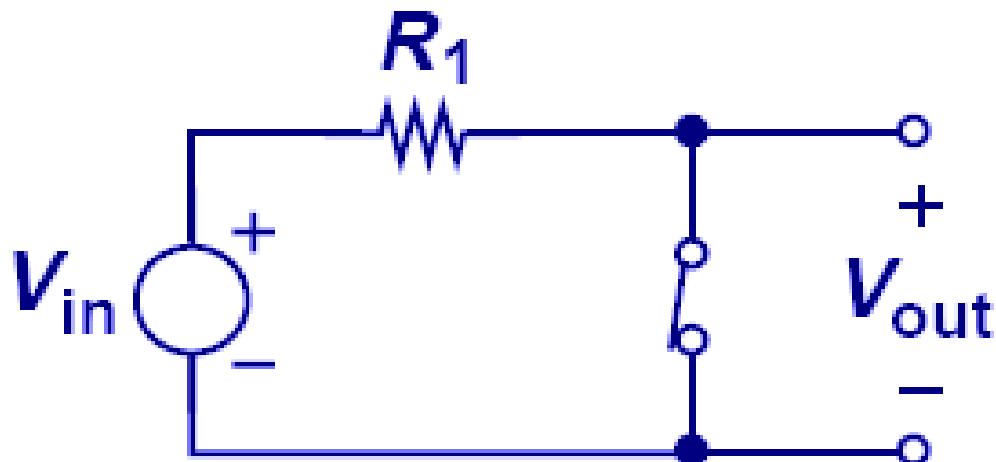




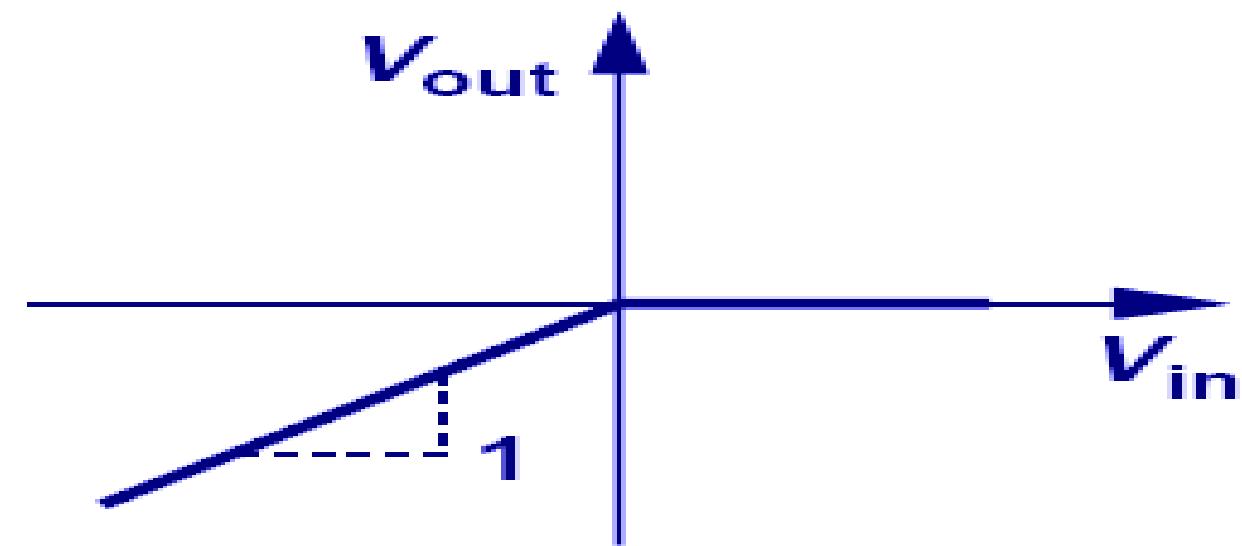
# Input / Output Characteristics

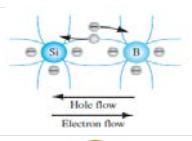
When  $V_{in}$  is greater than zero, the diode shorts, so  $V_{out} = 0$ .

$$V_{in} > 0$$

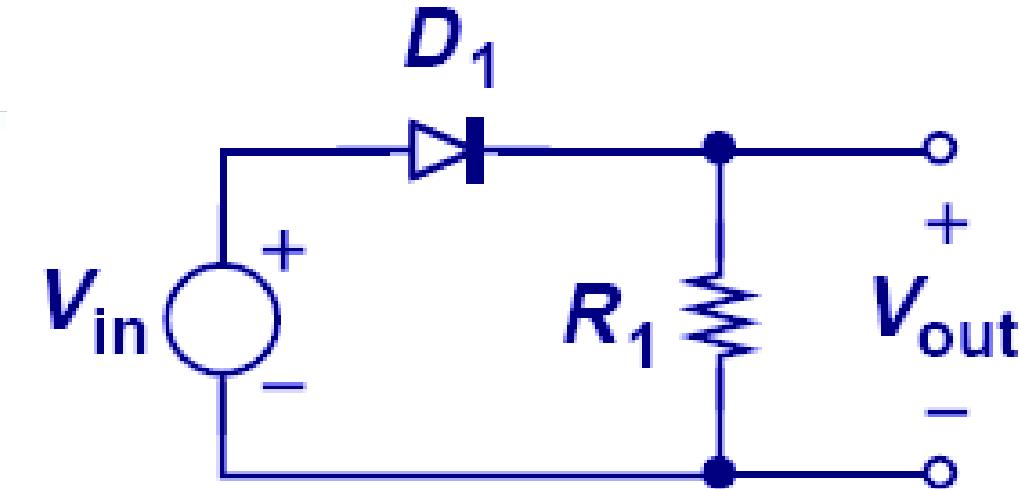
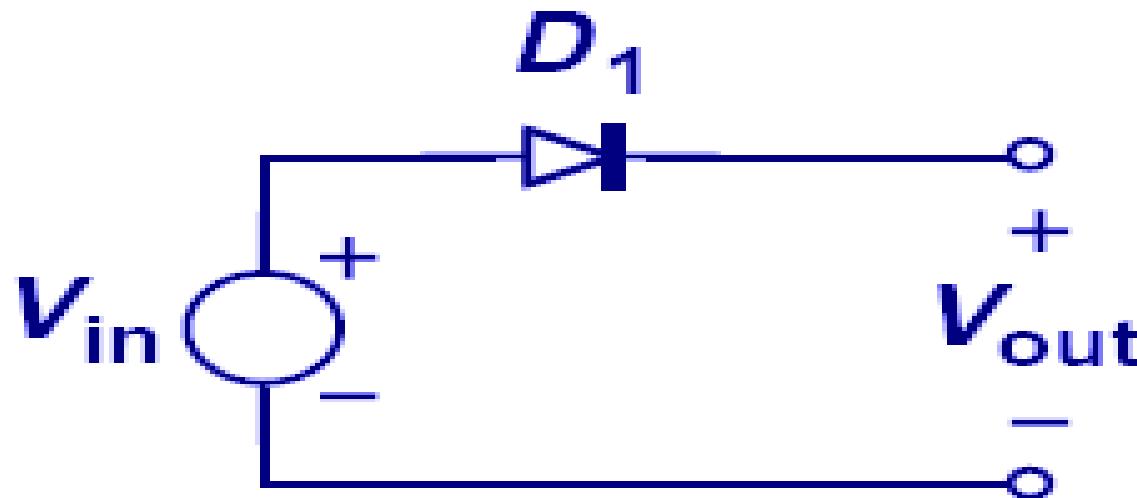


## IO Characteristics





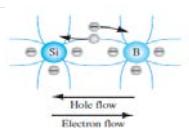
# Diode's Application: Rectifier



A rectifier is a device that converts AC to DC by blocking the flow of current in one direction

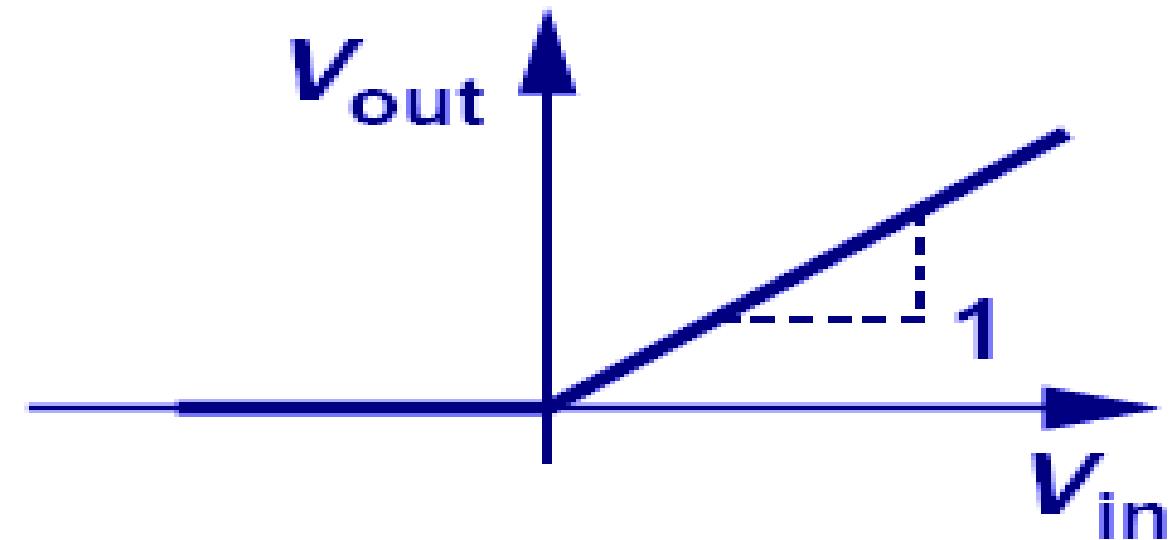
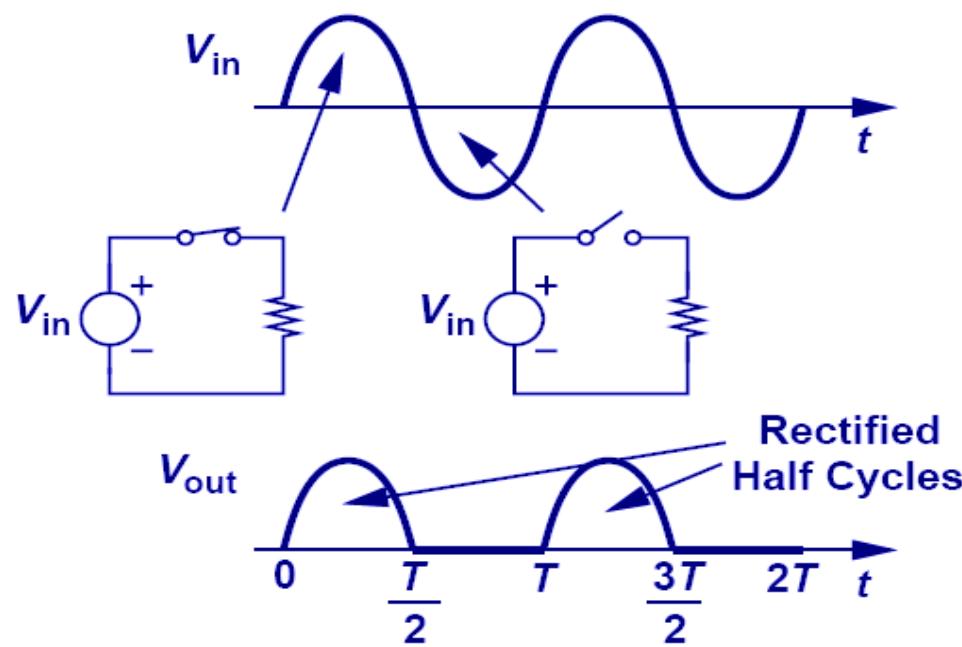
A rectifier passes positive-half cycle of a sinusoid and blocks the negative half-cycle or vice versa.

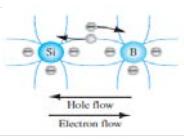




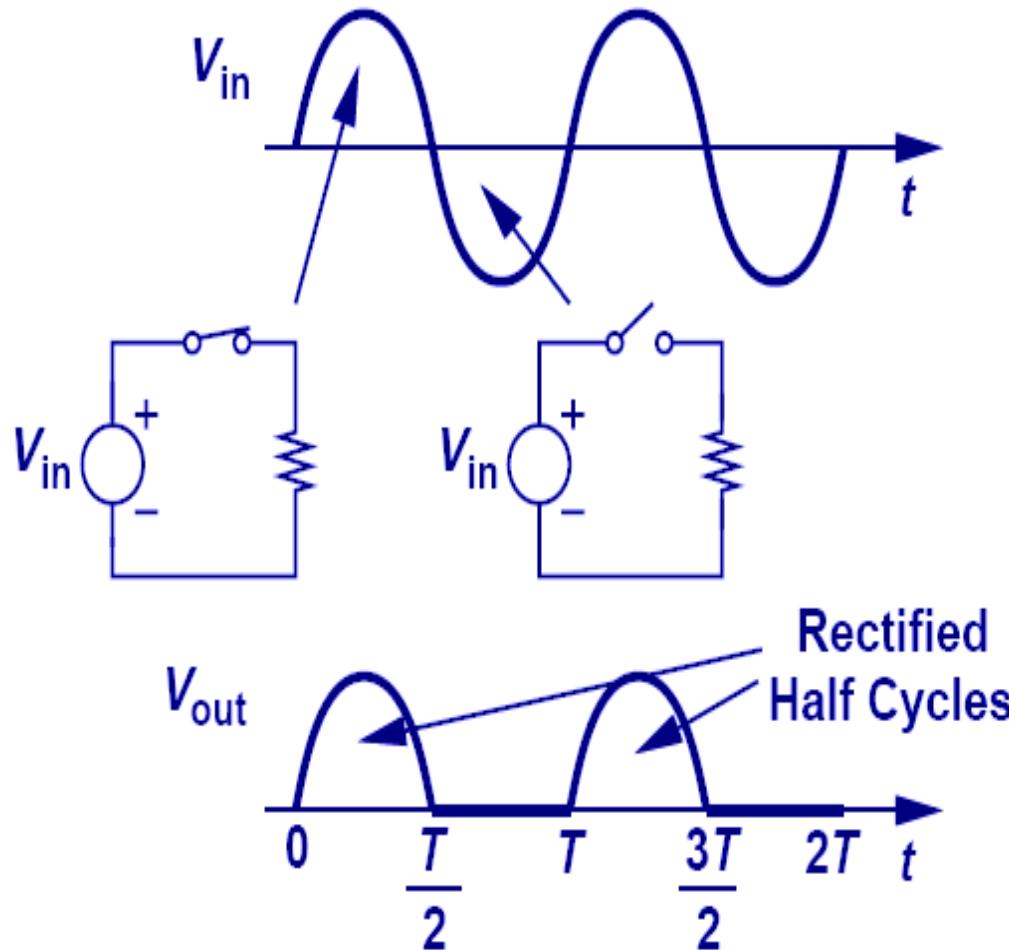
# Diode's Application: Rectifier

When  $V_{in}$  is greater than 0, diode shorts, so  $V_{out} = V_{in}$ ;  
however, when  $V_{in}$  is less than 0, diode opens, no current flows thru  $R_1$ ,  $V_{out} = I_{R1}R_1 = 0$ .





# Signal Strength Indicator SSI

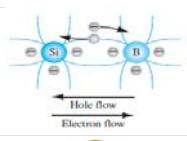


$$V_{out} = V_p \sin \omega t = 0 \quad \text{for } 0 \leq t \leq \frac{T}{2}$$

$$\begin{aligned} V_{out,avg} &= \frac{1}{T} \int_0^T V_{out}(t) dt = \frac{1}{T} \int_0^{T/2} V_p \sin \omega t dt \\ &= \frac{1}{T} \frac{V_p}{\omega} [-\cos \omega t]_0^{T/2} = \frac{V_p}{\pi} \end{aligned}$$

$\text{for } \frac{T}{2} \leq t \leq T$





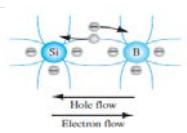
# Signal Strength Indicator SSI

$$V_{out,avg} = \frac{1}{T} \int_0^T V_{out}(t) dt = \frac{1}{T} \int_0^{T/2} V_p \sin \omega t dt$$
$$= \frac{1}{T} \frac{V_p}{\omega} [-\cos \omega t]_0^{T/2} = \frac{V_p}{\pi}$$

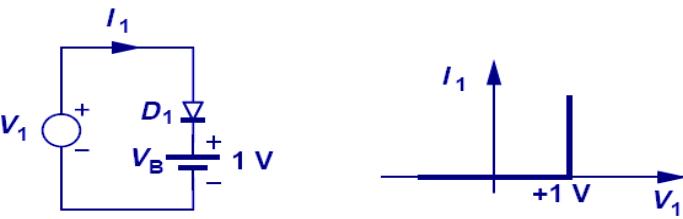
for  $\frac{T}{2} \leq t \leq T$

The averaged value of a rectifier output can be used as a signal strength indicator for the input, since  $V_{out,avg}$  is proportional to  $V_p$ , the input signal's amplitude.

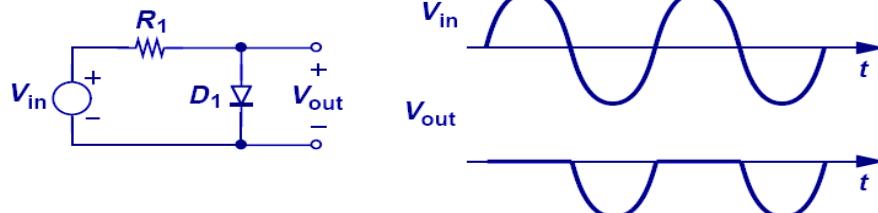
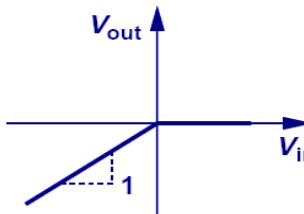




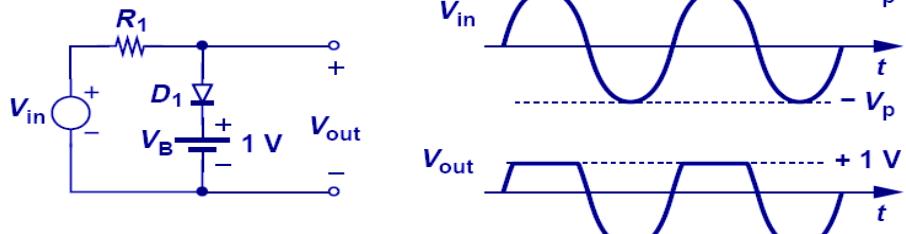
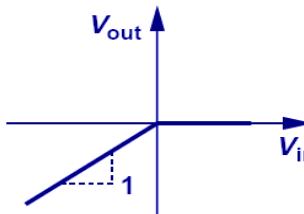
# Diode's Application: Limiter



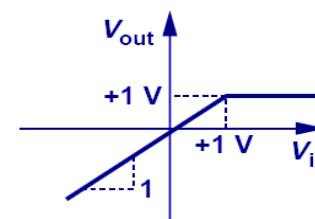
(a)



(b)



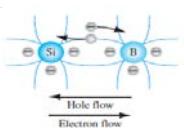
(c)



The purpose of a limiter is to force the output to remain below certain value.

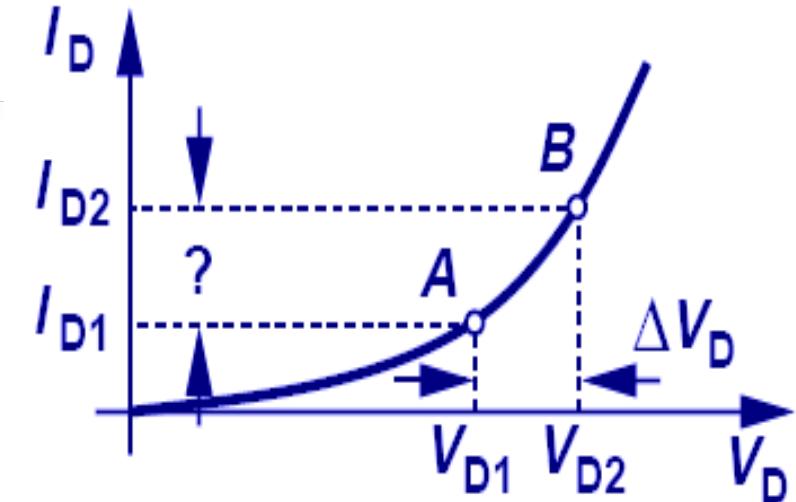
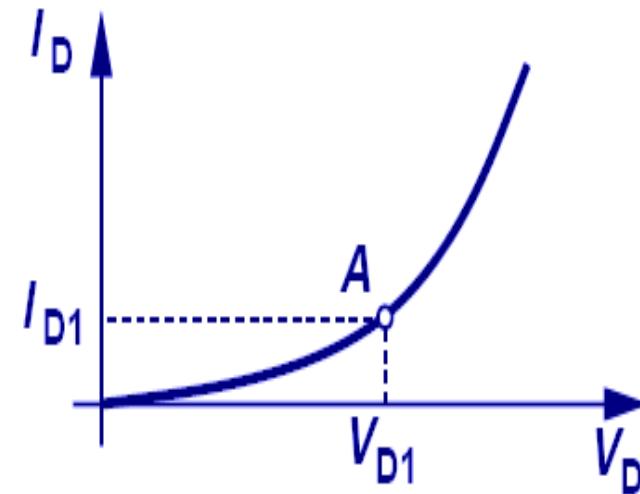
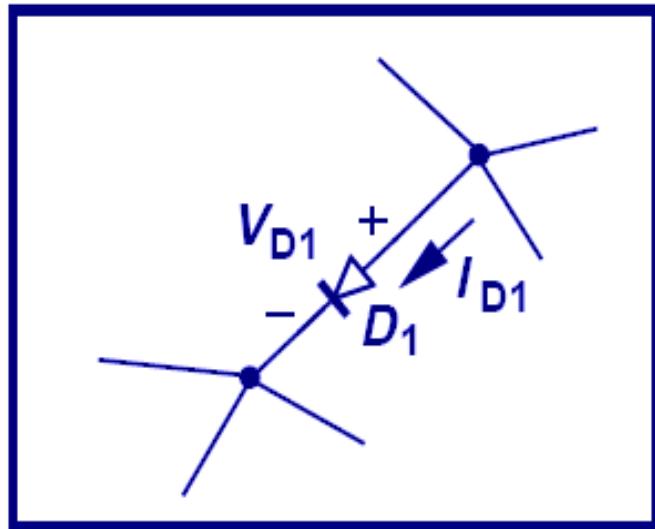
In a), the addition of a 1 V battery forces the diode to turn on after  $V_1$  has become greater than 1 V.





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DEPARTMENT OF COMPUTER ENGINEERING  
KWAME NKRUMAH UNIVERSITY OF SCIENCE  
AND TECHNOLOGY, KUMASI, GHANA

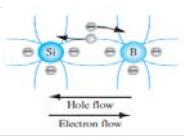
# Small-Signal Analysis



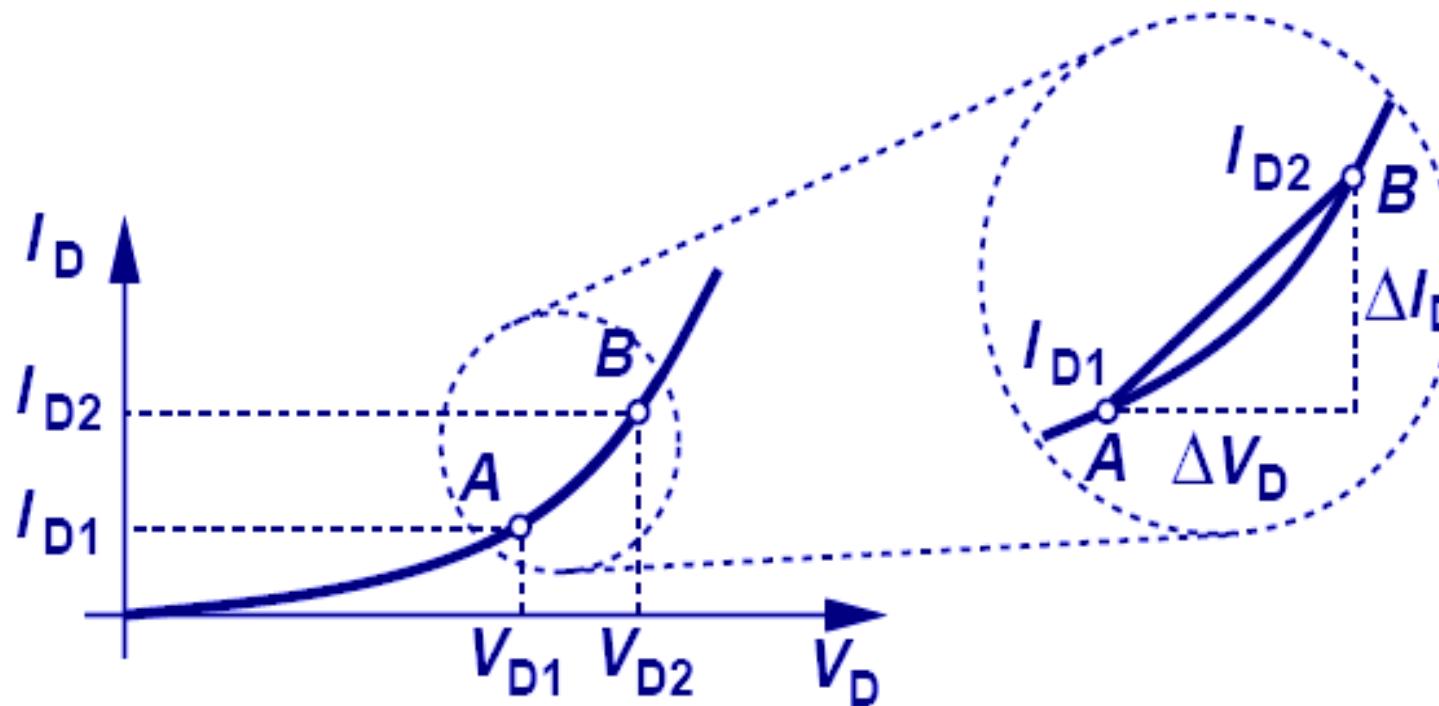
$$\Delta I_D = \frac{\Delta V}{V_T} I_{D1}$$

Small-signal analysis is performed around a bias point by perturbing the voltage by a small amount and observing the resulting linear current perturbation.





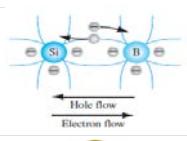
# Small-Signal Analysis in Detail



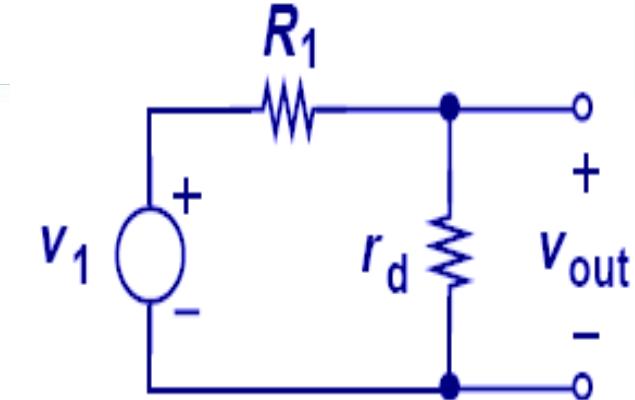
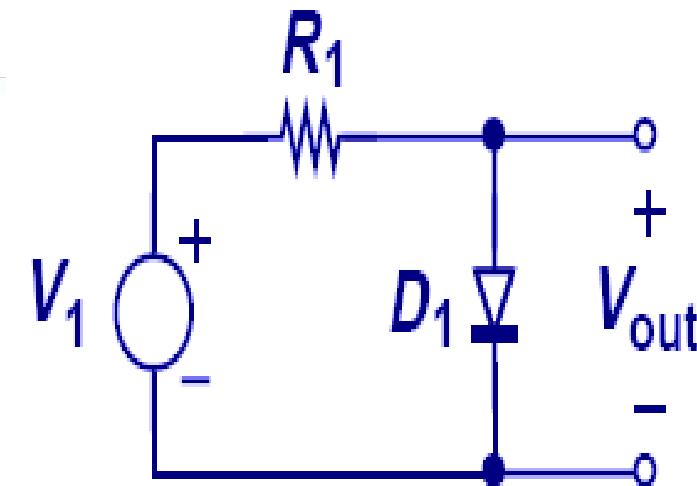
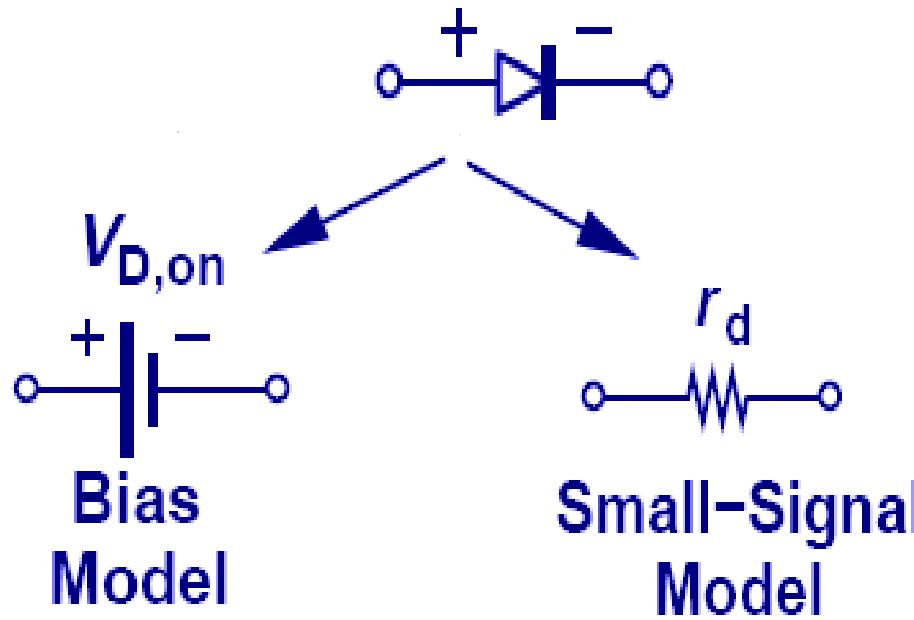
$$\begin{aligned}\frac{\Delta I_D}{\Delta V_D} &= \frac{dI_D}{dV_D} \Big|_{V_D=V_{D1}} \\ &= \frac{I_s}{V_T} \exp \frac{I_{D1}}{V_T} \\ &= \frac{I_{D1}}{V_T}\end{aligned}$$

If two points on the IV curve of a diode are close enough, the trajectory connecting the first to the second point is like a line, with the slope being the proportionality factor between change in voltage and change in current.





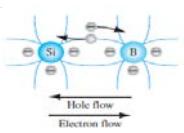
# Small-Signal Incremental Resistance



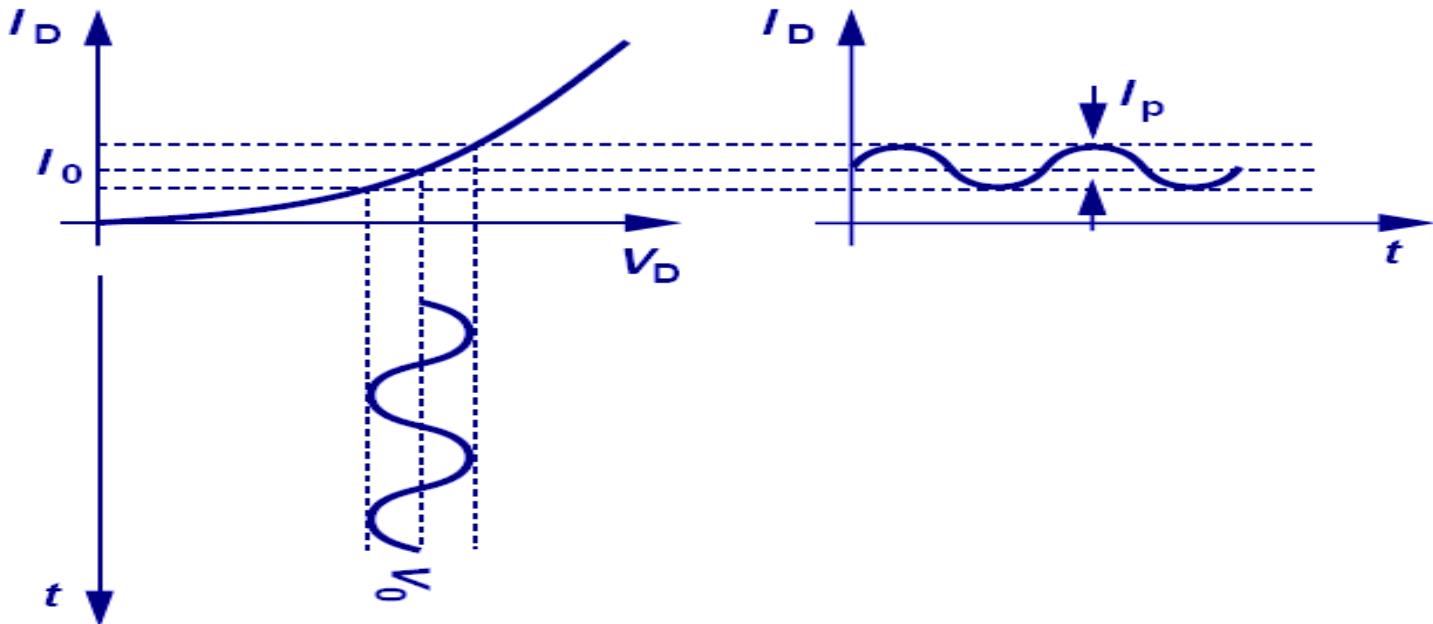
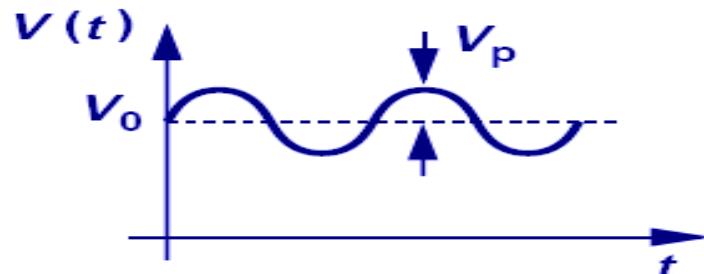
$$r_d = \frac{V_T}{I_D}$$

Since there's a linear relationship between the small signal current and voltage of a diode, the diode can be viewed as a linear resistor when only small changes are of interest.





# Small Sinusoidal Analysis

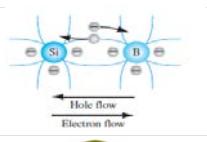


$$V(t) = V_0 + V_p \cos \omega t$$

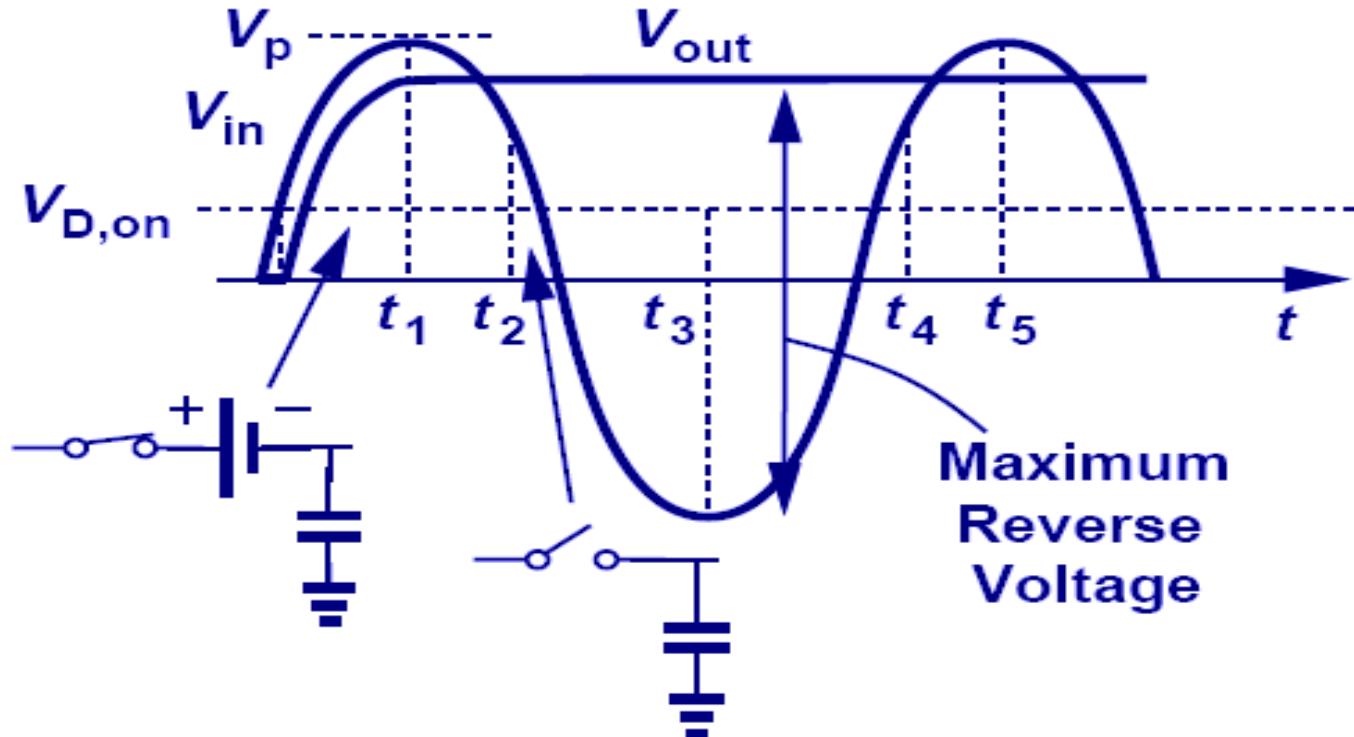
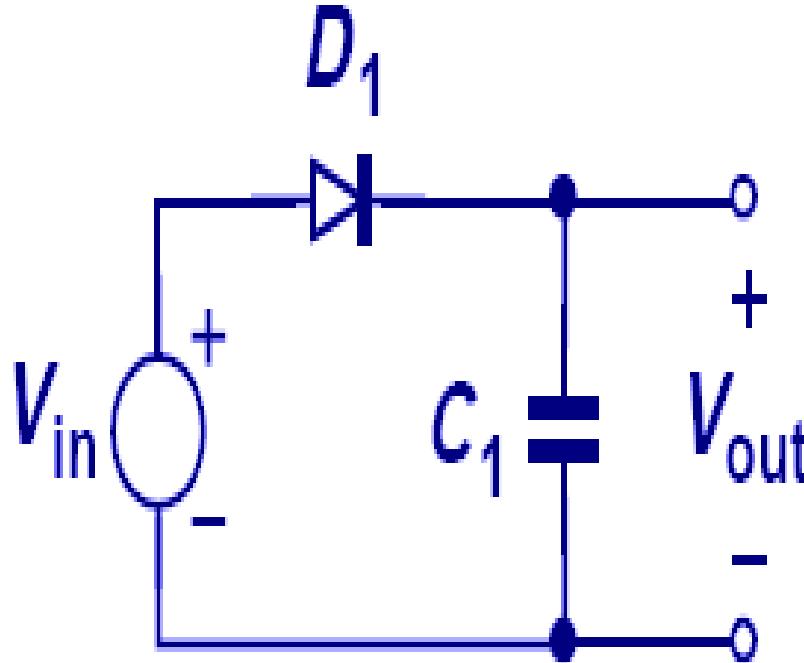
$$I_D(t) = I_0 + I_p \cos \omega t = I_s \exp \frac{V_0}{V_T} + \frac{V_T}{I_0} V_p \cos \omega t$$

If a sinusoidal voltage with small amplitude is applied, the resulting current is also a small sinusoid around a DC value.



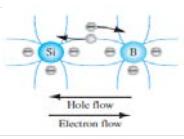


# Diode-Capacitor Circuit: Constant Voltage Model

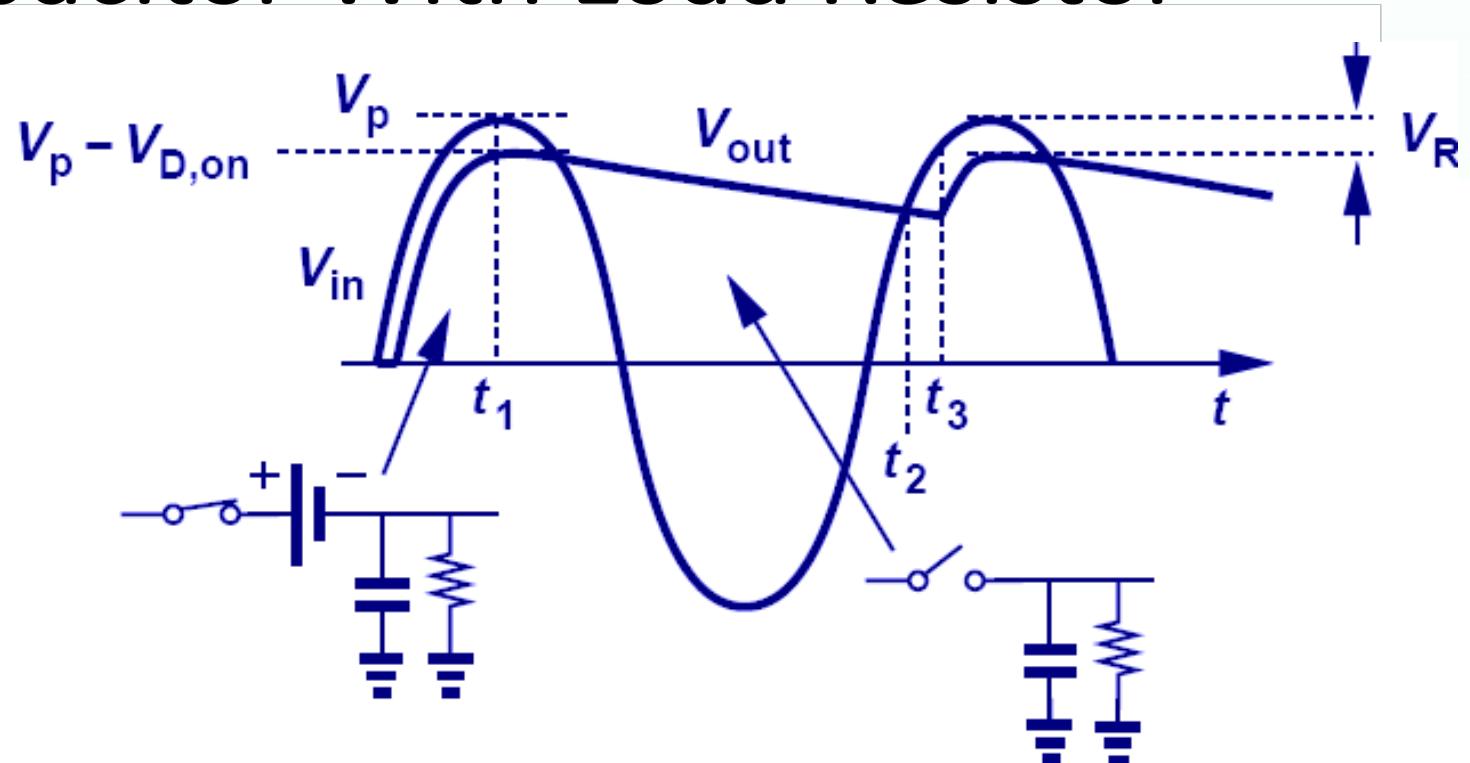
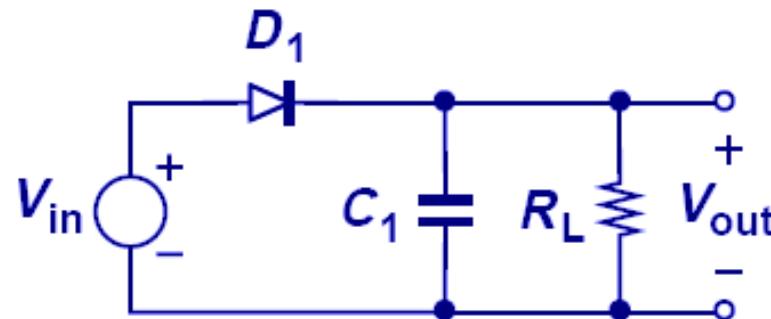


If the resistor in half-wave rectifier is replaced by a capacitor, a fixed voltage output is obtained since the capacitor (assumed ideal) has no path to discharge.



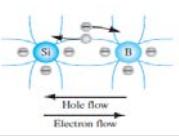


# Diode-Capacitor With Load Resistor

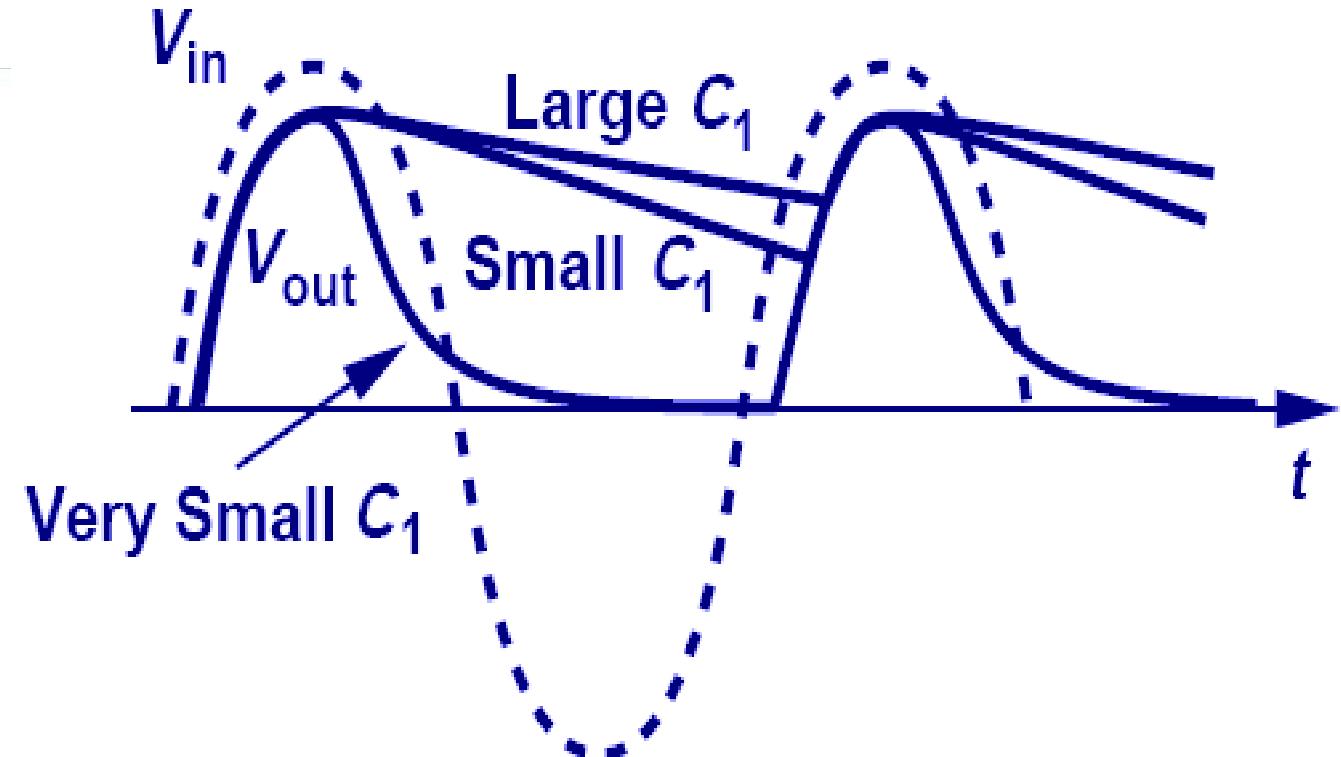
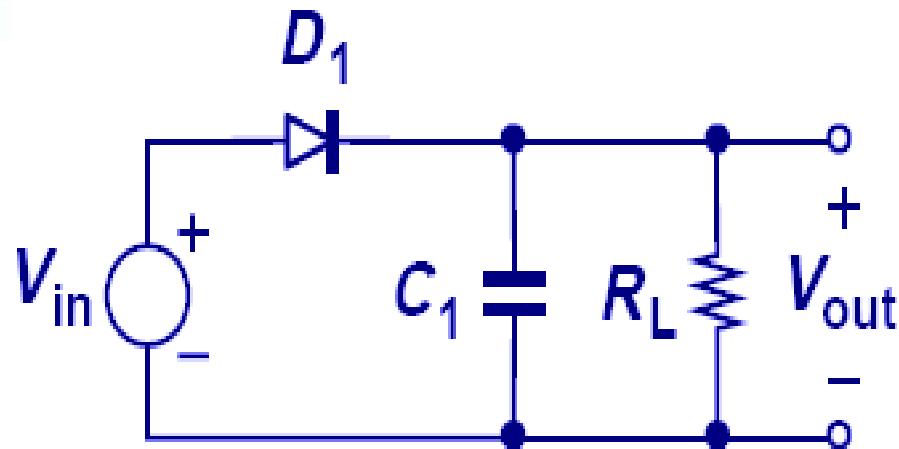


A path is available for capacitor to discharge.  
Therefore,  $V_{out}$  will not be constant and a ripple exists.



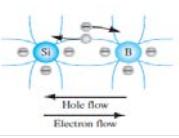


# Behavior for Different Capacitor Values



For large  $C_1$ ,  $V_{out}$  has small ripple.





# Peak to Peak Amplitude of Ripple

$$V_{out}(t) = (V_p - V_{D,on}) \exp \frac{-t}{R_L C_1} \quad 0 \leq t \leq T_{in}$$

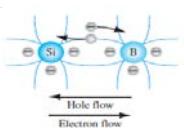
$$V_{out}(t) \approx (V_p - V_{D,on}) \left(1 - \frac{t}{R_L C_1}\right) \approx (V_p - V_{D,on}) - \frac{V_p - V_{D,on}}{R_L} \frac{t}{C_1}$$

$$V_R \approx \frac{V_p - V_{D,on}}{R_L} \cdot \frac{T_{in}}{C_1} \approx \frac{V_p - V_{D,on}}{R_L C_1 f_{in}}$$

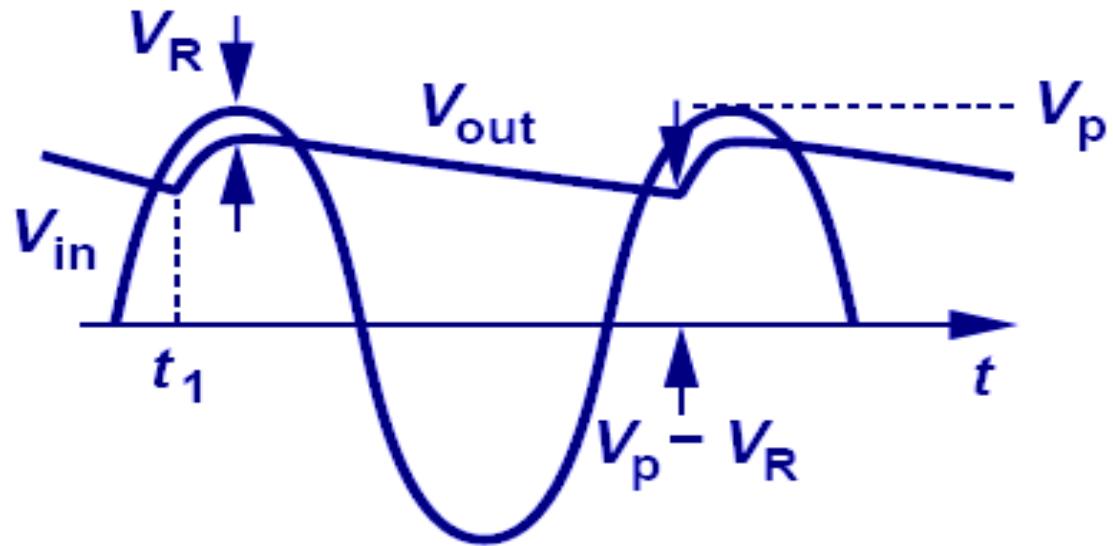
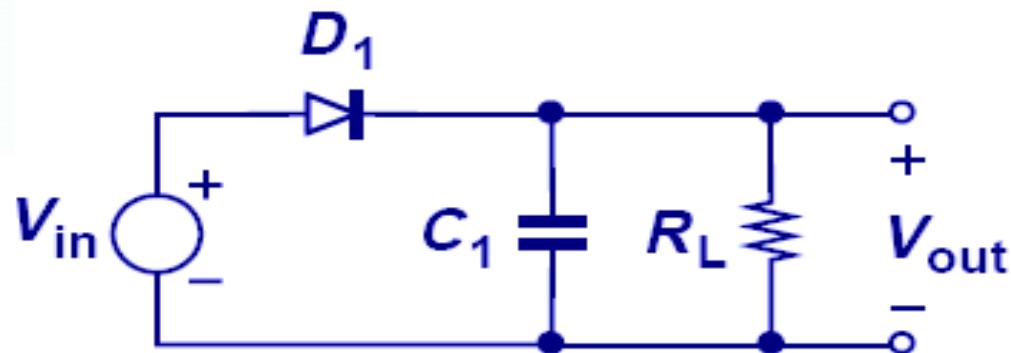
The ripple amplitude is the decaying part of the exponential.

Ripple voltage becomes a problem if it goes above 5 to 10% of the output voltage.





# Maximum Diode Current

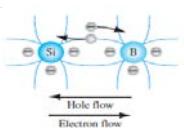


$$I_p \approx C_1 \omega_{in} V_p \sqrt{\frac{2V_R}{V_p}} + \frac{V_p}{R_L} \approx \frac{V_p}{R_L} (R_L C_1 \omega_{in} \sqrt{\frac{2V_R}{V_p}} + 1)$$

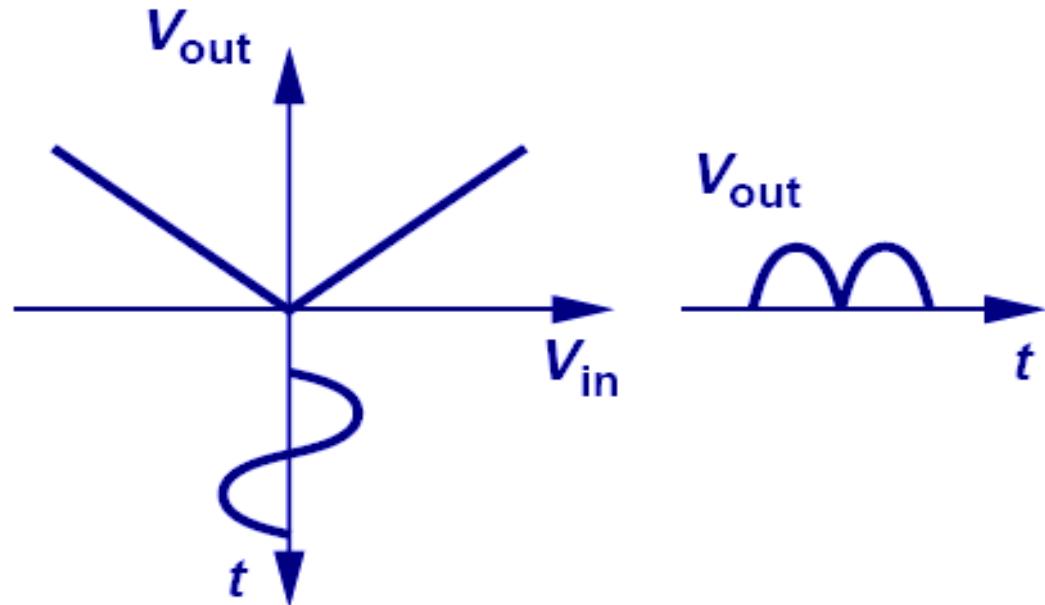
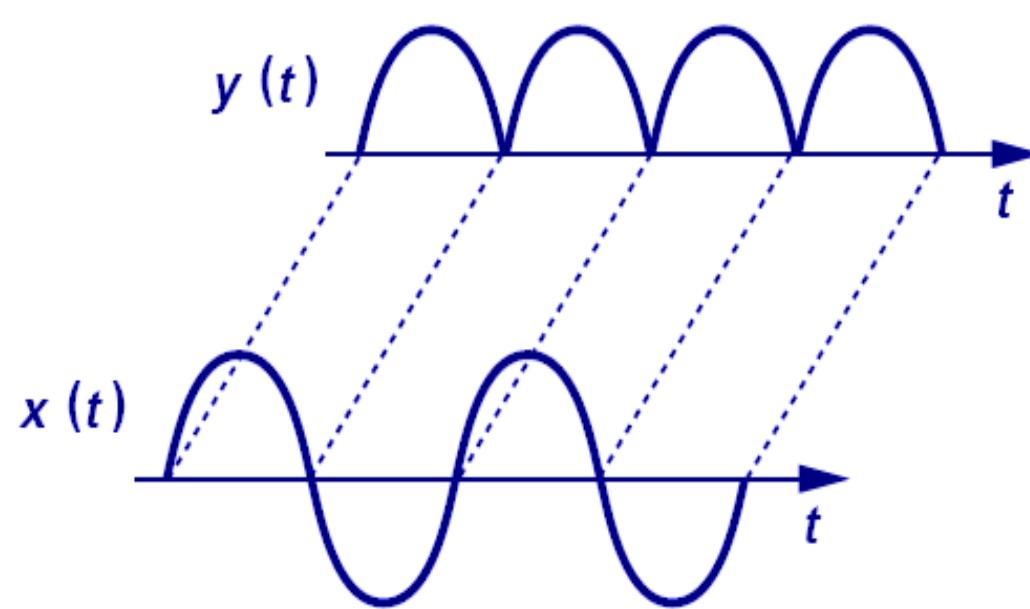
The diode has its maximum current at  $t_1$ , since that's when the slope of  $V_{out}$  is the greatest.

This current has to be carefully controlled so it does not damage the device.





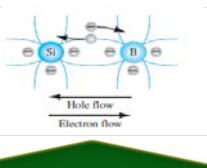
# Full-Wave Rectifier



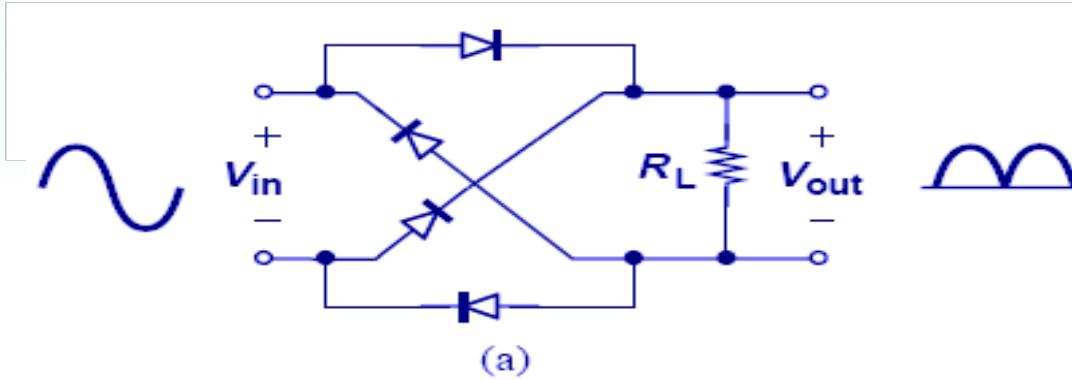
A full-wave rectifier passes both the negative and positive half cycles of the input, while inverting the negative half of the input.

A full-wave rectifier reduces the ripple by a factor of two.

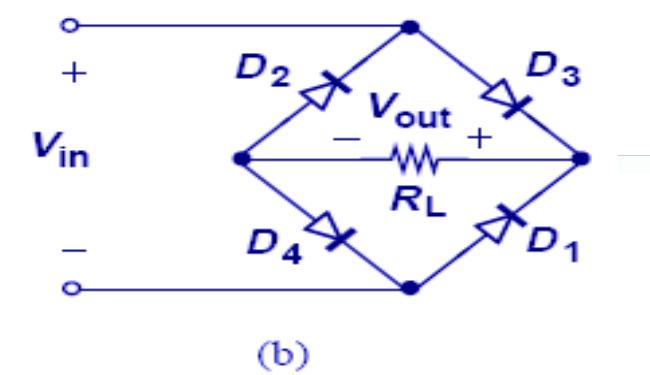




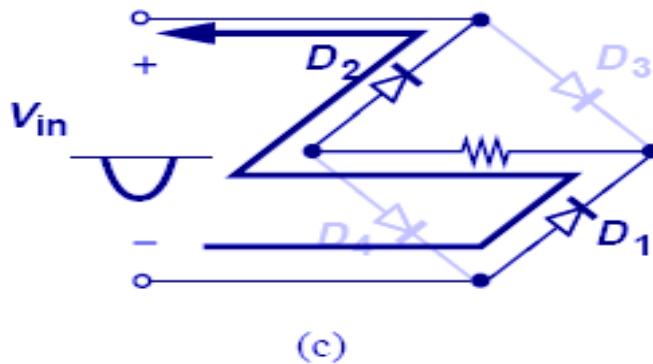
# Full-Wave Rectifier: Bridge Rectifier



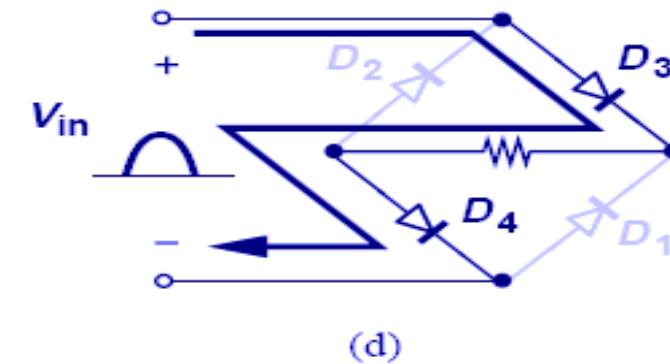
(a)



(b)



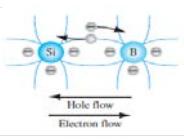
(c)



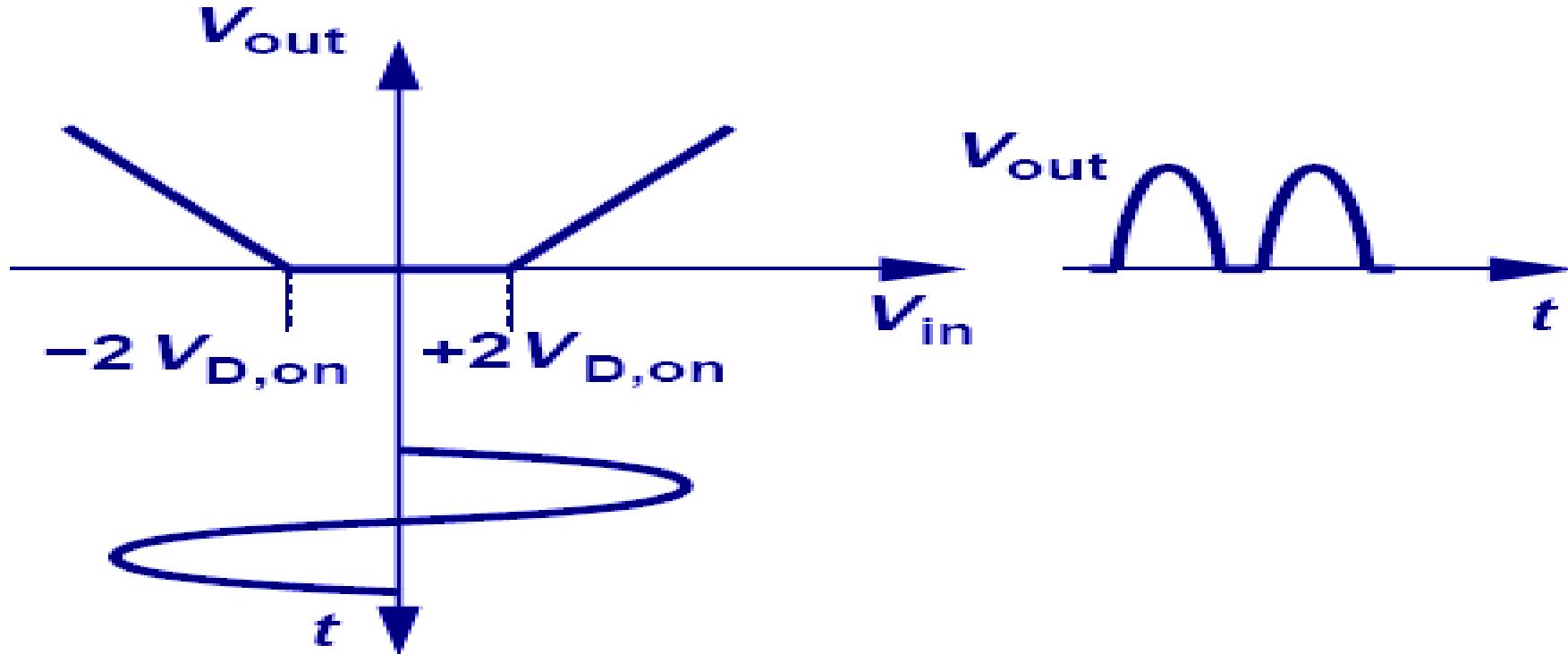
(d)

The figure above shows a full-wave rectifier, where  $D_1$  and  $D_2$  pass/invert the negative half cycle of input and  $D_3$  and  $D_4$  pass the positive half cycle.



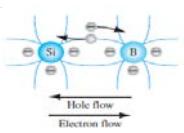


# Input/Output Characteristics of a Full-Wave Rectifier (Constant-Voltage Model)

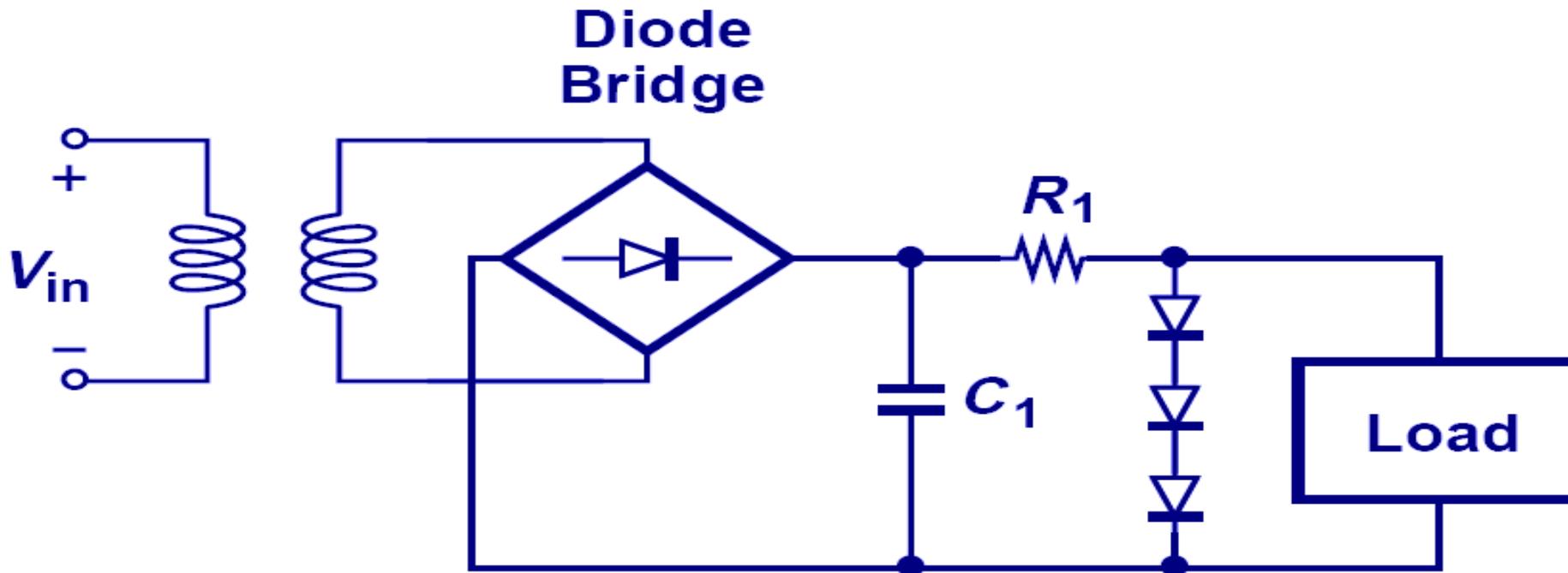


The dead-zone around  $V_{in}$  arises because  $V_{in}$  must exceed  $2 V_{D,ON}$  to turn on the bridge.



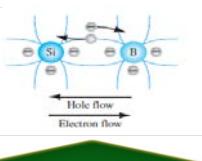


# Voltage Regulator

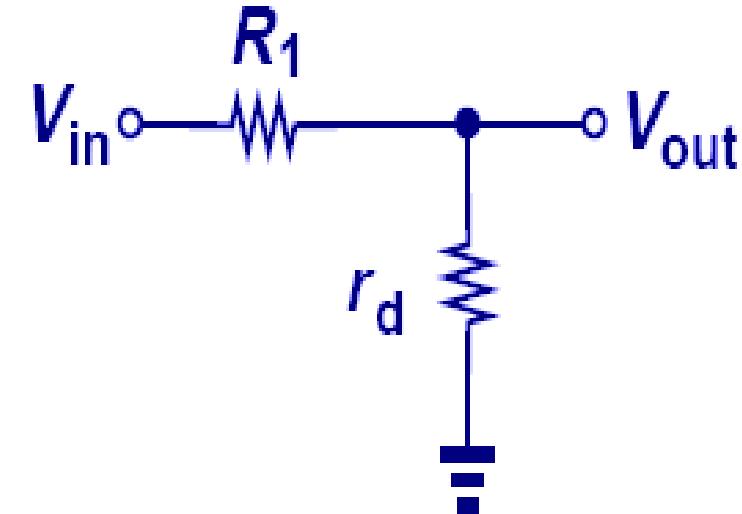
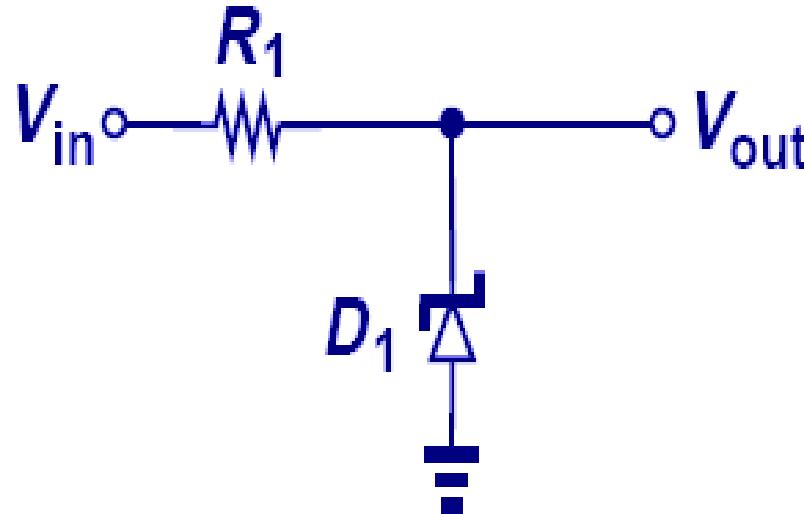


The ripple created by the rectifier can be unacceptable to sensitive load; therefore, a regulator is required to obtain a very stable output. Three diodes operate as a primitive regulator.





# Voltage Regulation With Zener Diode

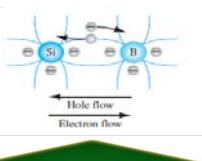


Voltage regulation can be accomplished with Zener diode.

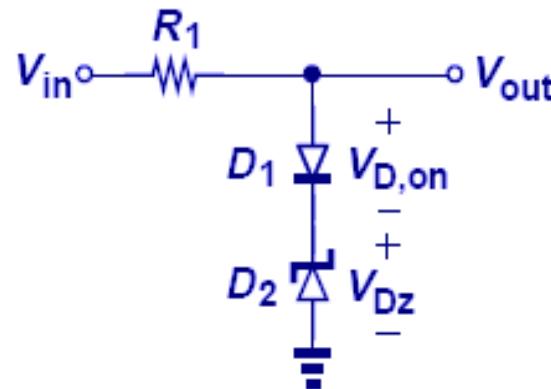
$$V_{out} = \frac{r_D}{r_D + R_1} V_{in}$$

Since  $r_d$  is small, large change in the input will not be reflected at the output.

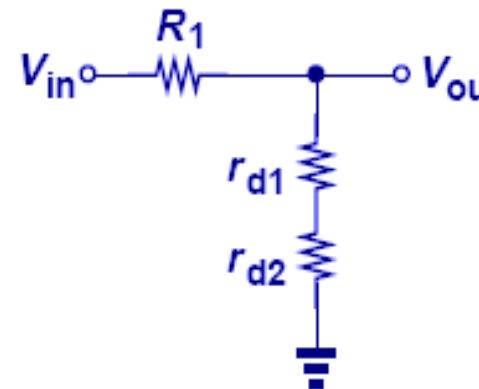




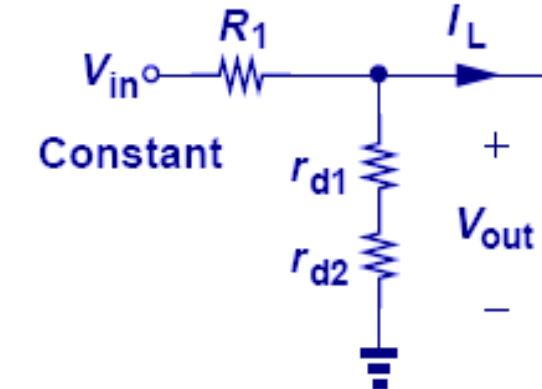
# Line Regulation VS. Load Regulation



(a)



(b)



(c)

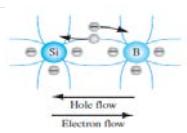
$$\frac{V_{out}}{V_{in}} = \frac{r_{d1} + r_{d2}}{r_{d1} + r_{d2} + R_1}$$

$$\left| \frac{V_{out}}{I_L} \right| = (r_{d1} + r_{d2}) \parallel R_1$$

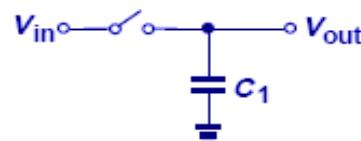
Line regulation is the suppression of change in  $V_{out}$  due to change in  $V_{in}$  (b).

Load regulation is the suppression of change in  $V_{out}$  due to change in load current (c).

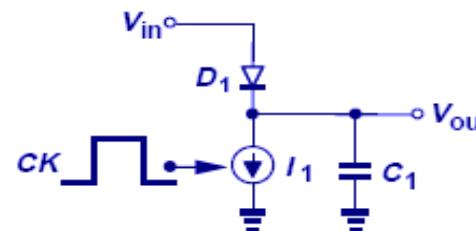




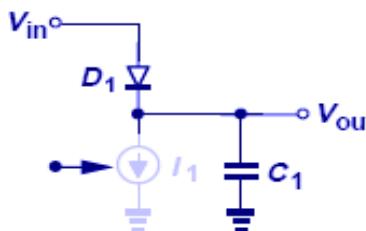
# Diode as Electronic Switch



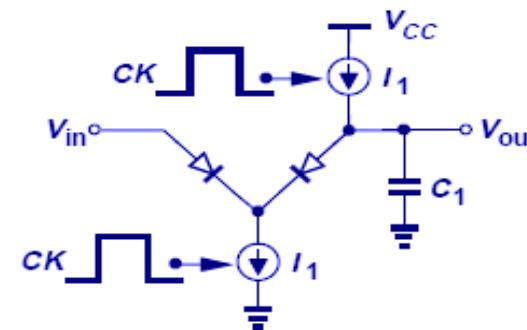
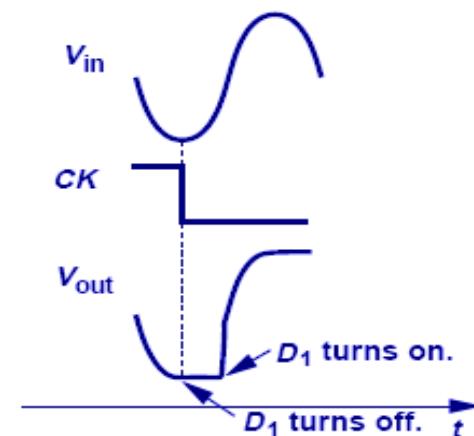
(a)



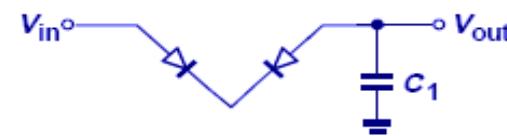
(b)



(c)



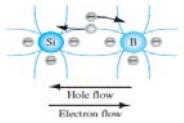
(d)



(e)

Diode as a switch finds application in logic circuits and data converters.





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# Thank You Very Much

Dipl.-Ing. B. Kommey

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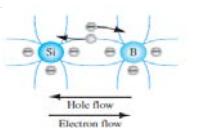
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

Tel.: 050 770 32 86

whatsup: 0049 172 4444 765

Skype\_id: calculus.affairs





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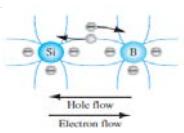
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**“A person starts to live when he  
can live outside himself”**

**Albert Einstein**





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# Overview

## Bipolar Transistors

BJT

Bipolar  
Transistor  
Basics

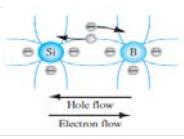
Voltage  
Controlled Device  
as Amplifying  
Element

Structure of  
a Bipolar  
Transistor

Operation  
of a Bipolar  
Transistor

Signal  
Models





# SEMICONDUCTOR DEVICES

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# Overview

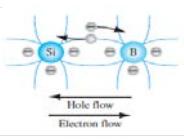
## Bipolar Transistor Basics

**Kirchhoff  
Voltage/  
Current Laws**

**Characteristics  
Curves**

**Ebers-Moll  
Model**





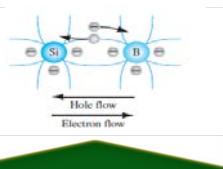
# Overview

## Signal Models

Large-Signal

Small-Signal





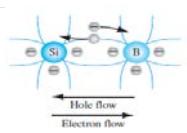
# Bipolar Transistors

A bipolar junction transistor consists of two PN junctions sandwiched very close together within a single crystal of semiconductor

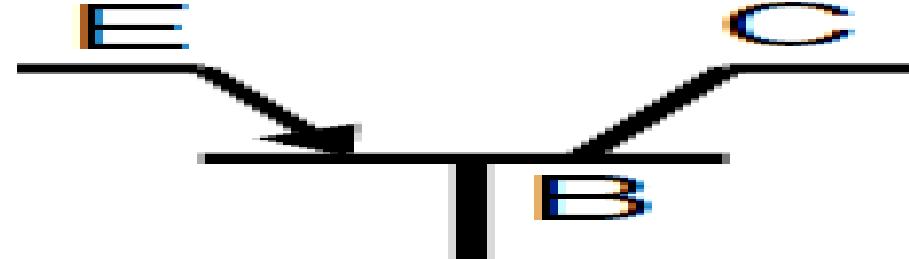
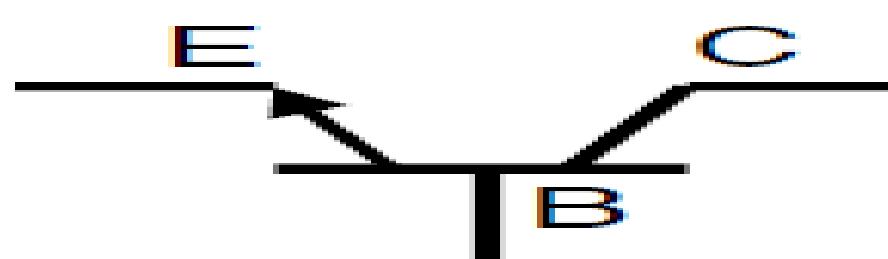
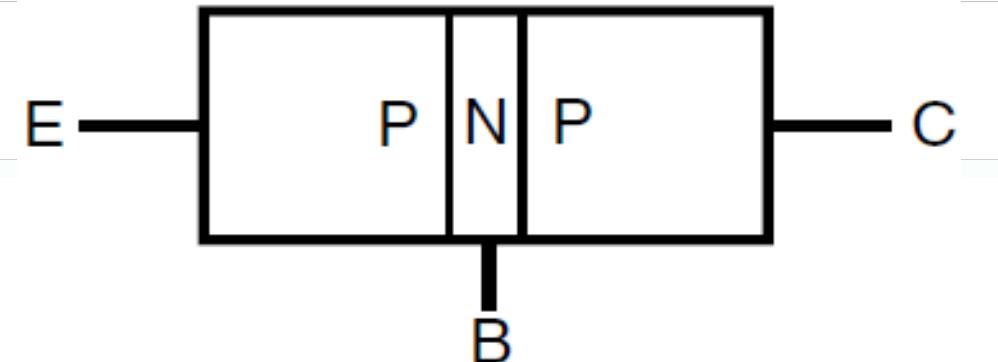
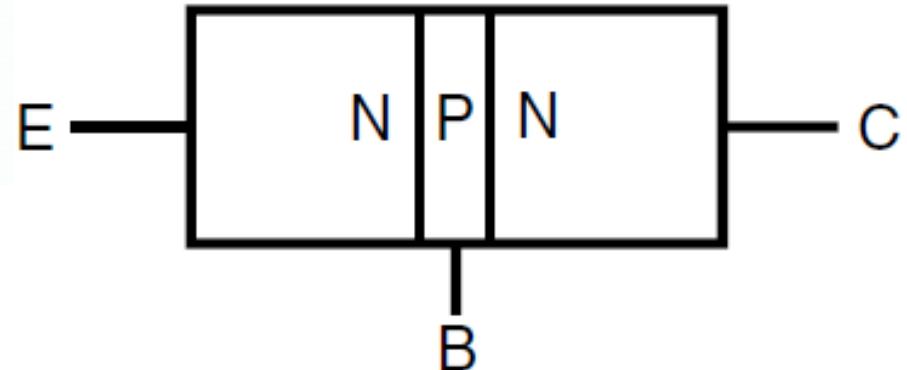
The region common to the two junctions, called the *base*, may be of either N-type or P-type material.

This thin region is surrounded by material of the opposite type, in regions known as the *emitter* and *collector*.





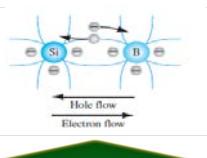
# Bipolar Transistors



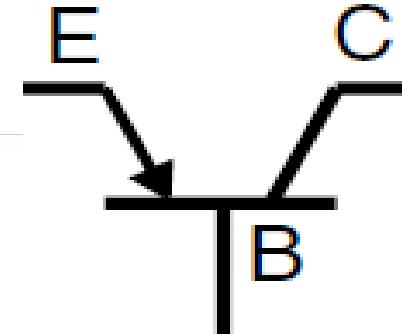
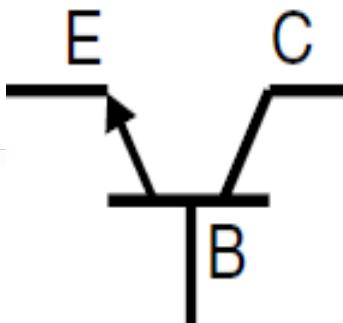
The arrow on the emitter lead points in the direction of positive current flow.

You can tell whether a transistor in a schematic diagram is PNP or NPN by the direction of the arrow





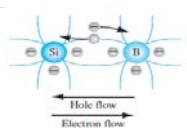
# Bipolar Transistors



A small current flowing *out* from the base controls a large current flowing *out* from the collector, with both currents flowing *in* through the emitter.

The ratio of collector current to base current is called  $\beta$  (or  $h_{FE}$ ) (range 20 to 300)





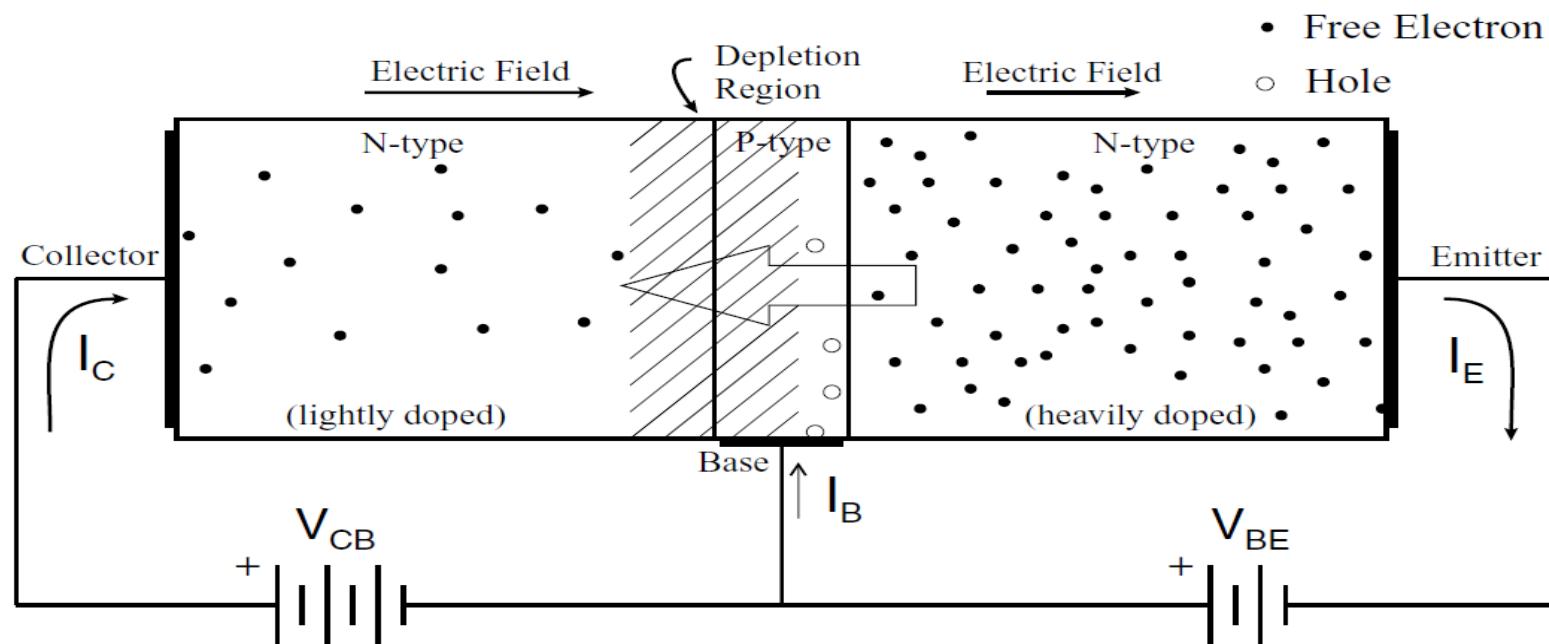
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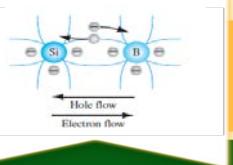
# Bipolar Transistors



$$\beta = hfe = \frac{I_c}{I_b}$$

A transistor is a voltage-controlled current source:  
small changes in the base voltage cause large  
changes in collector current.





# Bipolar Transistors

$V_{BE} \equiv V_B - V_E$  = potential of base relative to emitter,

$V_{CB} \equiv V_C - V_B$  = potential of collector relative to base

$V_{CE} \equiv V_C - V_E$  = potential of collector relative to emitter,

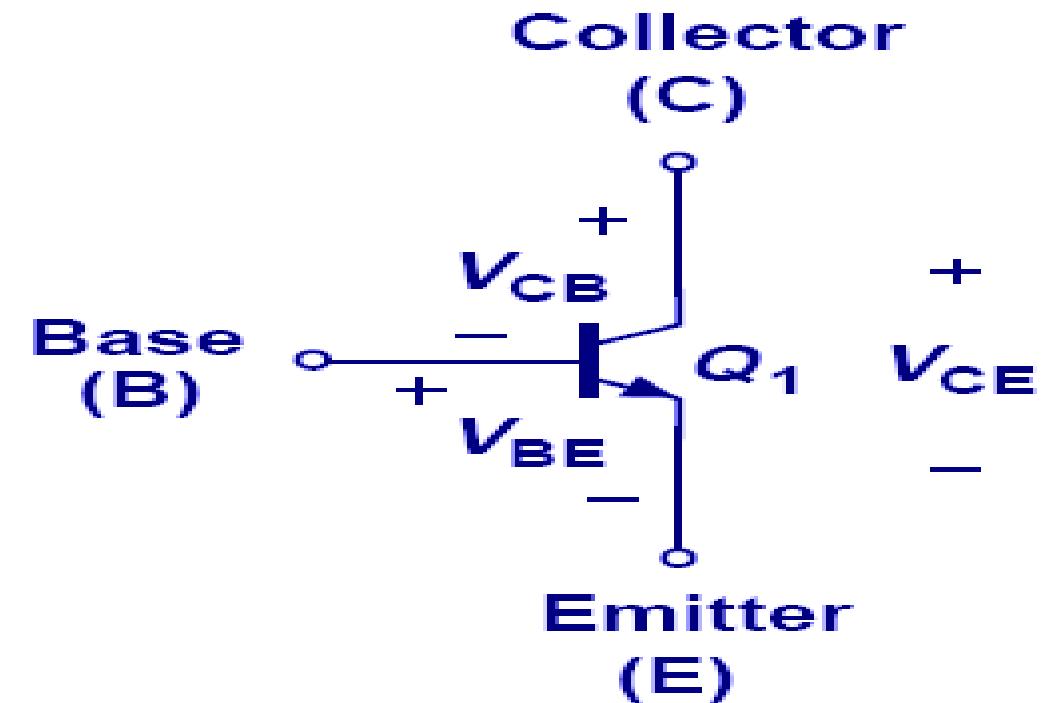
**Kirchhoff's voltage law:**  $V_{CE} = V_{BE} + V_{CB}$ .

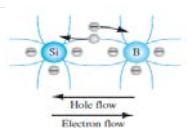
$I_C$  = current flowing into collector,

$I_E$  = current flowing out of emitter,

$I_B$  = current flowing into base,

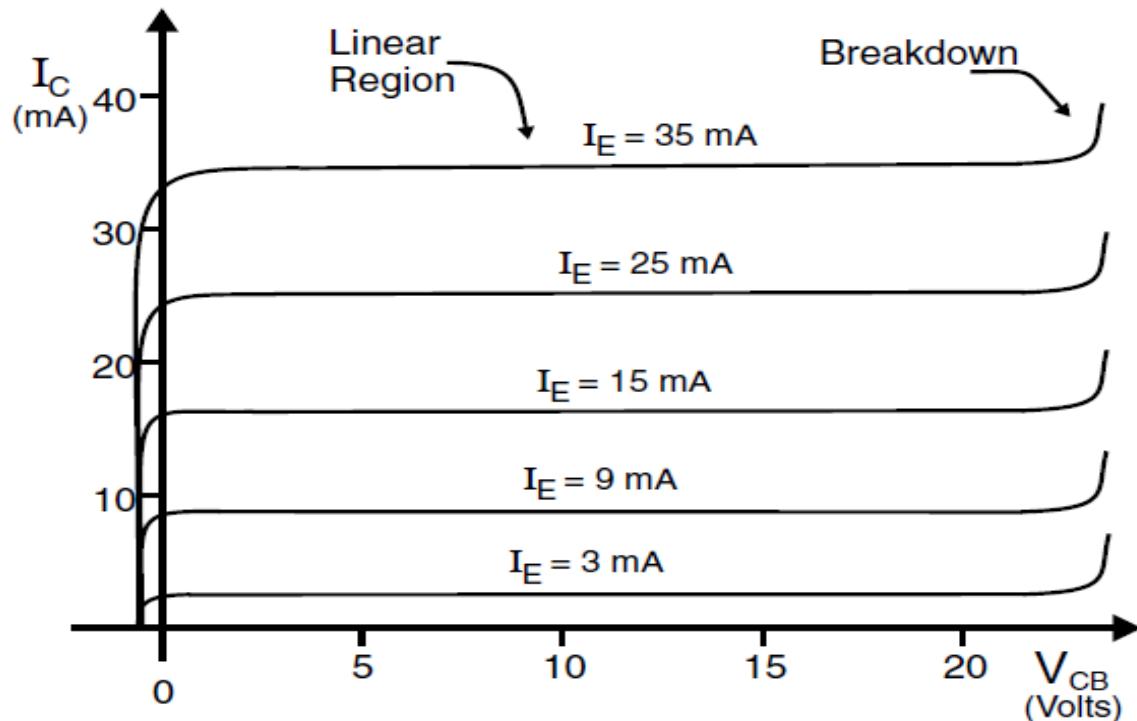
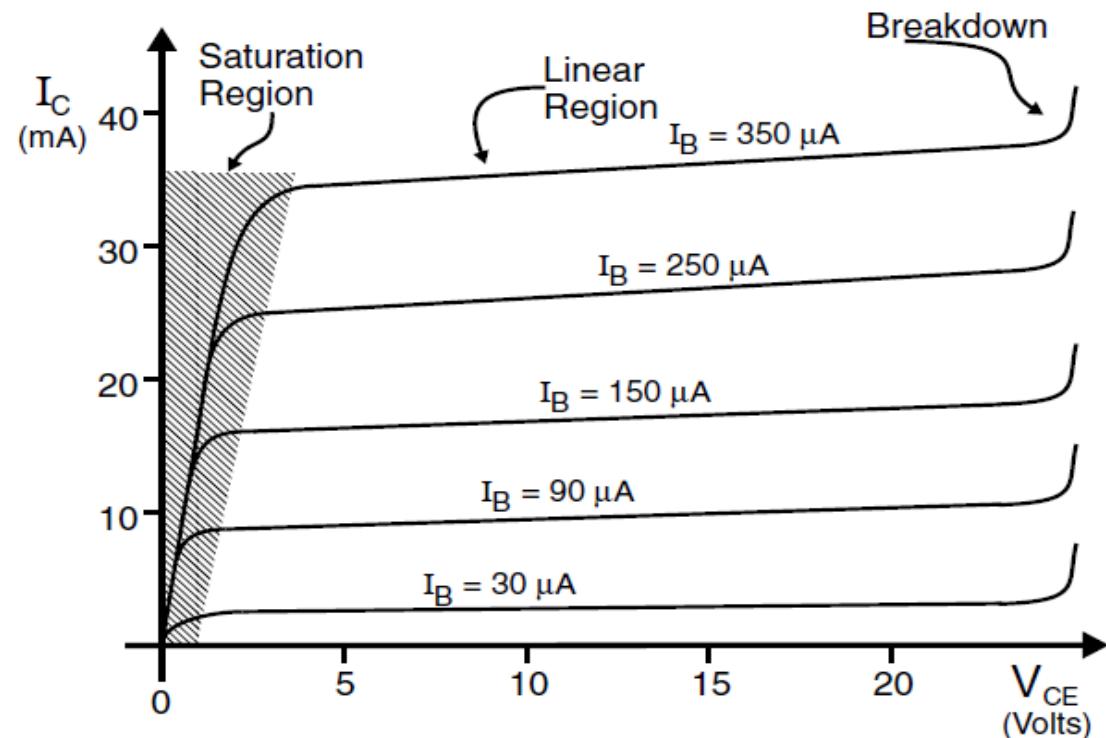
**Kirchhoff's current law:**  $I_E = I_C + I_B$ .





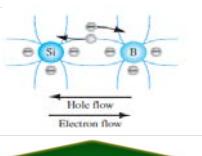
# Bipolar Transistors

The relationships between these voltages and currents are usually expressed in terms of characteristic curves



Characteristic curves for an npn bipolar transistor

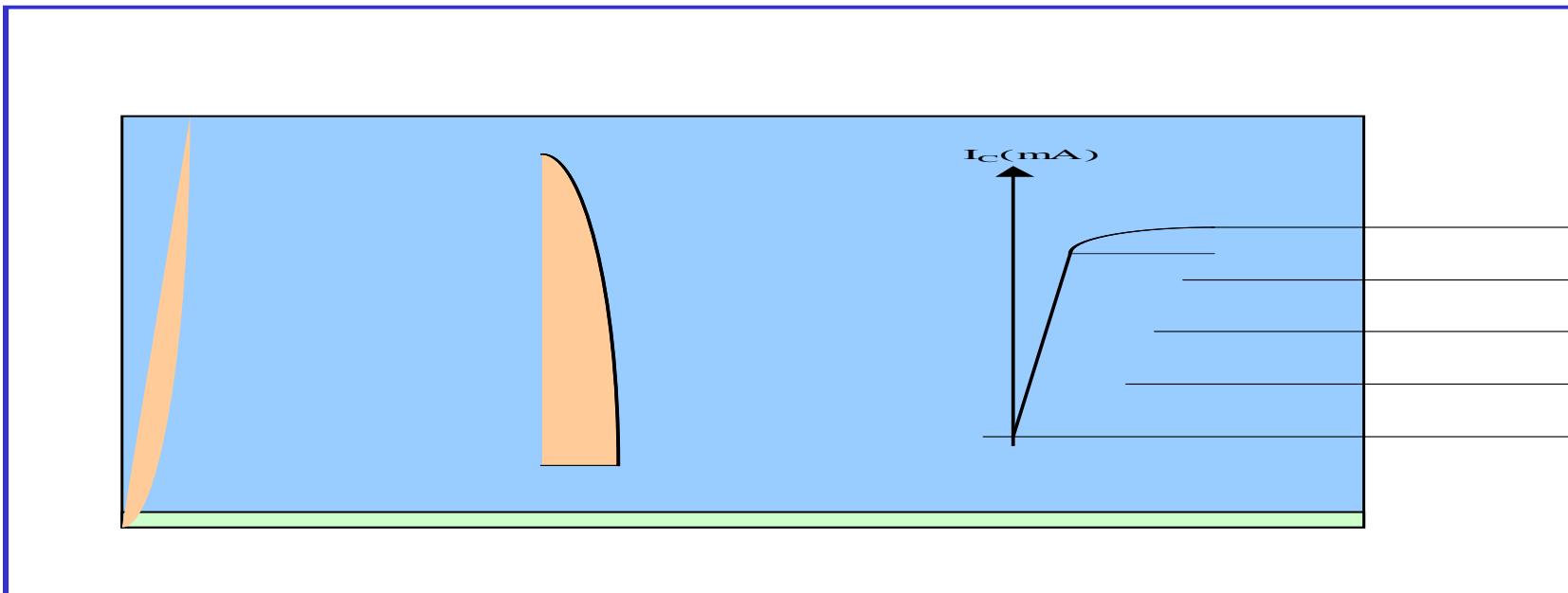


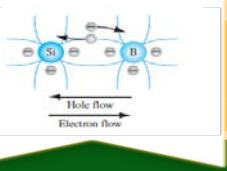


# Regions (Modes) of Operation of BJT

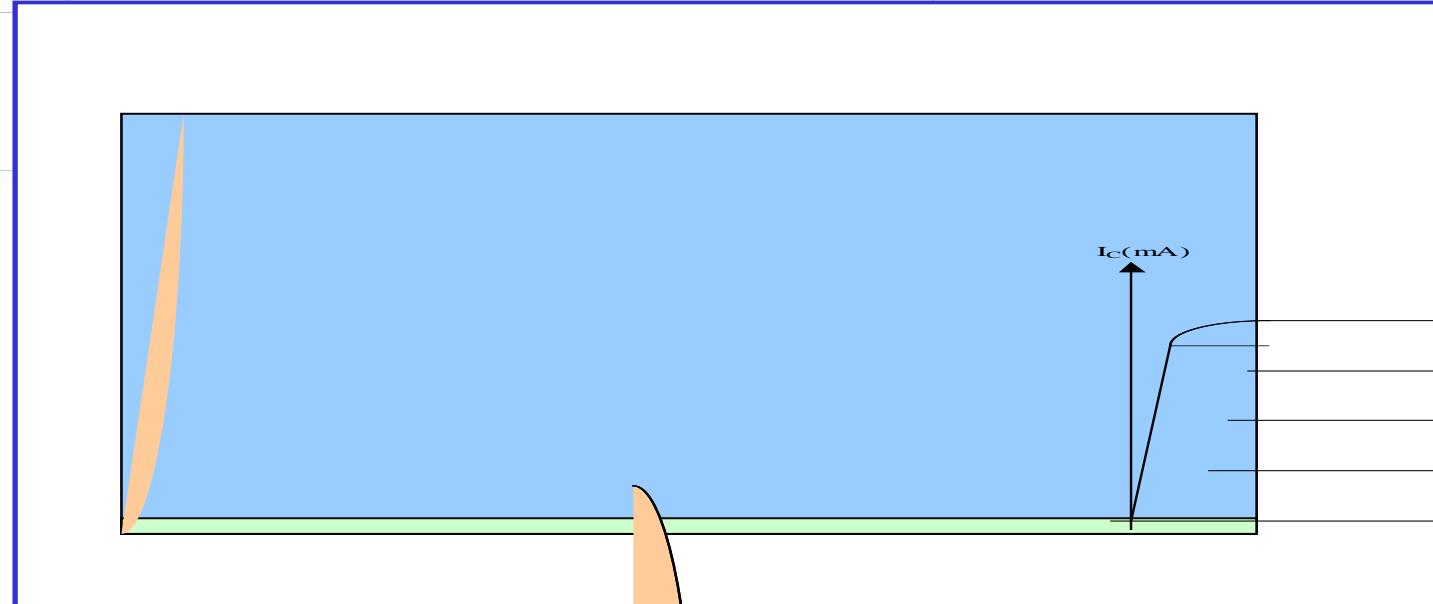
Active:

- Most important mode of operation
- Central to amplifier operation
- The region where current curves are practically flat





# Regions (Modes) of Operation of BJT



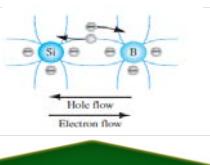
## Saturation:

- Barrier potential of the junctions cancel each other out causing a virtual short (behaves as on state Switch)

## Cutoff:

- Current reduced to zero
- Ideal transistor behaves like an open switch





# Ebers-Moll Transistor Model



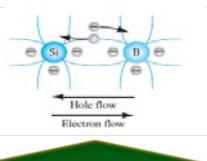
In the Ebers-Moll model, the amount of collector current that flows is determined by the amount of forward-bias that is applied to the base-emitter diode.

$$I_C = I_s (e^{eV_{BE}/kT} - 1)$$

$I_s$  is the reverse saturation current

The base current is related to the collector current by  $I_B = \frac{I_C}{\beta}$ .





## Ebers-Moll Transistor Model

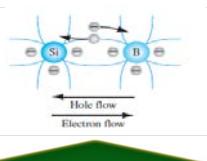
### Dynamic resistance of emitter

The dynamic resistance tells us how, for fixed base voltage, the emitter voltage would change in response to a change in emitter current

– for example, how the emitter voltage would differ if the emitter were driving a small load resistance as opposed to a large one

$$r_e \equiv \frac{\partial V_E}{\partial I_E} = \frac{kT}{e I_C}$$





# Ebers-Moll Transistor Model

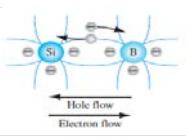


## Dynamic resistance of base

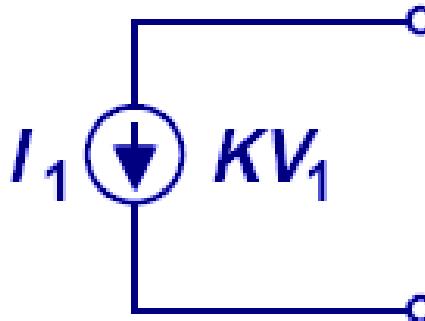
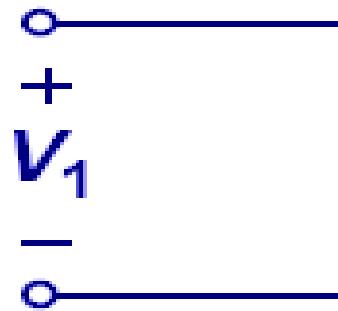
The dynamic resistance of the base tells us how, the base loads the current that is driving it

$$r_{BE} = \frac{\partial V_B}{\partial I_B} = \beta \frac{kT}{eI_c} + \frac{1}{I_c}$$

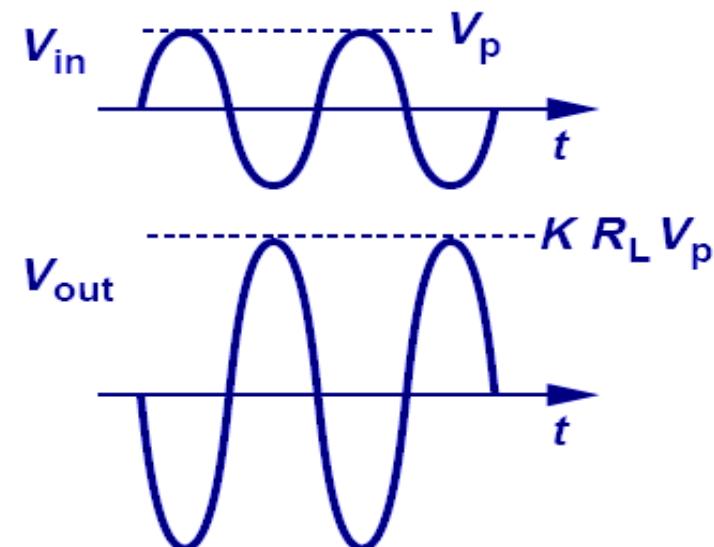
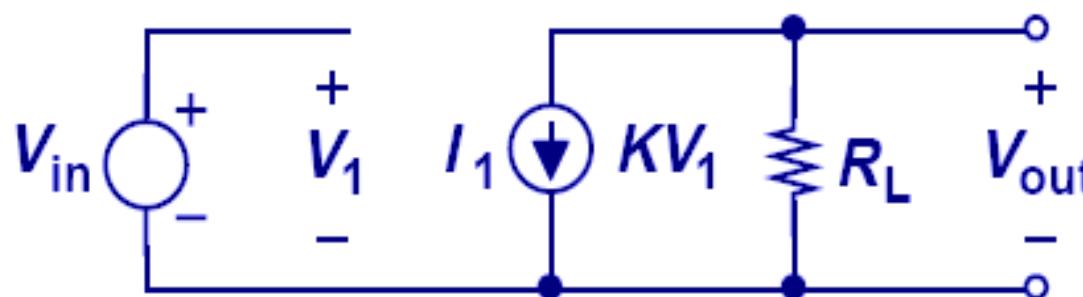




# Voltage-Dependent Current Source



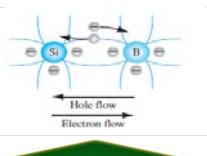
A voltage-dependent current source can act as an amplifier.



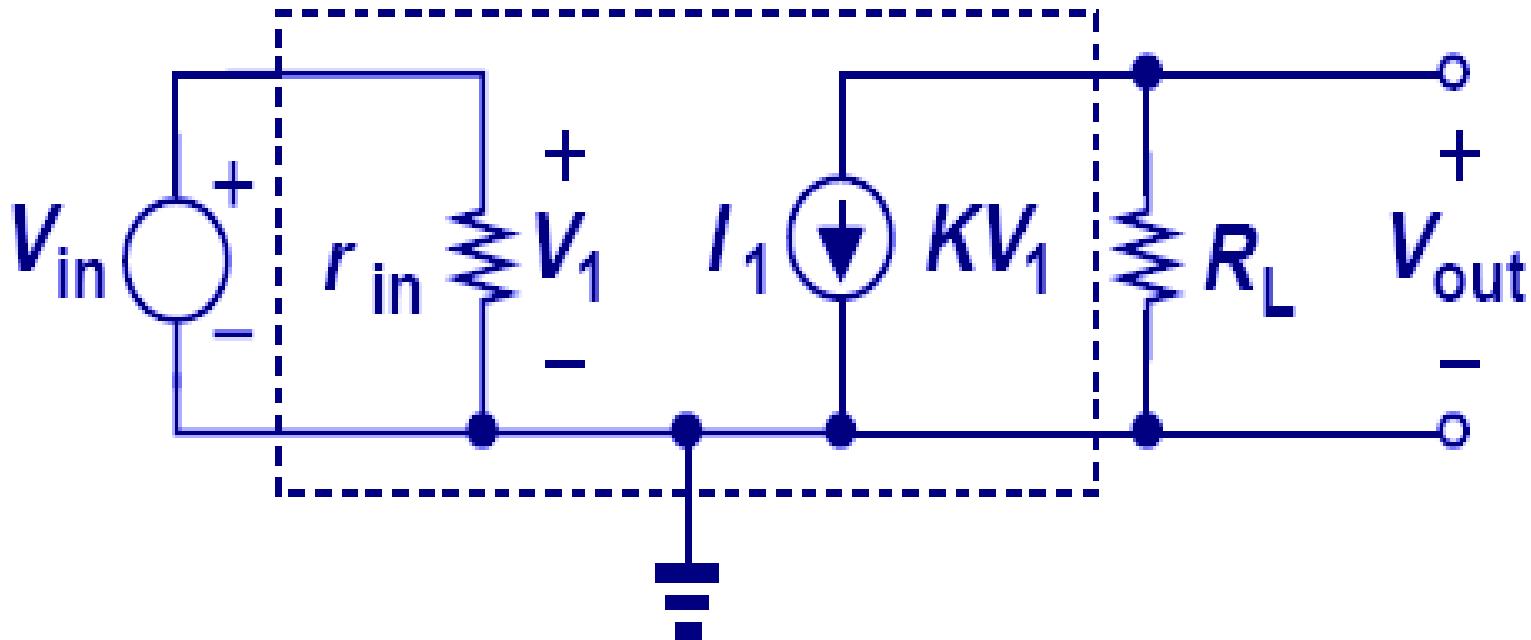
$$A_V = \frac{V_{out}}{V_{in}} = -KR_L$$

If  $KR_L$  is greater than 1, then the signal is amplified.



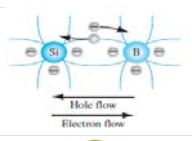


# Voltage-Dependent Current Source with Input Resistance



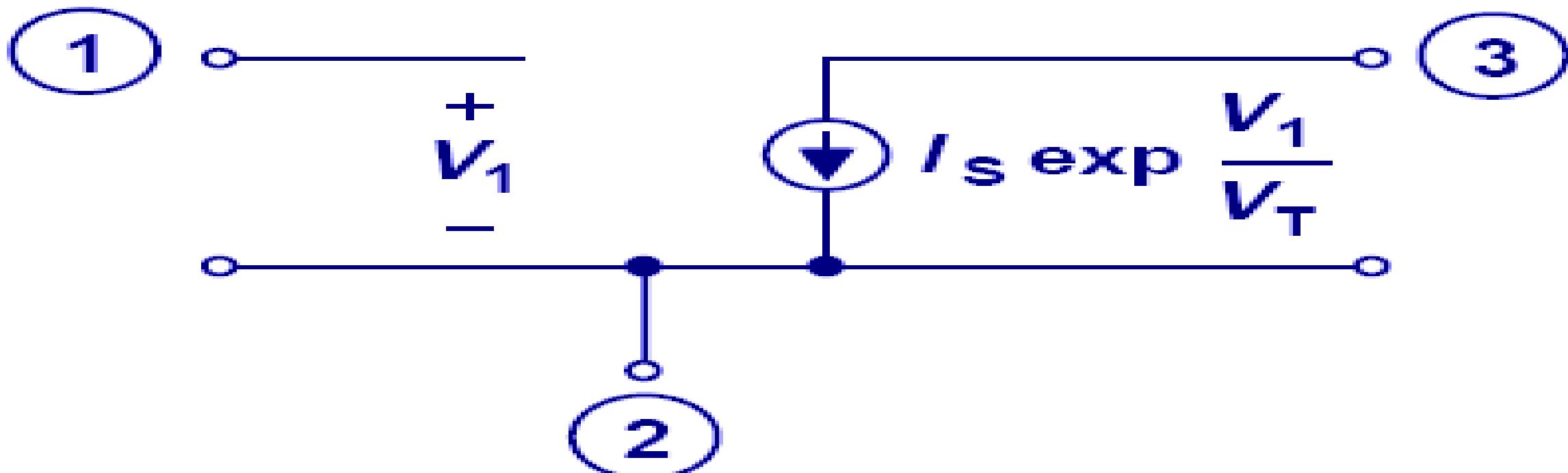
Regardless of the input resistance, the magnitude of amplification remains unchanged.

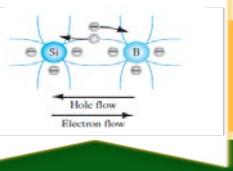




# Exponential Voltage-Dependent Current Source

Ideally, bipolar transistor can be modeled as a three-terminal exponential voltage-dependent current source

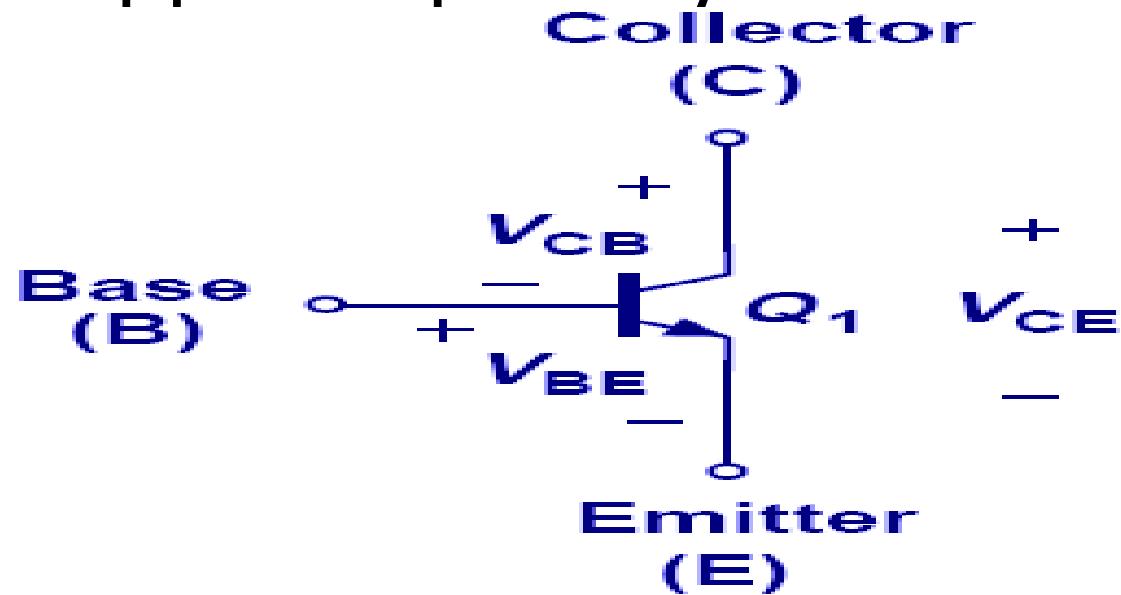
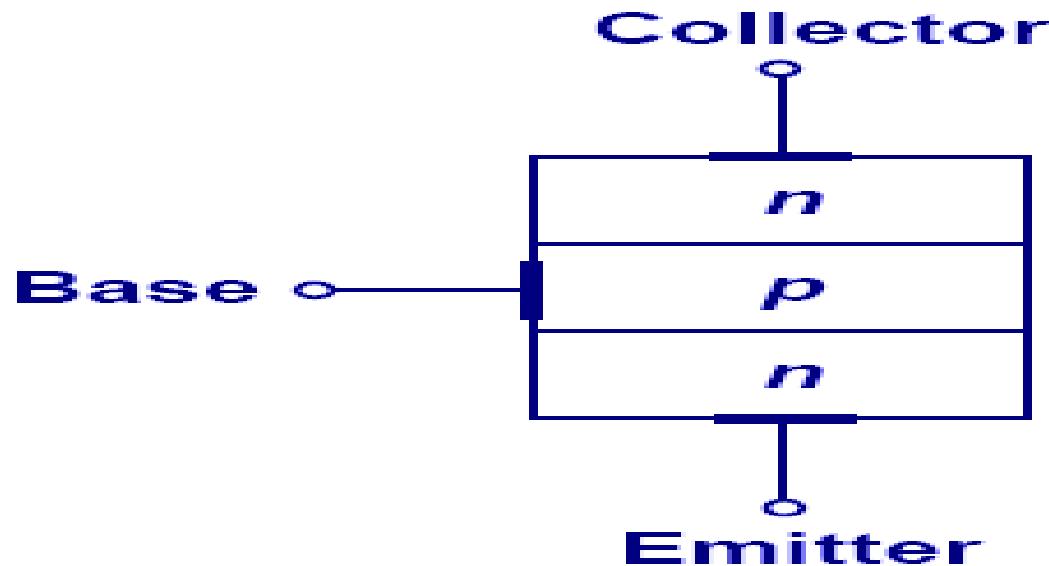


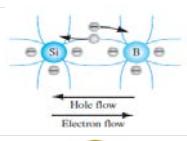


# Structure and Symbol of Bipolar Transistor

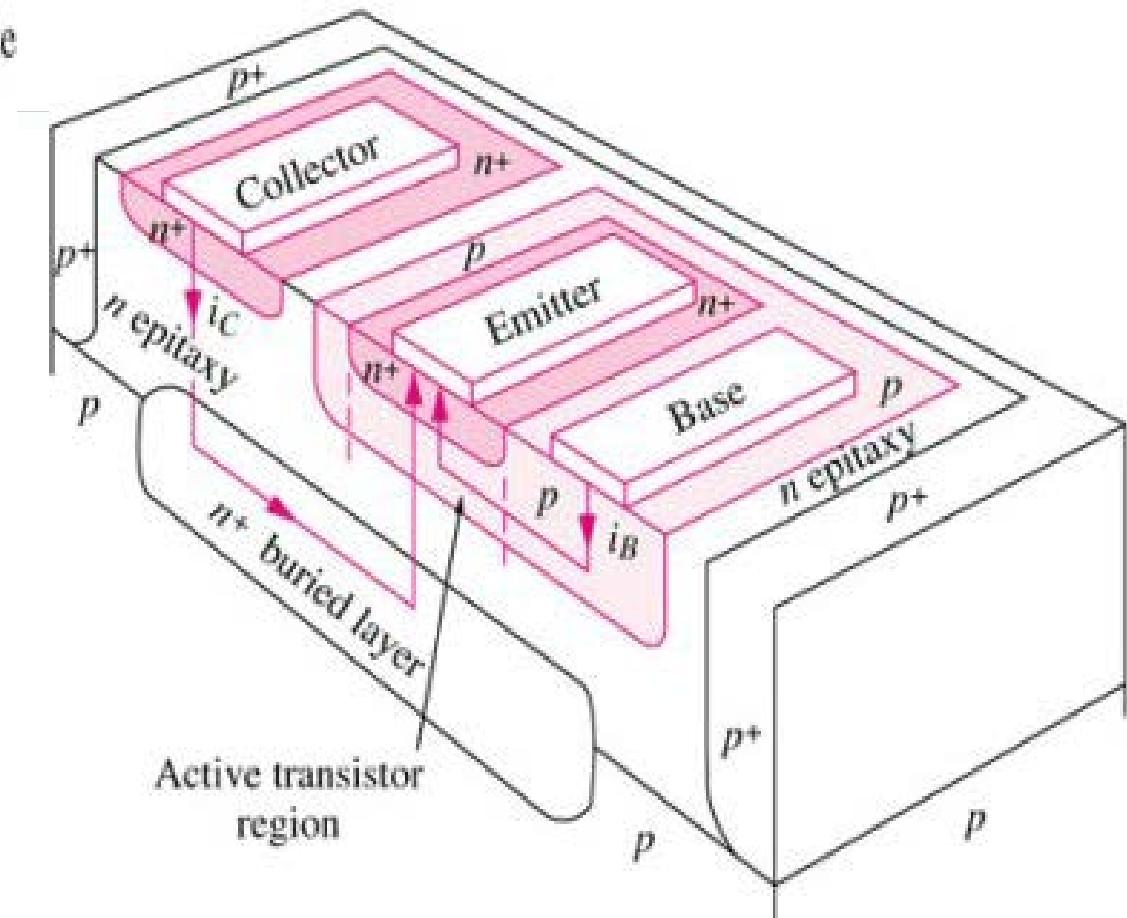
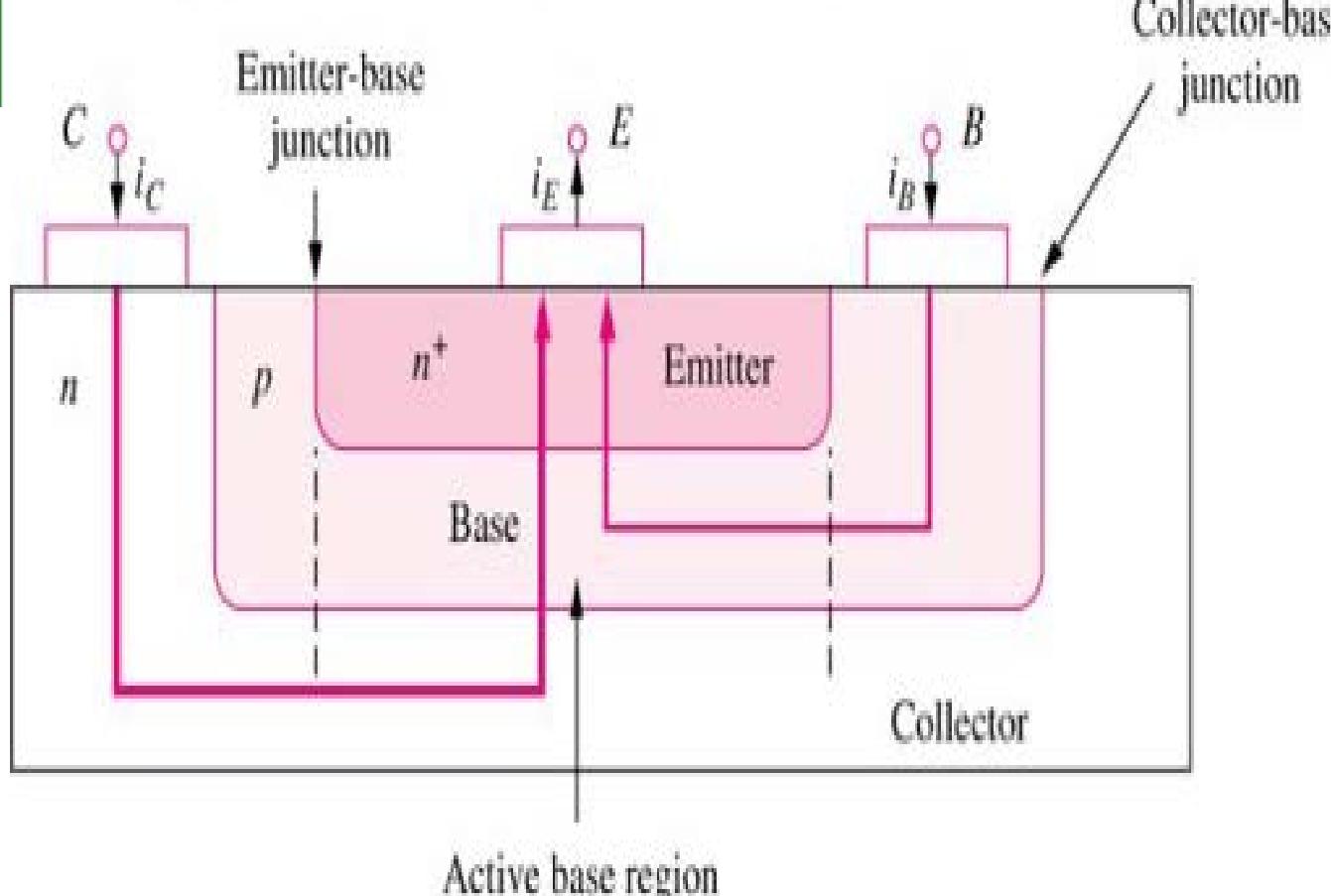
Bipolar transistor can be thought of as a sandwich of three doped Si regions.

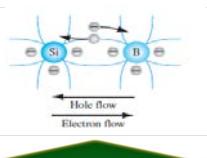
The outer two regions are doped with the same polarity, while the middle region is doped with opposite polarity.





# Structure and Symbol of Bipolar Transistor



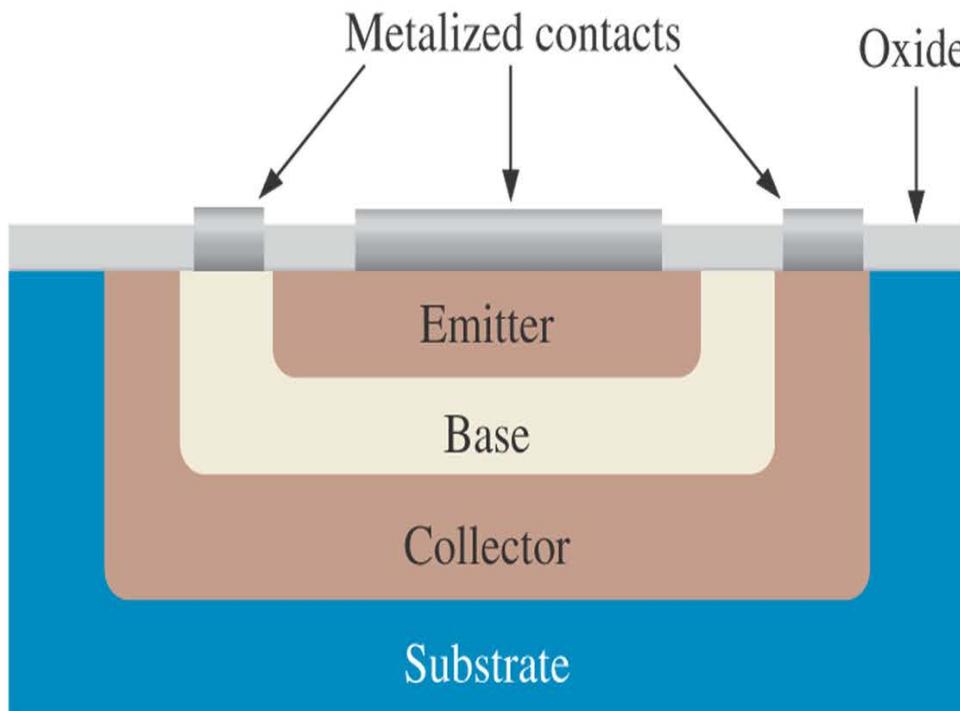


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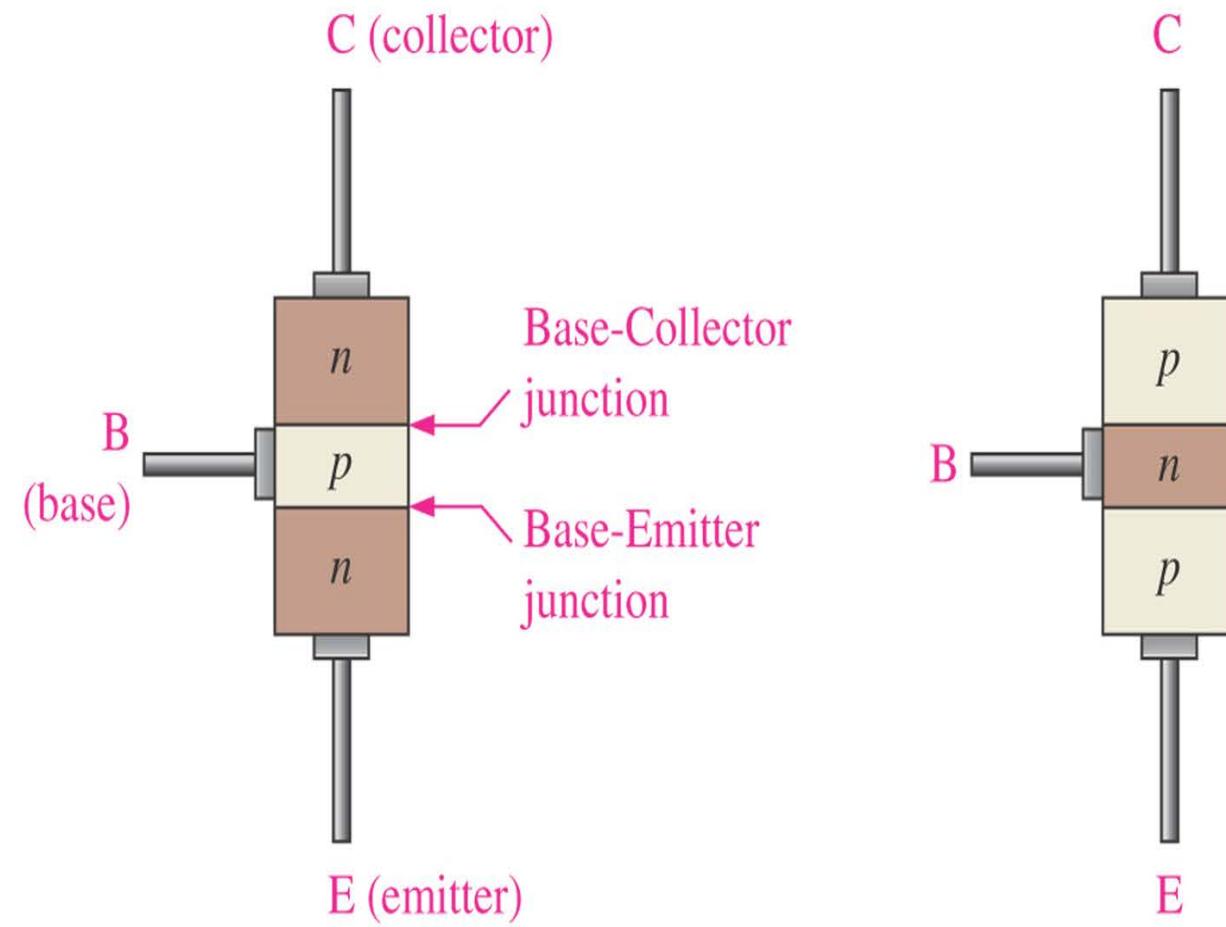
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# Structure and Symbol of Bipolar Transistor



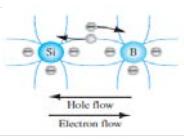
(a) Basic epitaxial planar structure



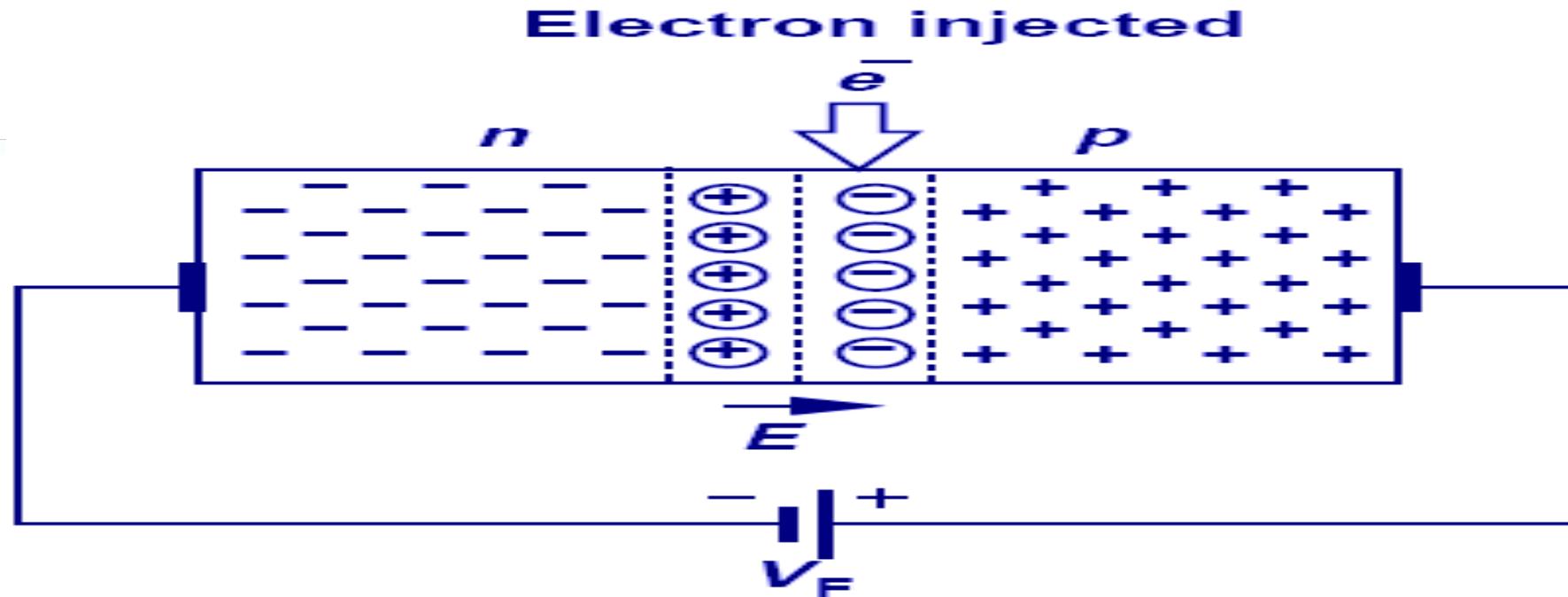
(b) *npn*

(c) *pnp*





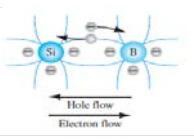
# Injection of Carriers



Reverse biased PN junction creates a large electric field that sweeps any injected minority carriers to their majority region.

This ability proves essential in the proper operation of a bipolar transistor.





# Collector Current

Applying the law of diffusion, we can determine the charge flow across the base region into the collector.

$$I_C = \frac{A_E q D_n n_i^2}{N_E W_B} \left( \exp \frac{V_{BE}}{V_T} - 1 \right)$$

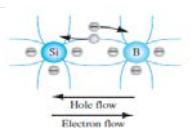
$$I_C = I_s \exp \frac{V_{BE}}{V_T}$$

$$I_s = \frac{A_E q D_n n_i^2}{N_E W_B}$$

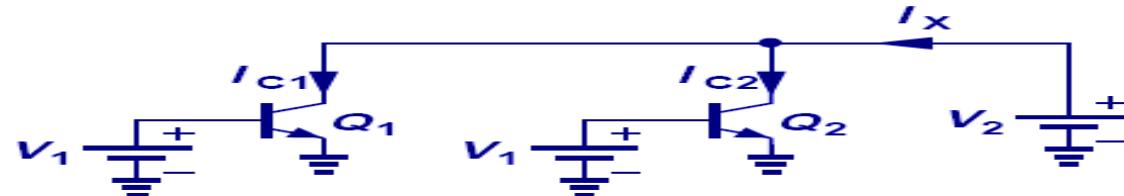
$$V_T = \frac{KT}{q}$$

The equation above shows that the transistor is indeed a voltage-controlled element, thus a good candidate as an amplifier.

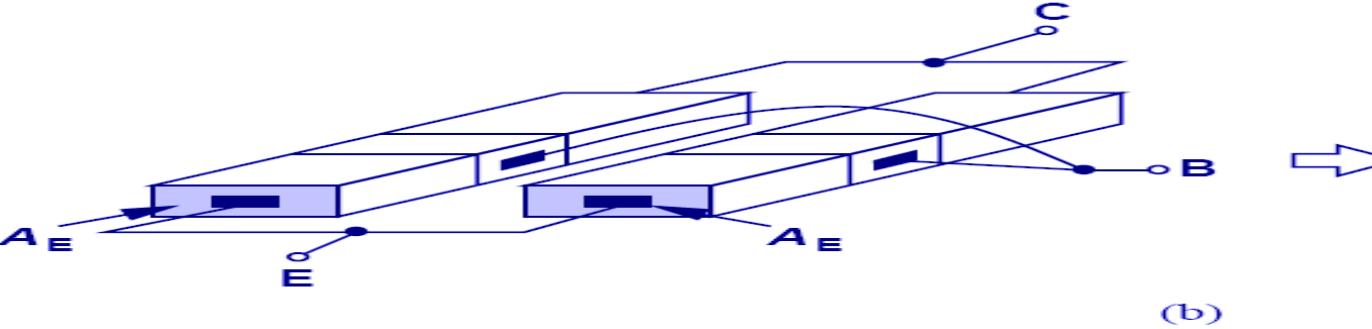
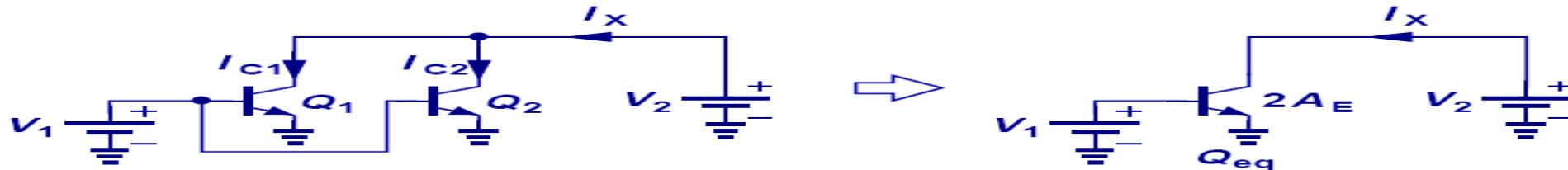




# Parallel Combination of Transistors



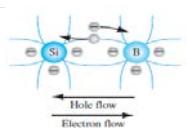
(a)



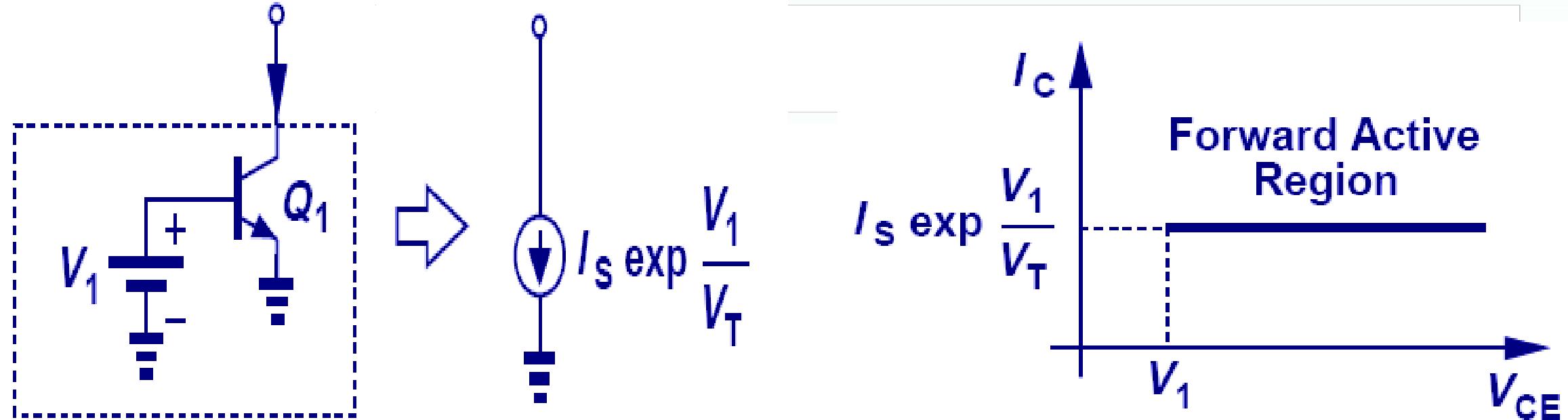
(b)

When two transistors are put in parallel and experience the same potential across all three terminals, they can be thought of as a single transistor with twice the emitter area.





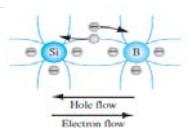
# Constant Current Source



Ideally, the collector current does not depend on the collector to emitter voltage.

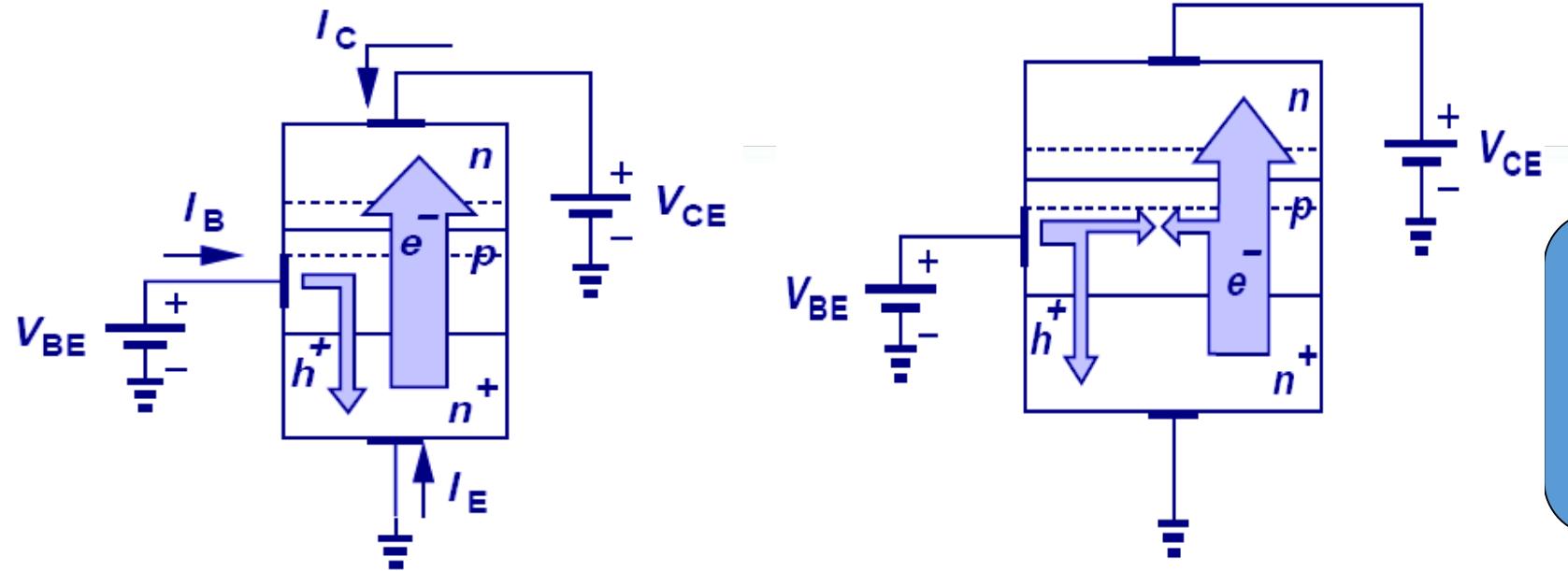
This property allows the transistor to behave as a constant current source when its base-emitter voltage is fixed.





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# Base Current

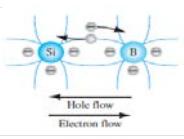


$$I_C = \beta I_B$$

Base current consists of two components:

- 1) Reverse injection of holes into the emitter and
- 2) recombination of holes with electrons coming from the emitter.





# Emitter Current

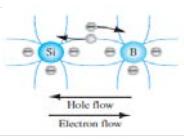
$$I_E = I_C + I_B$$

$$I_E = I_C \left( 1 + \frac{1}{\beta} \right)$$

$$\beta = \frac{I_C}{I_B}$$

Applying Kirchhoff's current law to the transistor, we can easily find the emitter current.





# DC $\beta$ and DC $\alpha$

$\beta$  = Common-emitter current gain

$\alpha$  = Common-base current gain

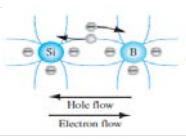
$$\beta = \frac{I_c}{I_B} \qquad \alpha = \frac{I_c}{I_E}$$

The relationships between the two parameters are:

$$\alpha = \frac{\beta}{\beta+1} \qquad \beta = \frac{\alpha}{1-\alpha}$$

Note:  $\alpha$  and  $\beta$  are sometimes referred to as  $\alpha_{dc}$  and  $\beta_{dc}$  because the relationships being dealt with in the BJT are DC.





# Summary of Currents

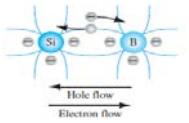
$$I_C = I_s \exp \frac{V_{BE}}{V_T}$$

$$I_B = \frac{1}{\beta} I_s \exp \frac{V_{BE}}{V_T}$$

$$I_E = \frac{\beta + 1}{\beta} I_s \exp \frac{V_{BE}}{V_T}$$

$$\frac{\beta}{\beta + 1} = \alpha$$





# Three Possible Configurations of BJT

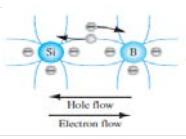
Biasing the transistor refers to applying voltages to the transistor to achieve certain operating conditions.

1. Common-Base Configuration (CB) : input =  $V_{EB}$  &  $I_E$   
output =  $V_{CB}$  &  $I_C$

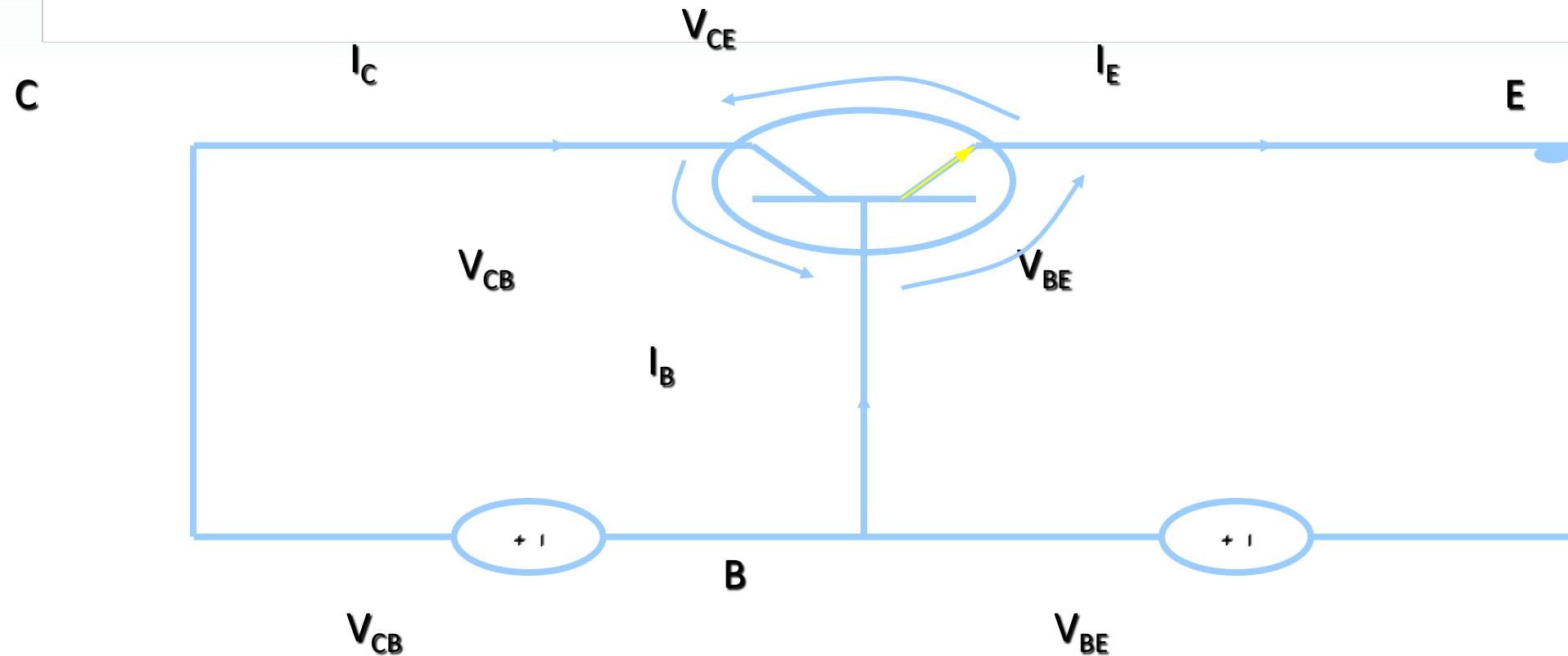
2. Common-Emitter Configuration (CE): input =  $V_{BE}$  &  $I_B$   
output=  $V_{CE}$  &  $I_C$

3. Common-Collector Configuration (CC) :input =  $V_{BC}$  &  $I_B$   
(Also known as Emitter follower) output =  $V_{EC}$  &  $I_E$



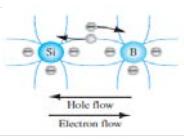


# Common-Base BJT Configuration



Circuit Diagram: NPN Transistor

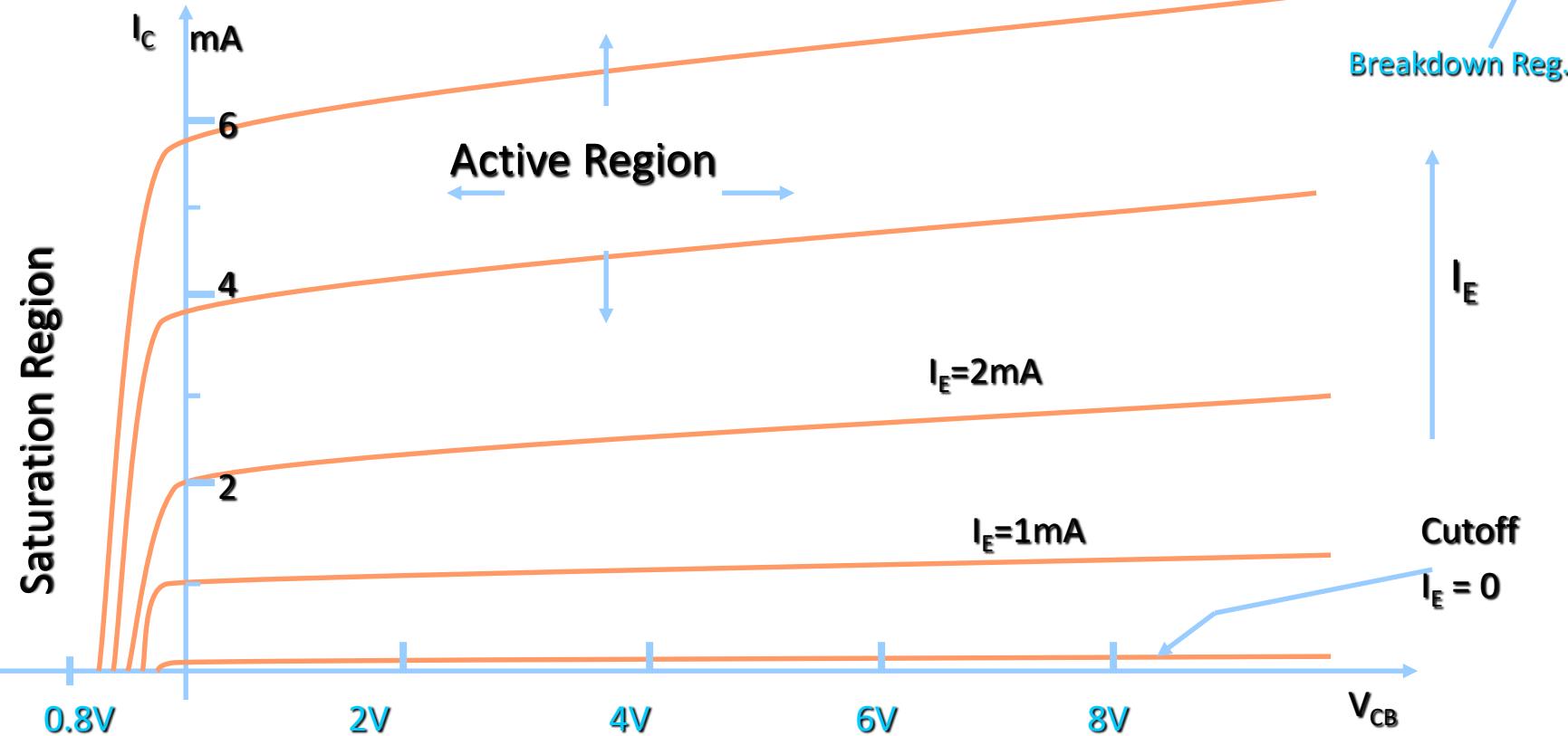


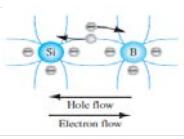


# Common-Base (CB) Characteristics

Although the Common-Base configuration is not the most common configuration, it is often helpful in the understanding operation of BJT

$V_c$ -  $I_c$  (output) Characteristic Curves

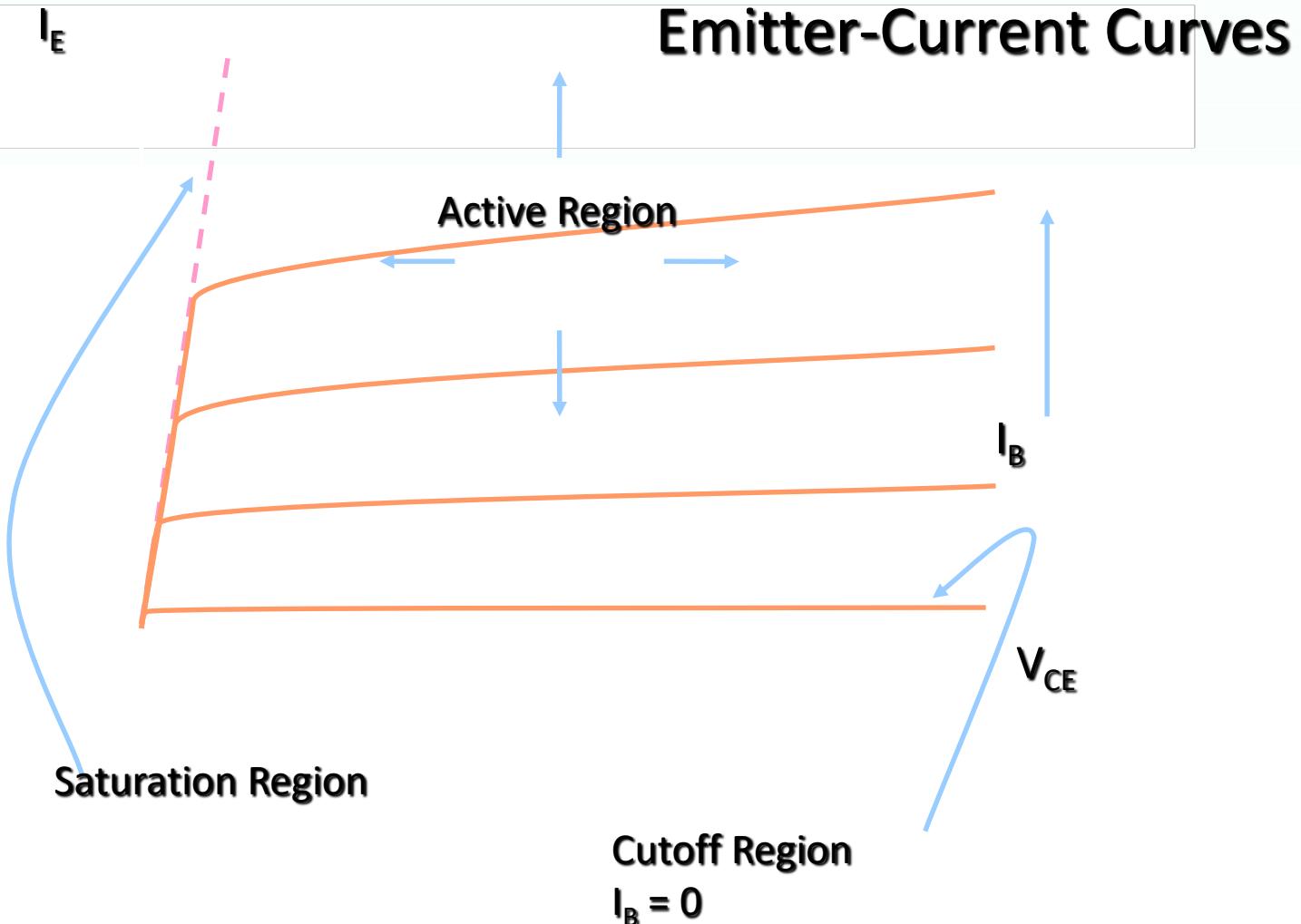


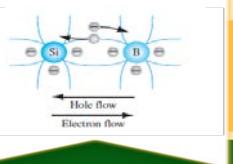


# Common-Collector BJT Characteristics

The Common-Collector biasing circuit is basically equivalent to the common-emitter biased circuit except instead of looking at  $I_C$  as a function of  $V_{CE}$  and  $I_B$  we are looking at  $I_E$ .

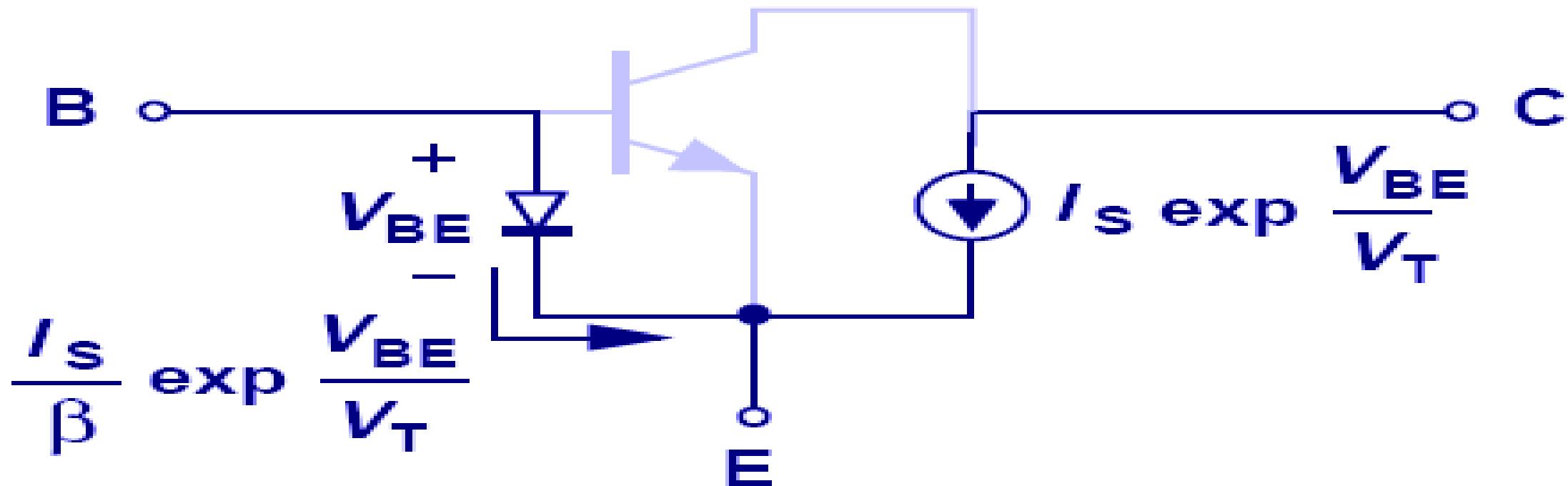
Also, since  $\alpha \sim 1$ , and  $\alpha = I_C/I_E$  that means  $I_C \sim I_E$

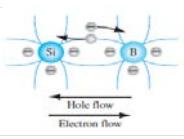




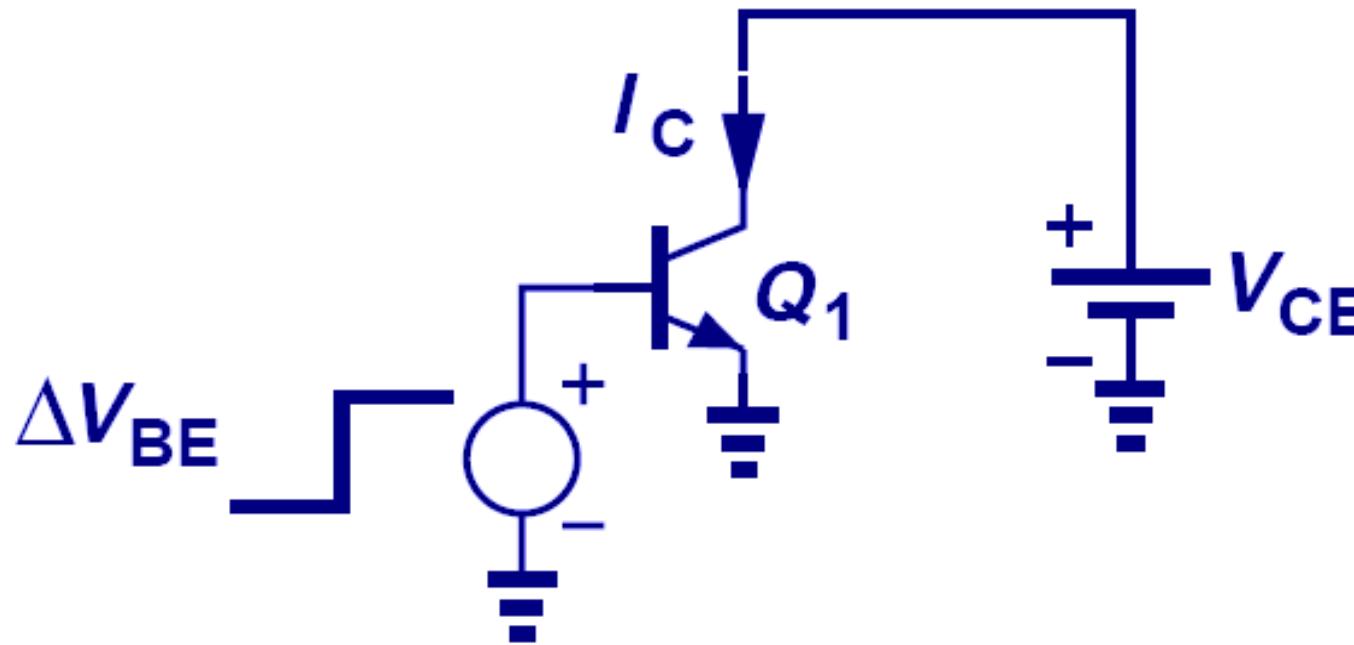
# Bipolar Transistor Large Signal Model

A diode is placed between base and emitter  
and a voltage controlled current source is placed between  
the collector and emitter.





# Transconductance



$$g_m = \frac{d}{dV_{BE}} \left( I_S \exp \frac{V_{BE}}{V_T} \right)$$

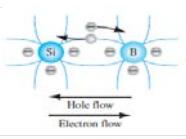
$$g_m = \frac{1}{V_T} I_S \exp \frac{V_{BE}}{V_T}$$

$$g_m = \frac{I_C}{V_T}$$

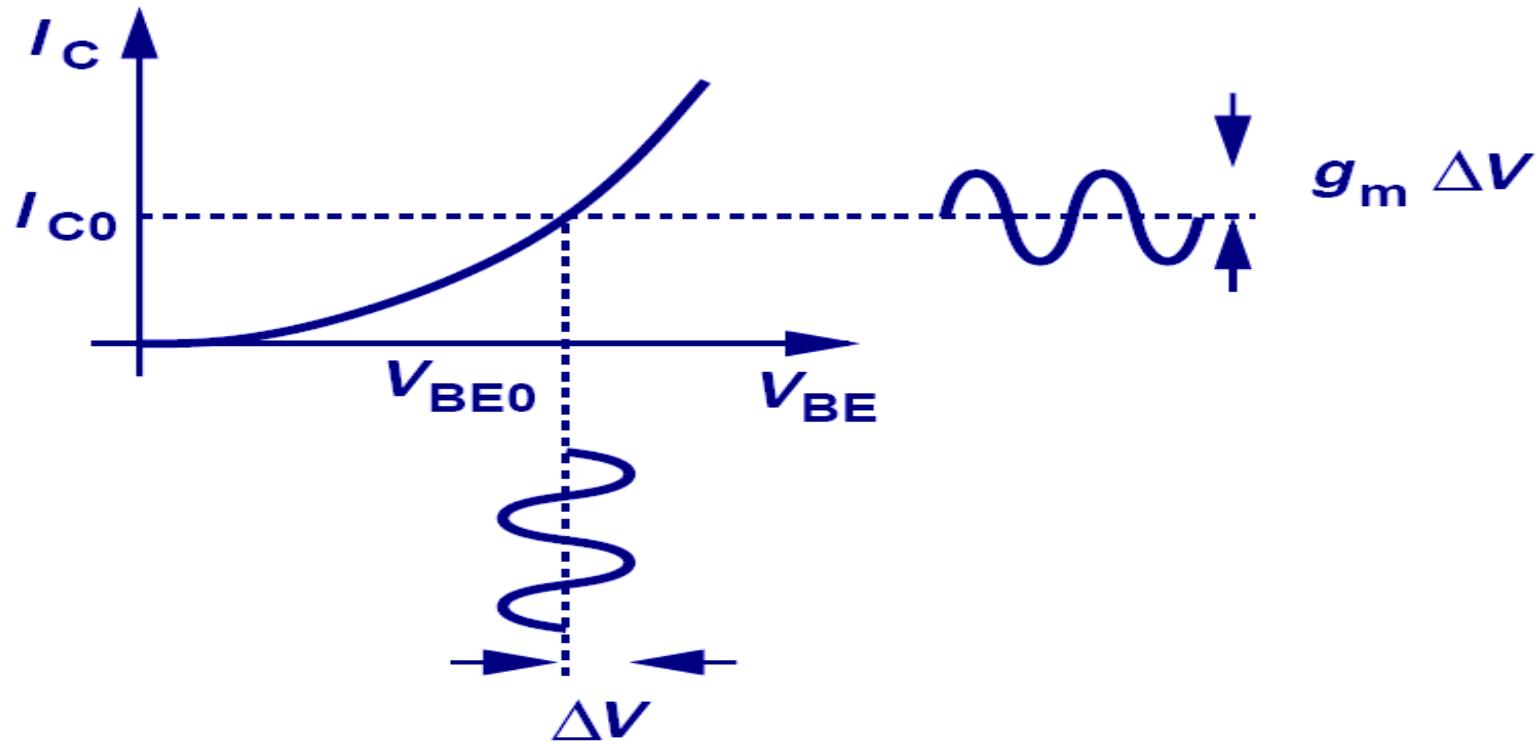
Transconductance,  $g_m$  shows a measure of how well the transistor converts voltage to current.

$g_m$  is one of the most important parameters in circuit design.



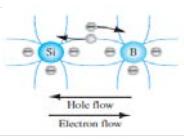


# Visualization of Transconductance

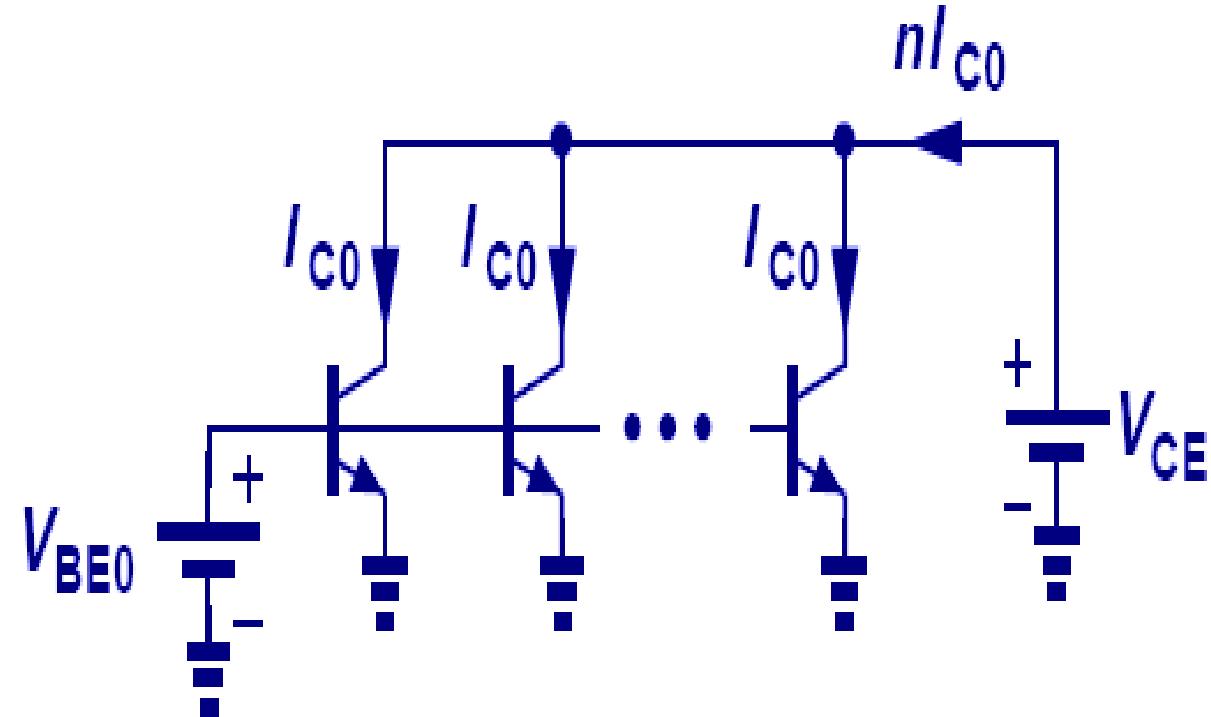
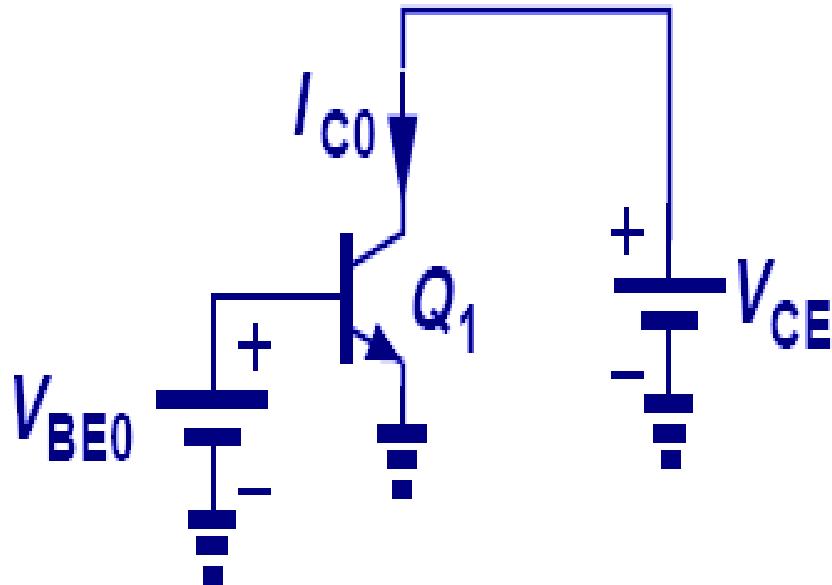


$g_m$  can be visualized as the slope of  $I_C$  versus  $V_{BE}$ .  
A large  $I_C$  has a large slope and therefore a large  $g_m$ .





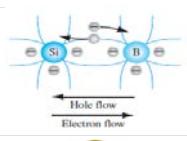
# Transconductance and Area



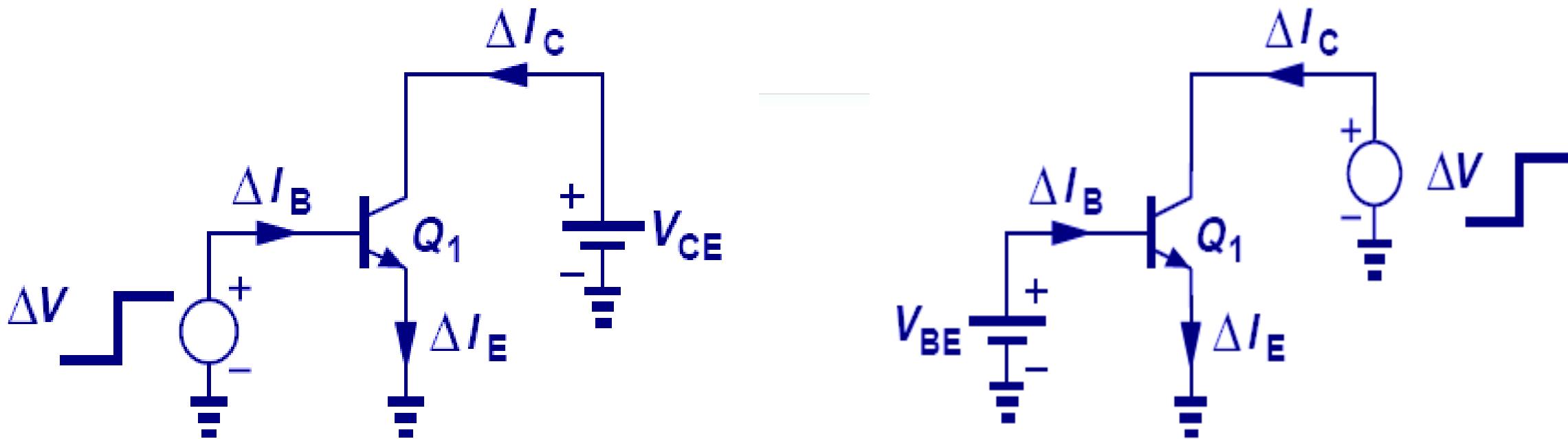
When the area of a transistor is increased by  $n$ ,  $I_S$  increases by  $n$ .

For a constant  $V_{BE}$ ,  $I_C$  and hence  $g_m$  increases by a factor of  $n$ .





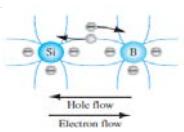
# Small-Signal Model: Derivation



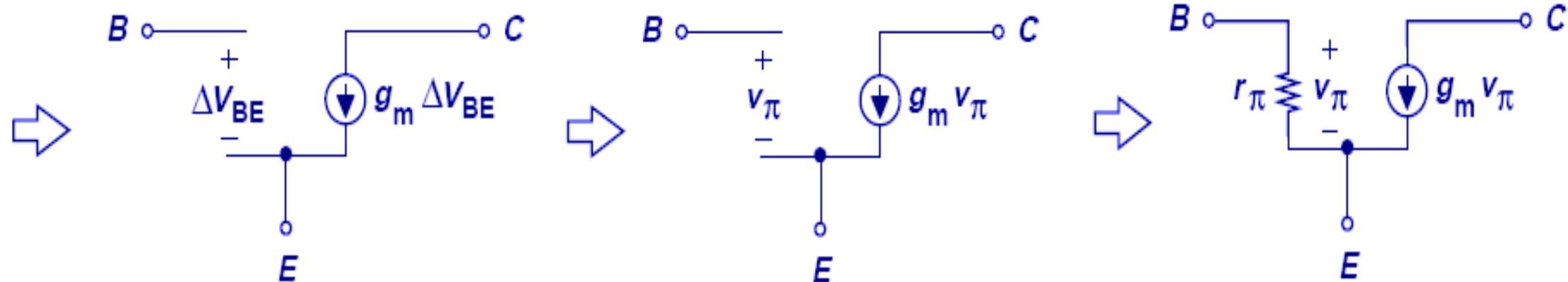
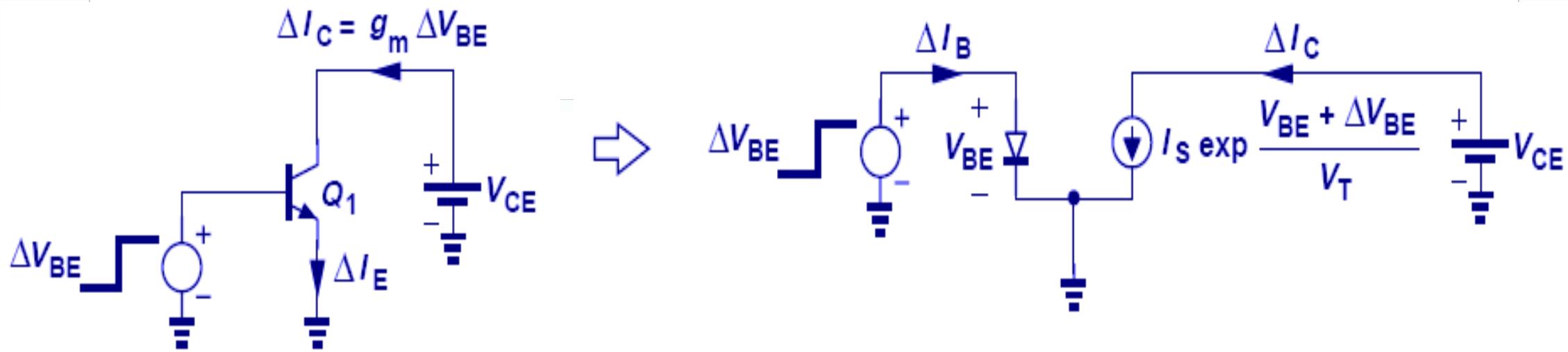
Small signal model is derived by perturbing voltage difference every two terminals while fixing the third terminal and analyzing the change in current of all three terminals.

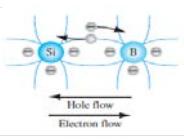
We then represent these changes with controlled sources or resistors.



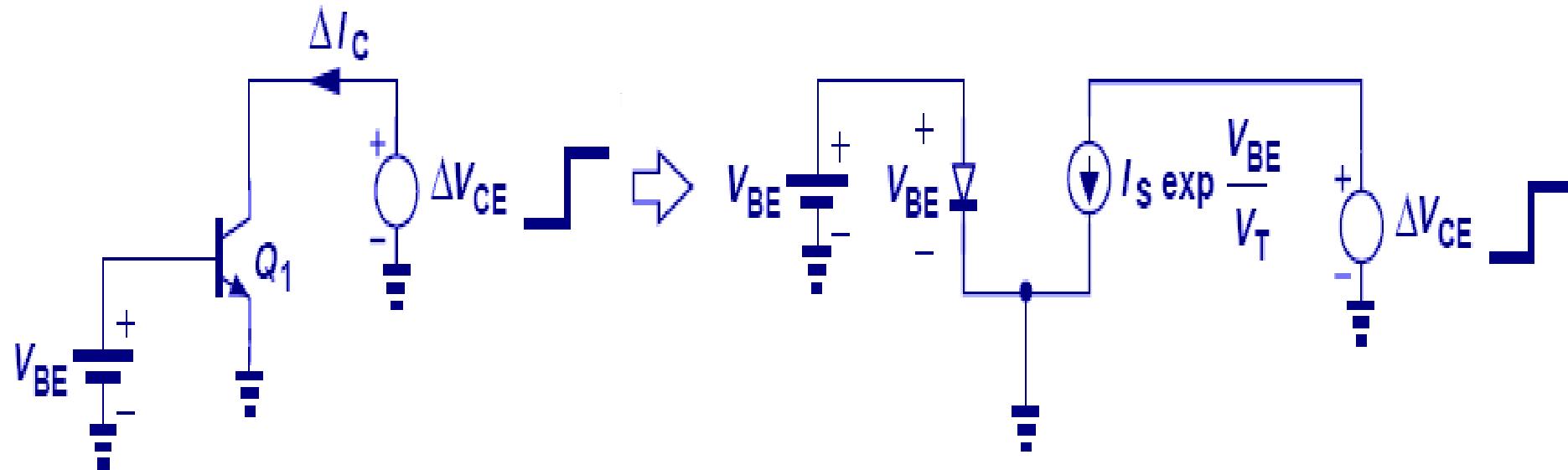


# Small-Signal Model: $V_{BE}$ Change





# Small-Signal Model: $V_{CE}$ Change

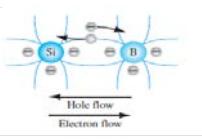


Ideally,  $V_{CE}$  has no effect on the collector current.

Thus, it will not contribute to the small signal model.

It can be shown that  $V_{CB}$  has no effect on the small signal model, either.

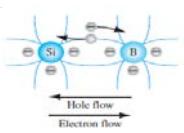




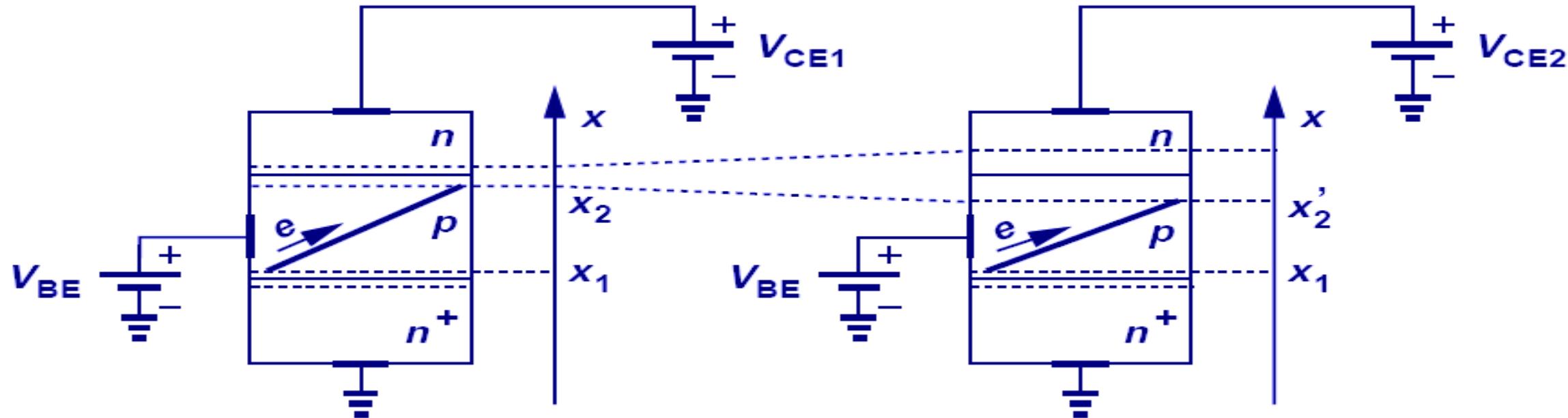
# AC Ground

Since the power supply voltage does not vary with time, it is regarded as a ground in small-signal analysis.





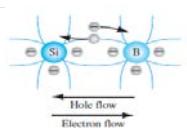
# Early Effect



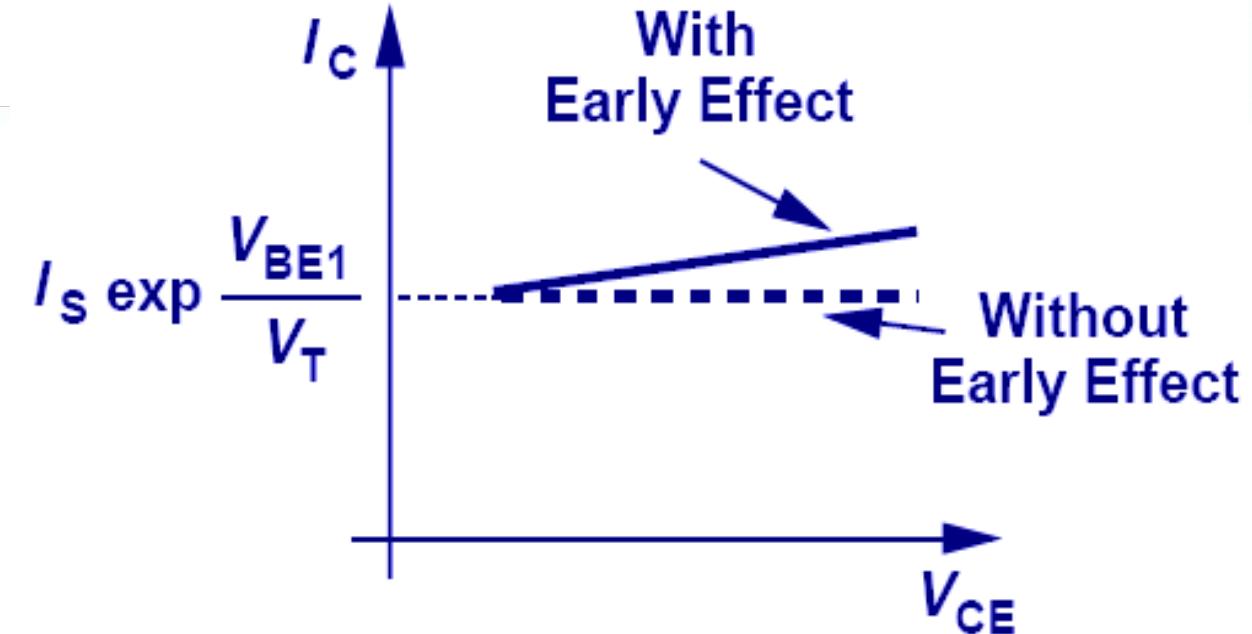
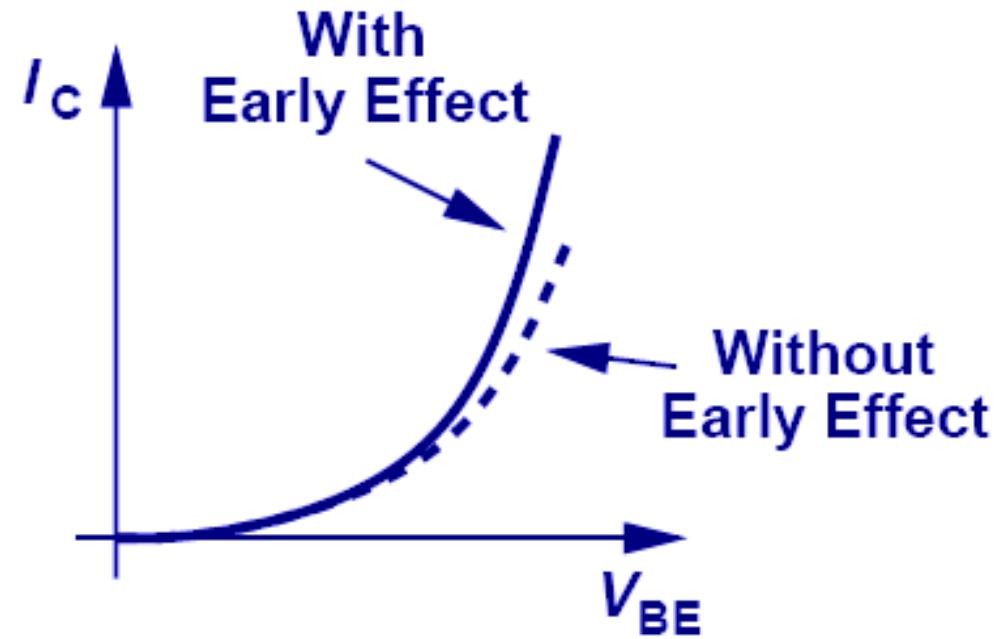
The claim that collector current does not depend on  $V_{CE}$  is not accurate.

As  $V_{CE}$  increases, the depletion region between base and collector increases. Therefore, the effective base width decreases, which leads to an increase in the collector current.





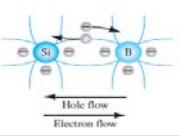
# Early Effect Illustration



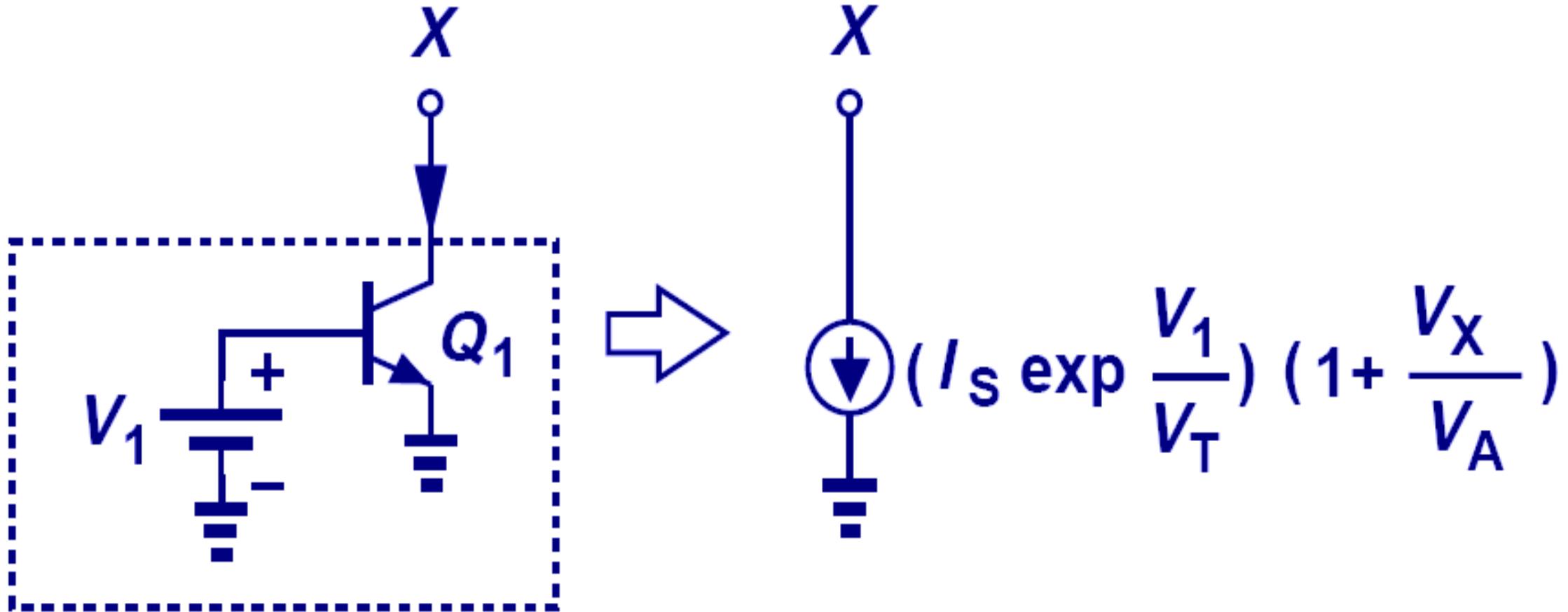
Early effect is the variation in width of the base in a BJT due to a variation in the applied base-to-collector voltage

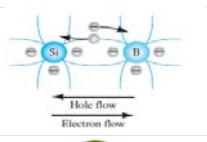
With Early effect, collector current becomes larger than usual and  $I_c$  is a function of  $V_{CE}$ .





# Early Effect Representation

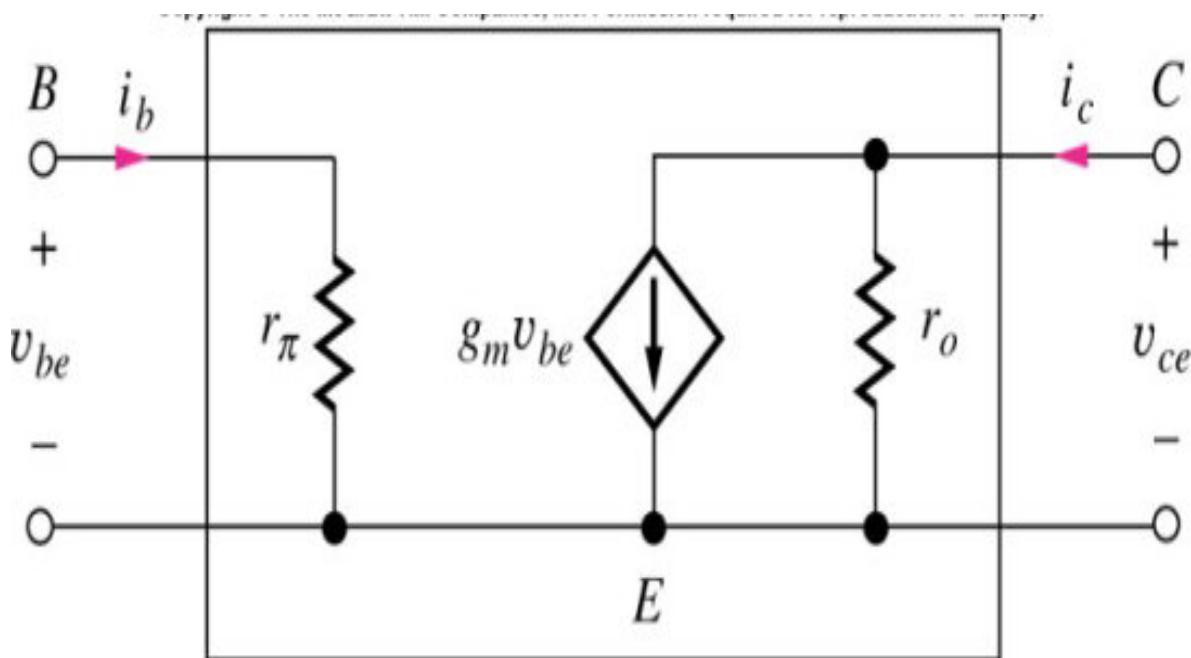




# Hybrid-Pi Model for the BJT

The hybrid-pi small-signal model is the intrinsic low-frequency representation of the BJT.

The small-signal parameters are controlled by the Q-point and are independent of the geometry of the BJT.



Transconductance:  $g_m = \frac{I_C}{V_T}$ ,  $V_T = \frac{kT}{q}$

Input resistance:  $R_{in}$

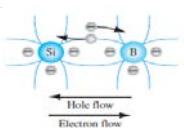
$$r_{\pi} = \frac{\beta_o V_T}{I_C} = \frac{\beta_o}{g_m}$$

Output resistance:

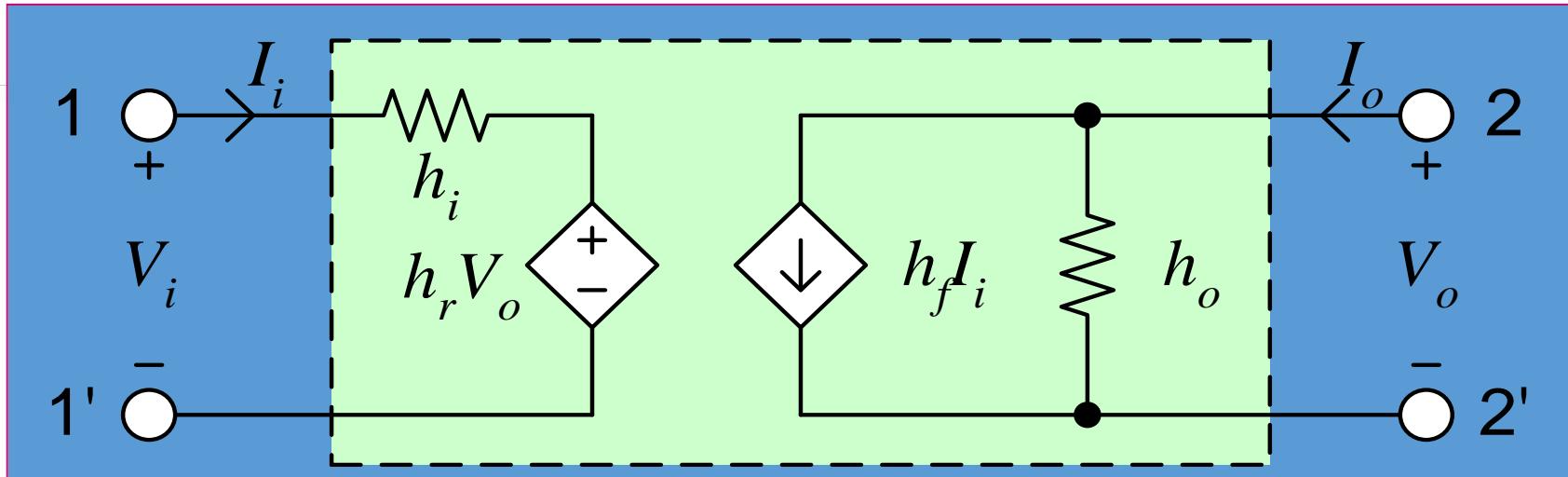
$$r_o = \frac{V_A + V_{CE}}{I_C}$$

Where,  $V_A$  is Early Voltage  
( $V_A = 100V$  for npn)





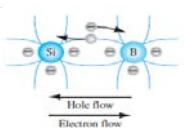
# Hybrid-Pi Model for The BJT



$$V_i = h_{11}I_i + h_{12}V_o = h_iI_i + h_rV_o$$

$$I_o = h_{21}I_i + h_{22}V_o = h_fI_i + h_oV_o$$





# $h$ -Parameters

$$h_{11} = \frac{V_i}{I_i} \Bigg| \Bigg| V_o = 0$$

$$h_{12} = \frac{V_i}{V_o} \Bigg| \Bigg| I_i = 0$$

$$h_{21} = \frac{I_o}{I_i} \Bigg| \Bigg| V_o = 0$$

$$h_{22} = \frac{I_o}{V_o} \Bigg| \Bigg| I_i = 0$$

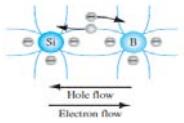
$h_{11} = h_i$  = Input Resistance

$h_{12} = h_r$  = Reverse Transfer Voltage Ratio

$h_{21} = h_f$  = Forward Transfer Current Ratio

$h_{22} = h_o$  = Output Admittance





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# Thank You Very Much

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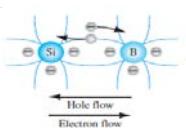
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

Tel.: 050 770 32 86

Whatsup: 0049 172 4444 765

Skype\_id: calculus.affairs





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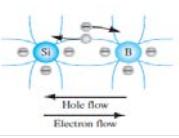
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“Paper is to write things down  
that we need to remember. Our  
brains are used to think”

**Albert Einstein**





# Overview

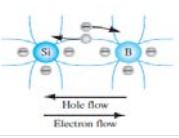
## Bipolar Amplifiers

General Concepts

Operating Point  
Analysis

Amplifier  
Topologies





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# Overview

## Bipolar Amplifiers

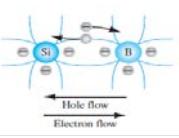
### General Concepts

**Input/Output  
Impedances**

**Biasing**

**DC and Small-Signal  
Analysis**





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# Overview

## Bipolar Amplifiers

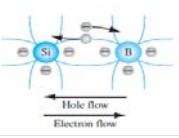
### Operating Point Analysis

**Simple  
Biasing**

**Emitter  
Degeneration**

**Self-Biasing**





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# Overview

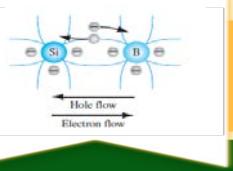
## Bipolar Amplifiers

### Amplifier Topologies

**Common-  
Emitter  
Stage**

**Common-  
Base Stage**





# Introduction to Amplifiers

The BJT is an excellent amplifier when biased in the forward-active region.

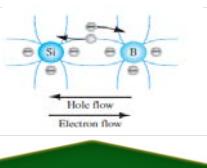
The FET can be used as an amplifier if operated in the saturation region.

In these regions, the transistors can provide high voltage, current and power gains.

DC bias is provided to stabilize the operating point in the desired operation region.

The **dc operating point** between saturation and cutoff is called the Q-point. The goal is to set the Q-point such that it does not go into saturation or cutoff when an ac signal is applied





# Introduction to Amplifiers

The DC Q-point also determines

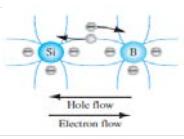
The small-signal parameters of the transistor

The voltage gain, input resistance, and output resistance

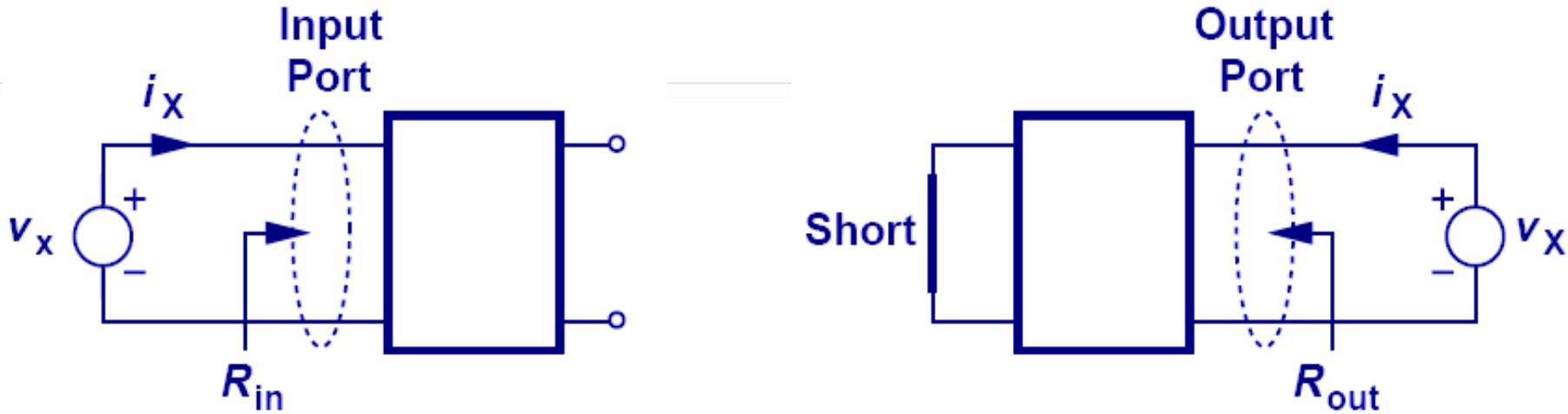
The maximum input and output signal amplitudes

The overall power consumption of the amplifier





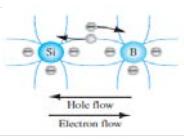
# Input/Output Impedances



$$R_x = \frac{V_x}{i_x}$$

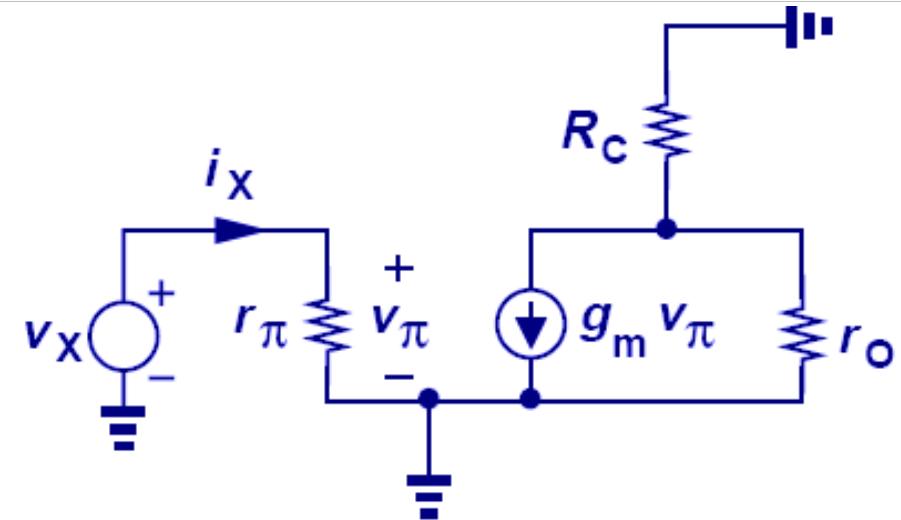
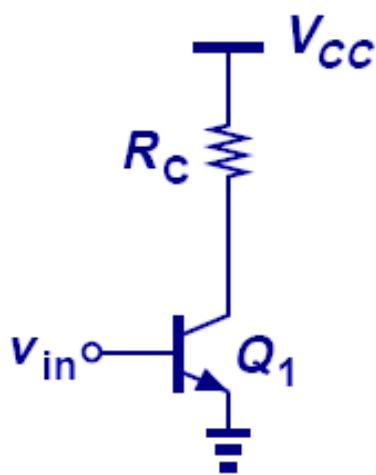
The techniques of measuring input and output impedances.





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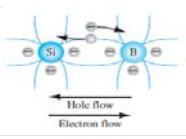
# Input Impedance Example



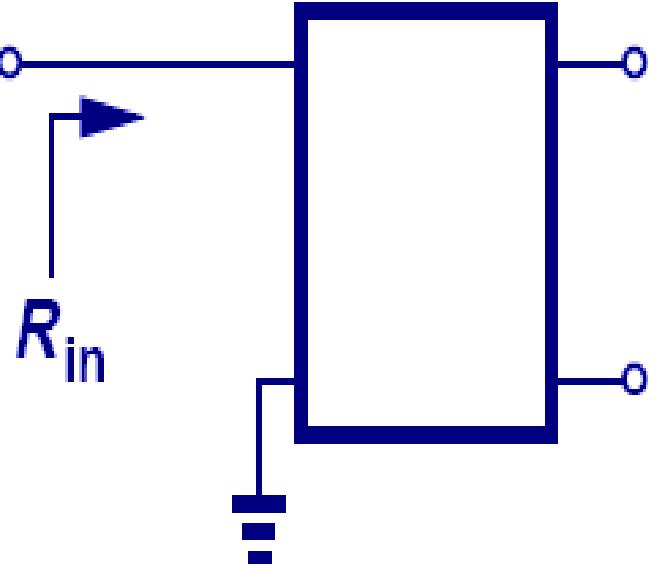
$$\frac{v_x}{i_x} = r_\pi$$

When calculating input/output impedance, small-signal analysis is assumed.

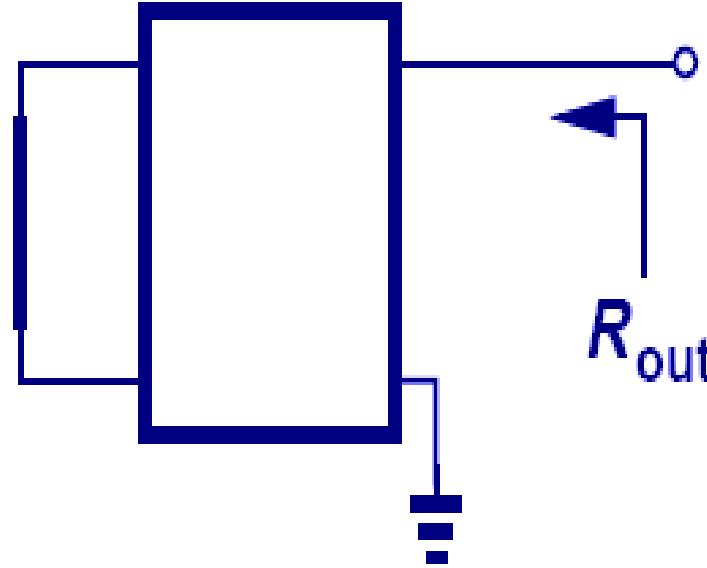




# Impedance at a Node

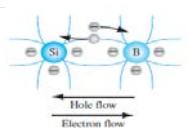


Short

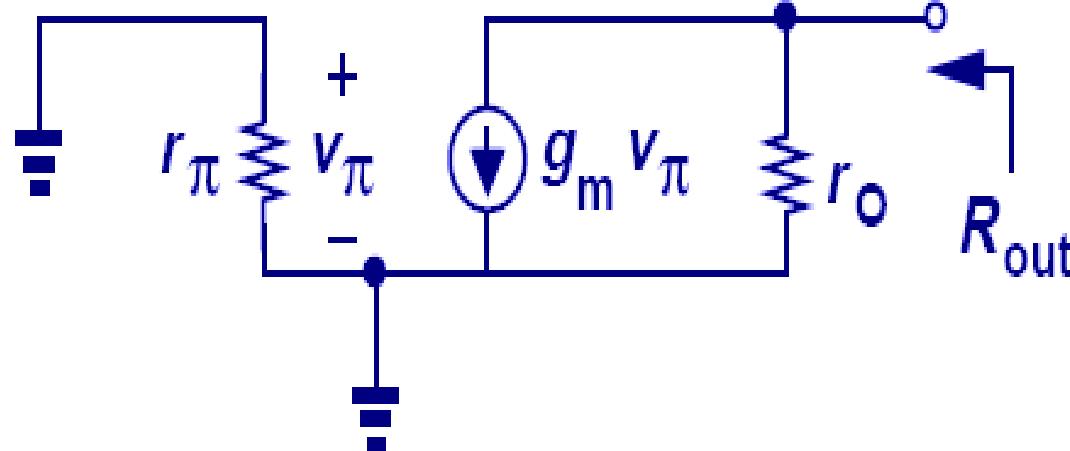
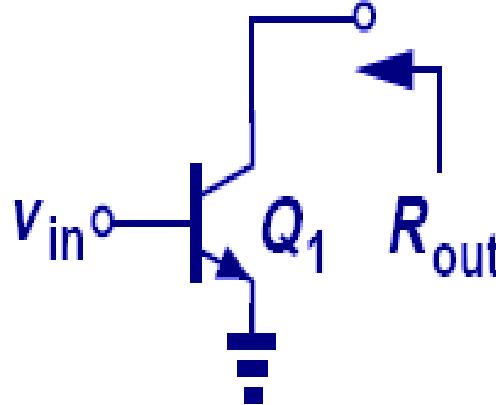


When calculating I/O impedances at a port, we usually ground one terminal while applying the test source to the other terminal of interest.





# Impedance at Collector

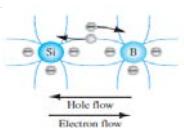


$$R_{out} = r_o$$

Early effect is the variation in width of the base in a BJT due to a variation in the applied base-to-collector voltage

With Early effect, the impedance seen at the collector is equal to the intrinsic output impedance of the transistor (if emitter is grounded).



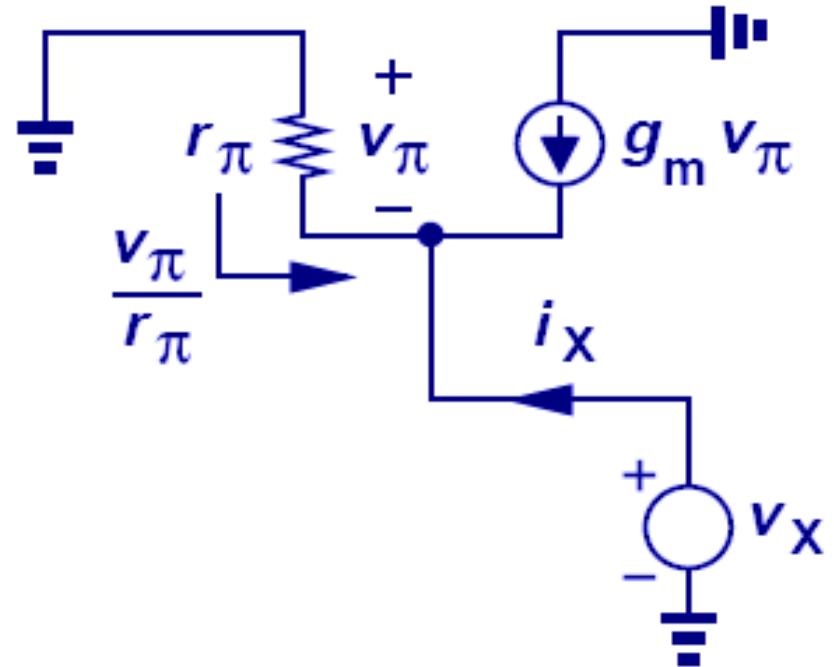
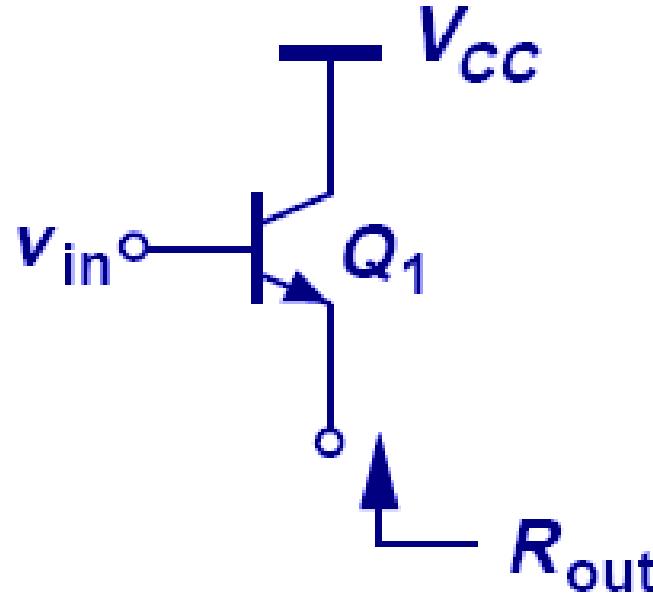


# SEMICONDUCTOR DEVICES

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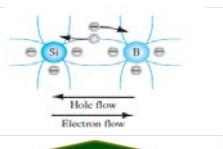
# Impedance at Emitter



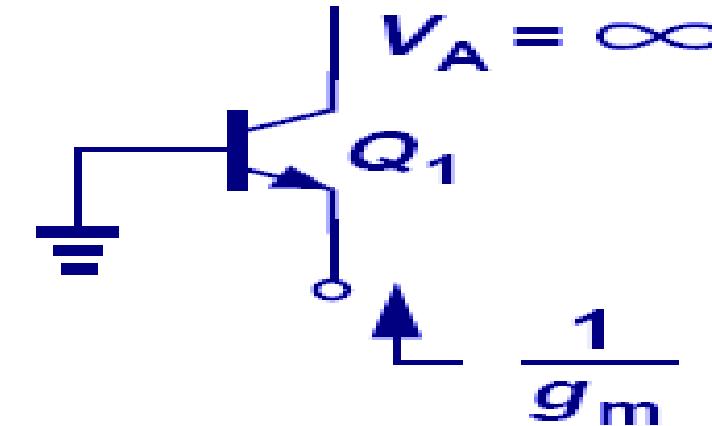
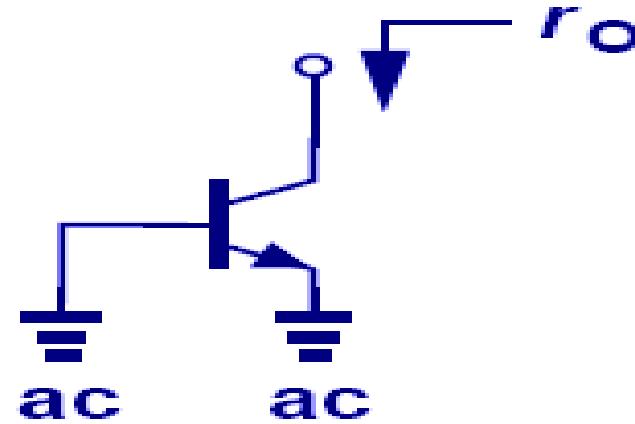
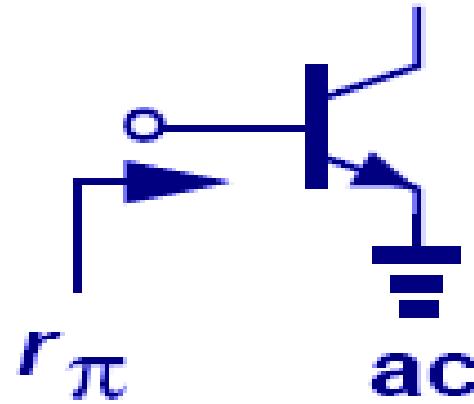
$$\frac{v_x}{i_x} = \frac{1}{g_m + \frac{1}{r_\pi}}$$
$$R_{out} \approx \frac{1}{g_m} \quad (V_A = \infty)$$

The impedance seen at the emitter of a transistor is approximately equal to one over its transconductance (if the base is grounded).





# Three Master Rules of Transistor Impedances

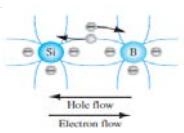


Rule # 1: looking into the base, the impedance is  $r_\pi$  if emitter is (ac) grounded.

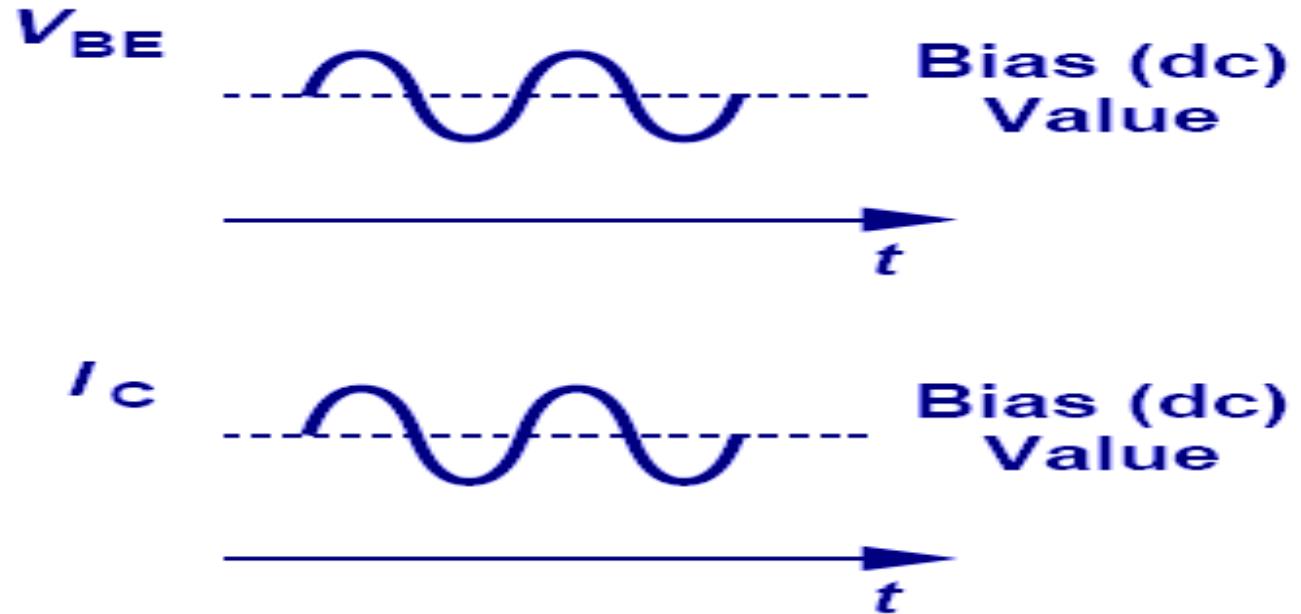
Rule # 2: looking into the collector, the impedance is  $r_o$  if emitter is (ac) grounded.

Rule # 3: looking into the emitter, the impedance is  $1/g_m$  if base is (ac) grounded and Early effect is neglected.





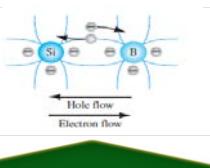
# Biasing of BJT



Transistors and circuits must be biased because

- (1) transistors must operate in the active region,
- (2) their small-signal parameters depend on the bias conditions.

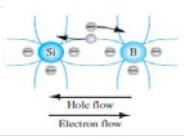




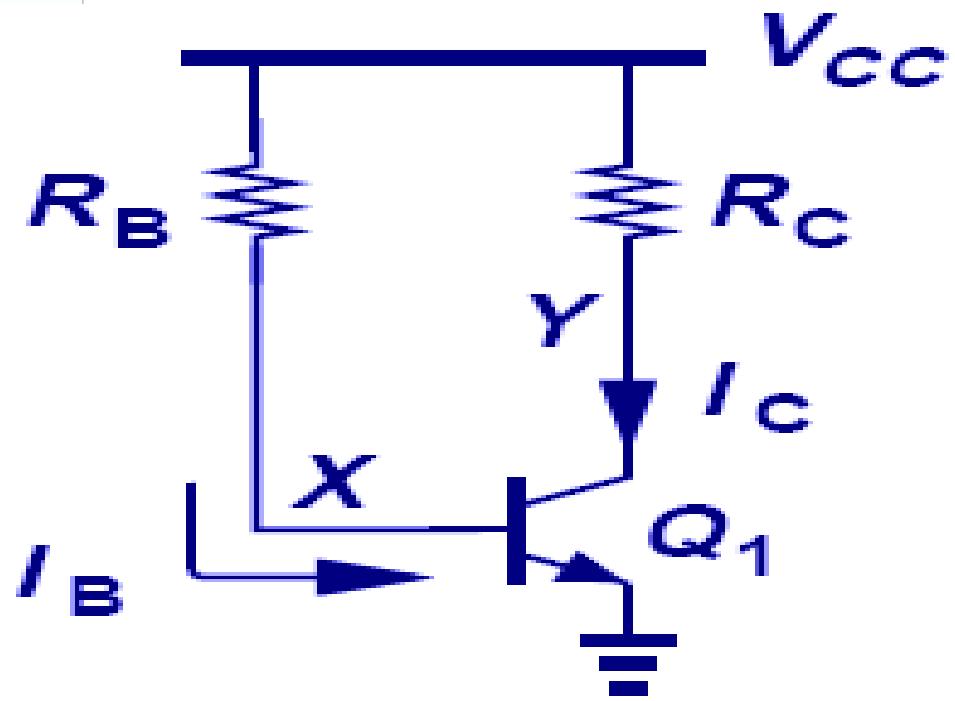
# Methods For BJT Biasing

- Base resistor method
- Emitter bias method
- Biasing with collector-feedback resistor
- Voltage-divider bias





# Biasing with Base Resistor



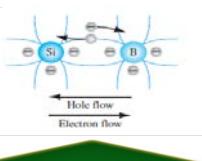
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B}$$

Assuming a constant value for  $V_{BE}$ , one can solve for both  $I_B$  and  $I_C$  and determine the terminal voltages of the transistor.

Bias point is sensitive to  $\beta$  variations.





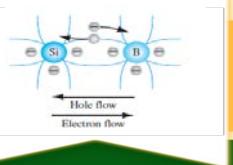
# Biasing with Base Resistor

This method is also called fixed bias method

$$\text{The stability factor } S = \frac{\beta + 1}{1 - \beta \left( \frac{dI_B}{dI_C} \right)}$$

Since  $I_B$  is independent of  $I_C$ ,  $dI_B/dI_C = 0$ , hence  $S = \beta + 1$



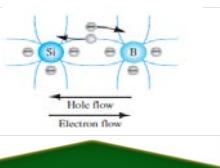


# Biasing with Base Resistor

## Advantages

- The biasing circuit is simple, since one resistance  $R_B$  is required
- Biasing conditions can easily be set and the calculations are simple
- There is no loading of the source by the biasing circuit, since no resistor is employed across base-emitter junction



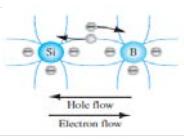


# Biasing with Base Resistor

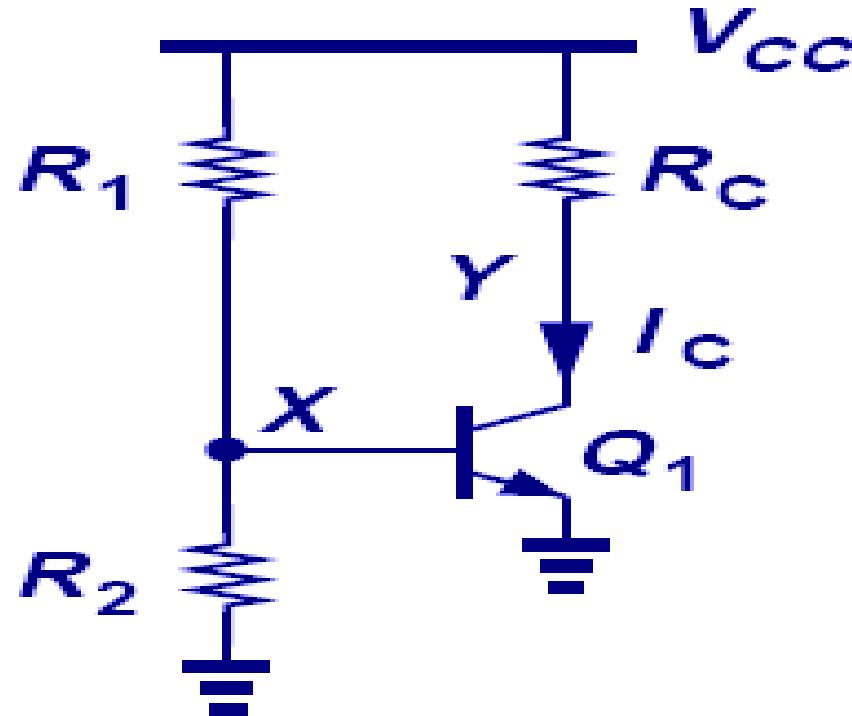
## Disadvantages

- The biasing provides poor stabilization
- The stability factor is very high and hence there are strong chances of thermal runaway. Poor thermal stability





# Improved Biasing: Resistive Divider

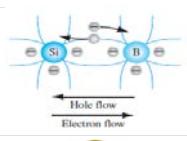


$$V_X = \frac{R_2}{R_1 + R_2} V_{CC}$$

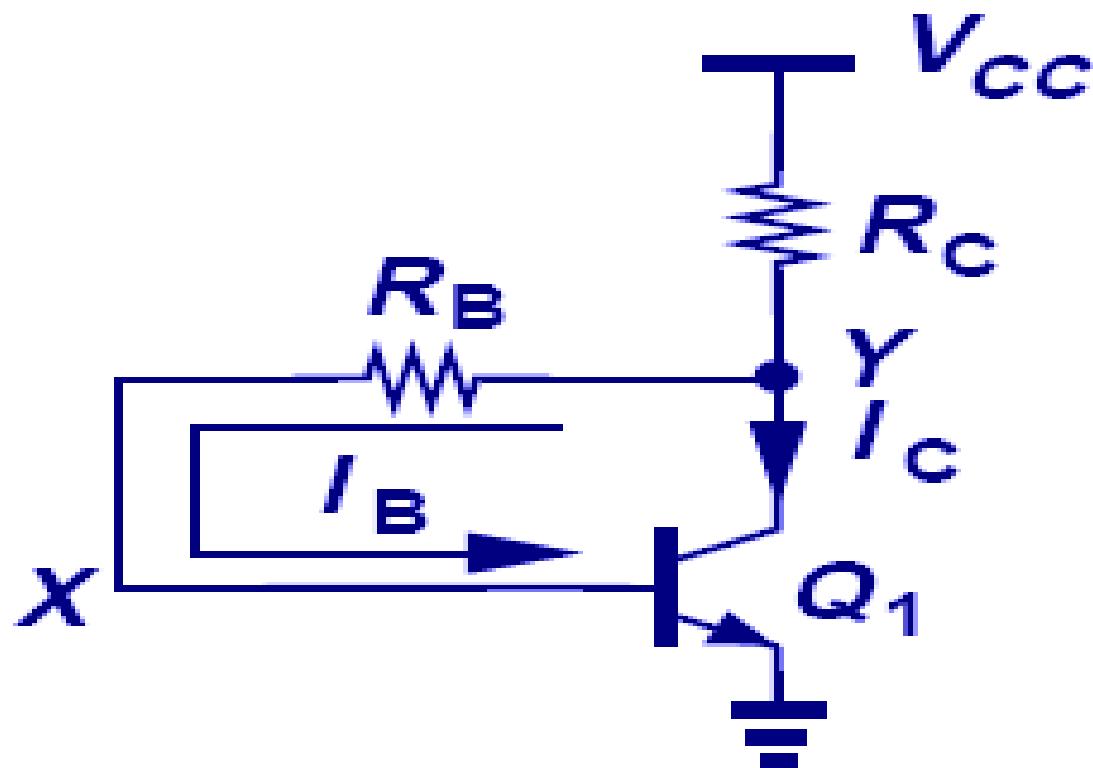
$$I_C = I_S \exp\left(\frac{R_2}{R_1 + R_2} \frac{V_{CC}}{V_T}\right)$$

Using resistor divider to set  $V_{BE}$ , it is possible to produce a collector current  $I_C$  that is relatively independent of  $\beta$  if base current is small.





# Self-Biasing Technique (Collector-Feedback)



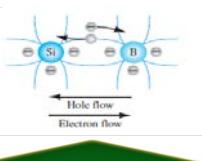
## Disadvantage

The circuit provides a negative feedback which reduces the gain of the amplifier

This bias method utilizes the collector voltage to provide the necessary  $V_x$  and  $I_B$ .

One important characteristic of this technique is that collector has a higher potential than the base, thus guaranteeing active operation of the transistor.





# Self-Biasing Design Guidelines

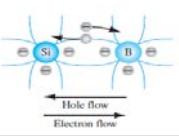
$$R_C \gg \frac{R_B}{\beta}$$

(1) provides insensitivity to  $\beta$  .

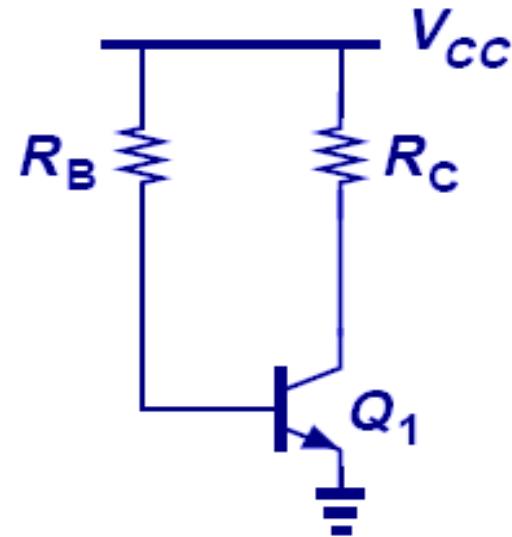
$$\Delta V_{BE} \ll V_{CC} - V_{BE}$$

(2) provides insensitivity to variation in  $V_{BE}$  .

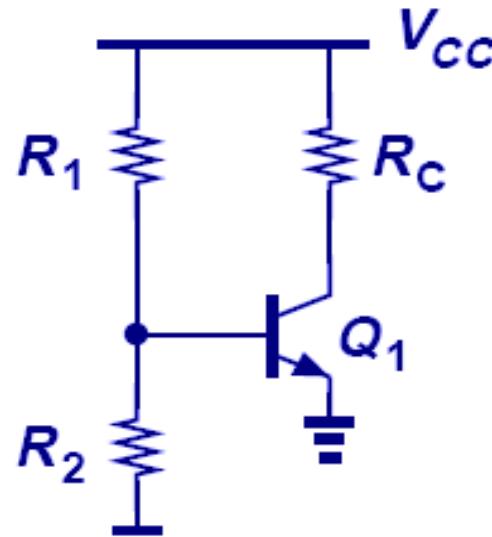




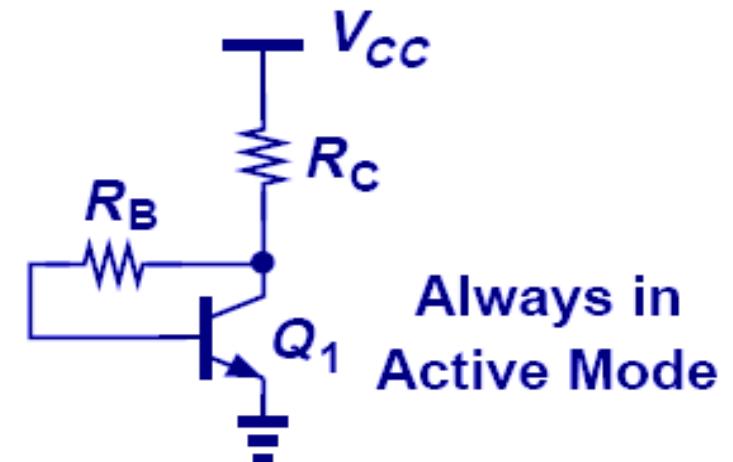
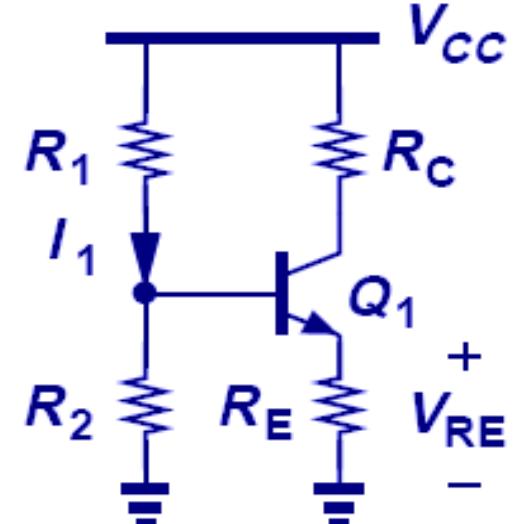
# Summary of Biasing Techniques



Sensitive  
to  $\beta$

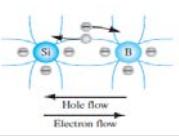


Sensitive  
to Resistor Error

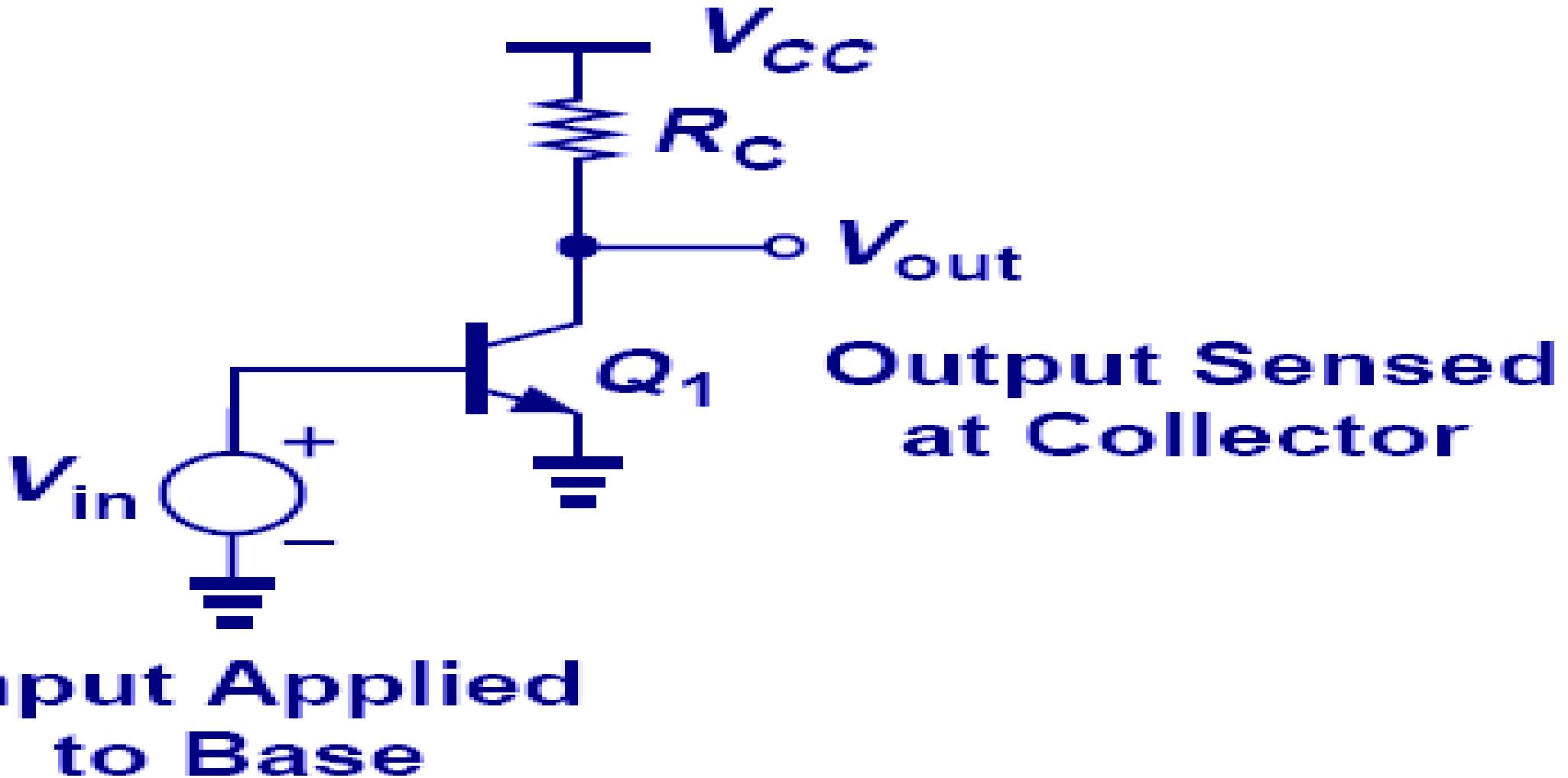


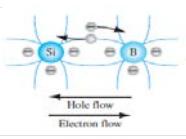
Always in  
Active Mode



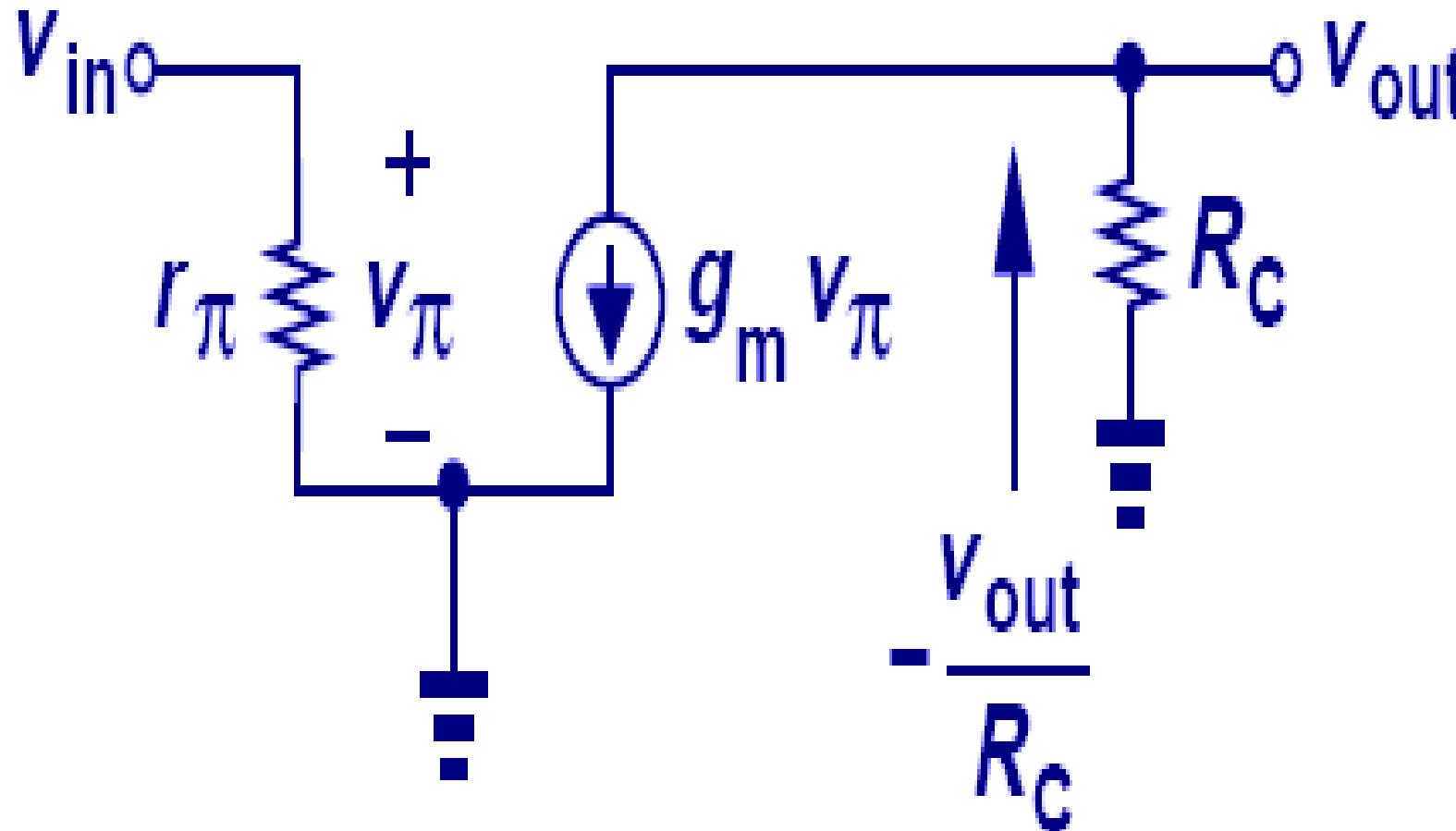


# Common-Emitter Topology





# Small Signal of CE Amplifier

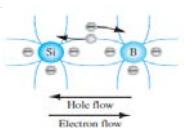


$$A_v = \frac{V_{out}}{V_{in}}$$

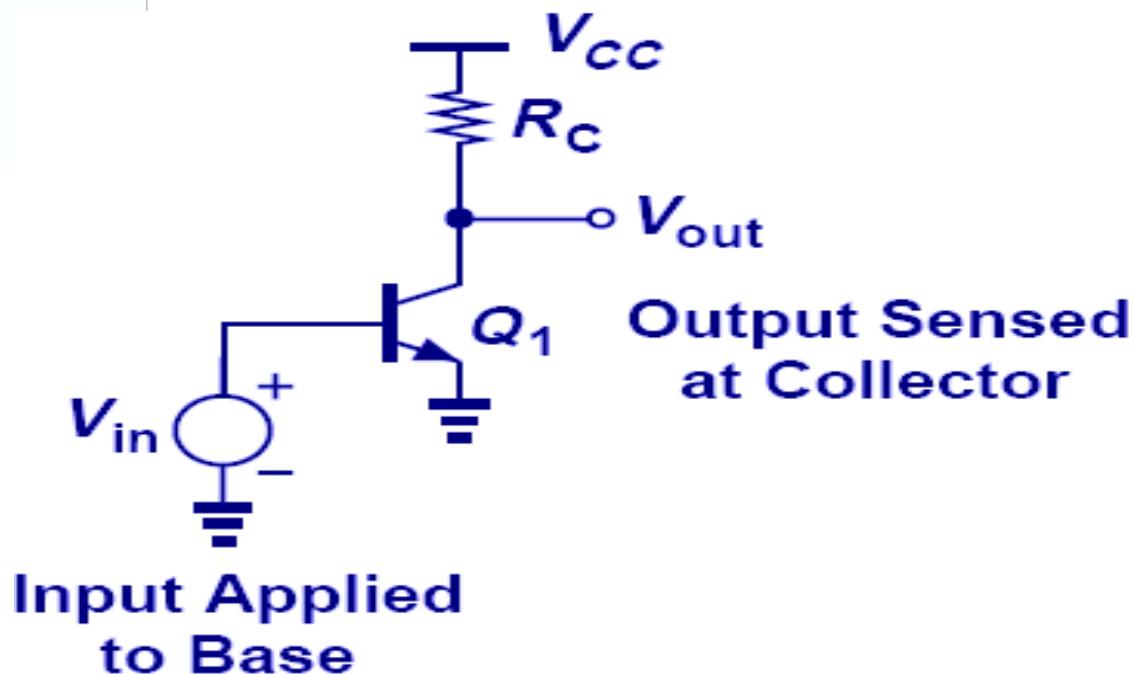
$$-\frac{V_{out}}{R_C} = g_m v_\pi = g_m v_{in}$$

$$A_v = -g_m R_C$$





# Limitation on CE Voltage Gain

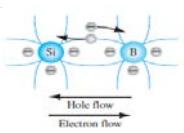


$$|A_v| = \frac{I_C R_C}{V_T} \quad |A_v| = \frac{V_{RC}}{V_T} \quad |A_v| < \frac{V_{CC} - V_{BE}}{V_T}$$

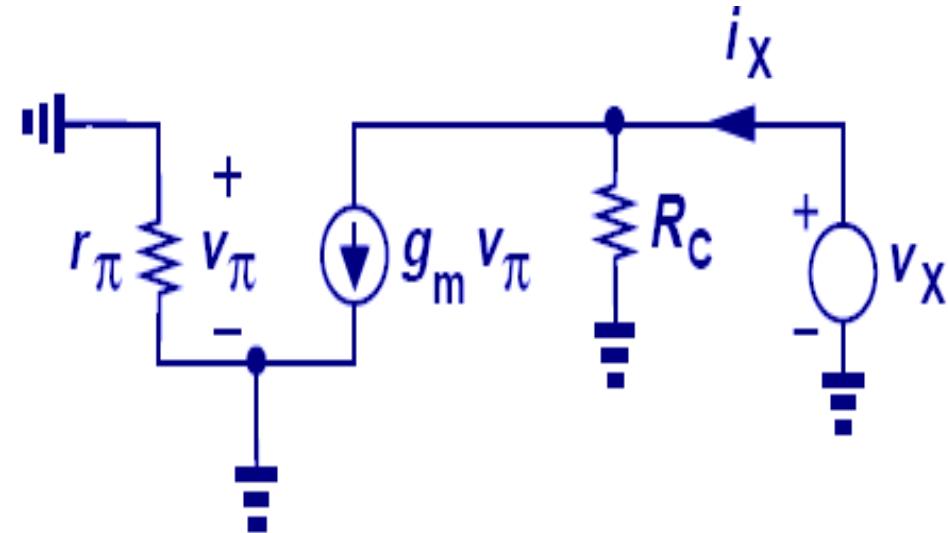
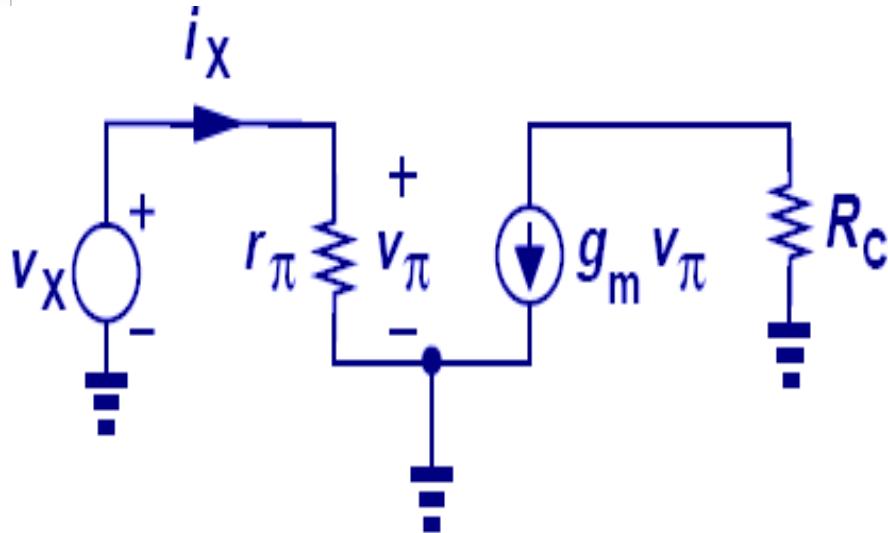
Since  $g_m$  can be written as  $I_C/V_T$ , the CE voltage gain can be written as the ratio of  $V_{RC}$  and  $V_T$ .

$V_{RC}$  is the potential difference between  $V_{CC}$  and  $V_{CE}$ , and  $V_{CE}$  cannot go below  $V_{BE}$  in order for the transistor to be in active region.





# I/O Impedances of CE Stage

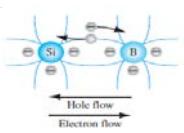


$$R_{in} = \frac{v_x}{i_x} = r_\pi$$

$$R_{out} = \frac{v_x}{i_x} = R_c$$

When measuring output impedance, the input port has to be grounded so that  $V_{in} = 0$ .





# Intrinsic Gain

$$A_v = -g_m (R_C \parallel r_o)$$

$$R_{out} = R_C \parallel r_o$$

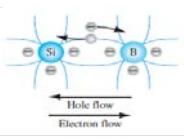
$$A_v = -g_m r_o$$

$$|A_v| = \frac{V_A}{V_T}$$

As  $R_C$  goes to infinity, the voltage gain reaches the product of  $g_m$  and  $r_o$ , which represents the maximum voltage gain the amplifier can have.

The intrinsic gain is independent of the bias current.





# Current Gain

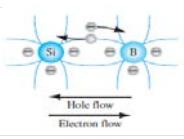
$$A_I = \frac{i_{out}}{i_{in}}$$

$$A_I|_{CE} = \beta$$

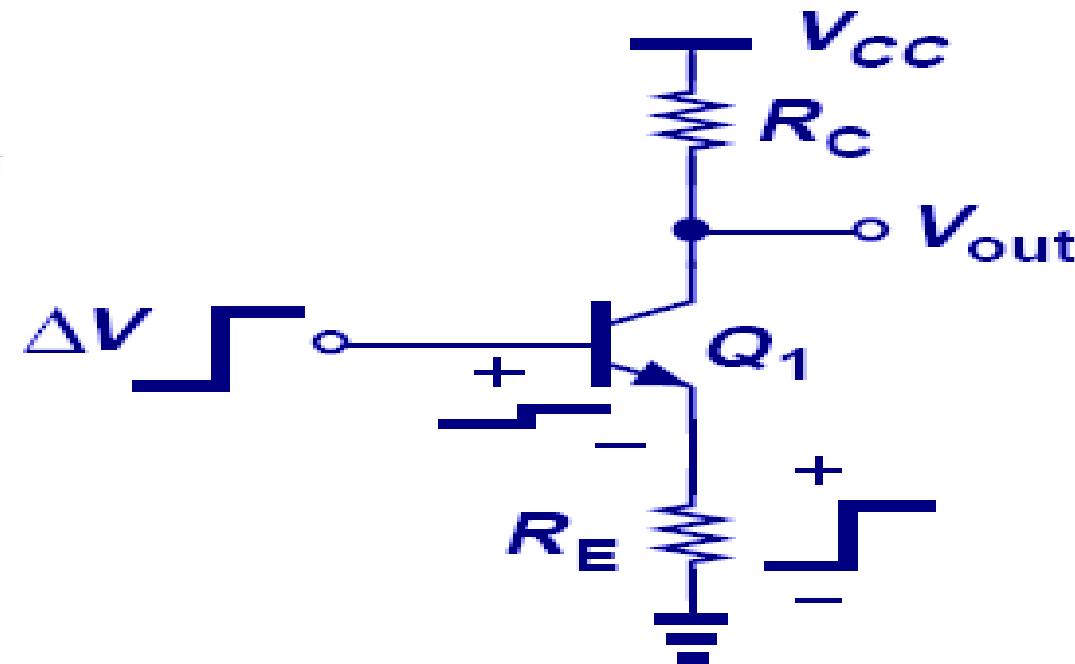
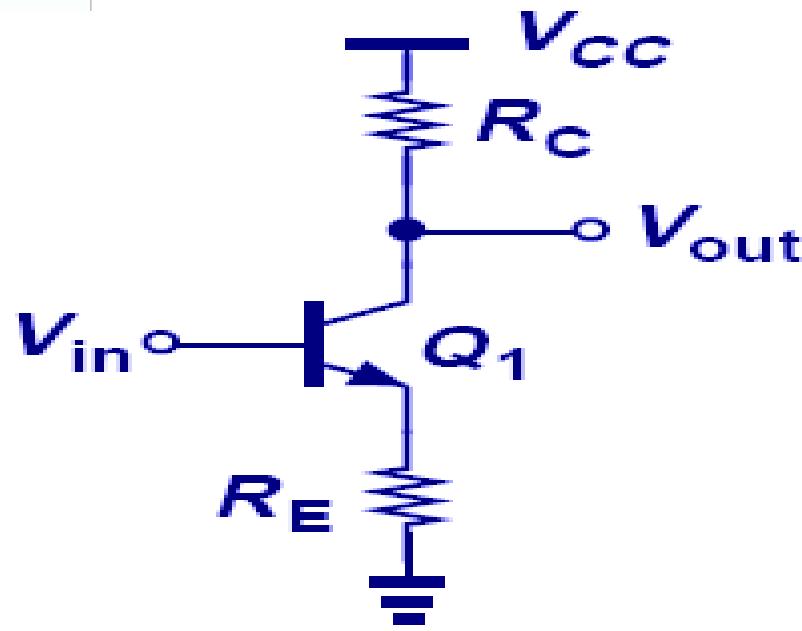
Another parameter of the amplifier is the current gain, which is defined as the ratio of current delivered to the load to the current flowing into the input.

For a CE stage, it is equal to  $\beta$ .





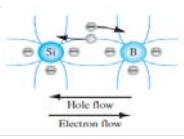
# Emitter Degeneration



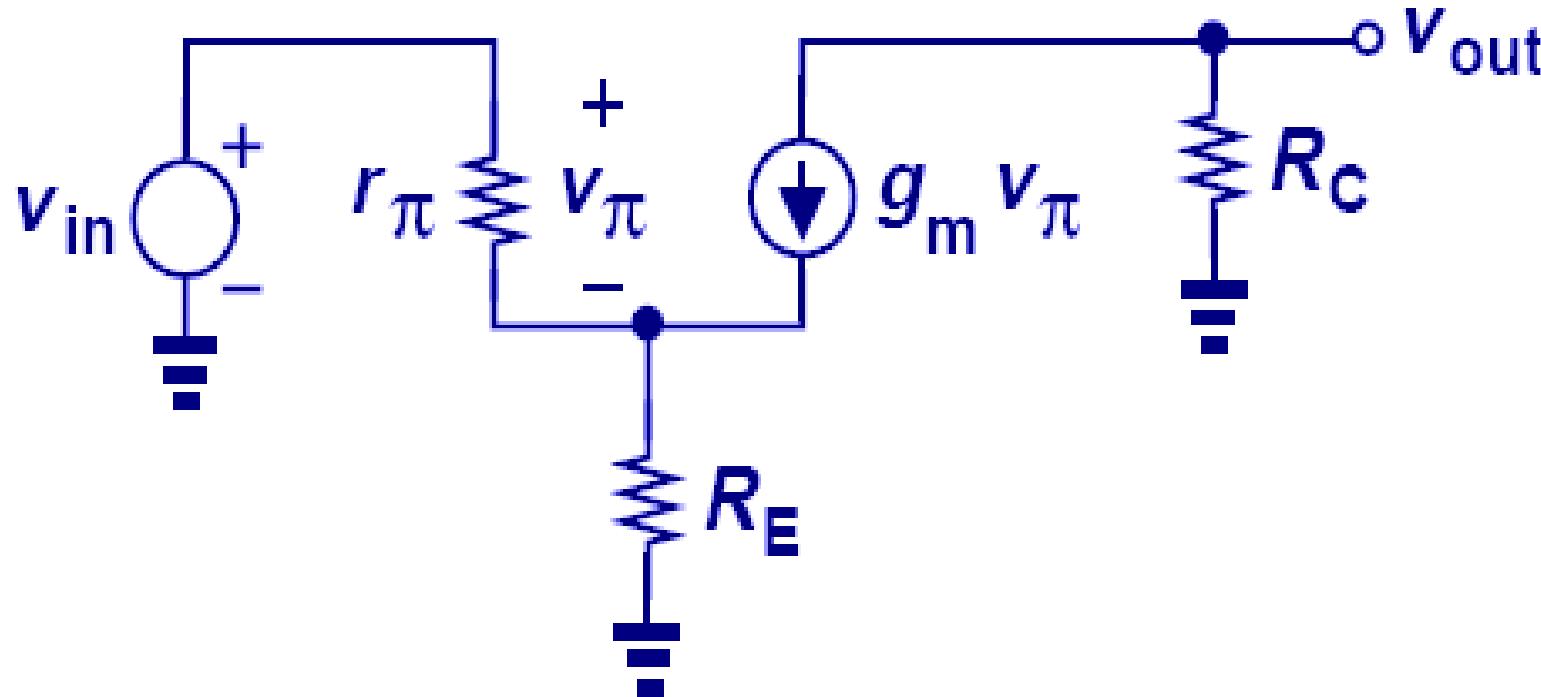
By inserting a resistor in series with the emitter, we “degenerate” the CE stage.

This topology will decrease the gain of the amplifier but improve other aspects, such as linearity, and input impedance.





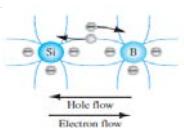
# Small-Signal Model



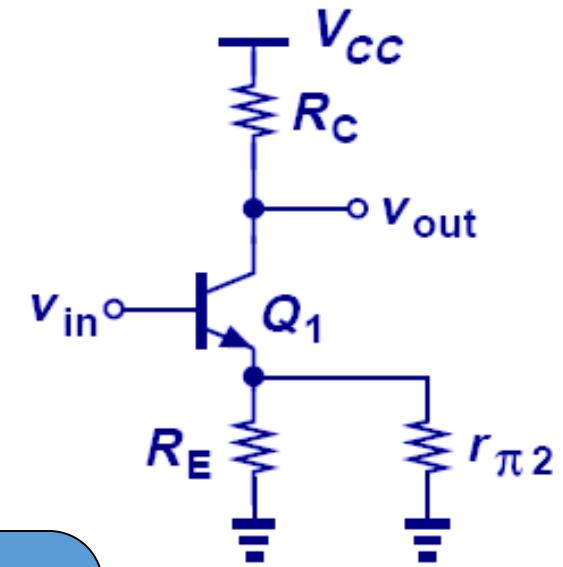
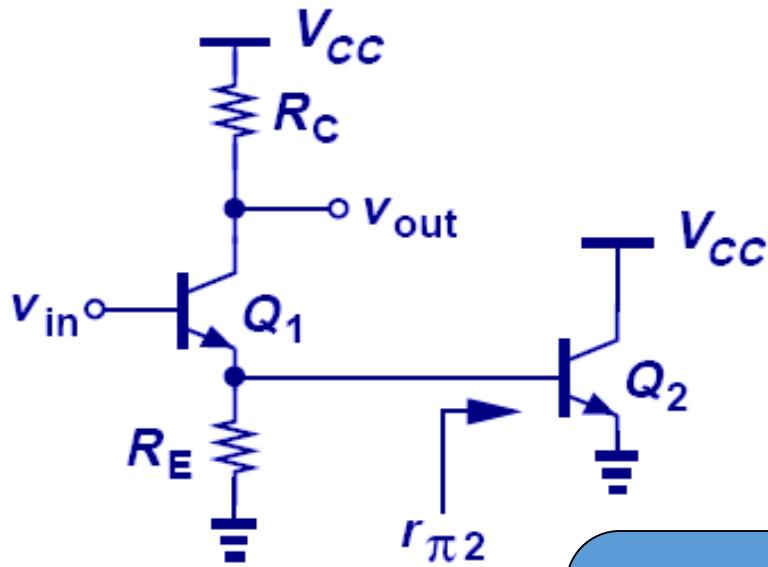
$$A_v = -\frac{g_m R_C}{1 + g_m R_E}$$
$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

Interestingly, this gain is equal to the total load resistance to ground divided by  $1/g_m$  plus the total resistance placed in series with the emitter.





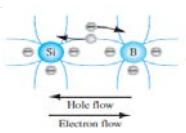
# Emitter Degeneration Example



$$A_v = -\frac{R_C}{\frac{1}{g_{m1}} + R_E \parallel r_{\pi 2}}$$

The input impedance of Q<sub>2</sub> can be combined in parallel with R<sub>E</sub> to yield an equivalent impedance that degenerates Q<sub>1</sub>.



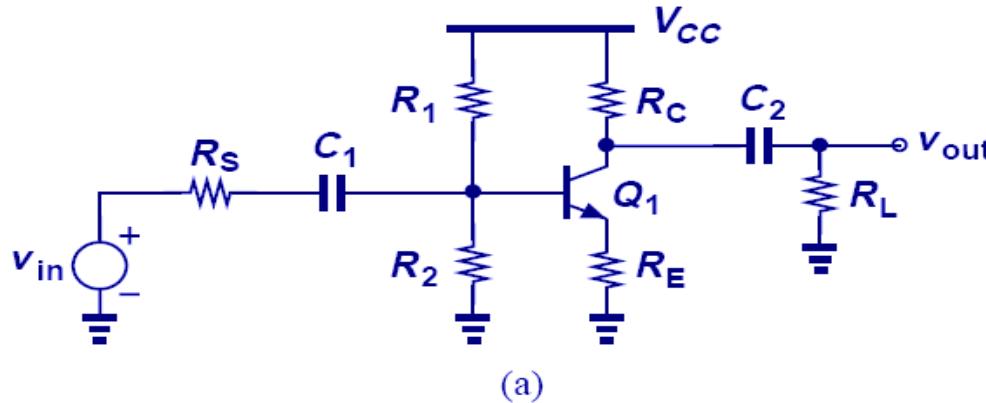


# SEMICONDUCTOR DEVICES

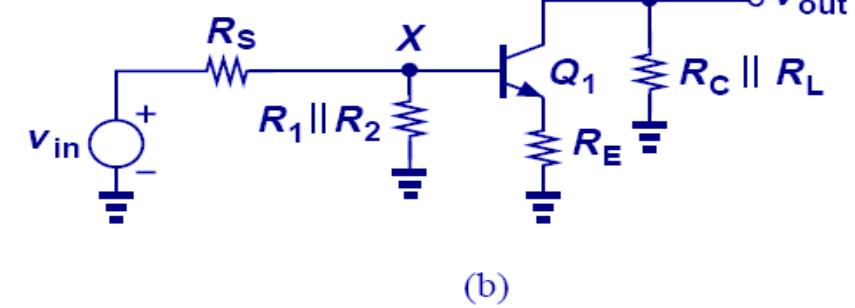
## DEPARTMENT OF COMPUTER ENGINEERING

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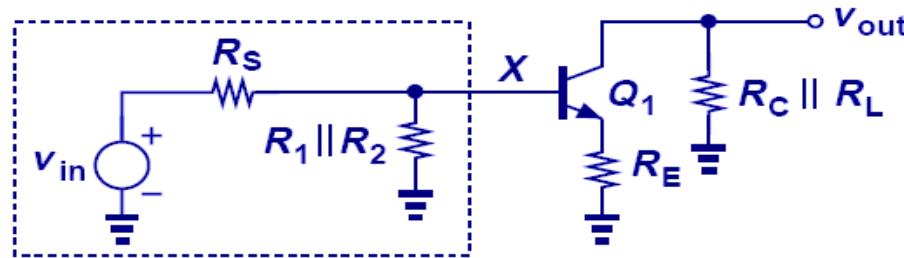
# Complete CE Stage



(a)



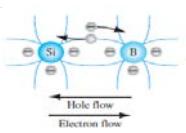
(b)



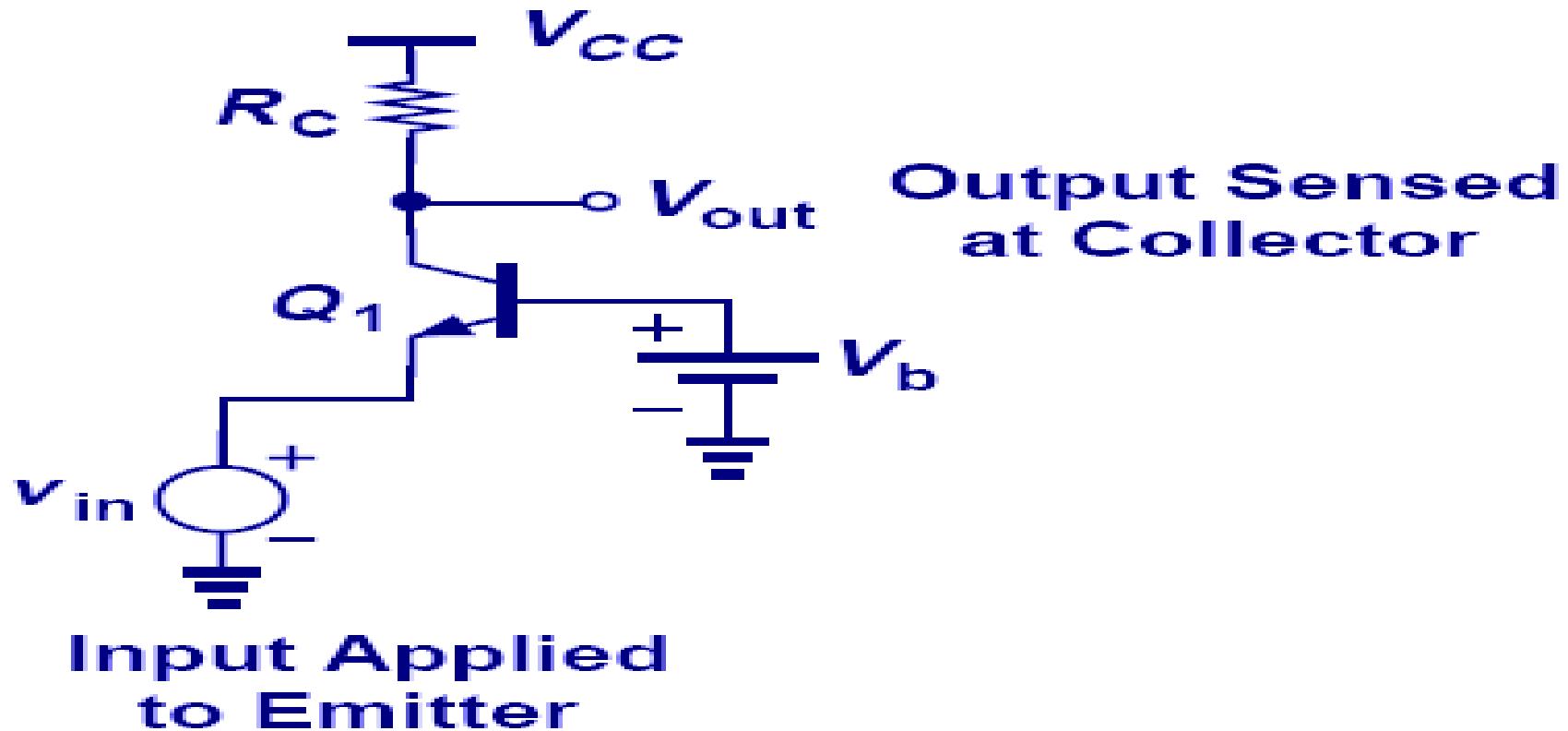
(b)

$$A_v = \frac{-R_C \parallel R_L}{g_m + R_E + \frac{R_s \parallel R_1 \parallel R_2}{\beta + 1}}$$



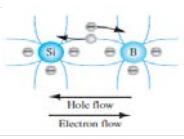


# Common Base (CB) Amplifier

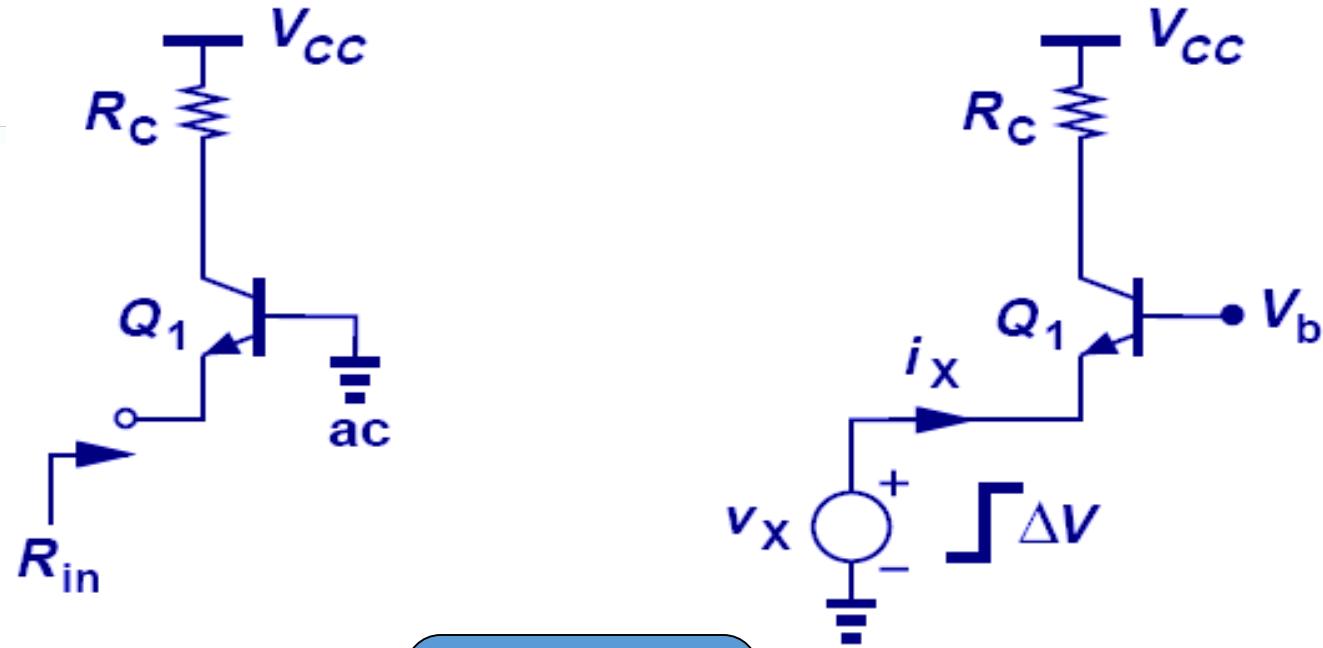


In common base topology, where the base terminal is biased with a fixed voltage, emitter is fed with a signal, and collector is the output.





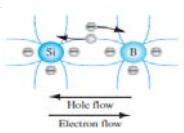
# Input Impedance of CB



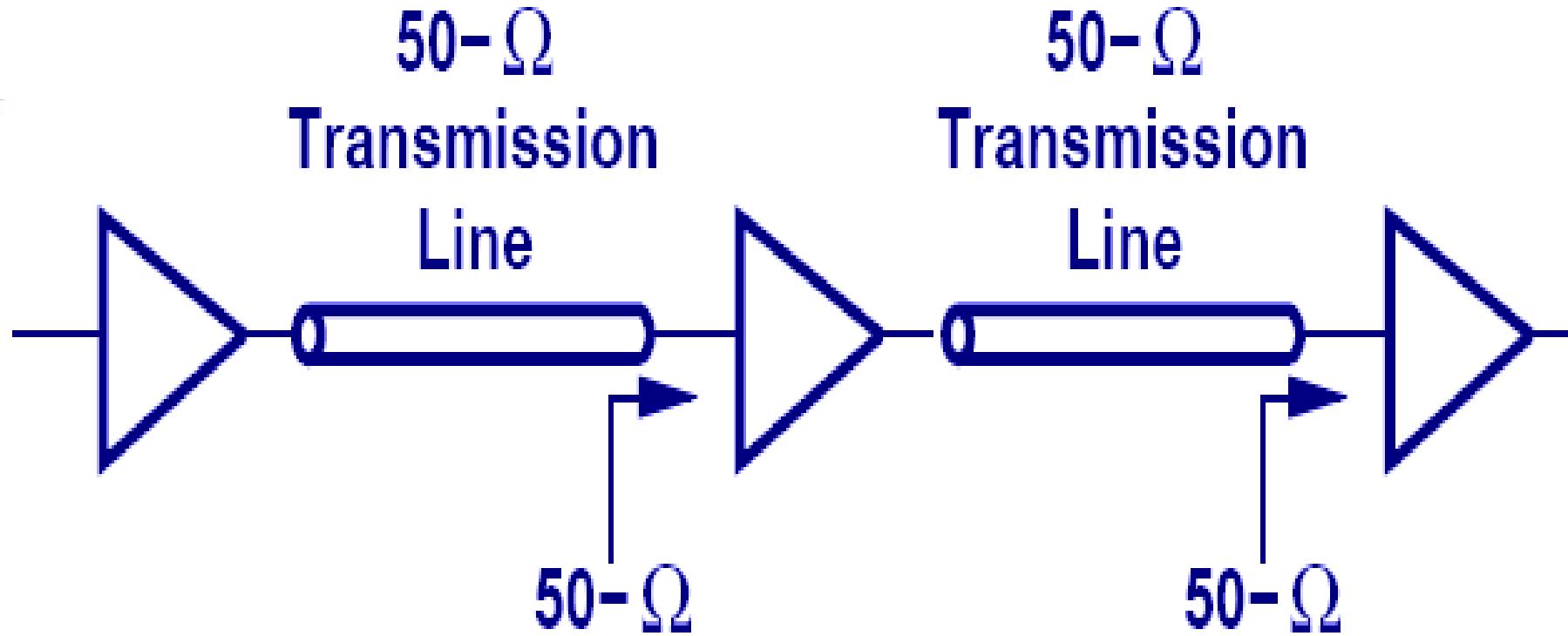
$$R_{in} = \frac{1}{g_m}$$

The input impedance of CB stage is much smaller than that of the CE stage.





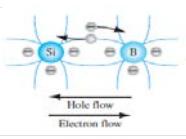
# Practical Application of CB Stage



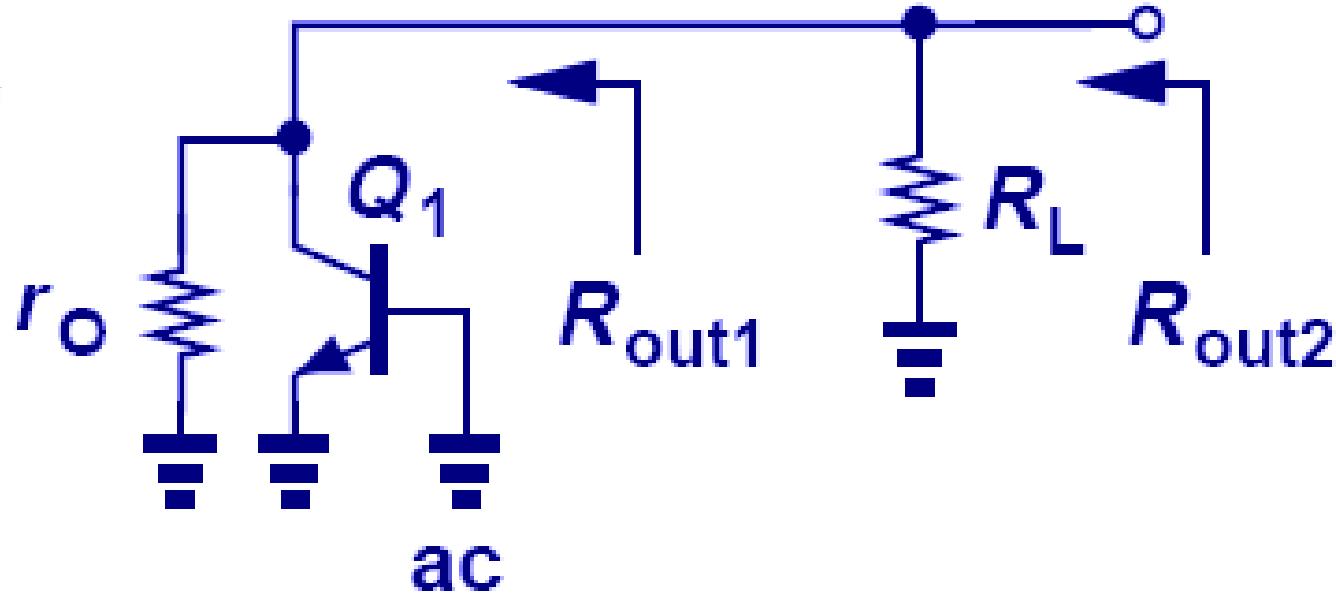
To avoid “reflections”, need impedance matching.

CB stage’s low input impedance can be used to create a match with  $50\ \Omega$ .





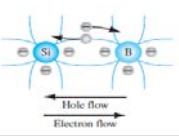
# Output Impedance of CB Stage



$$R_{out} = r_o \parallel R_C$$

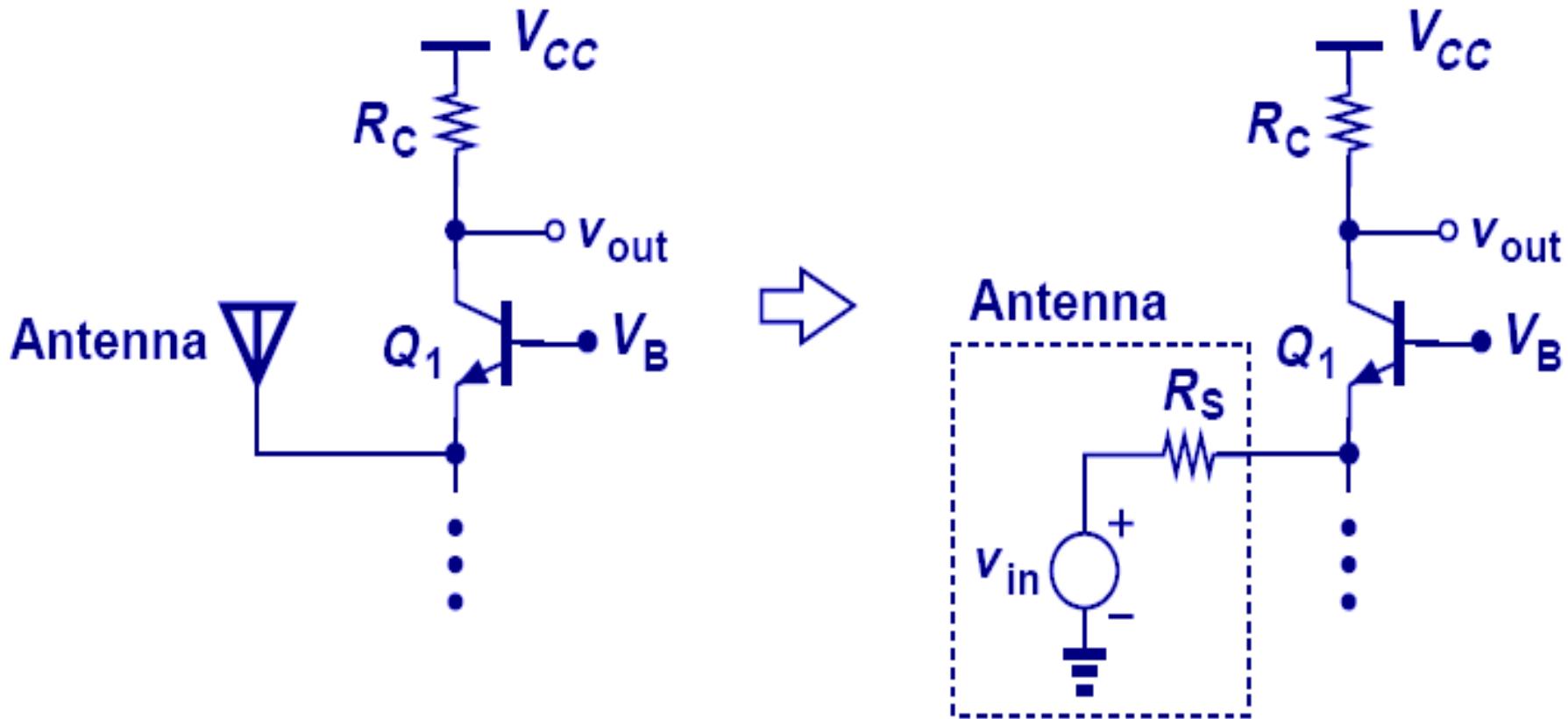
The output impedance of CB stage is similar to that of CE stage.

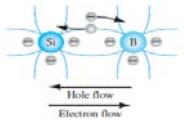




# Practical Example of CB Stage

An antenna usually has low output impedance; therefore, a correspondingly low input impedance is required for the following stage.





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# Thank You Very Much

Dipl.-Ing. B. Kommey

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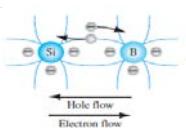
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

050 770 32 86

Whatsup: 0049 172 4444 765

Skype\_id: calculus.affairs





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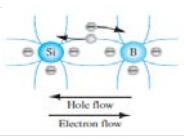
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“Technological change is like an axe in the hands of a pathological criminal”

**Albert Einstein**





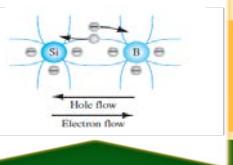
# Overview

## Field-Effect Transistor FET

**Junction Field-Effect  
Transistor JFET**

**Metal-Oxide  
Semiconductor MOSFET**





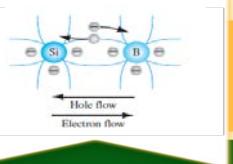
# Field-Effect Transistors FET

The field-effect transistor (FET) controls the current between two points but does so differently than the bipolar transistor.

The FET operates by the effects of an electric field on the flow of electrons through a single type of semiconductor material.

This is why the FET is sometimes called a unipolar transistor.





# Field-Effect Transistors FET

Current moves within the FET in a channel, from the source (**S**) connection to the drain (**D**) connection.

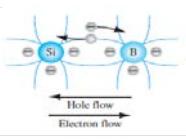
A gate (**G**) terminal generates an electric field that controls the current.

The channel is made of either **N-type** or **P-type** semiconductor material

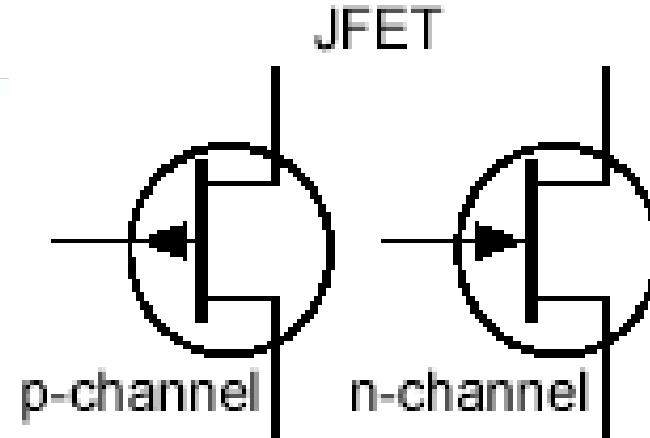
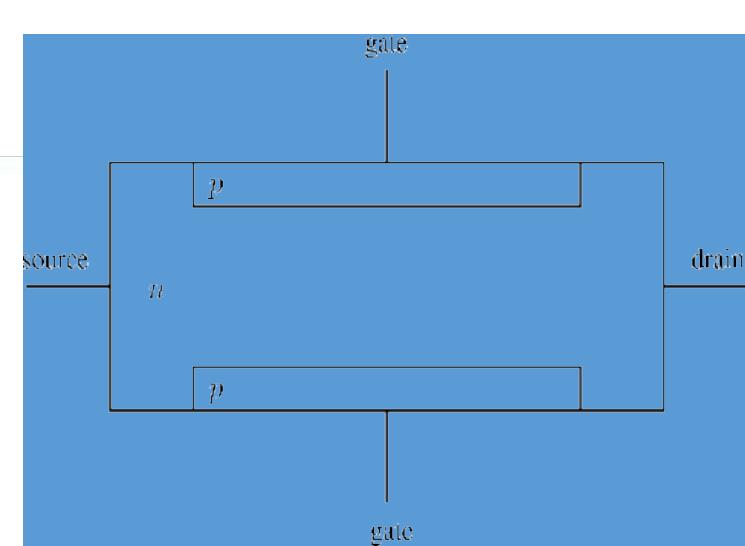
FET is specified as either an **N-channel** or **P-channel** device

Majority carriers flow from source to drain.



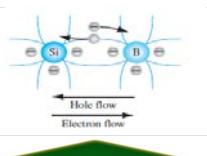


# Field-Effect Transistors FET

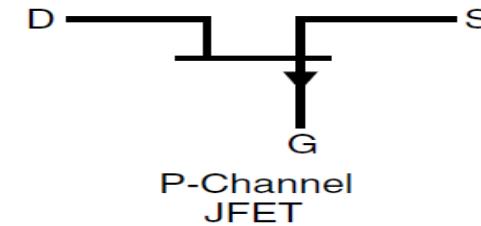
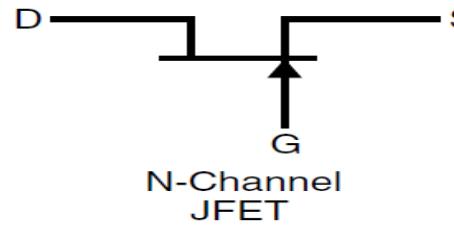
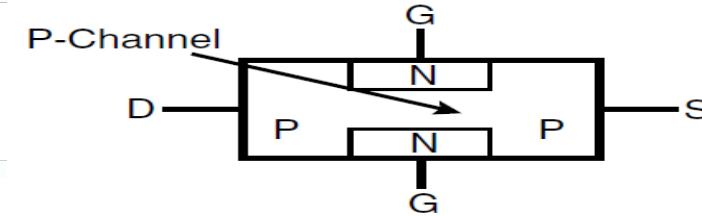
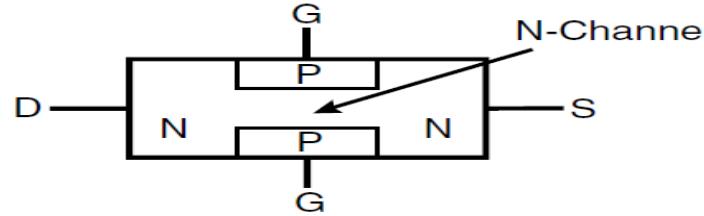


- In N-channel devices, electrons flow so the drain potential must be higher than that of the Source ( $V_{DS} > 0$ )
- In P-channel devices, the flow of holes requires that  $V_{DS} < 0$





# Field-Effect Transistors FET

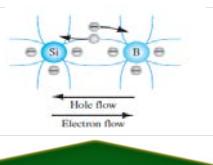


Like bipolar junction transistors, field-effect transistors (FETs) are three terminal semiconductor devices capable of power gain.

Qualitatively, they operate much like junction transistors, but they have much higher input impedance and lower transconductance and voltage gain.

Also, they have a larger variation in their ' $V_{BE}$ ' equivalent (called  $V_{GS}$ ) than bipolar transistors





# Field-Effect Transistors FET

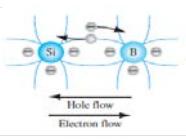
a conducting *channel* between the *drain* and *source* terminals is controlled by a voltage applied to the *gate* terminal.

The channel can be made of either N-type or P-type material.

N-channel is more common since the conductivity of N-type semiconductor (in which electrons carry the current) is higher than that of P-type (in which holes do)

The gate region of a JFET consists of material of opposite type to that of the channel; thus, the gate and channel form a diode



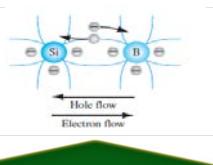


# Field-Effect Transistors FET

The transconductance of a JFET is proportional to  $\sqrt{I_D}$

$$g_m = \Delta I_D / \Delta V_{GS} .$$





# FET Advantages over BJT

Unipolar device i. e. operation depends on only one type of charge carriers ( $h$  or  $e$ )

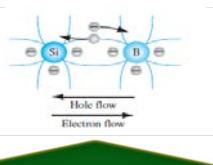
Voltage controlled Device (gate voltage controls drain current)

Very high input impedance ( $\approx 10^9$ - $10^{12} \Omega$ )

Source and drain are interchangeable in most Low-frequency applications

Low Voltage Low Current Operation is possible (Low-power consumption)





# FET Advantages over BJT

Less Noisy as Compared to BJT

No minority carrier storage (Turn off is faster)

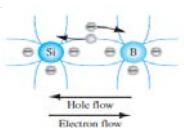
Self limiting device

Very small in size, occupies very small space in ICs

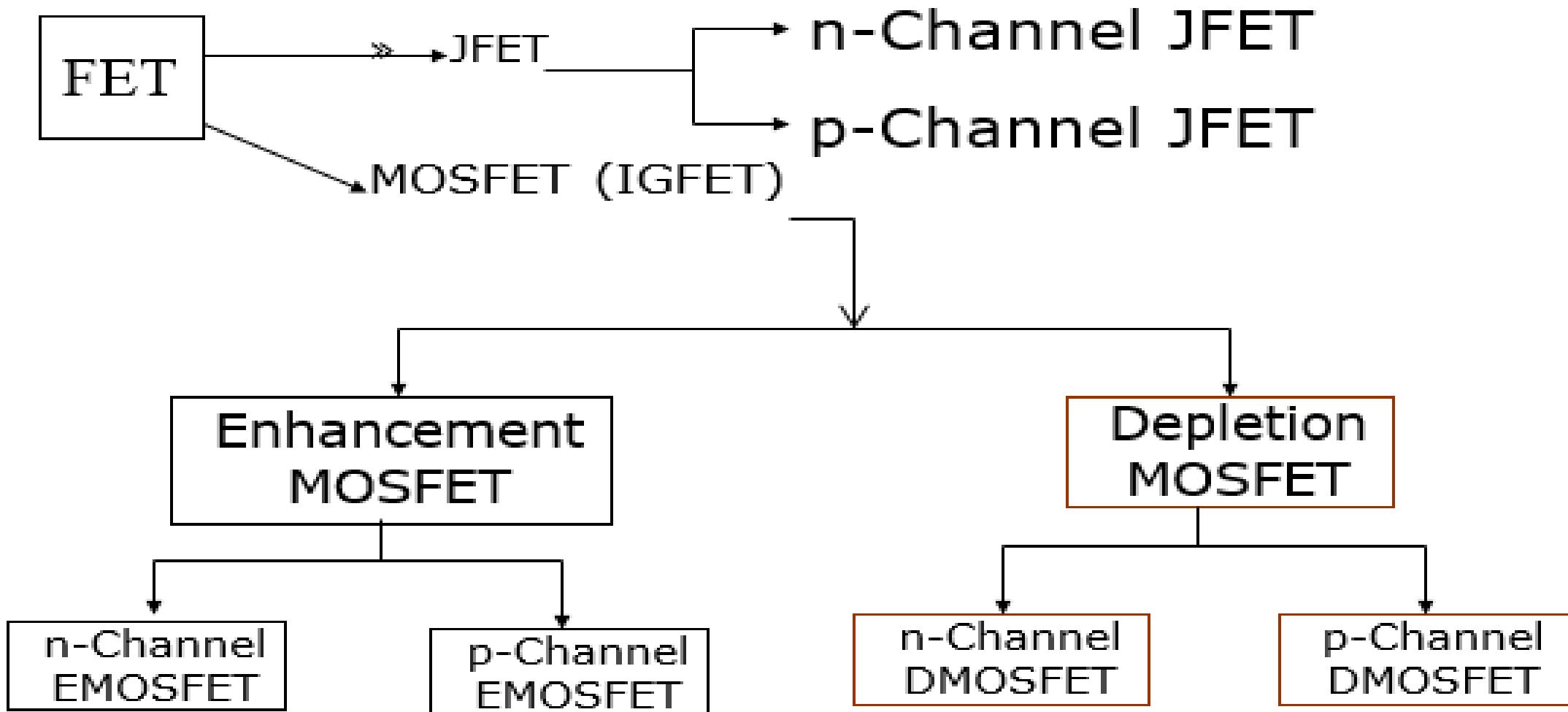
Low voltage low current operation is possible in MOSFETS

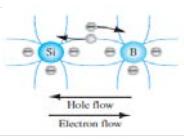
Zero temperature drift of output is possible



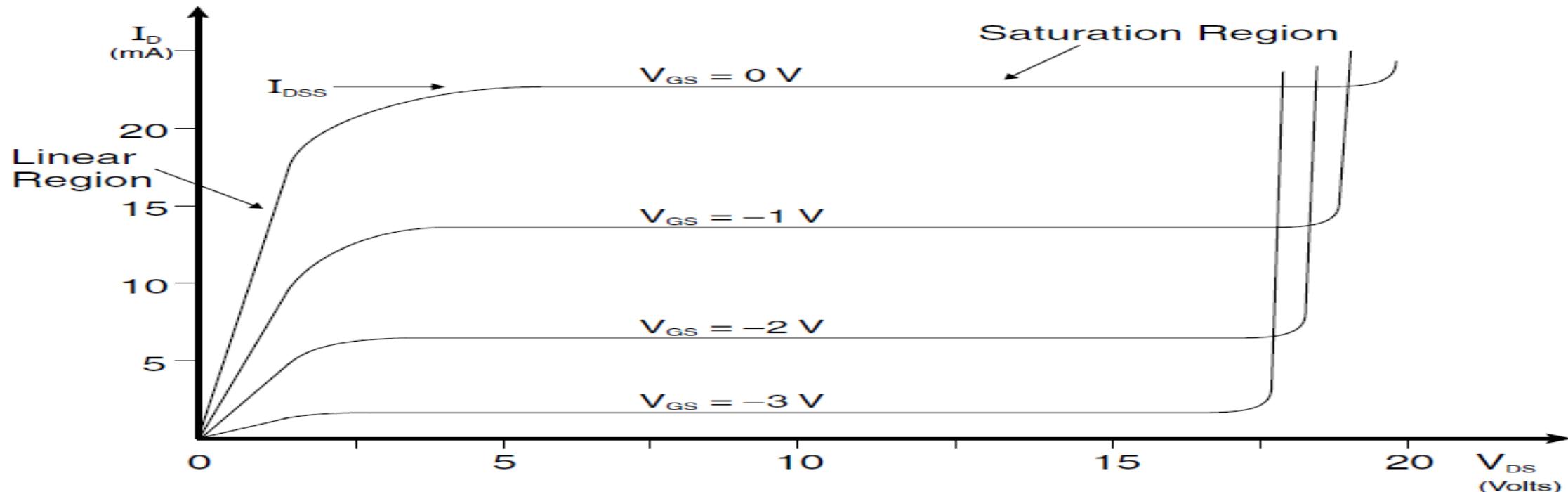


# Types of FET





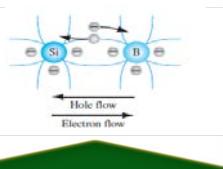
# Characteristics of JFET



The voltage-controlled current-source behavior occurs as long as the drain-source voltage  $V_{DS}$  is sufficiently high.

This is called the *saturation* region of the FET characteristic





# Characteristic of JFET

For  $V_{DS}$  smaller than a volt or two, a JFET behaves like a voltage controlled resistor rather than a current source,

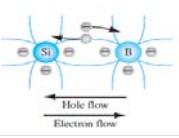
i.e. the *slope* of the  $I-V$  characteristic is controlled by the gate–source voltage.

This is the *linear* region of the FET characteristic, useful for automatic gain control (AGC) and modulation applications

For FETs operated in the saturation region, the relationship is quadratic:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$
 where  $V_p$  is the pinch-off voltage and  $I_{DSS}$  is the saturation drain current for  $V_{GS} = 0$  (i.e. gate shorted to source).





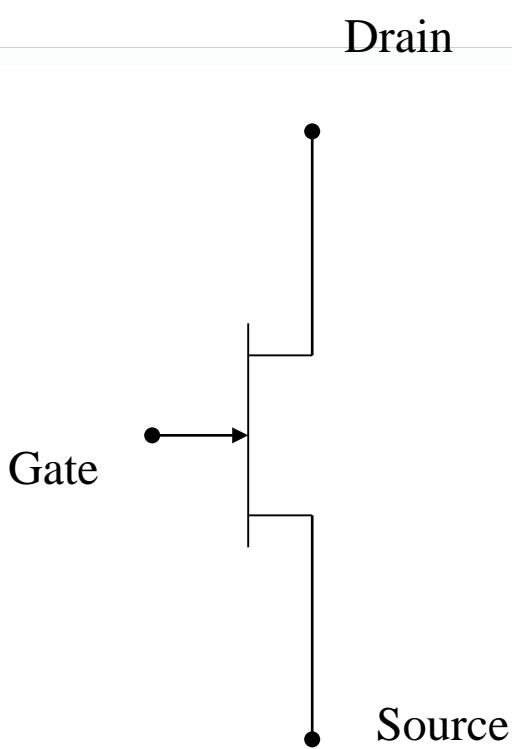
# SEMICONDUCTOR DEVICES

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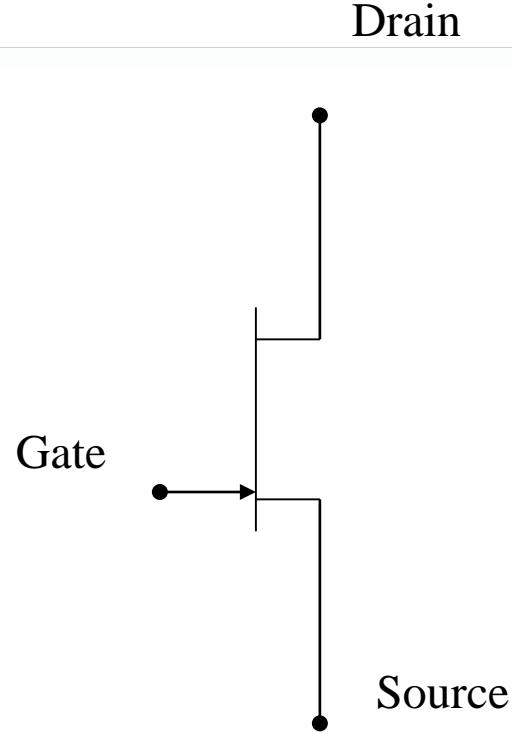
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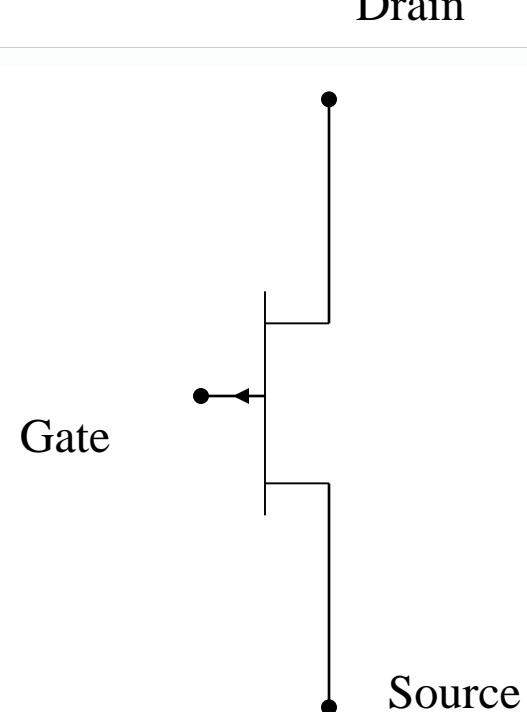
# JFET Symbols



n-channel JFET

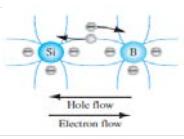


n-channel JFET  
Offset-gate symbol



p-channel JFET





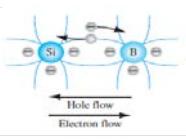
# Operation Regions of JFET

## Ohmic Region

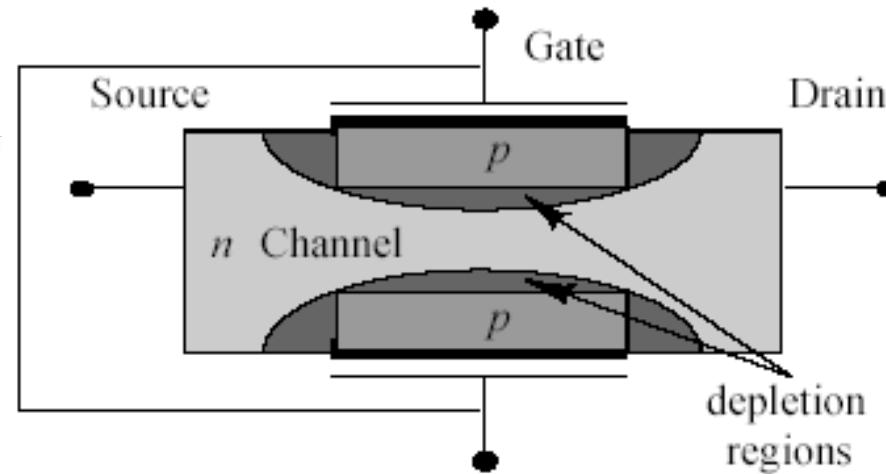
## Saturation Region

## Breakdown Region





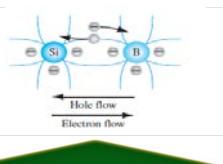
# JFET- Ohmic Region



Ohmic Region - the depletion regions that form around the gate section (for small drain-source voltages)

These regions widen as gate voltage increases and thus the channel narrows



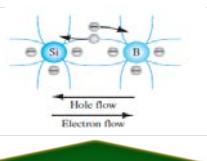


## JFET- Ohmic Region

As the gate-source voltage is increased above  $-V_p$  for small values of the drain-source voltage, the pn-junction between gate and channel becomes more reverse biased and the width of the depletion region increases, narrowing the channel

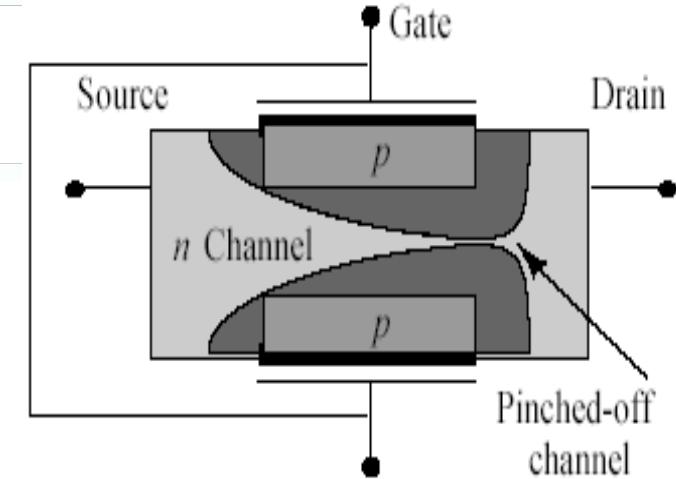
This increases the channel resistance, giving the voltage-controlled resistor behaviour of the ohmic region





# JFET – Saturation Region

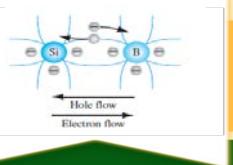
As the drain-source voltage is increased, the depletion regions further widen near the drain end and the channel becomes narrower, because the reverse bias of the pn junction is larger near the drain



For sufficiently large drain-source voltage, the channel will eventually be **pinched off** and any further increase in  $V_{DS}$  will not change the drain current.

This is the saturation region





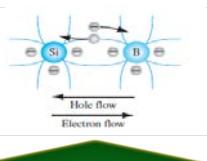
# JFET – Breakdown Region

When the drain-source voltage increase above a breakdown voltage,  $V_B$ , the drain current will increase very quickly due to avalanche condition

This causes excessive generation of heat and the destruction of the JFET

This is the **breakdown** region





## JFET Equations

The following equations describe the operation of n-channel JFETs. They also apply for p-channel JFETs by substituting  $V_{SG}$  for  $V_{GS}$  and  $V_{SD}$  for  $V_{DS}$

Cut – off region :  $V_{GS} < -V_P$       Breakdown region :  $V_{DS} > V_B$

Ohmic region :  $V_{DS} < 0.25(V_{GS} + V_P)$ ,  $V_{GS} > -V_P$

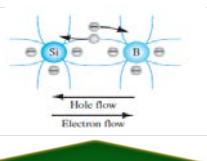
$$R_{DS} = \frac{V_P^2}{2I_{DSS}(V_{GS} + V_P)} \quad (\text{equivalent drain - to - source resistance})$$

$$i_D = \frac{V_{DS}}{R_{DS}}$$

Saturation region :  $V_{DS} \geq V_{GS} + V_P$ ,  $V_{GS} > -V_P$

$$i_D = \frac{I_{DSS}}{V_P^2} (V_{GS} + V_P)^2$$





# Applications of JFET

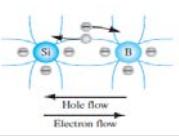
## MOSFET

-Primary component in high-density VLSI chips such as memories and microprocessors

## JFET

-Finds application especially in analog and RF circuit design





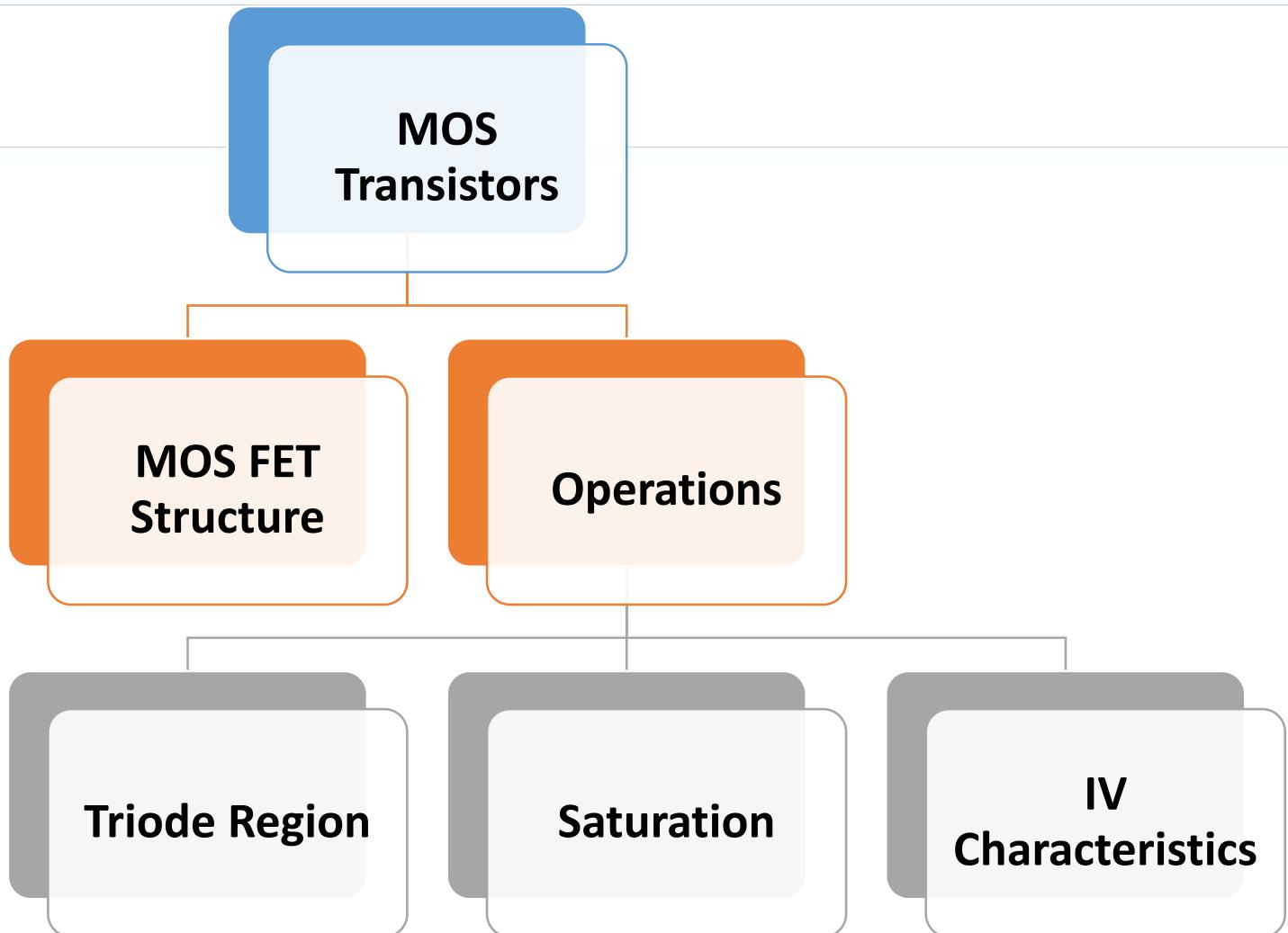
# SEMICONDUCTOR DEVICES

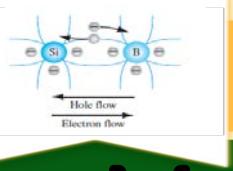
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# Overview

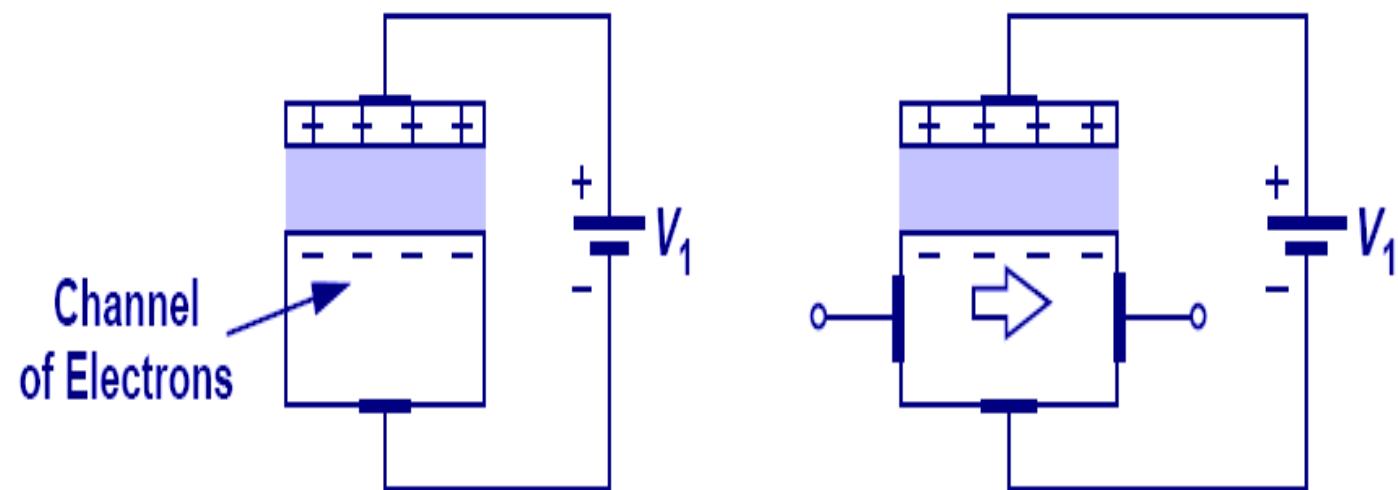
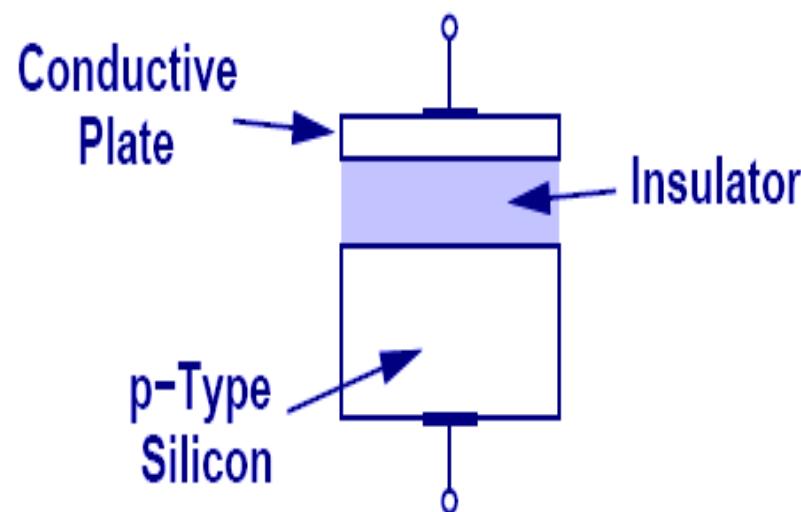


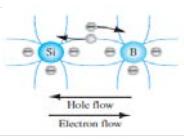


# Metal-Oxide-Semiconductor (MOS) Capacitor

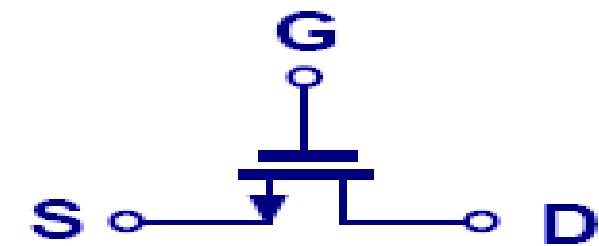
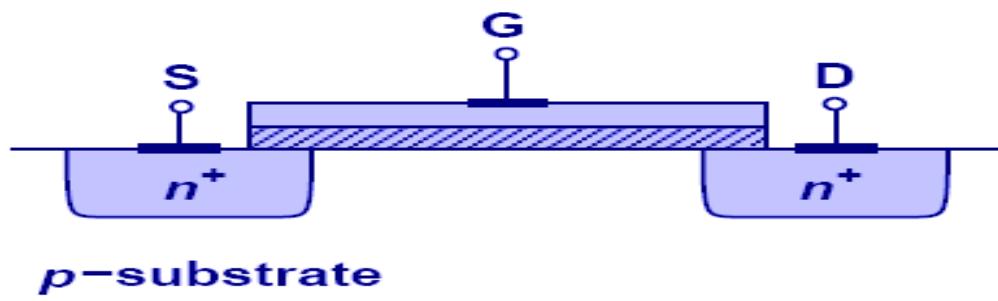
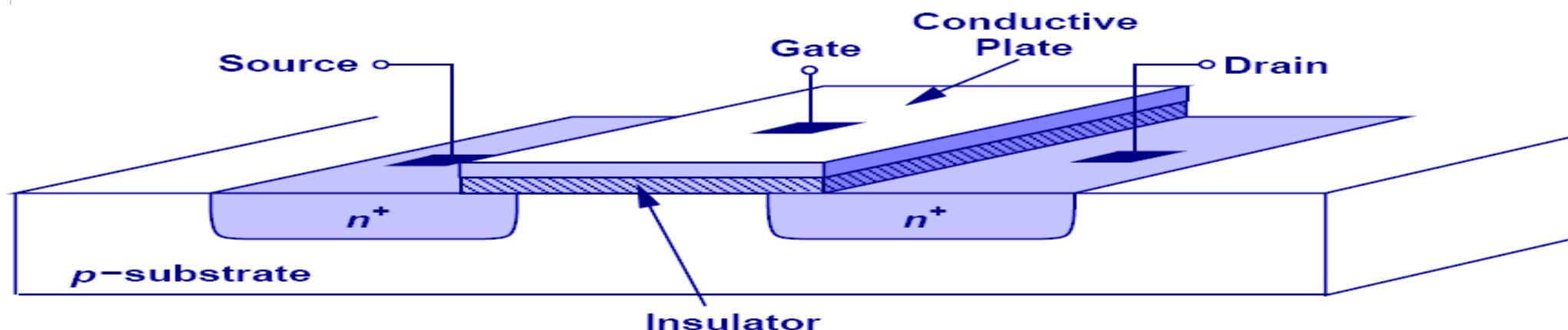
The MOS structure can be thought of as a parallel-plate capacitor, with the top plate being the positive plate, oxide being the dielectric, and Si substrate being the negative plate.

(We are assuming P-substrate.)



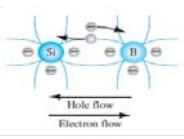


# Structure and Symbol of MOSFET

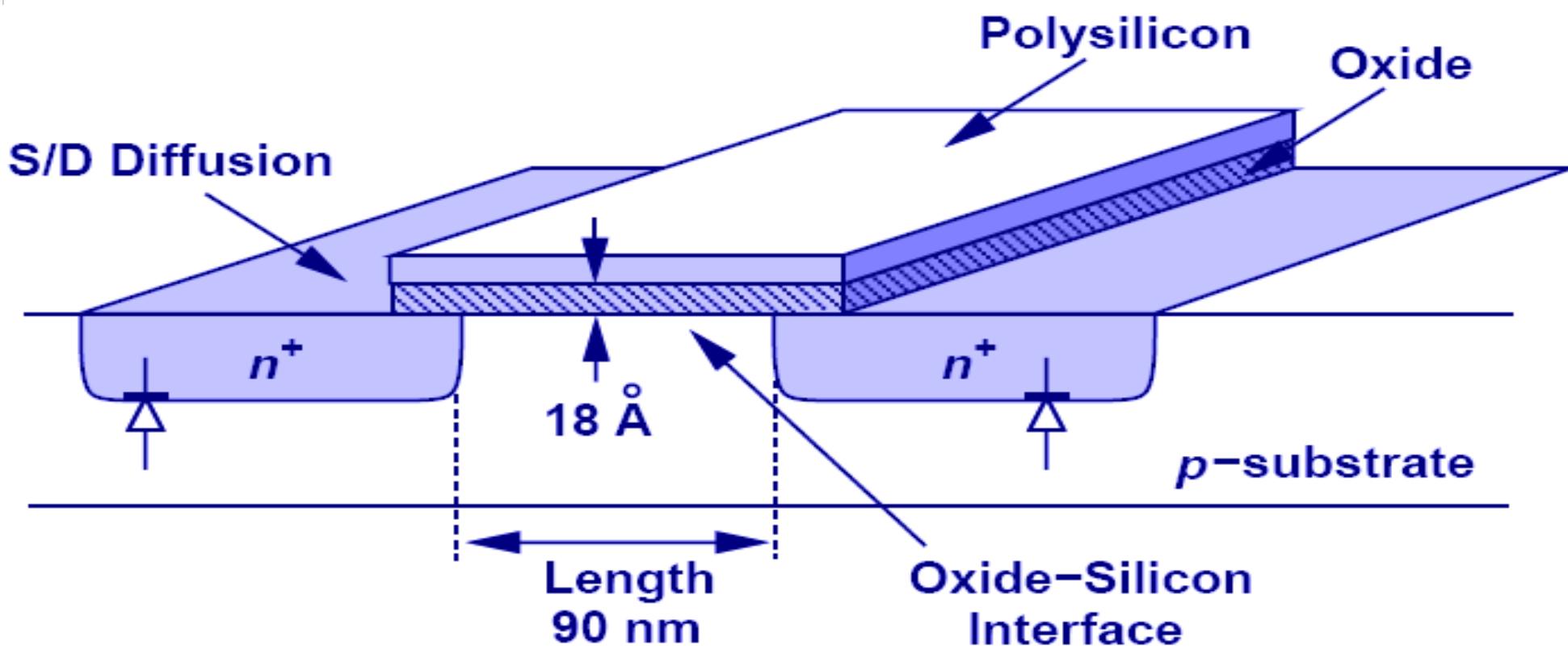


This device is symmetric,  
so either of the n+ regions can be source or drain.



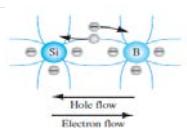


# State of the Art MOSFET Structure



The gate is formed by poly-silicon, and the insulator by Silicon dioxide.





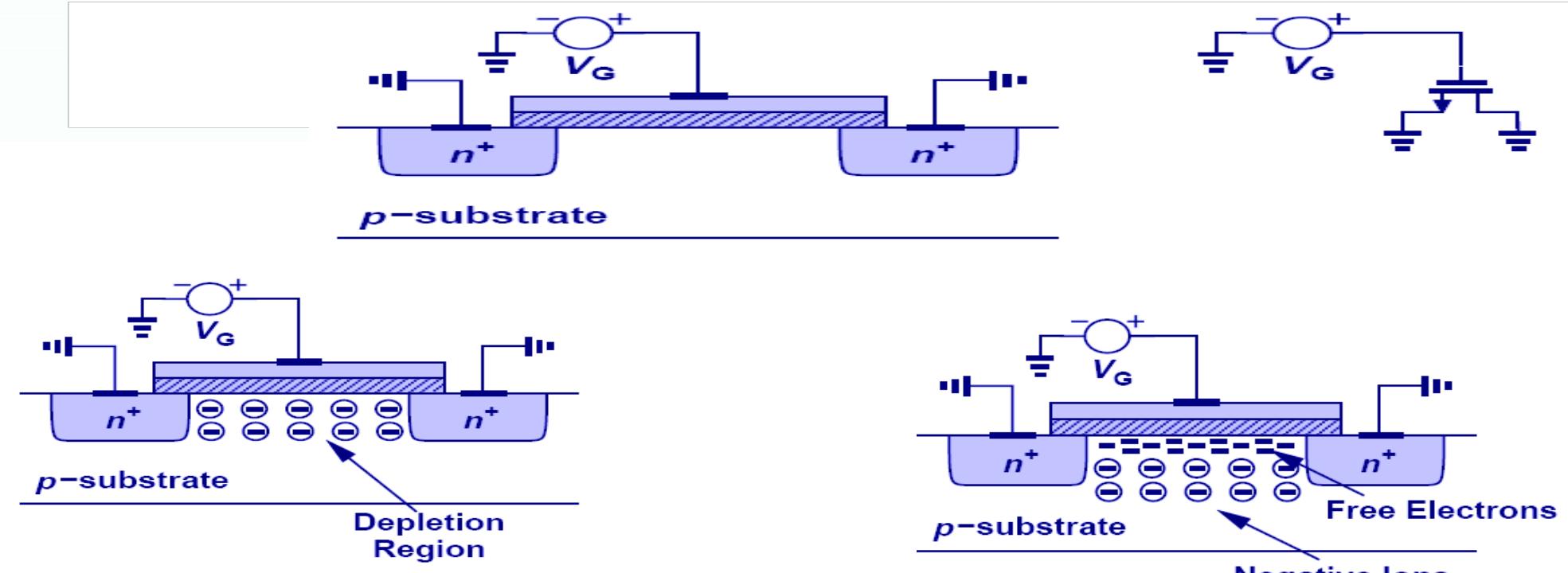
# SEMICONDUCTOR DEVICES

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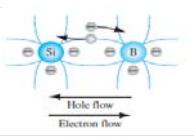
# Formation of Channel



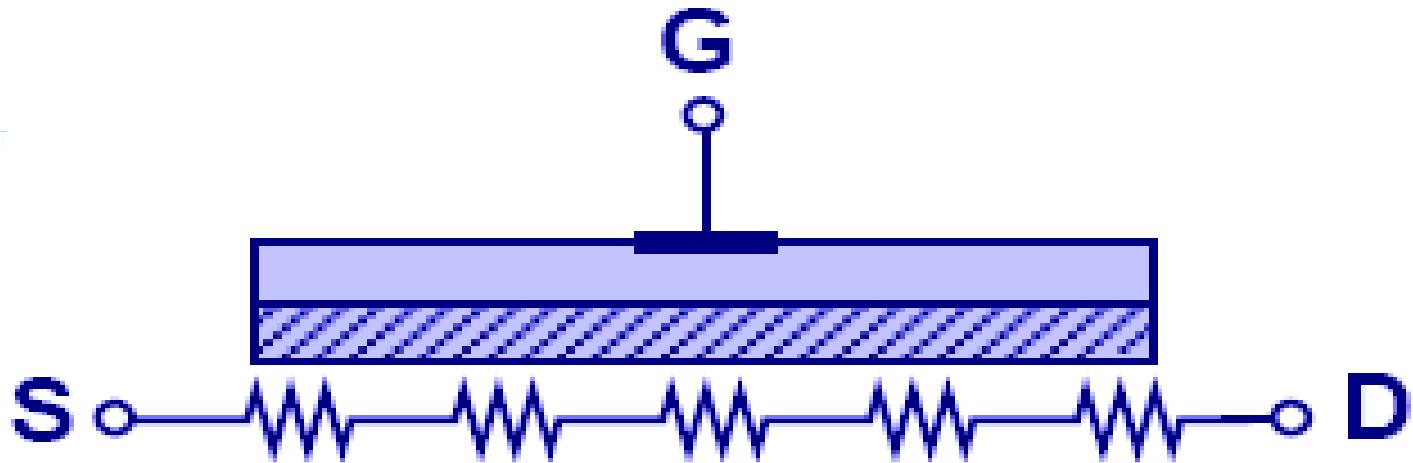
First, the holes are repelled by the positive gate voltage, leaving behind negative ions and forming a depletion region.

Next, electrons are attracted to the interface, creating a channel (“inversion layer”).





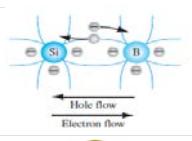
# Voltage-Dependent Resistor



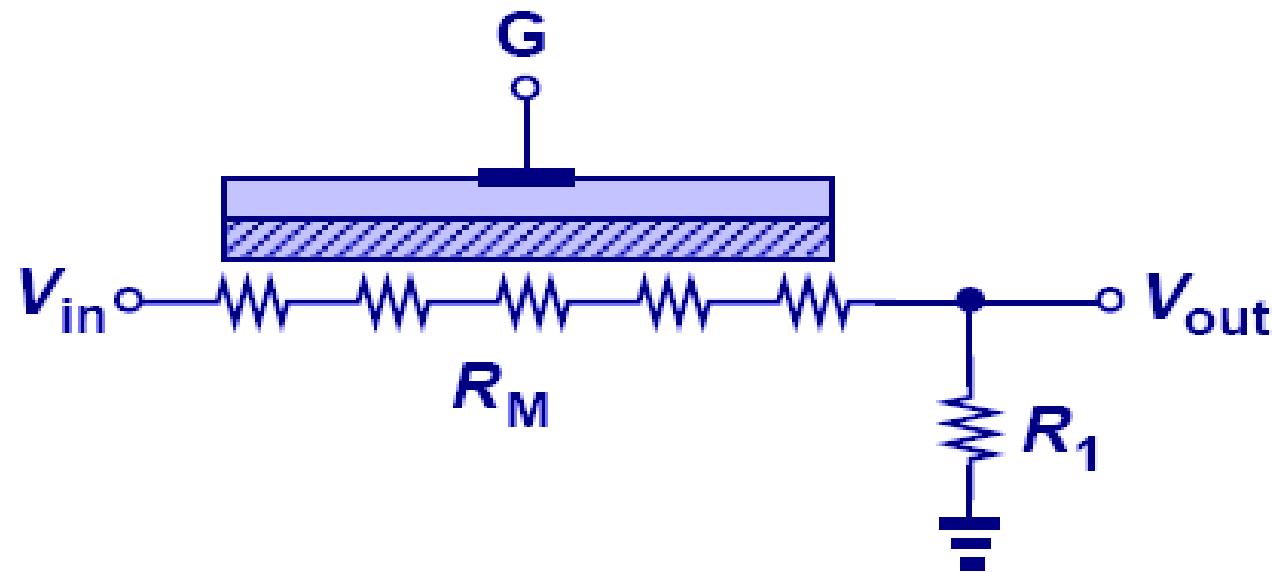
The inversion channel of a MOSFET can be seen as a resistor.

Since the charge density inside the channel depends on the gate voltage, this resistance is also voltage-dependent.





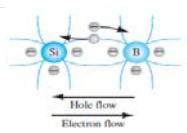
# Voltage-Controlled Attenuator



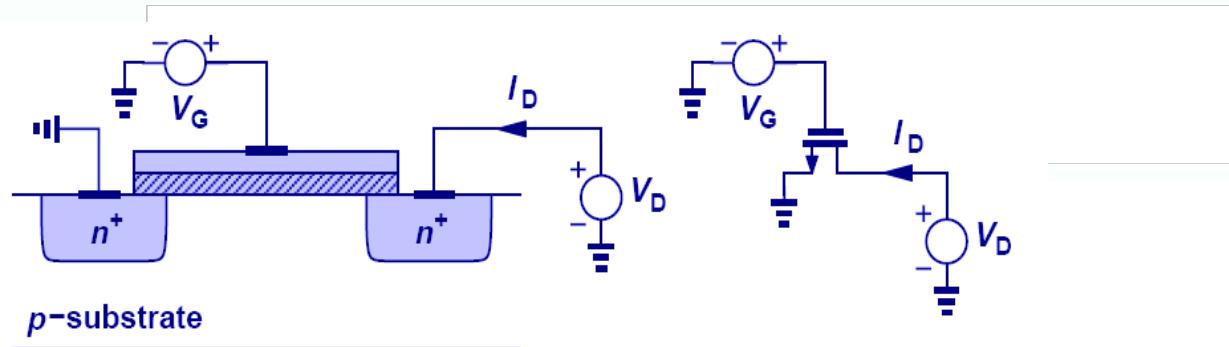
As the gate voltage decreases, the output drops because the channel resistance increases.

This type of gain control finds application in cell phones to avoid saturation near base stations.

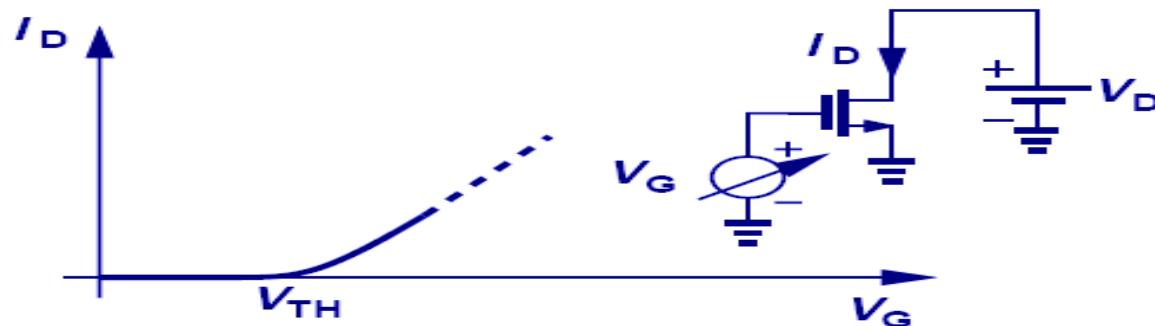




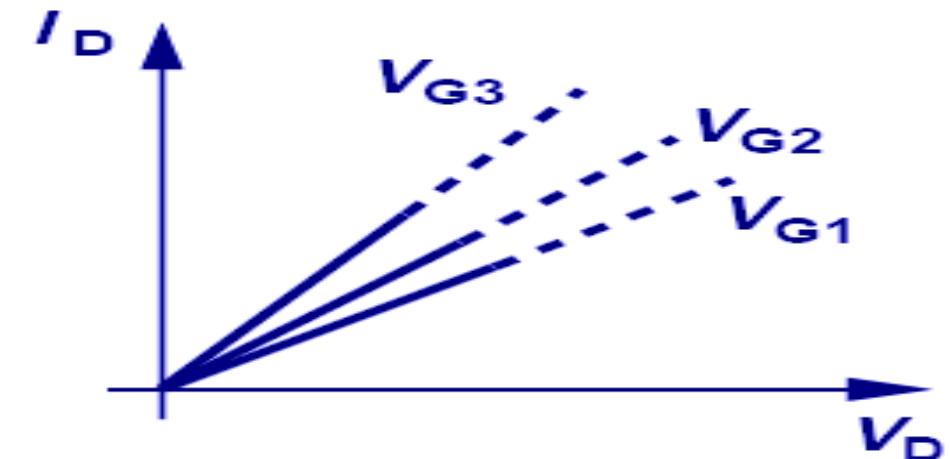
# MOSFET Characteristics



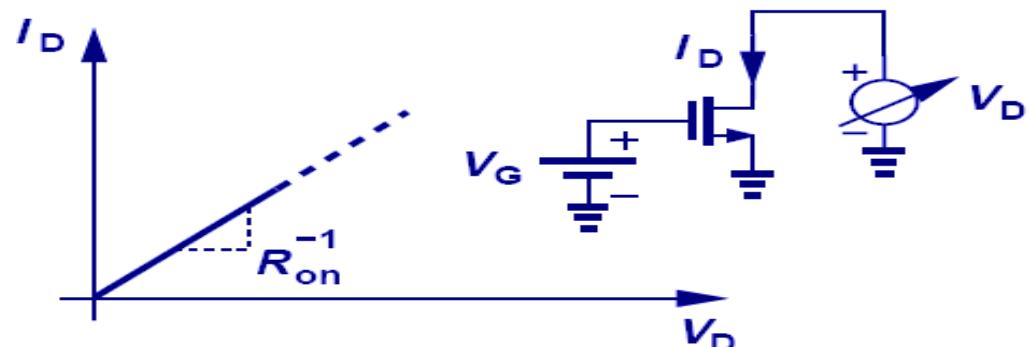
The MOS characteristics are measured by varying  $V_G$  while keeping  $V_D$  constant,

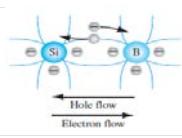


and varying  $V_D$  while keeping  $V_G$  constant.



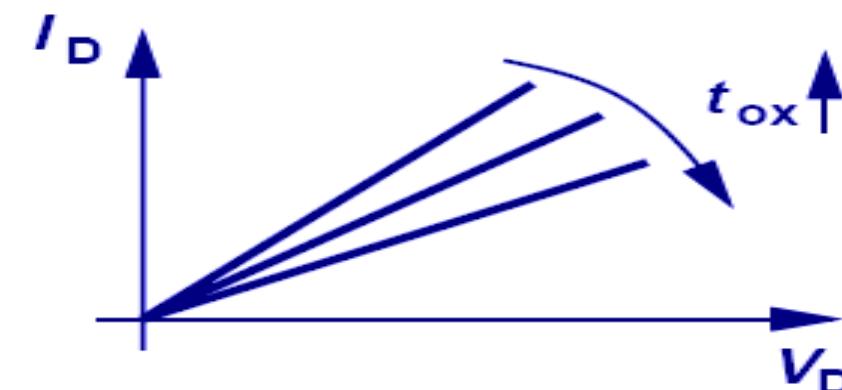
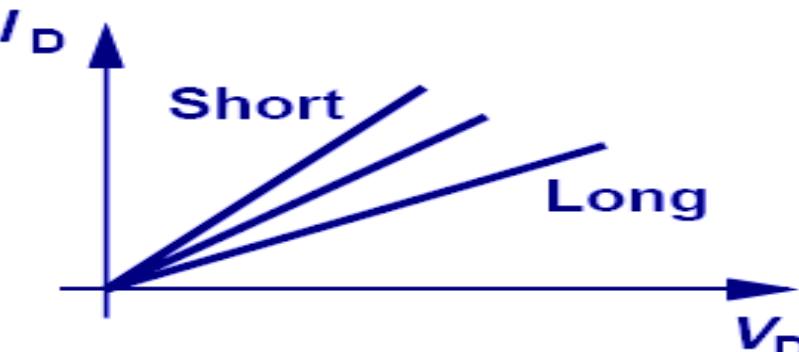
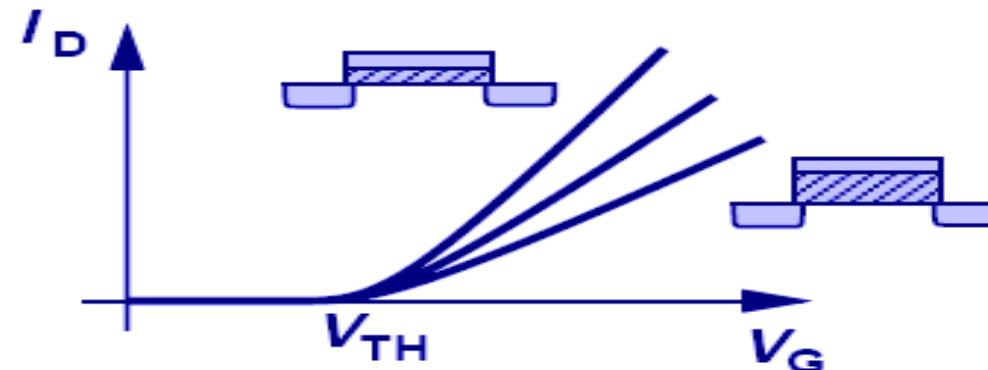
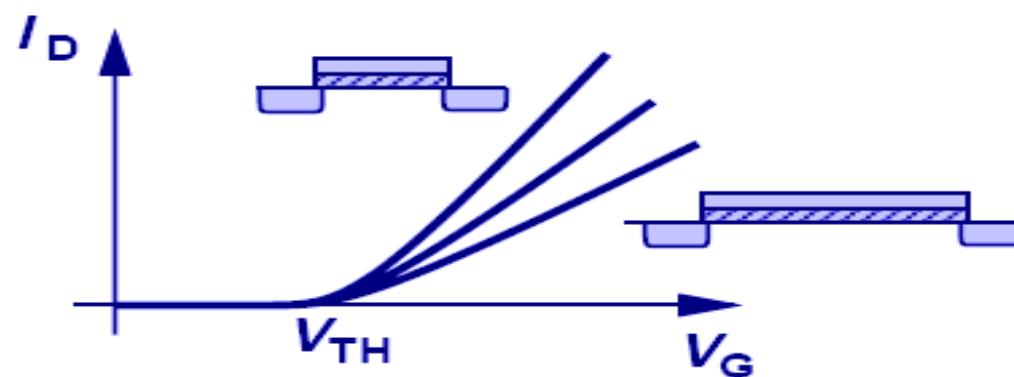
the voltage dependence of channel resistance

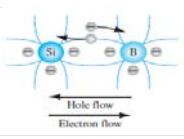




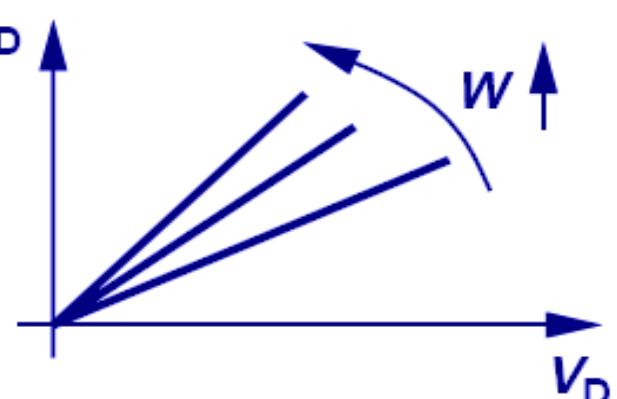
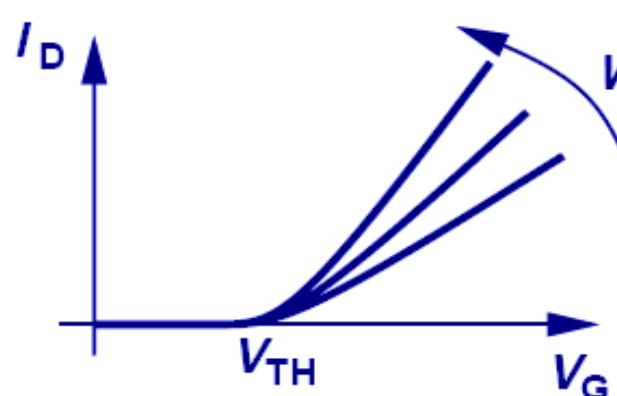
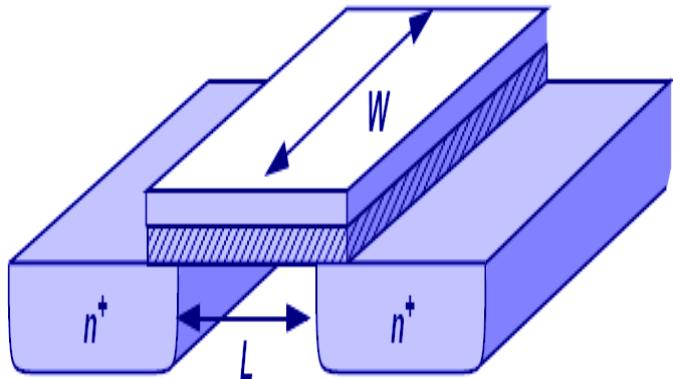
# Gate Length L and Oxide Thickness $t_{ox}$ Dependence

Small gate length L and oxide thickness  $t_{ox}$  yield low channel resistance, which will increase the drain current.





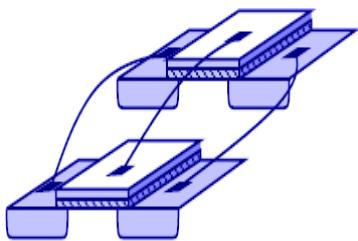
# Effect of Width (W)

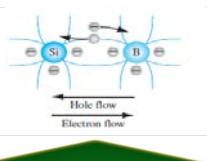


As the gate width  $W$  increases, the current increases due to a decrease in resistance.

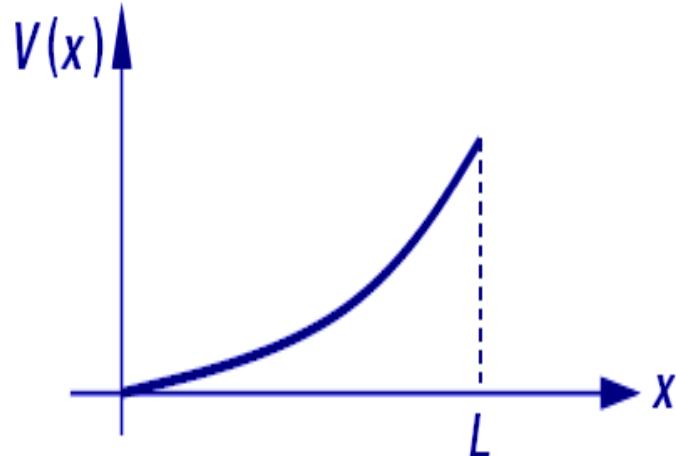
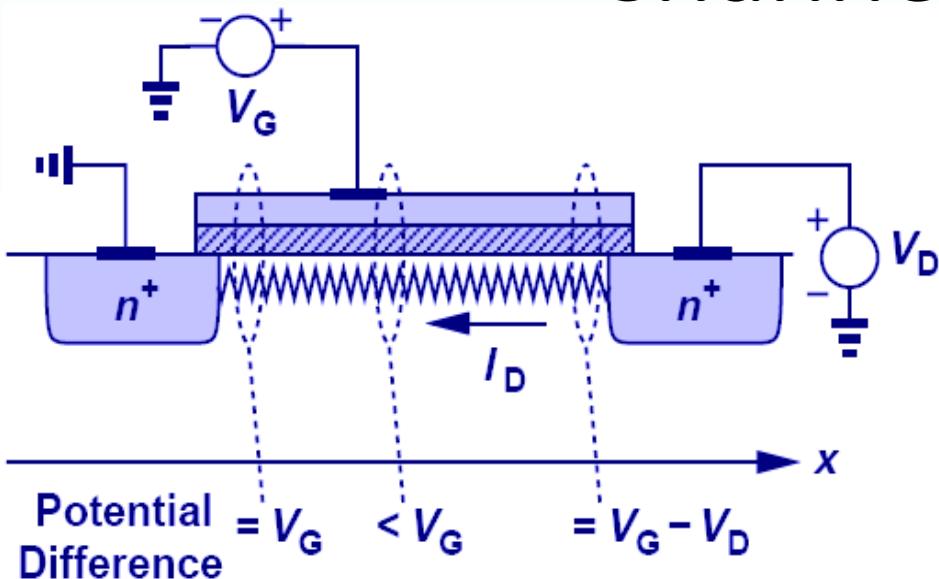
However, gate capacitance also increases thus, limiting the speed of the circuit.

An increase in  $W$  can be seen as two devices in parallel.

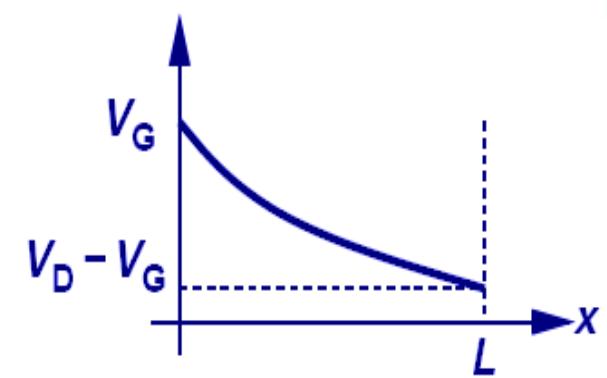




# Channel Potential Variation

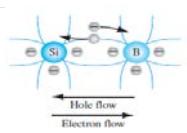


Gate-Substrate  
Potential Difference

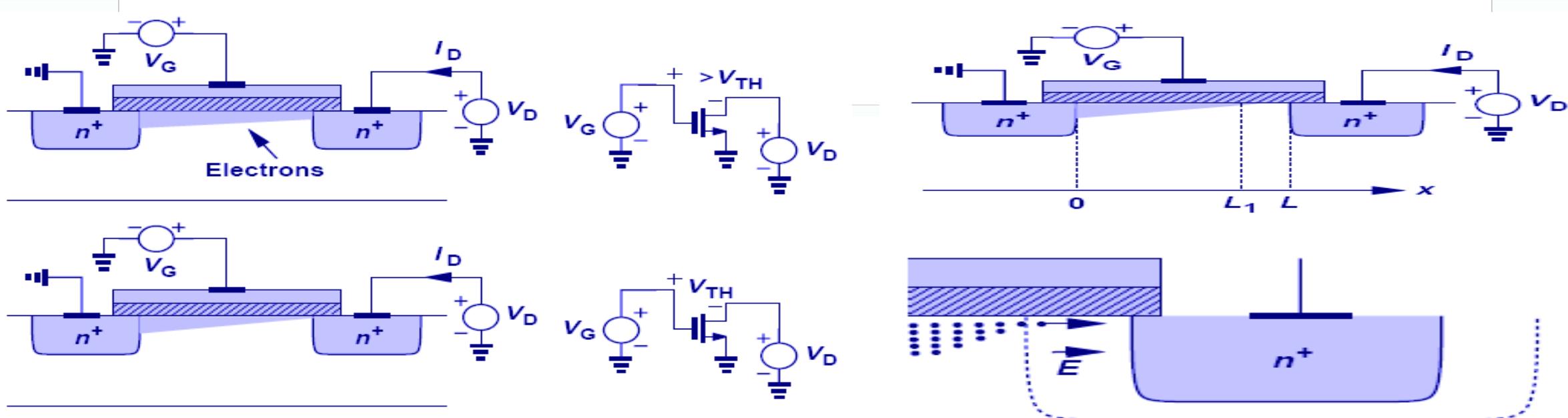


Since there's a channel resistance between drain and source, and if drain is biased higher than the source, channel potential increases from source to drain, and the potential between gate and channel will decrease from source to drain.





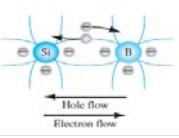
# Channel Pinch-Off



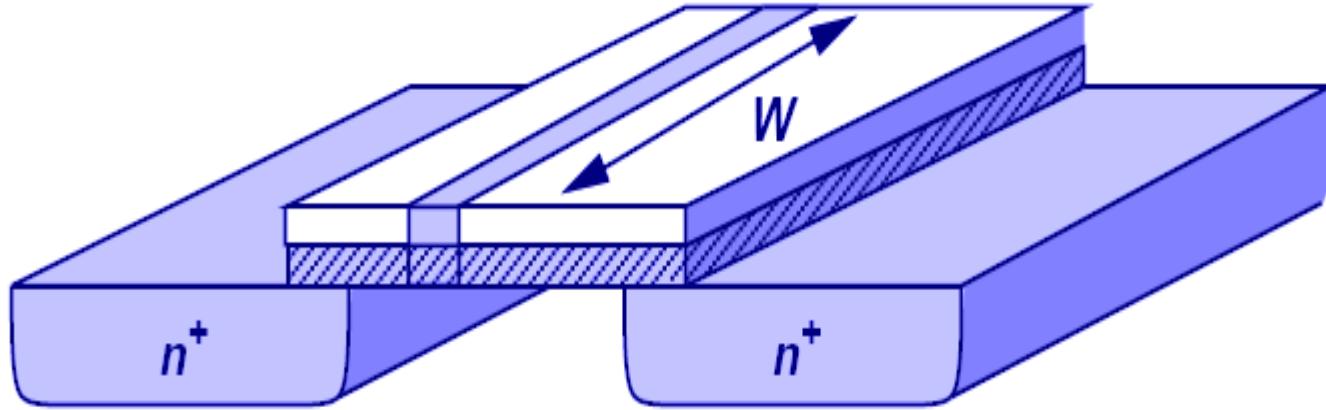
As the potential difference between drain and gate becomes more positive, the inversion layer beneath the interface starts to pinch off around drain.

When  $V_D - V_G = V_{th}$ , the channel at drain totally pinches off, and when  $V_D - V_G > V_{th}$ , the channel length starts to decrease.





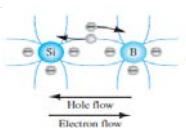
# Channel Charge Density



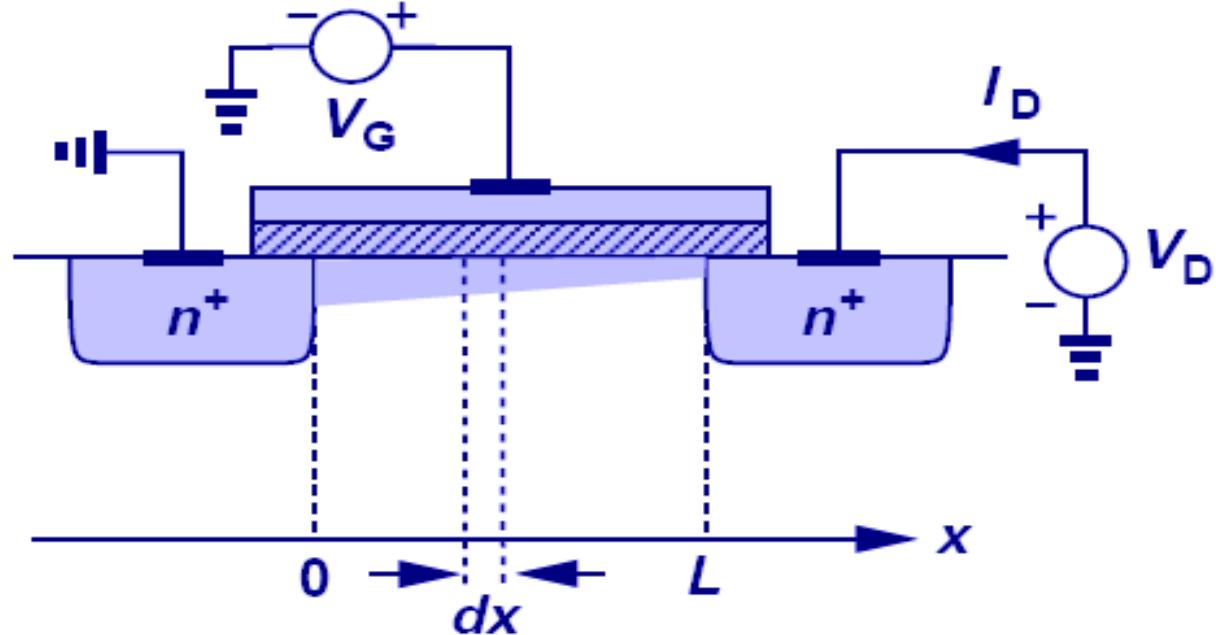
$$Q = WC_{ox} (V_{GS} - V_{TH})$$

The channel charge density is equal to the gate capacitance times the gate voltage in excess of the threshold voltage.





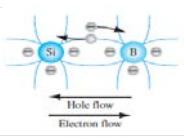
# Charge Density at a Point



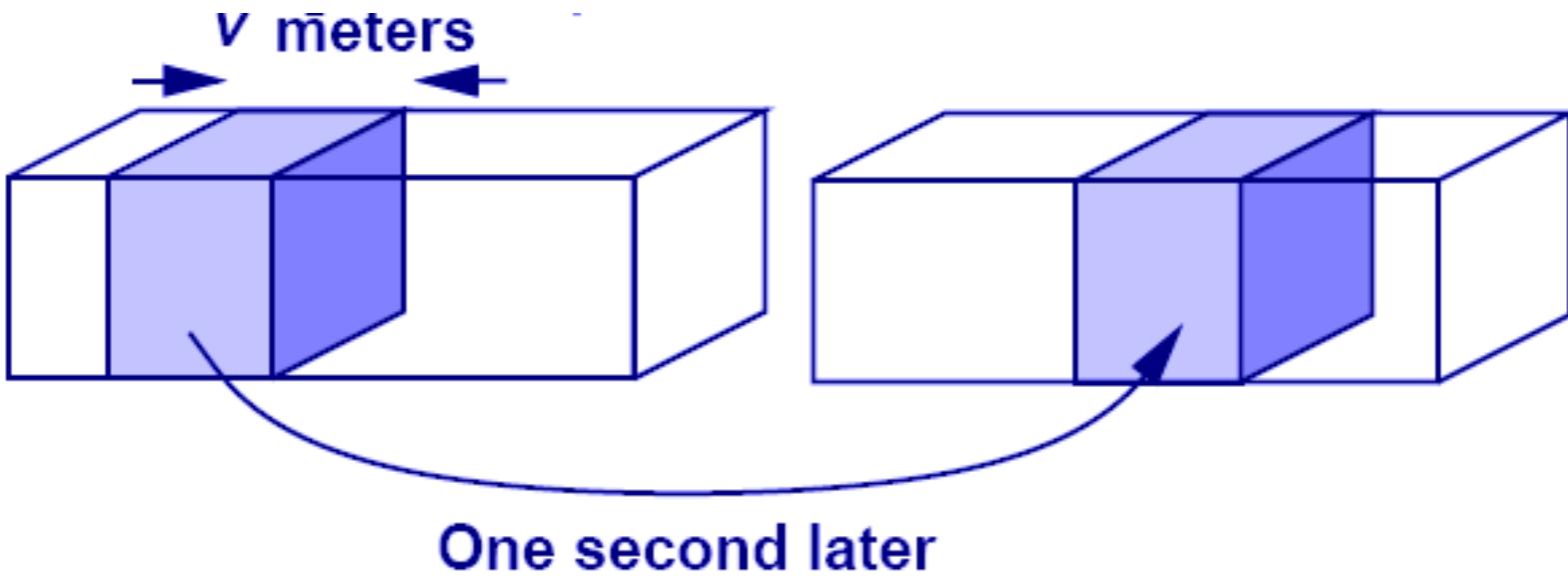
$$Q(x) = WC_{ox} [V_{GS} - V(x) - V_{TH}]$$

Let  $x$  be a point along the channel from source to drain, and  $V(x)$  its potential; the expression above gives the charge density (per unit length).





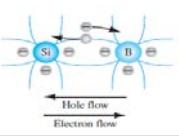
# Charge Density and Current



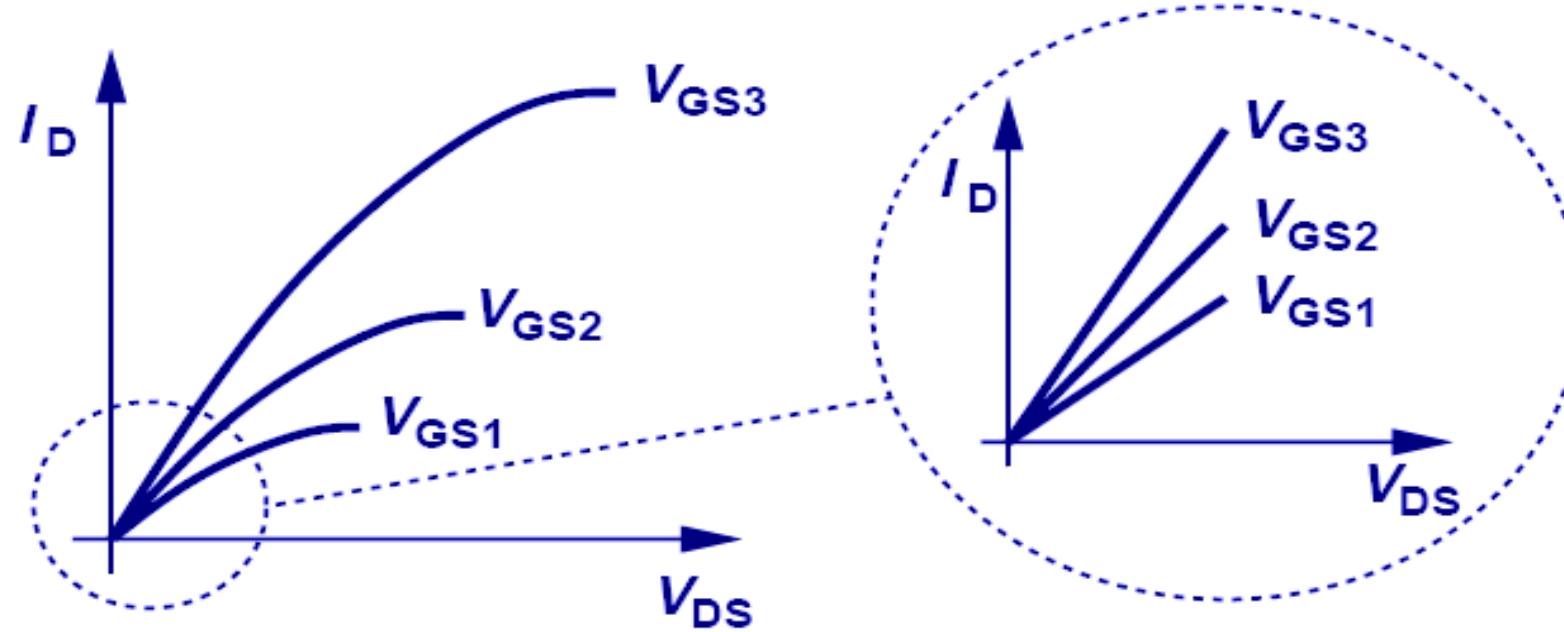
$$I = Q \cdot v$$

The current that flows from source to drain (electrons) is related to the charge density in the channel by the charge velocity.





# Linear Resistance

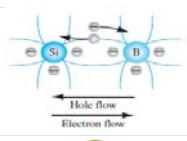


$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

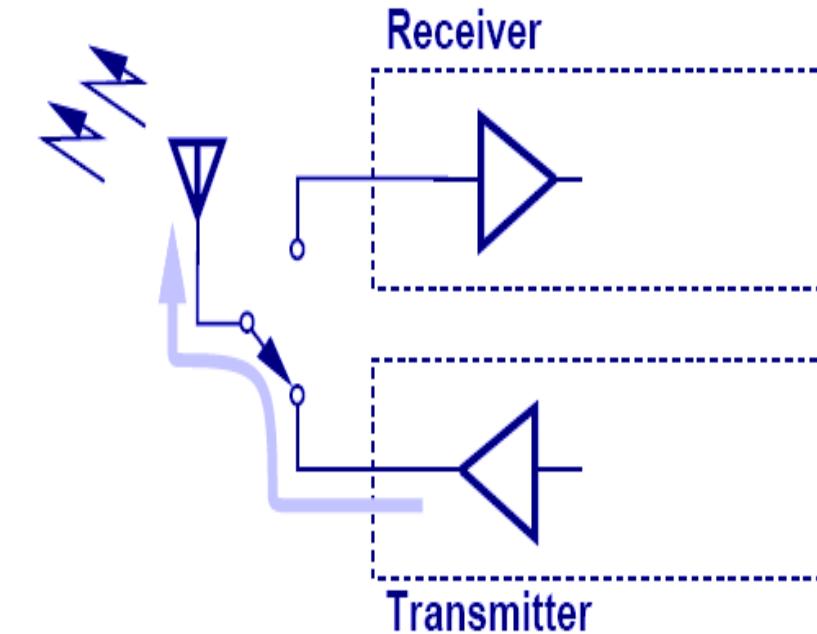
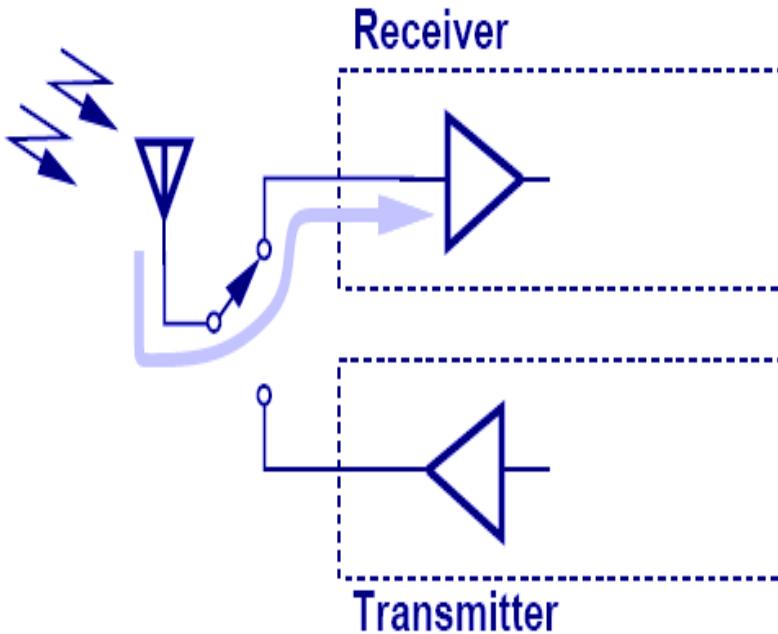
At small  $V_{DS}$ , the transistor can be viewed as a resistor, with the resistance depending on the gate voltage.

It finds application as an electronic switch.



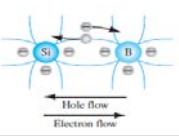


# Application of Electronic Switches

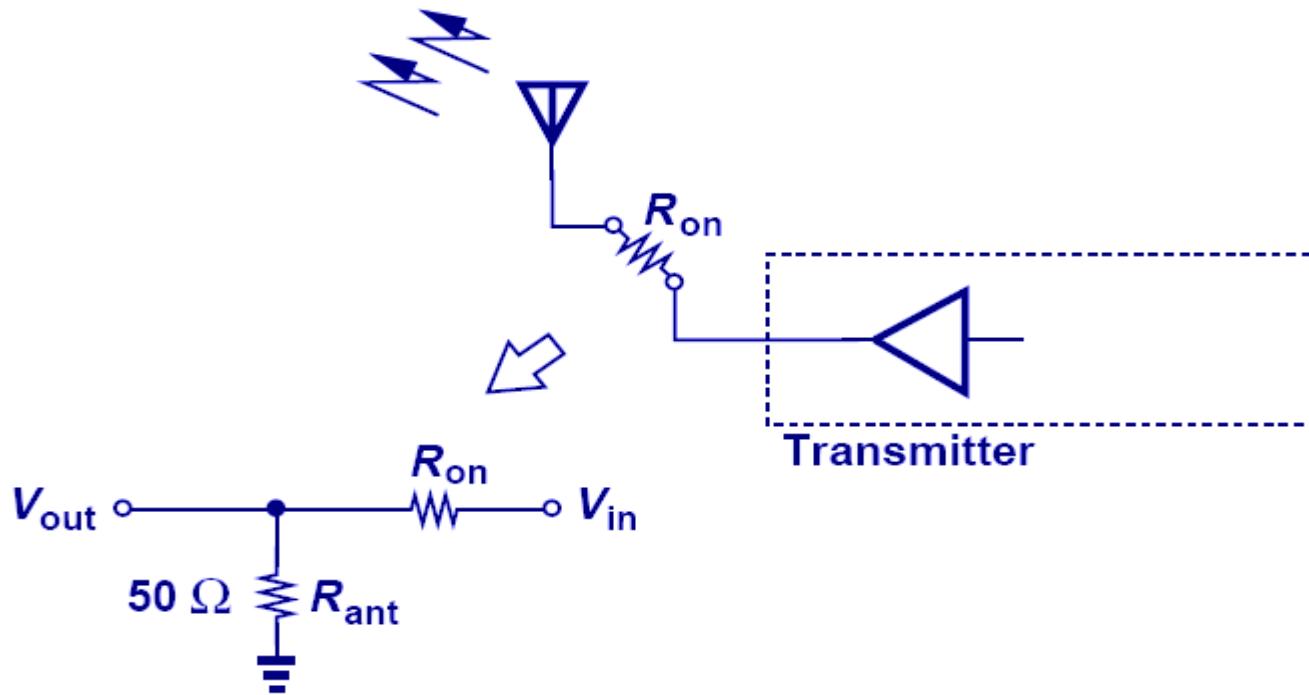


In a cordless telephone system in which a single antenna is used for both transmission and reception, a switch is used to connect either the receiver or transmitter to the antenna.



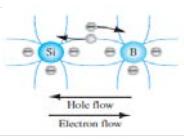


# Effects of On-Resistance

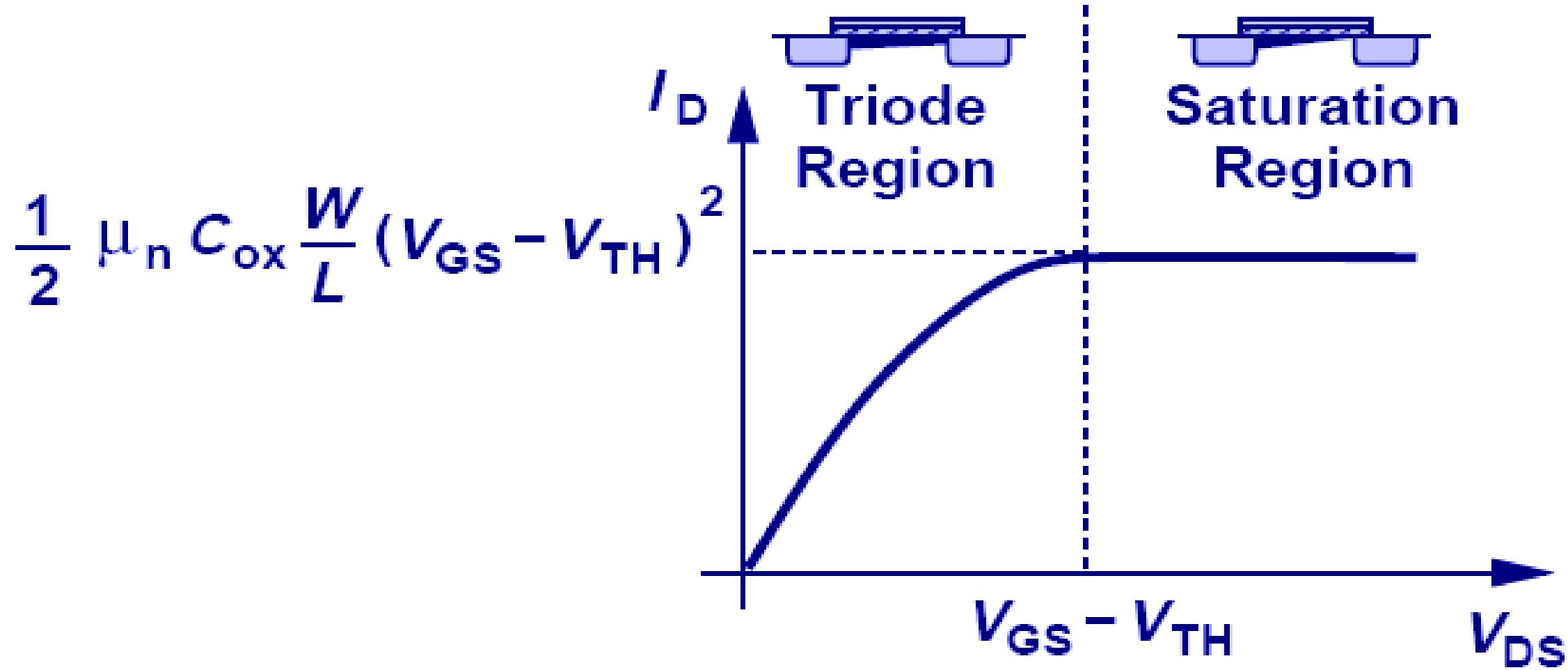


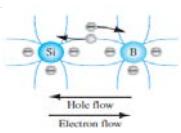
To minimize signal attenuation,  $R_{on}$  of the switch has to be as small as possible. This means larger W/L aspect ratio and greater  $V_{GS}$ .





# Different Regions of Operation





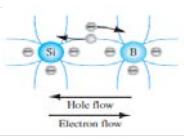
# Transconductance

$\frac{W}{L}$ Constant $V_{GS} - V_{TH}$ Variable	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant
$g_m \propto \sqrt{I_D}$ $g_m \propto V_{GS} - V_{TH}$	$g_m \propto I_D$ $g_m \propto \frac{W}{L}$	$g_m \propto \sqrt{\frac{W}{L}}$ $g_m \propto \frac{1}{V_{GS} - V_{TH}}$

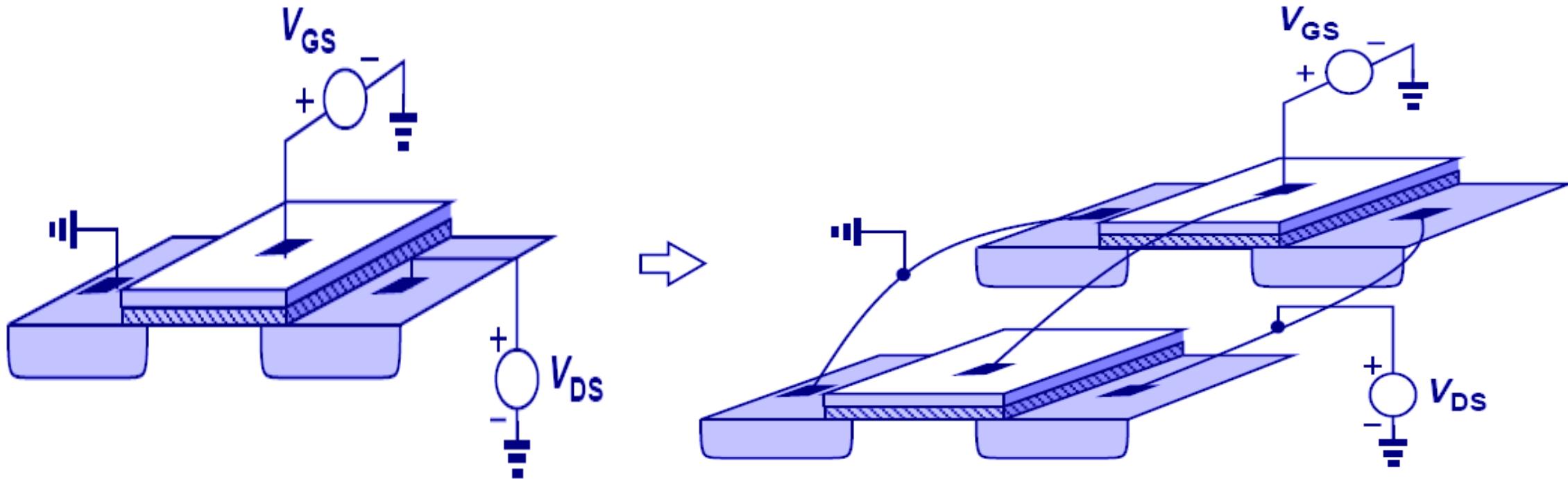
$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \quad g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

Transconductance is a measure of how strong the drain current changes when the gate voltage changes.  
It has three different expressions.



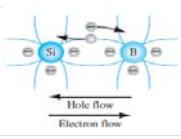


# Doubling of $g_m$ Due to Doubling W/L



If  $W/L$  is doubled, effectively two equivalent transistors are added in parallel, thus doubling the current (if  $V_{GS} - V_{TH}$  is constant) and hence  $g_m$ .



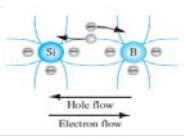


# Comparison of Bipolar and MOS Transistors

Bipolar Transistor	MOSFET
<p><b>Exponential Characteristic</b></p> <p>Active: <math>V_{CB} &gt; 0</math></p> <p>Saturation: <math>V_{CB} &lt; 0</math></p> <p>Finite Base Current</p> <p>Early Effect</p> <p>Diffusion Current</p> <p>-</p>	<p><b>Quadratic Characteristic</b></p> <p>Saturation: <math>V_{DS} &gt; V_{GS} - V_{TH}</math></p> <p>Triode: <math>V_{DS} &lt; V_{GS} - V_{TH}</math></p> <p>Zero Gate Current</p> <p>Channel-Length Modulation</p> <p>Drift Current</p> <p>Voltage-Dependent Resistor</p>

Bipolar devices have a higher  $g_m$  than MOSFETs for a given bias current due to its exponential IV characteristics.





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# Thank You Very Much

Dipl.-Ing. B. Kommey

[bkommey.coe@knust.edu.gh](mailto:bkommey.coe@knust.edu.gh)

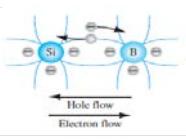
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

Tel: 050 770 32 86

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Skype\_id: calculus.affairs





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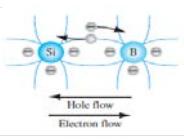
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**“A ship is always safe at the shore- but that is NOT what it is built for”**

**Albert Einstein**





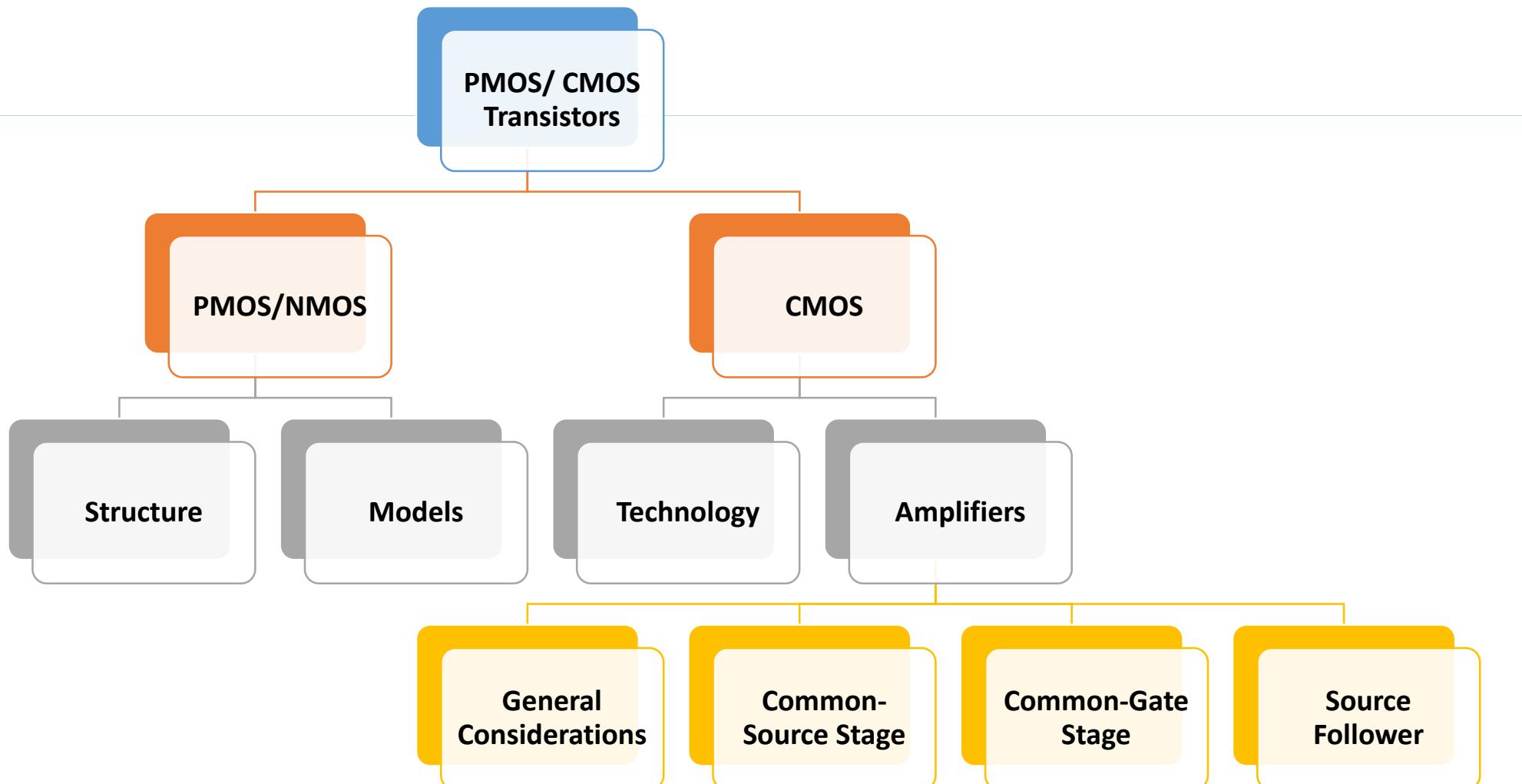
# SEMICONDUCTOR DEVICES

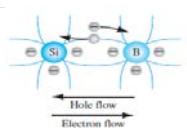
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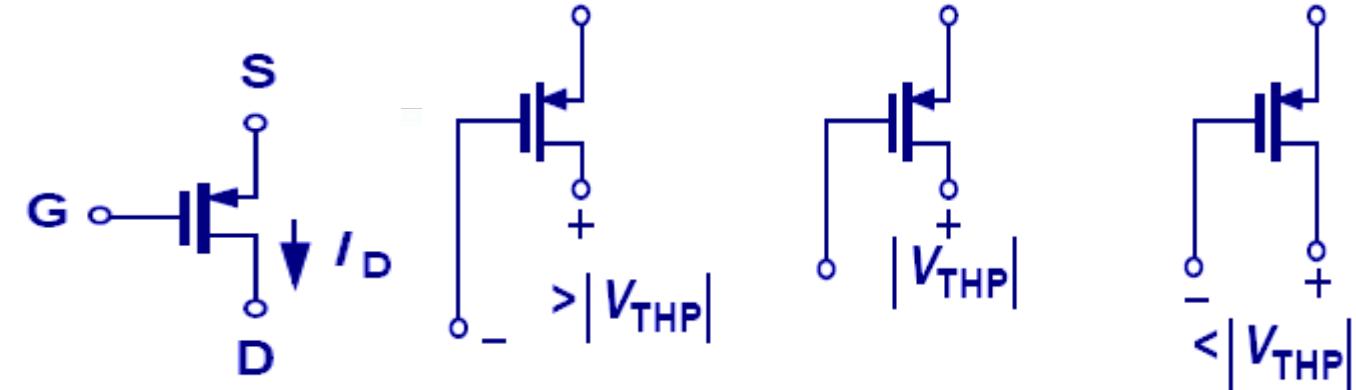
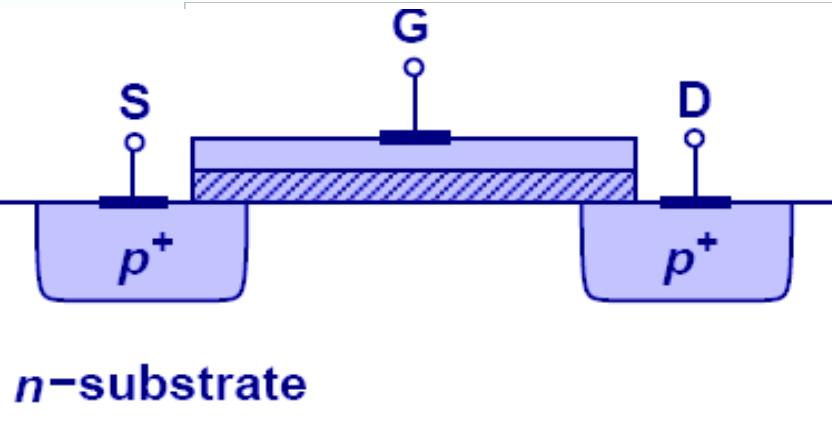


# Overview





# PMOS Transistor

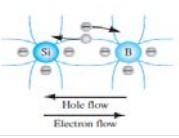


Just like the PNP transistor in bipolar technology, it is possible to create a MOS device where holes are the dominant carriers.

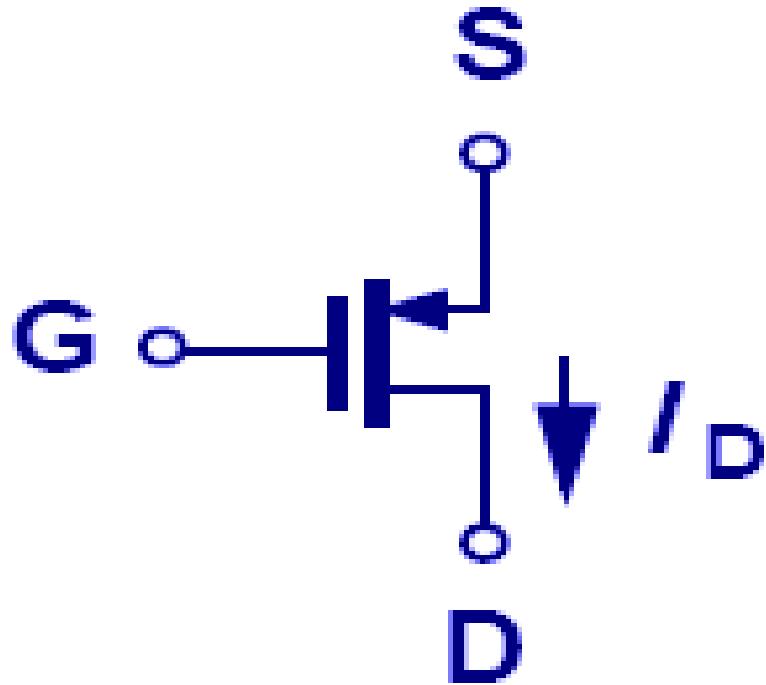
It is called the PMOS (p-channel) transistor.

It behaves like an NMOS (n-channel) device with all the polarities reversed.





# PMOS Equations



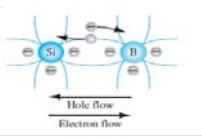
$$I_{D,sat} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 - \lambda V_{DS})$$

$$I_{D,tri} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$$

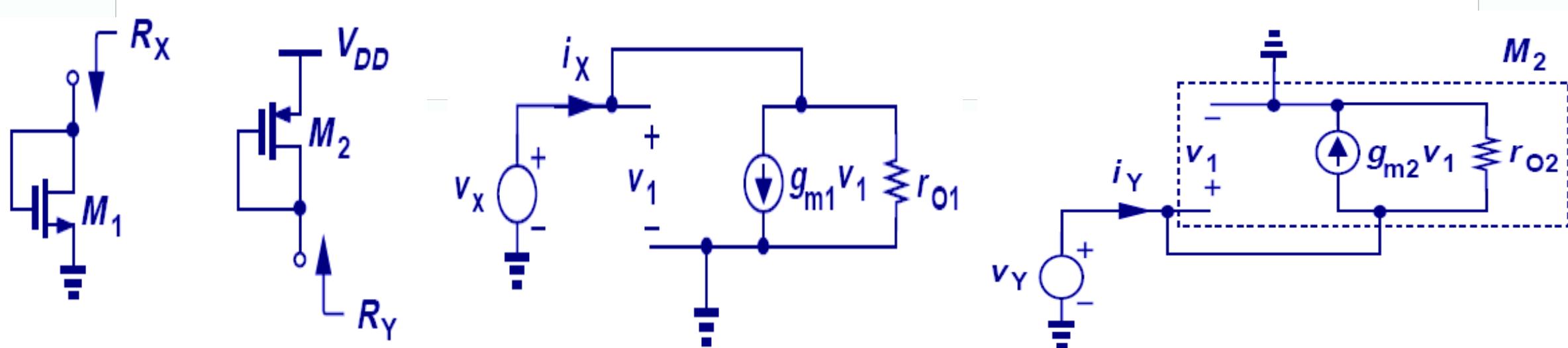
$$I_{D,sat} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)^2 (1 + \lambda |V_{DS}|)$$

$$I_{D,tri} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} [2(|V_{GS}| - |V_{TH}|)|V_{DS}| - V_{DS}^2]$$



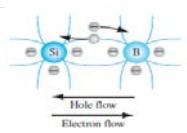


# Small-Signal Model of PMOS Device

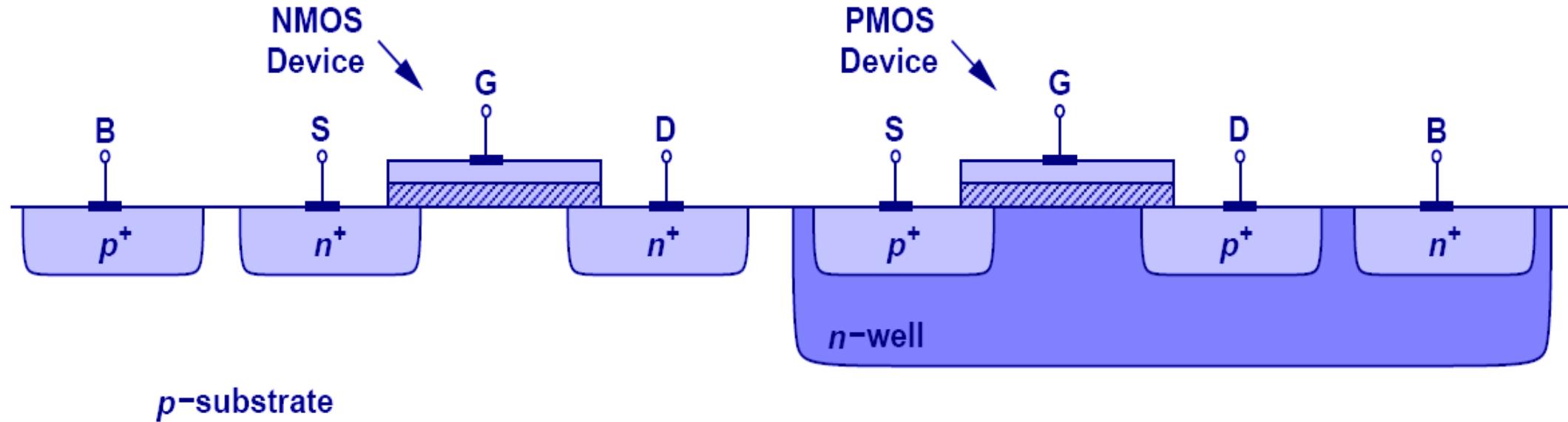


The small-signal model of PMOS device is identical to that of NMOS transistor;  
therefore,  $R_X$  equals  $R_Y$  and hence  $(1/gm) \parallel r_o$ .





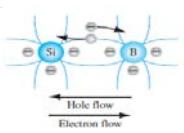
# CMOS Technology



It is possible to grow an n-well inside a p-substrate to create a technology where both NMOS and PMOS can coexist.

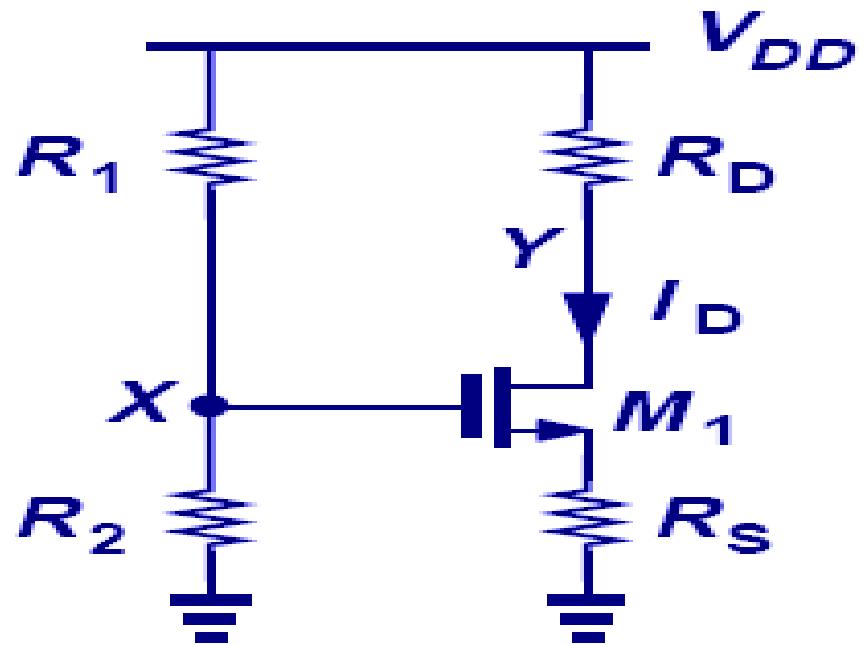
It is known as CMOS, or “Complementary MOS”.





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# MOS Biasing



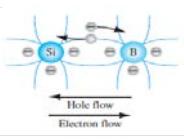
$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left( \frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH} \right)}$$

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_s}$$

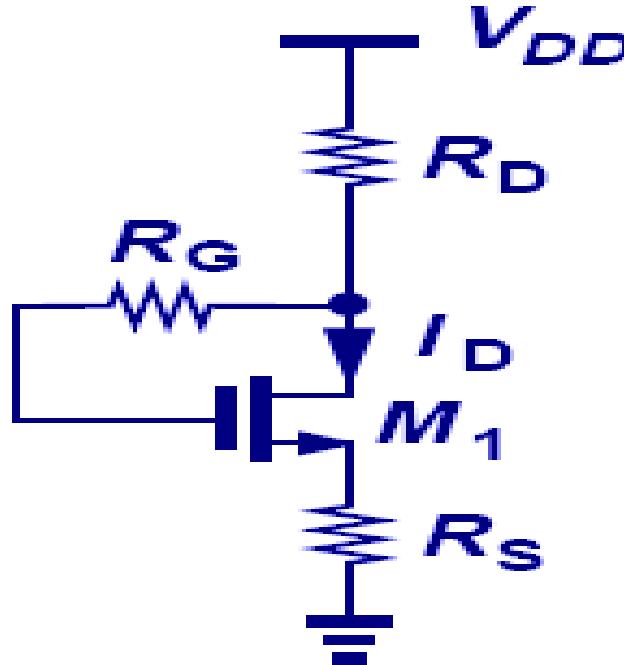
Voltage at X is determined by  $V_{DD}$ ,  $R_1$ , and  $R_2$ .

$V_{GS}$  can be found using the equation above, and  $I_D$  can be found by using the NMOS current equation.





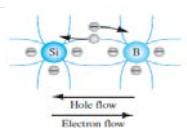
# Self-Biased MOS Stage



$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$

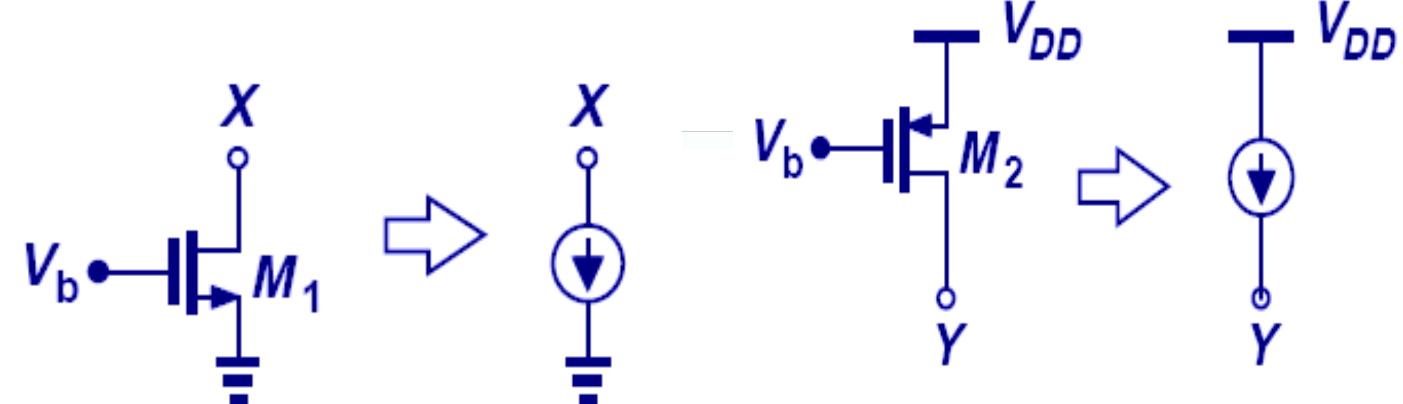
if  $M_1$  is in saturation and no potential drop appears across  $R_G$ .



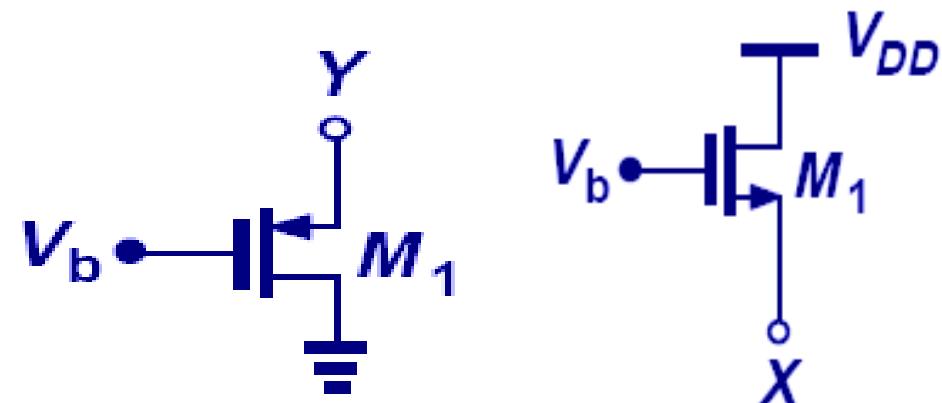


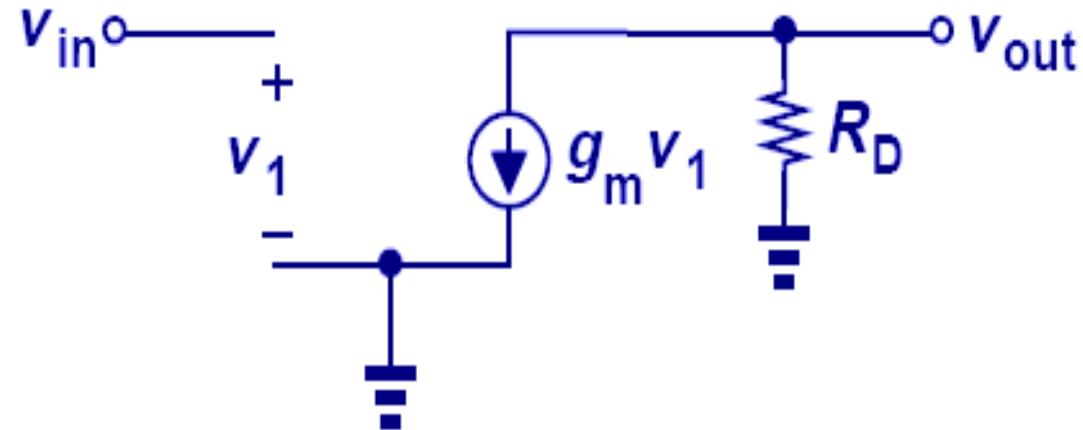
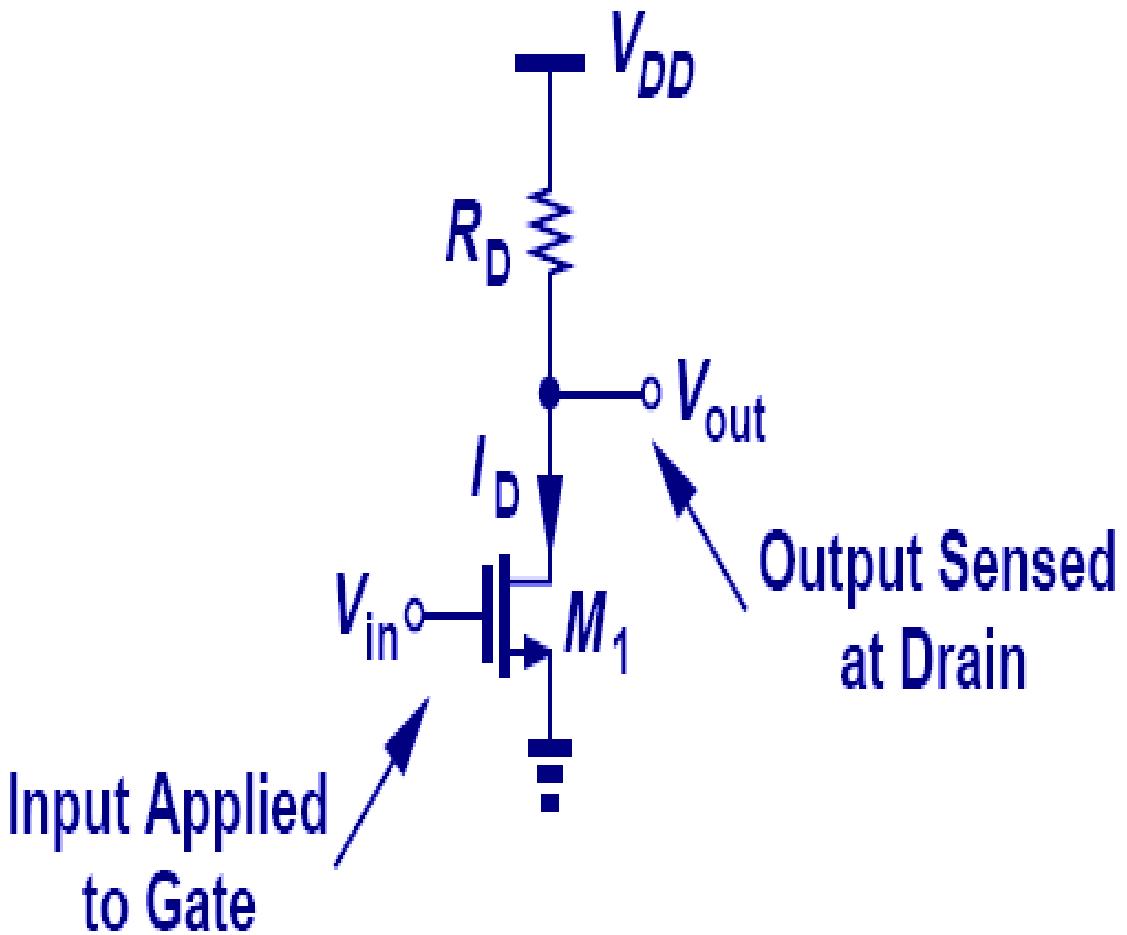
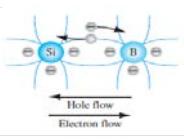
# Current Sources

When in saturation region, a MOSFET behaves as a current source.



NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from  $V_{DD}$  to a point (sources current).



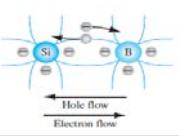


$$\lambda = 0$$

$$A_v = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D R_D}$$





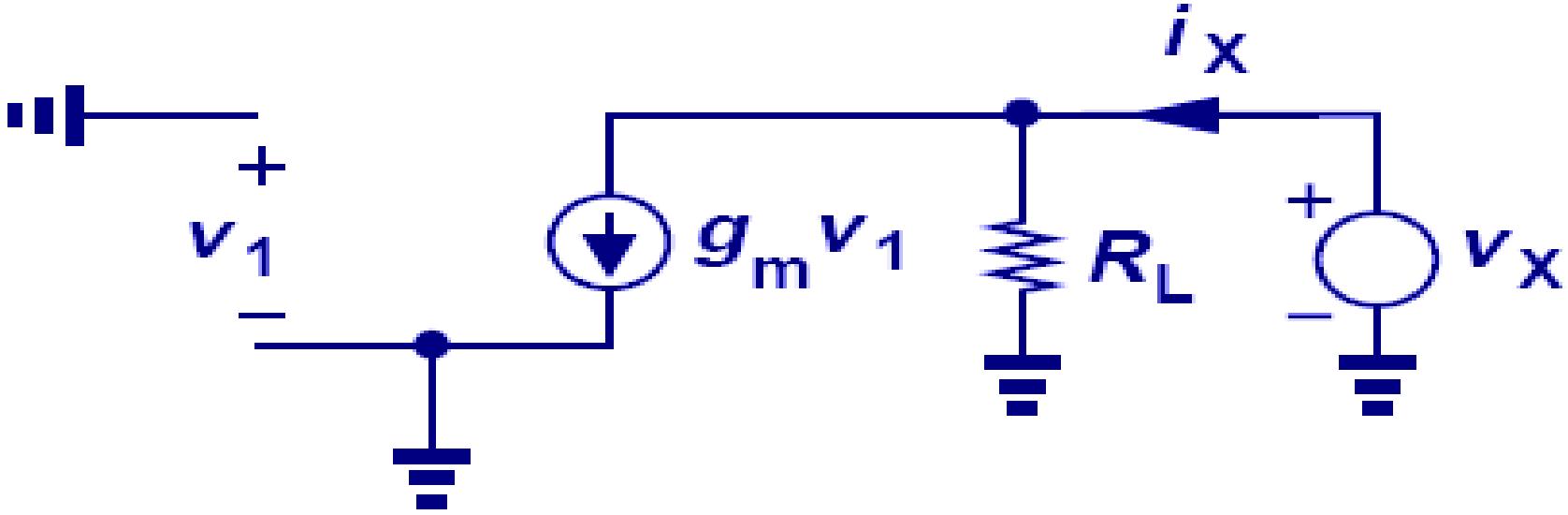
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# CS Stage with $\lambda=0$

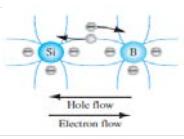


$$A_v = -g_m R_L$$

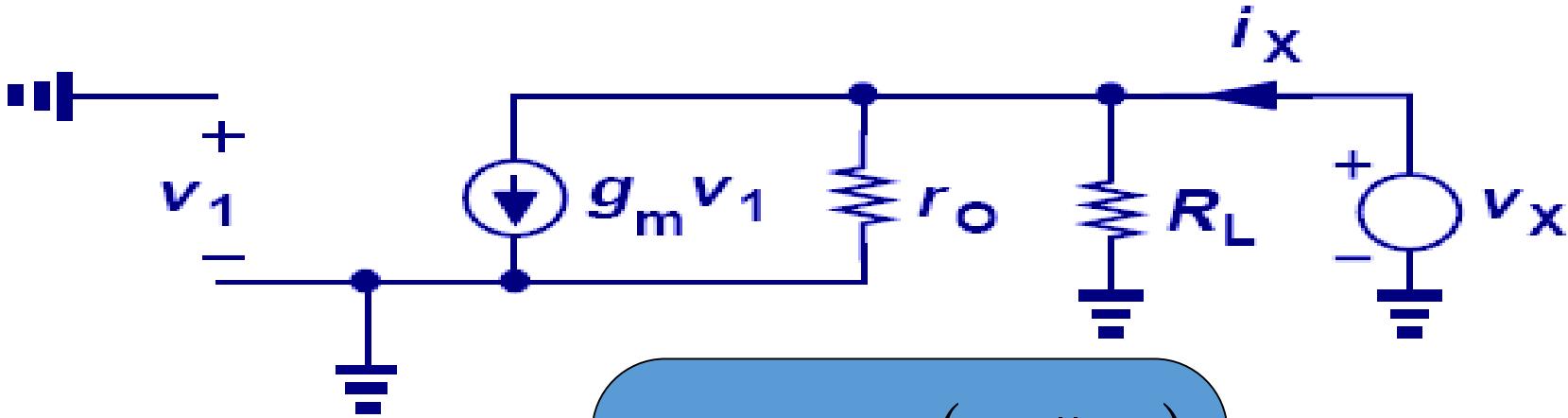
$$R_{in} = \infty$$

$$R_{out} = R_L$$





# CS Stage with $\lambda \neq 0$



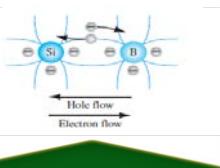
$$A_v = -g_m (R_L \parallel r_o)$$

$$R_{in} = \infty$$

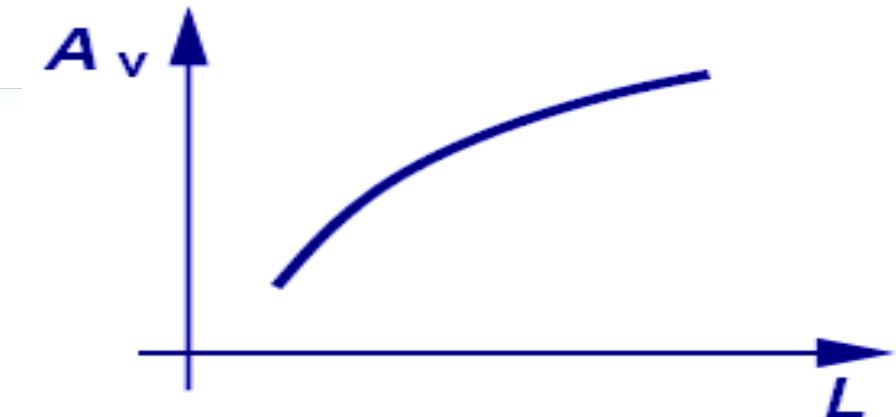
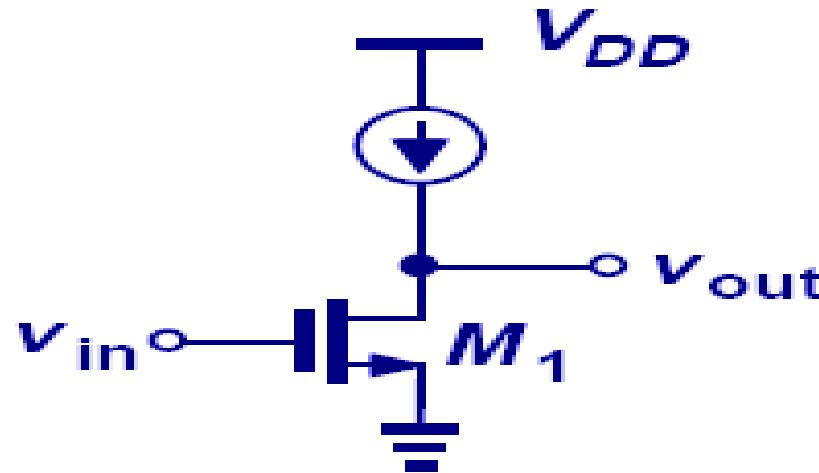
$$R_{out} = R_L \parallel r_o$$

Early effect and channel length modulation affect CE and CS stages in a similar manner.





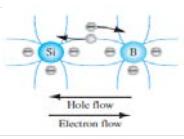
# CS Gain Variation with Channel Length



Since  $\lambda$  is inversely proportional to  $L$ , the voltage gain actually becomes proportional to the square root of  $L$ .

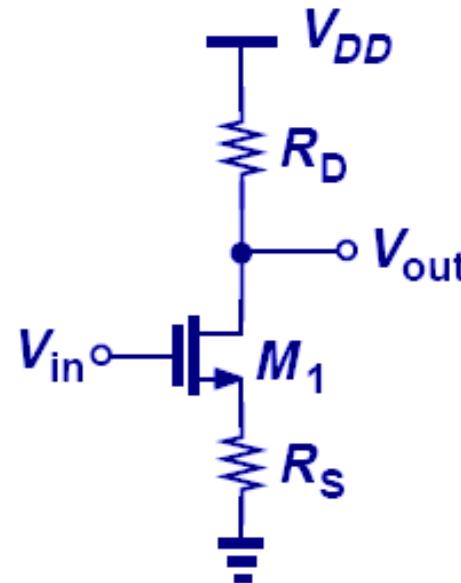
$$|A_v| = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L}}}{\lambda \sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$





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# CS Stage with Degeneration

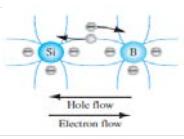


$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_s}$$

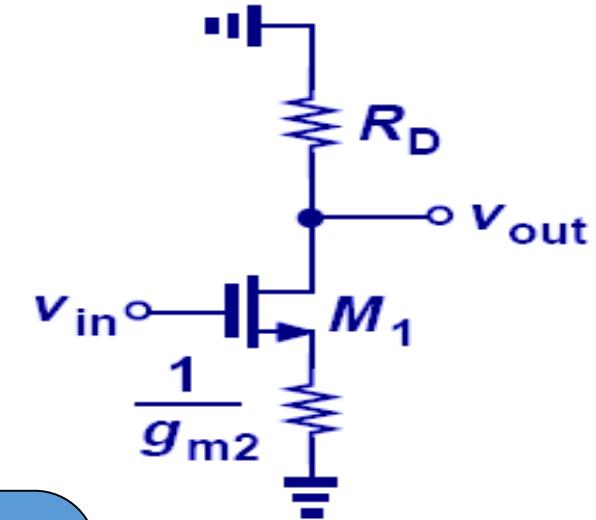
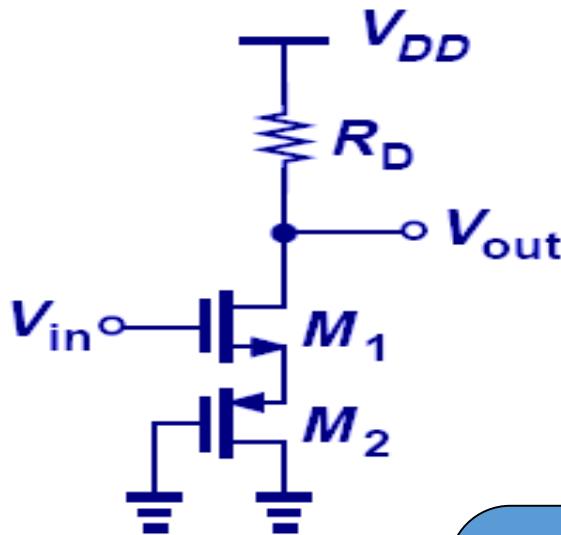
$$\lambda = 0$$

Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.





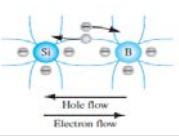
# Example of CS Stage with Degeneration



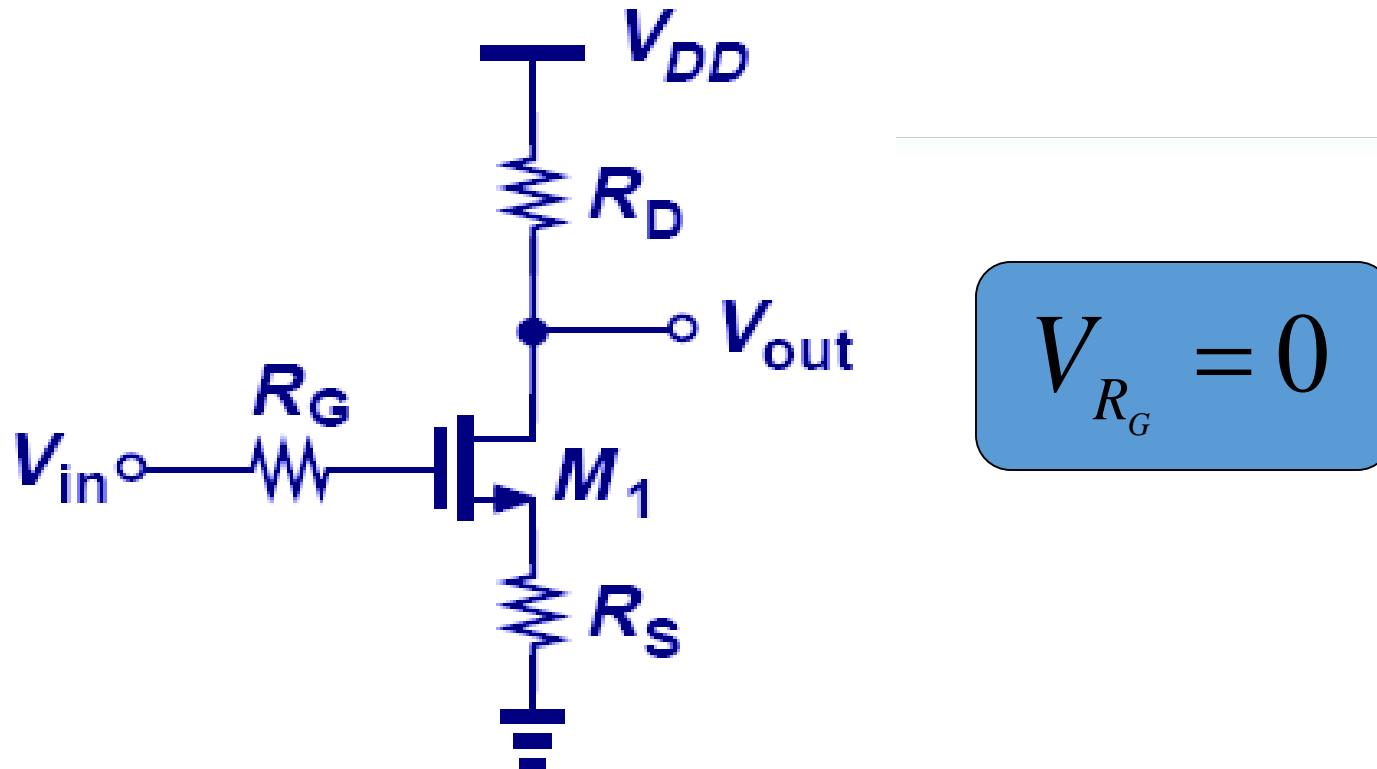
$$A_v = - \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

A diode-connected device degenerates a CS stage.



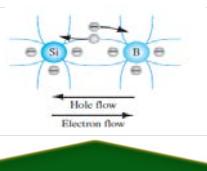


# CS Stage with Gate Resistance

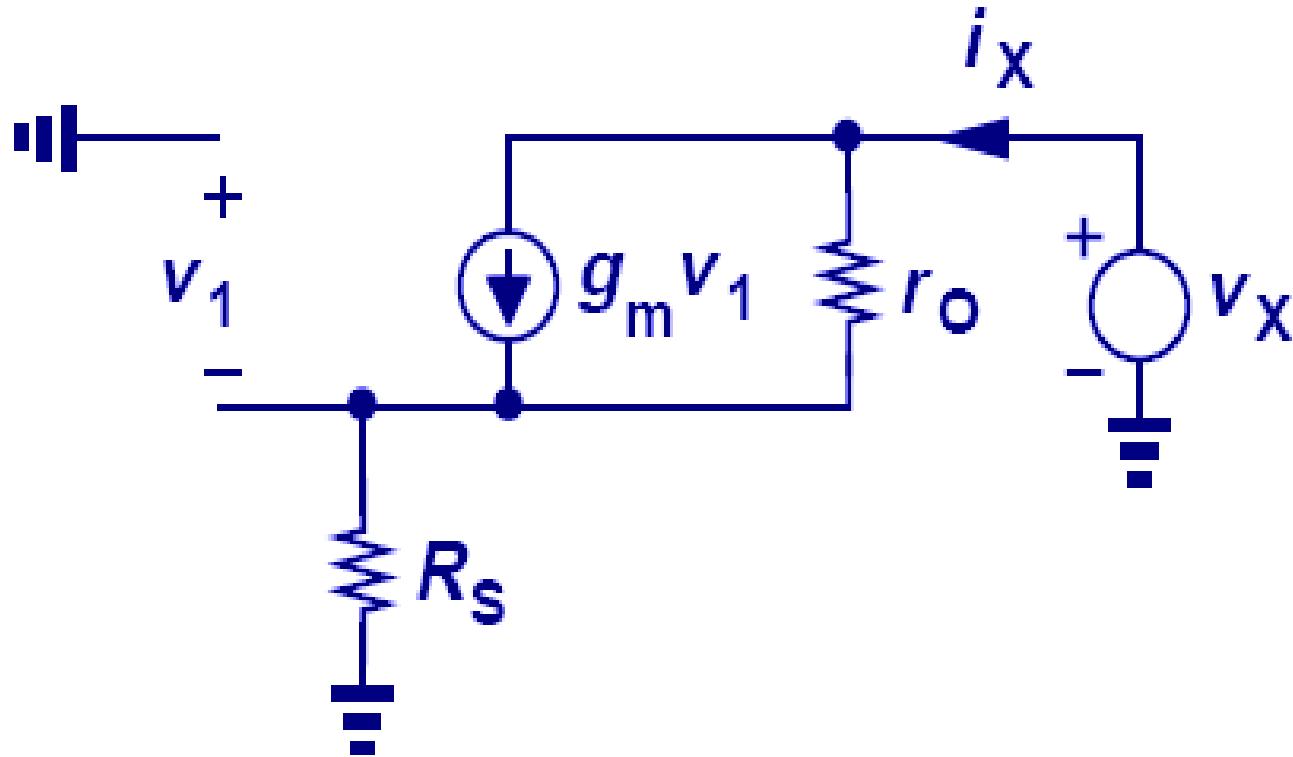


Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.





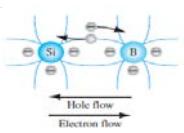
# Output Impedance of CS Stage with Degeneration



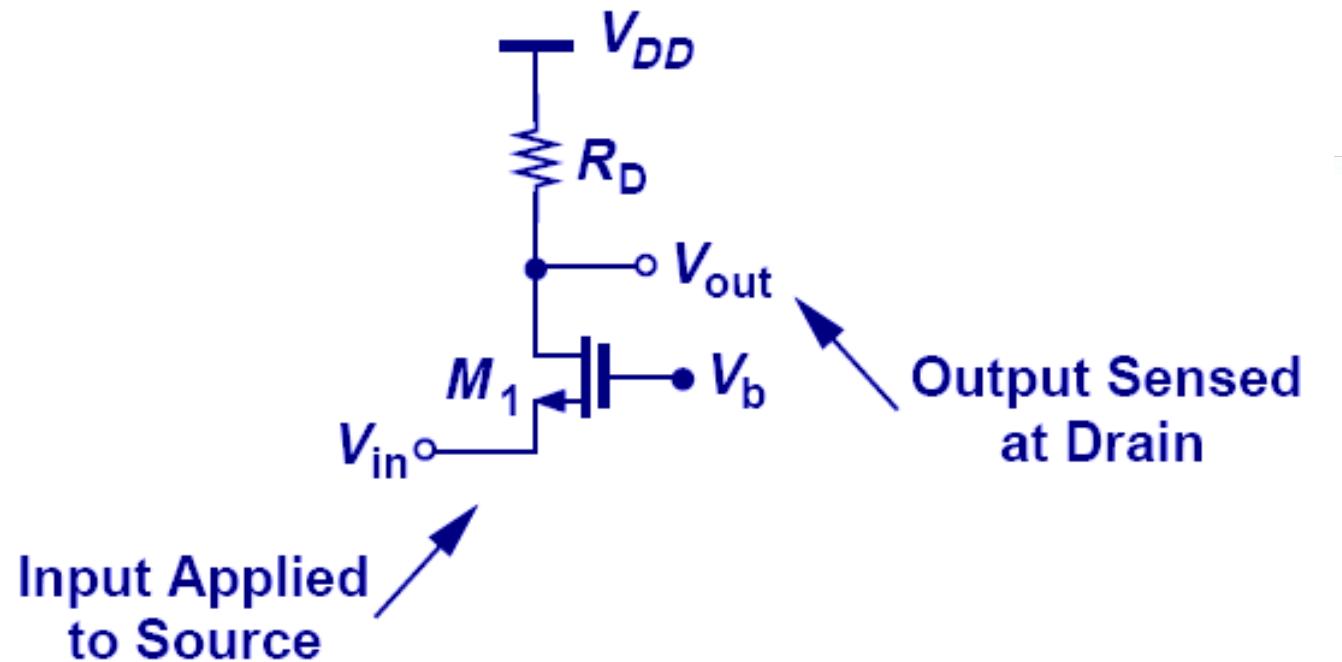
$$r_{out} \approx g_m r_o R_s + r_o$$

Similar to the bipolar counterpart, degeneration boosts output impedance.





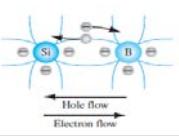
# Common-Gate Stage



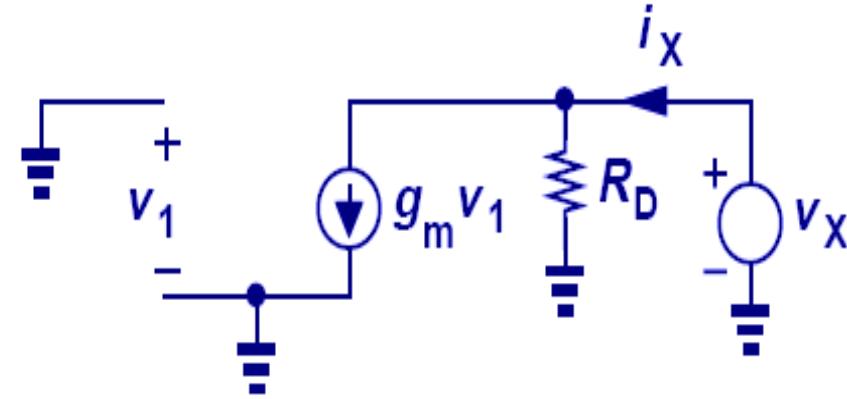
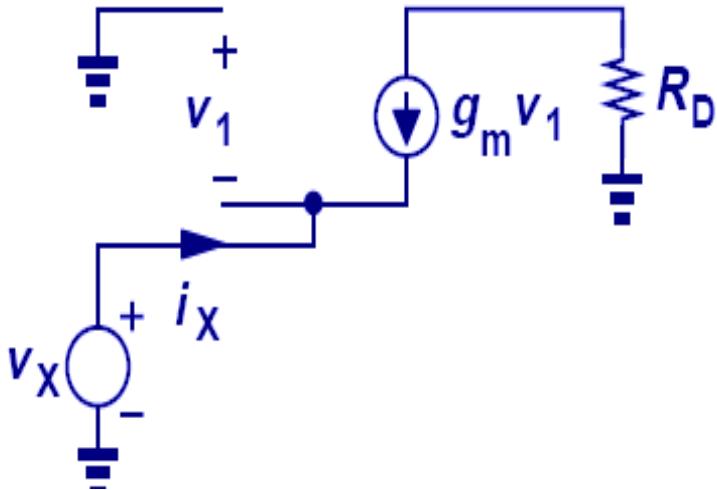
$$A_v = g_m R_D$$

Common-gate stage is similar to common-base stage:  
a rise in input causes a rise in output.  
So the gain is positive.





# I/O Impedances of CG Stage



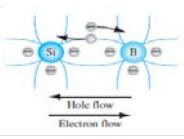
$$R_{in} = \frac{1}{g_m}$$

$$\lambda = 0$$

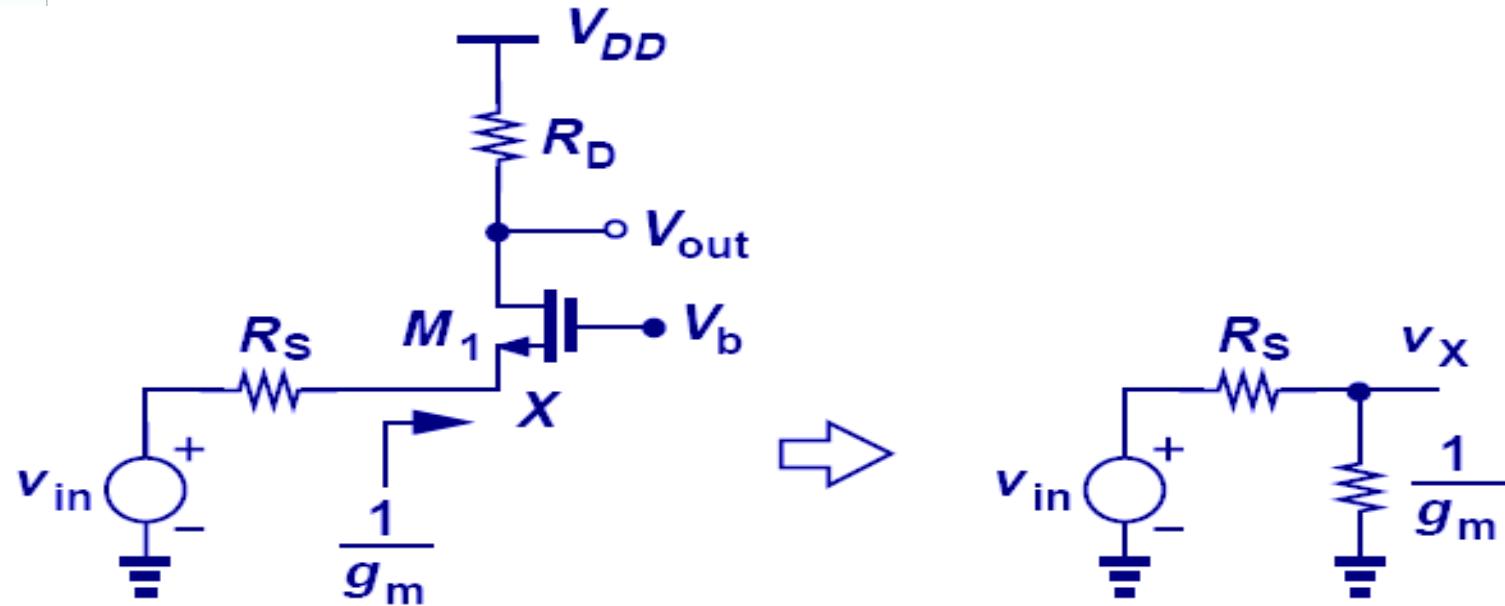
$$R_{out} = R_D$$

The input and output impedances of CG stage are similar to those of CB stage.





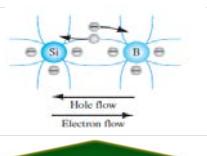
# CG Stage with Source Resistance



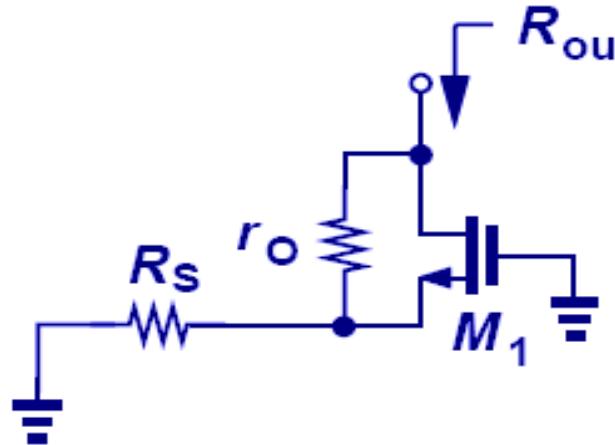
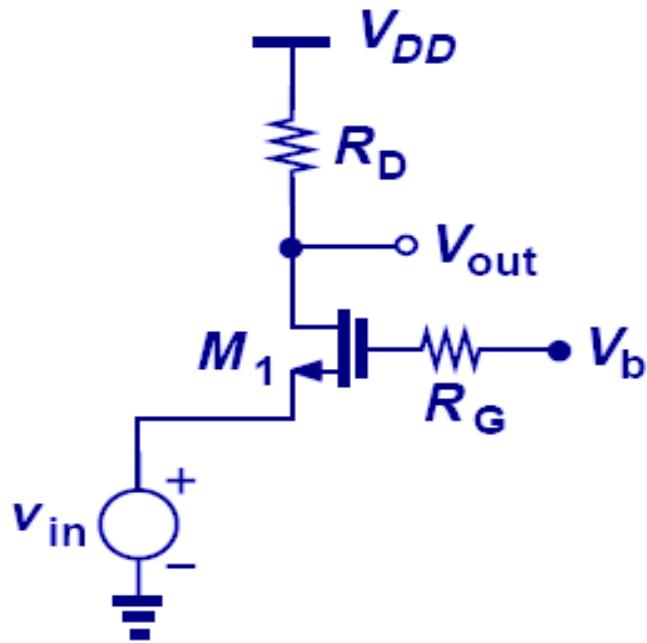
$$A_v = \frac{R_D}{\frac{1}{g_m} + R_s}$$

When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.





# Generalized CG Behavior

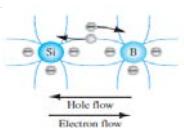


$$R_{out} = (1 + g_m r_o) R_s + r_o$$

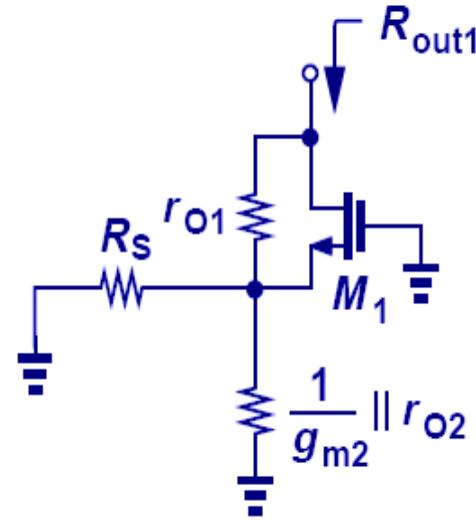
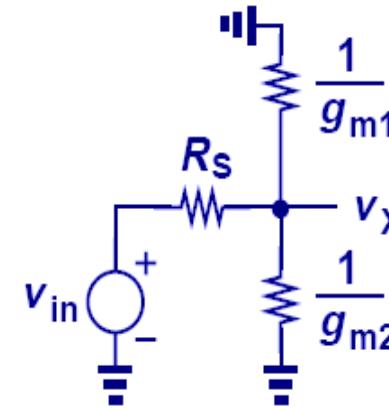
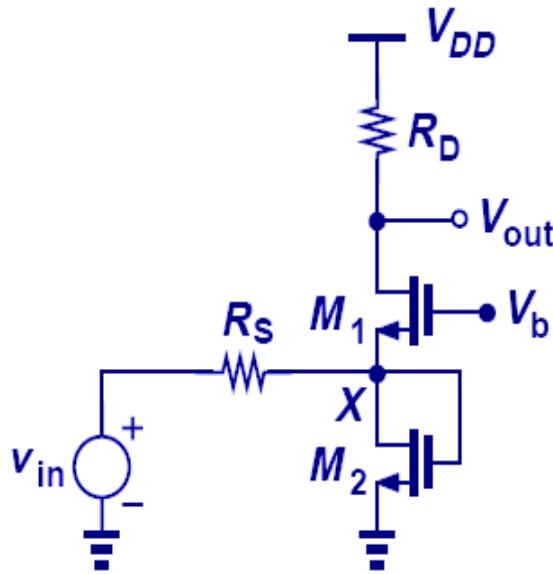
When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it ( at low frequencies).

The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.





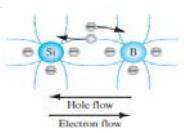
# Example of CG Stage



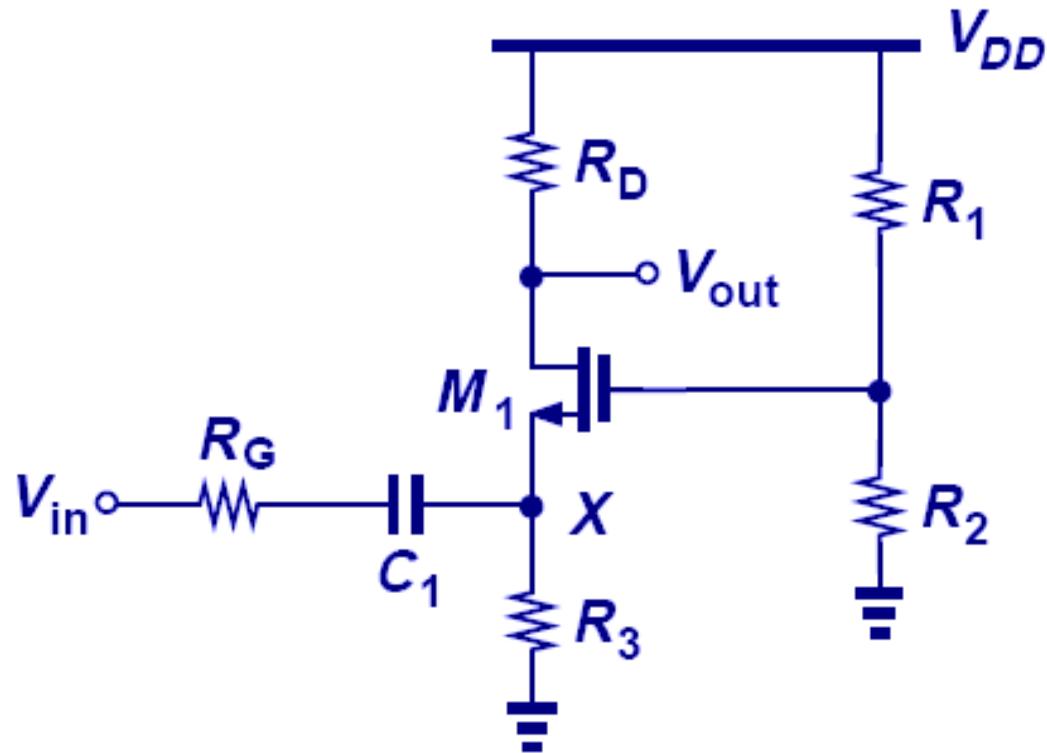
$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}R_D}{1 + (g_{m1} + g_{m2})R_s} \quad R_{out} \approx \left[ g_{m1}r_{o1} \left( \frac{1}{g_{m2}} \parallel R_s \right) + r_{o1} \right] \parallel R_D$$

Diode-connected  $M_2$  acts as a resistor to provide the bias current.





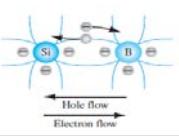
# CG Stage with Biasing



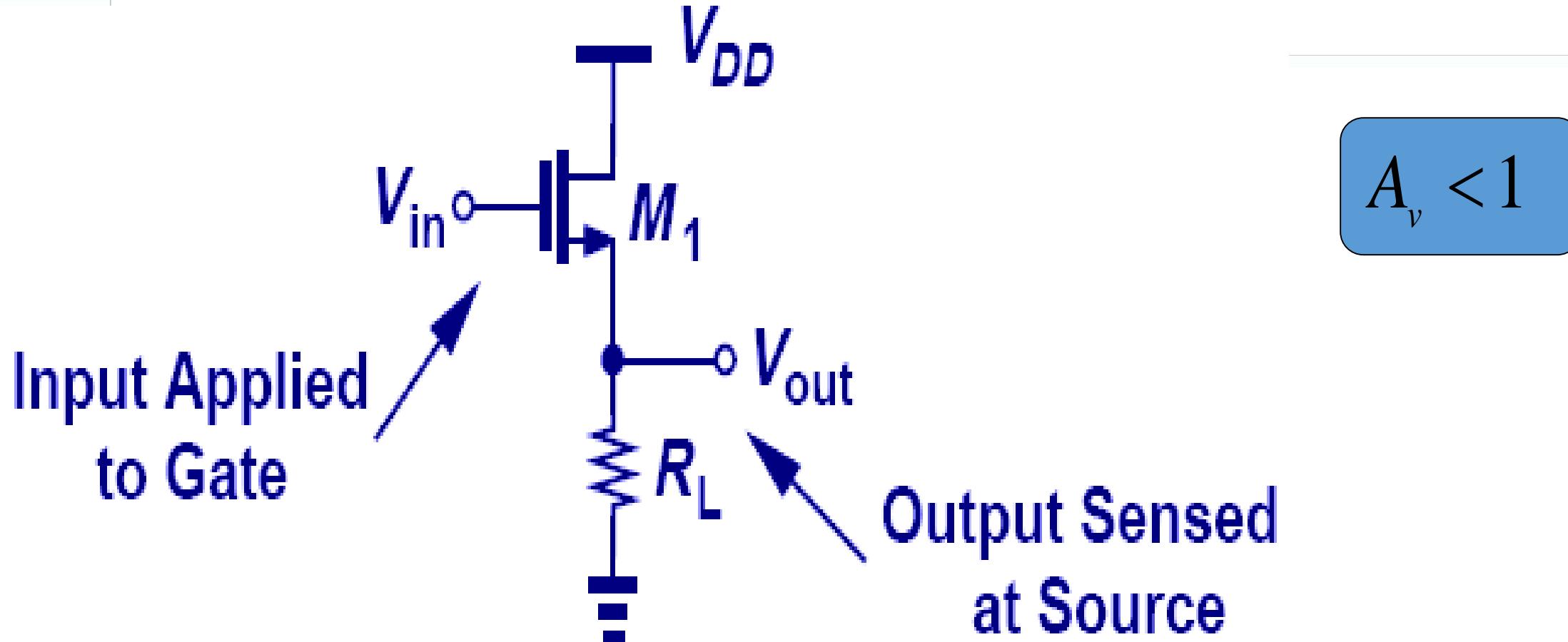
$$\frac{v_{out}}{v_{in}} = \frac{R_3 \parallel (1/g_m)}{R_3 \parallel (1/g_m) + R_S} \cdot g_m R_D$$

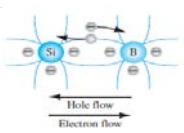
$R_1$  and  $R_2$  provide gate bias voltage, and  $R_3$  provides a path for DC bias current of  $M_1$  to flow to ground.



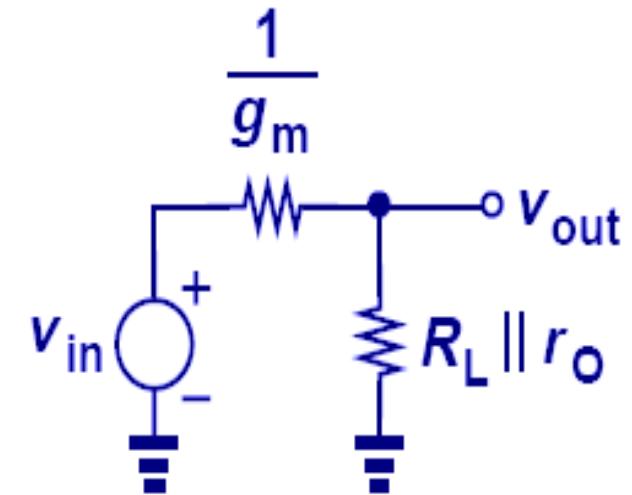
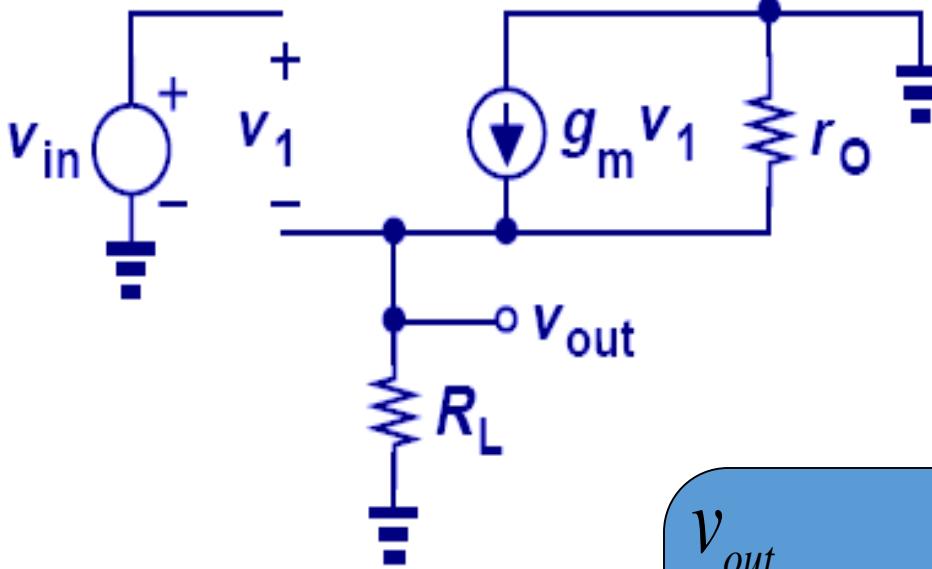


# Source Follower Stage





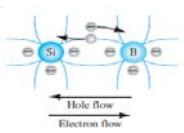
# Source Follower Core



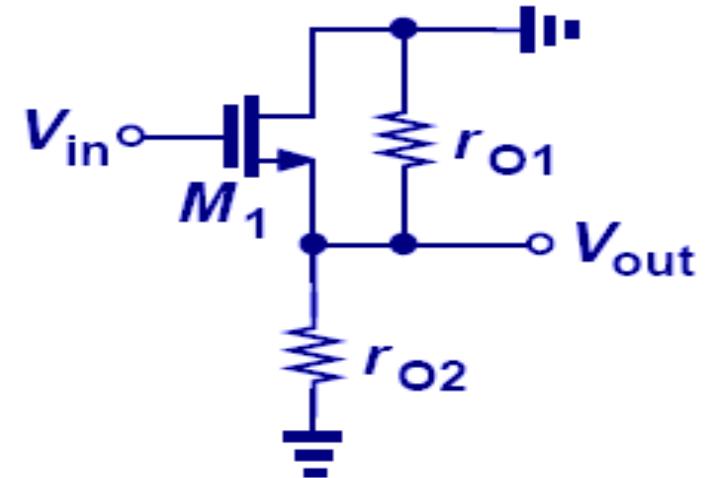
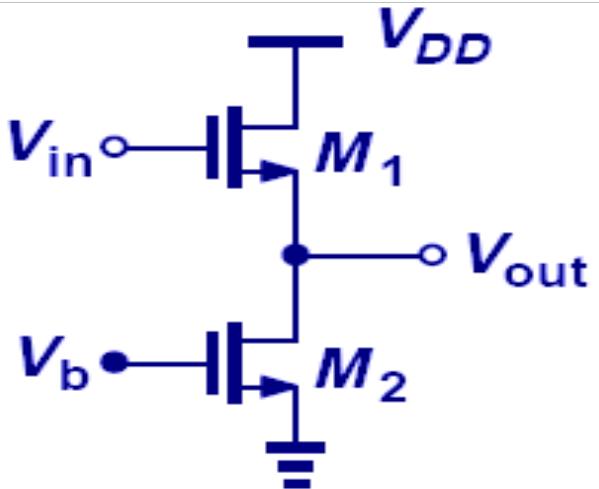
$$\frac{v_{out}}{v_{in}} = \frac{r_o \parallel R_L}{\frac{1}{g_m} + r_o \parallel R_L}$$

Similar to the emitter follower, the source follower can be analyzed as a resistor divider.





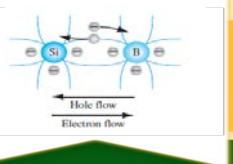
# Source Follower Example



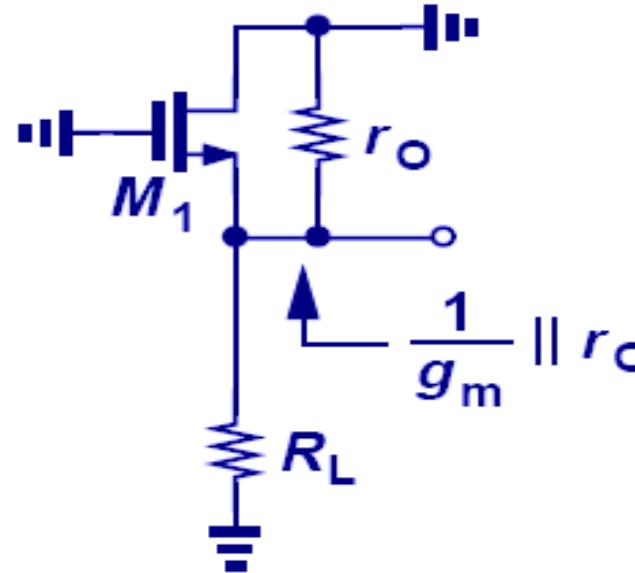
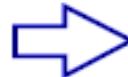
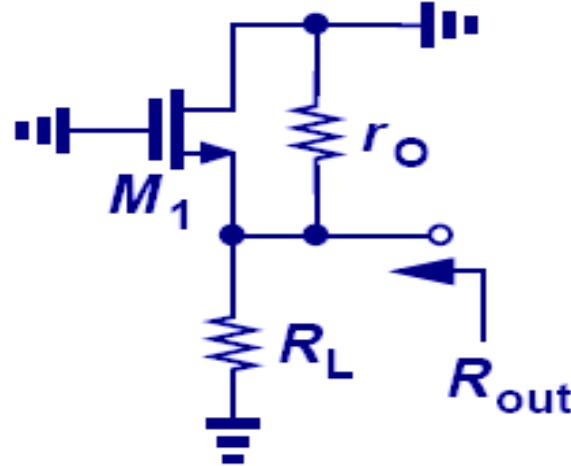
In this example,  $M_2$  acts as a current source.

$$A_v = \frac{r_{O1} \parallel r_{O2}}{\frac{1}{g_m1} + r_{O1} \parallel r_{O2}}$$





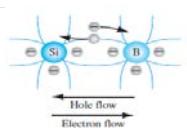
# Output Resistance of Source Follower



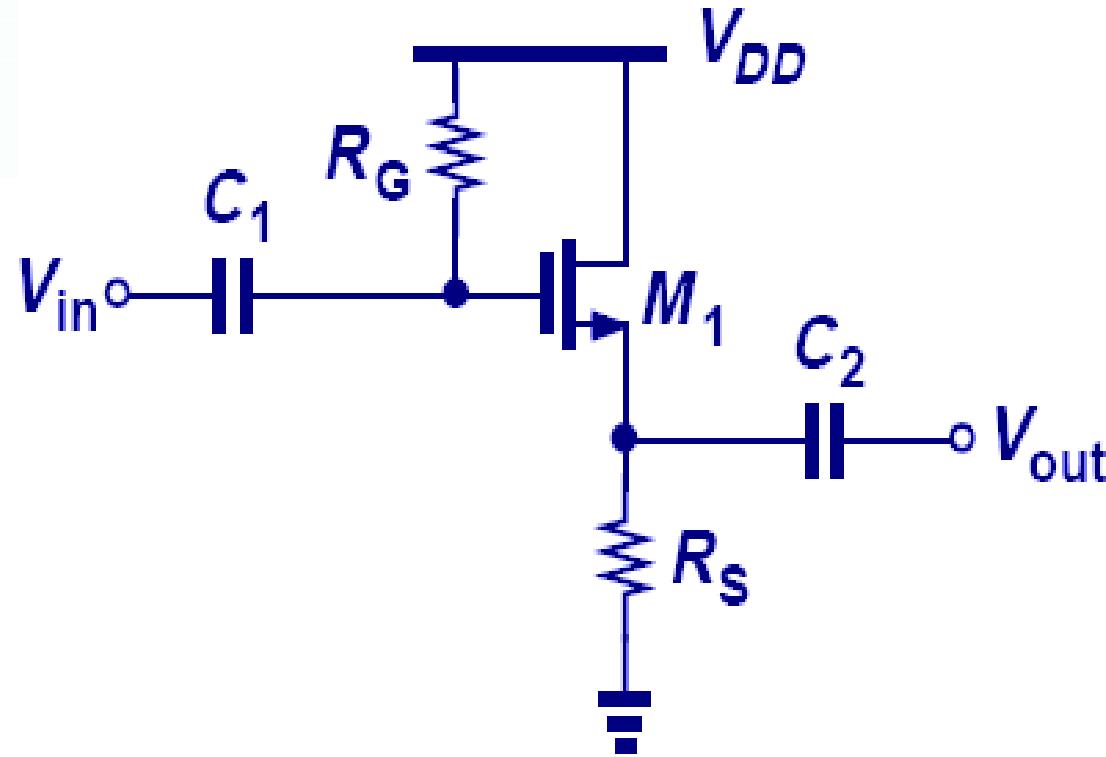
$$R_{out} = \frac{1}{g_m} \parallel r_o \parallel R_L \approx \frac{1}{g_m} \parallel R_L$$

The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.





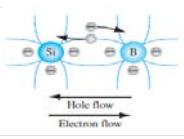
# Source Follower with Biasing



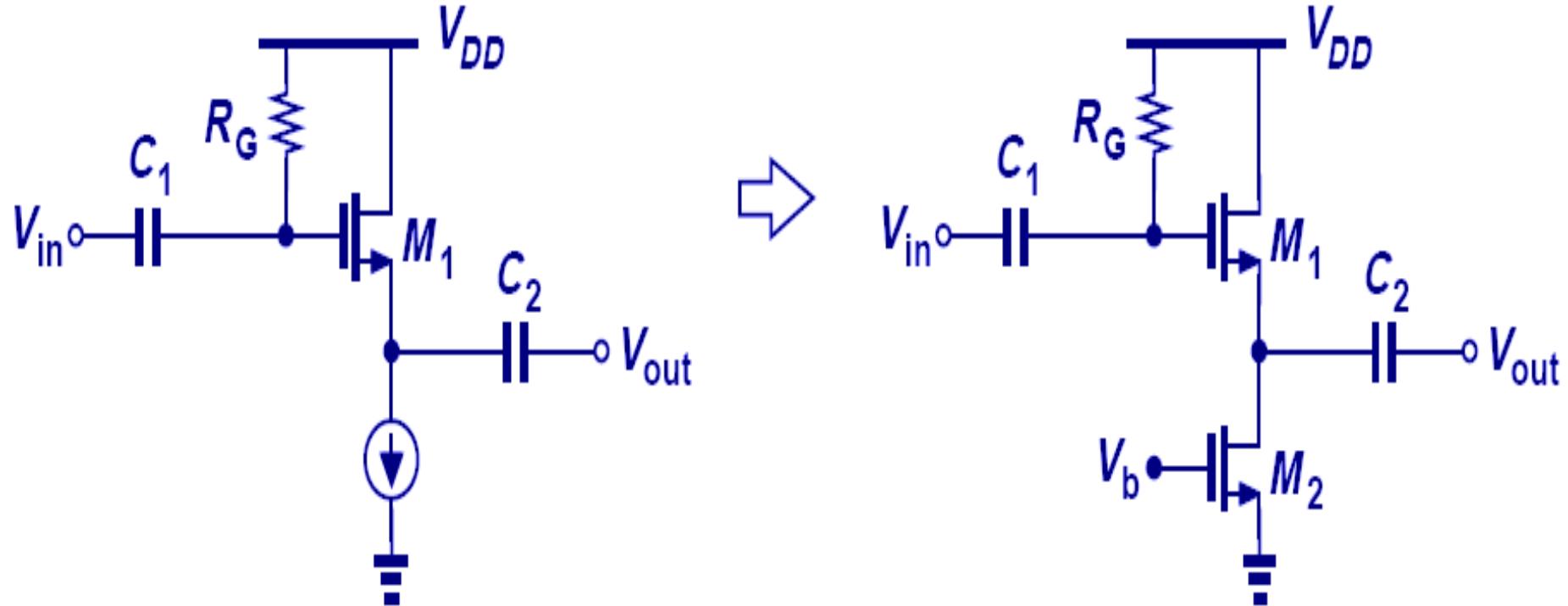
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - I_D R_S - V_{TH})^2$$

$R_G$  sets the gate voltage to  $V_{DD}$ , whereas  $R_S$  sets the drain current.  
The quadratic equation above can be solved for  $I_D$ .



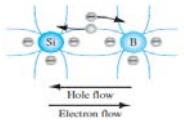


# Supply-Independent Biasing



If  $R_s$  is replaced by a current source, drain current  $I_D$  becomes independent of supply voltage.





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# Thank You Very Much

Dipl.-Ing. B. Kommey

[bkommey.coe@knust.edu.gh](mailto:bkommey.coe@knust.edu.gh)

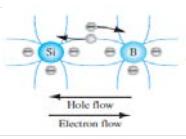
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

Tel: 050 770 32 86

Whatsup: 0049 172 4444 765

Skype\_id: calculus.affairs





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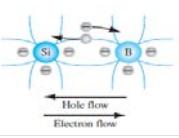
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**“Learn from yesterday, live for today,  
hope for tomorrow.  
The important thing is to not stop  
questioning.”**

**Albert Einstein**





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# Overview

## Operational Amplifier

General Considerations

Op-Amp-Based Circuits

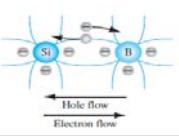
Linear Functions

Nonlinear Functions

Op-Amp Nonidealities

Design Examples





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# Overview

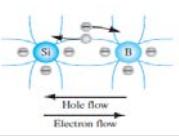
## Linear Functions

**Noninverting  
Amplifier**

**Inverting  
Amplifier**

**Integrator  
/Differentiator**





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# Overview

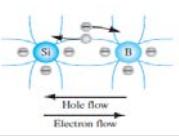
## Nonlinear Functions

Precision  
Rectifier

Logarithmic  
Amplifier

Square Root  
Circuit





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# Overview

## Op-Amp Nonidealities

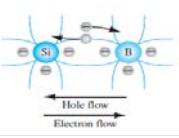
DC Offsets

Input Bias

Speed Limitations

Finite Input and  
Output Impedances





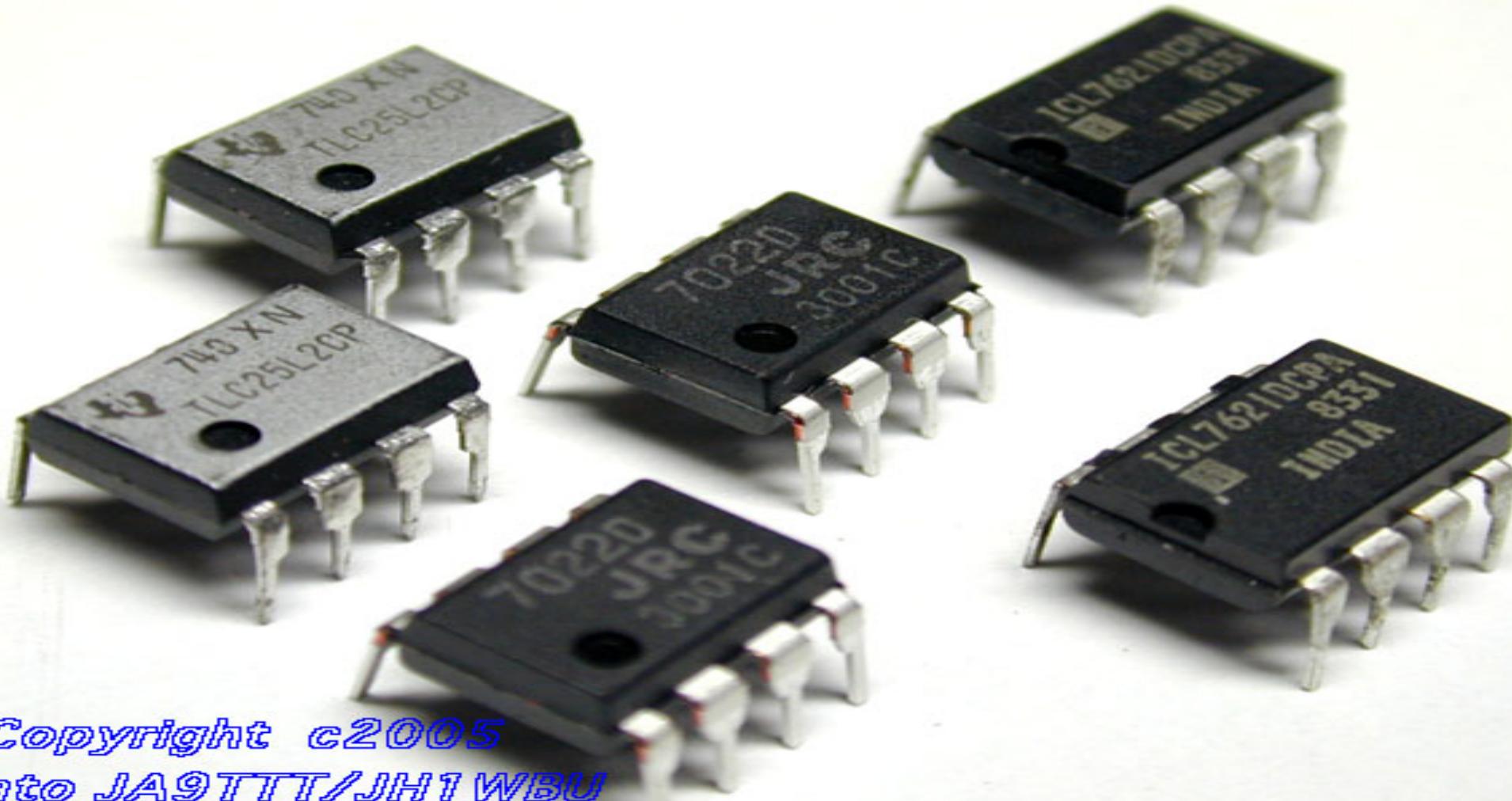
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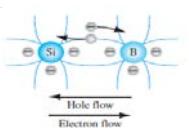
# Introduction to OP



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*T.Kato JA9TTT/JHT WBU*





# Introduction to OP

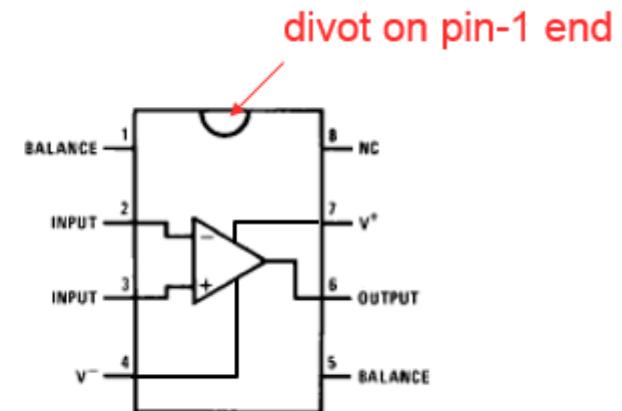
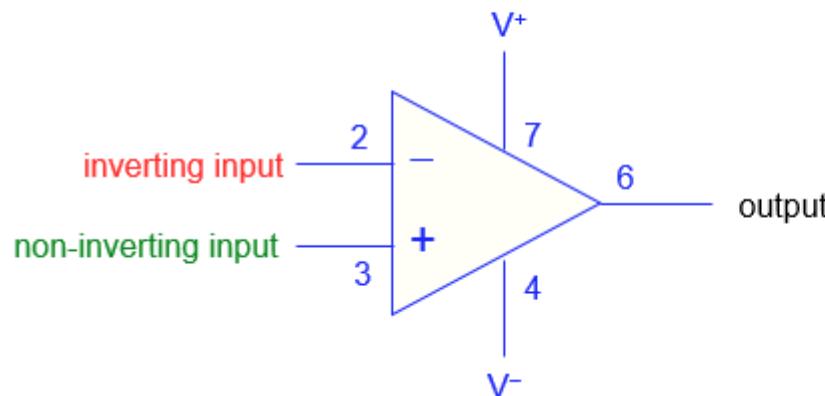
OP (-also called amplifiers or buffers in general)

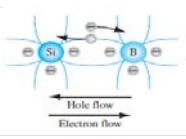
Op is drawn as a triangle in a schematic

Op has two inputs (inverting and non-inverting)

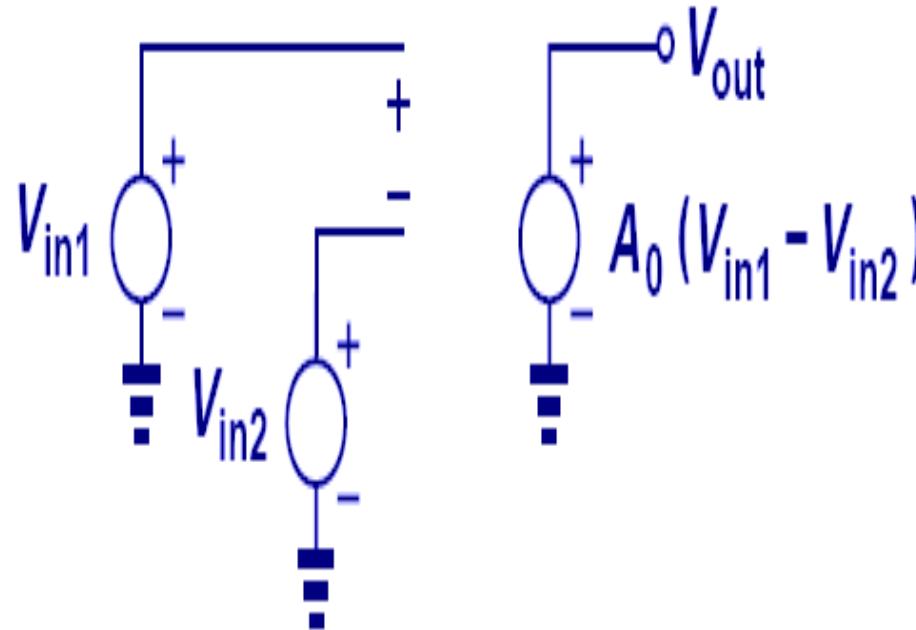
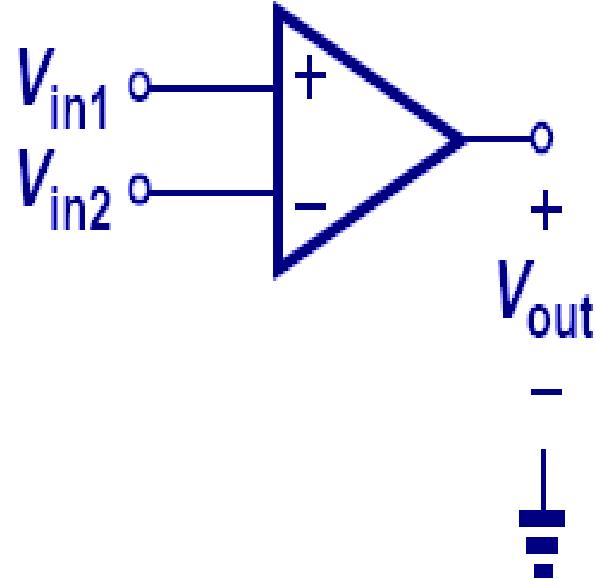
Op has one output

Op also has power connections (NB: no explicit ground)





# Basic Operational Amplifier

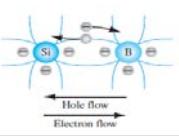


Internal Op-  
amplifier formula

$$V_{out} = A_0(V_{in1} - V_{in2})$$

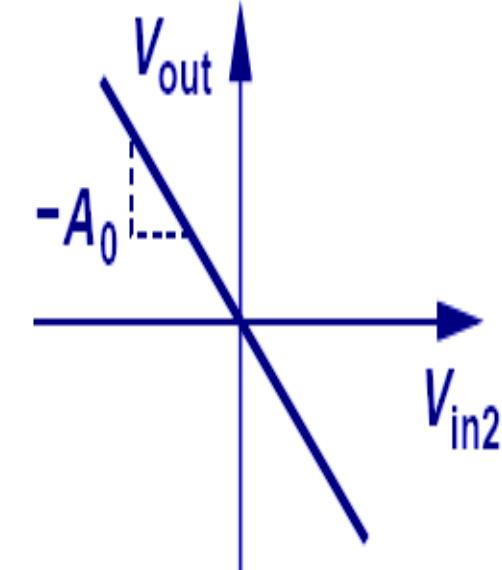
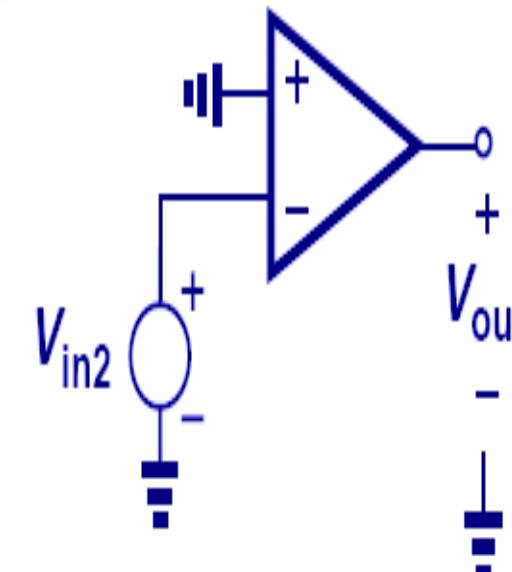
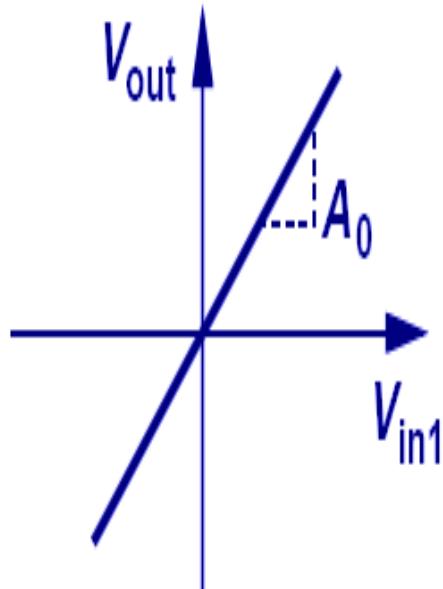
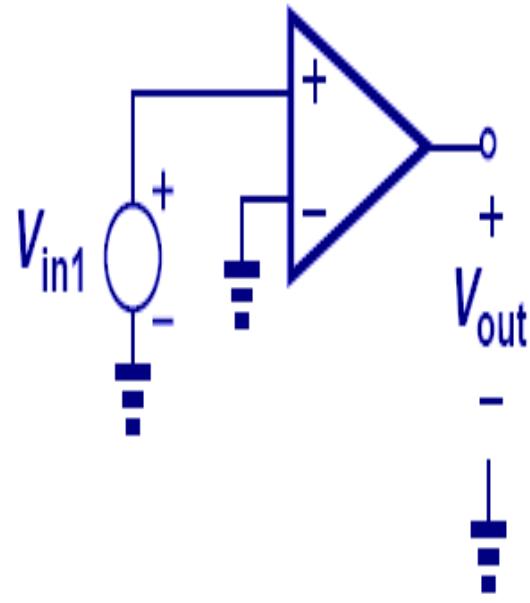
Op amp is a circuit that has two inputs and one output.  
It amplifies the difference between the two inputs.





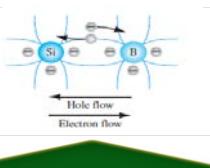
# Inverting and Non-inverting Op Amp

If the negative input is grounded, the gain is positive.



If the positive input is grounded, the gain is negative.





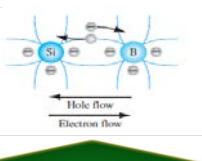
# Ideal Operational Amplifier

Infinite gain

(- a voltage difference at the two inputs  
is magnified infinitely)

(-meaning that the difference between  
+ and – terminal is amplified by say  
200000)





# Ideal Operational Amplifier

## Infinite input impedance

(-no current flows into the inputs)

(-impedance is about  $10^{12}\Omega$  for FET)

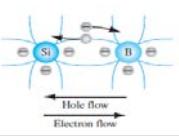
Zero output impedance

(-rock-solid independent of load )

Infinite speed

(-limited to few MHz range)





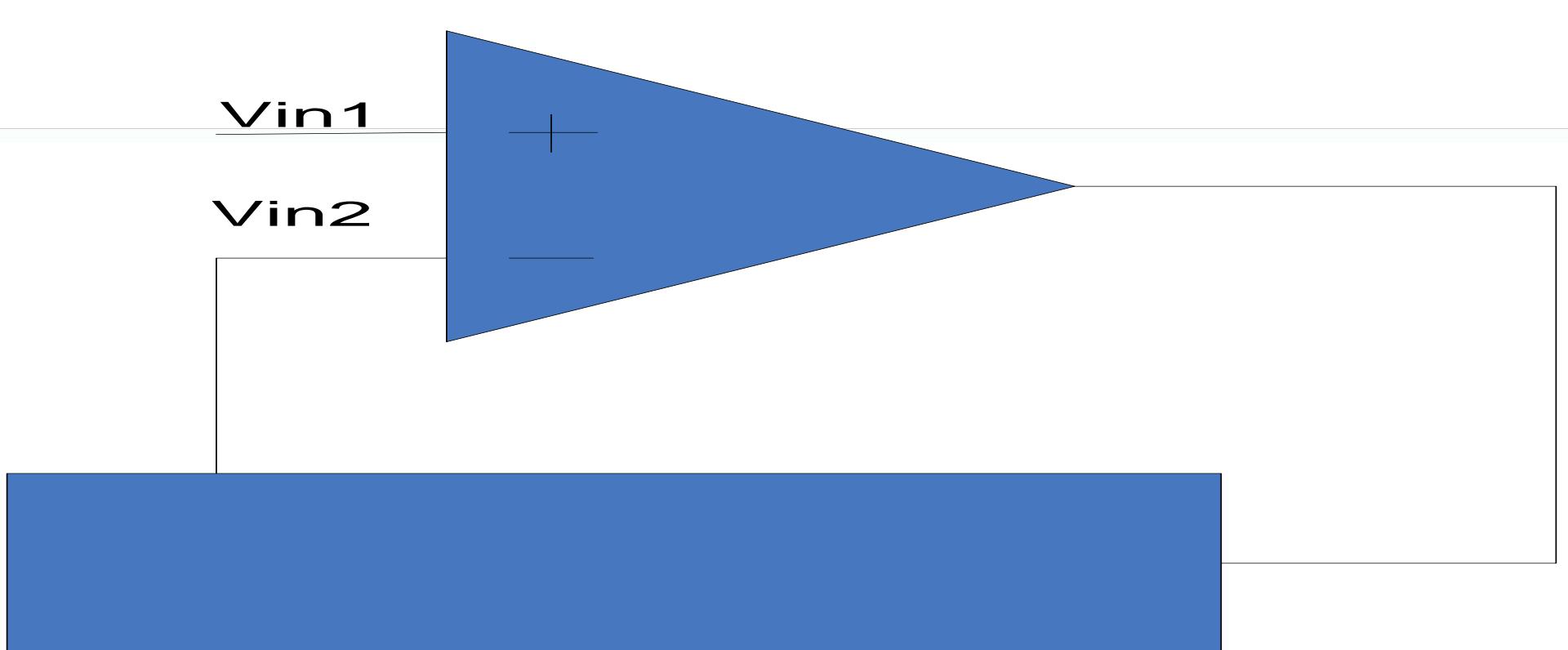
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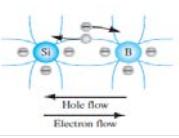


# Virtual Short



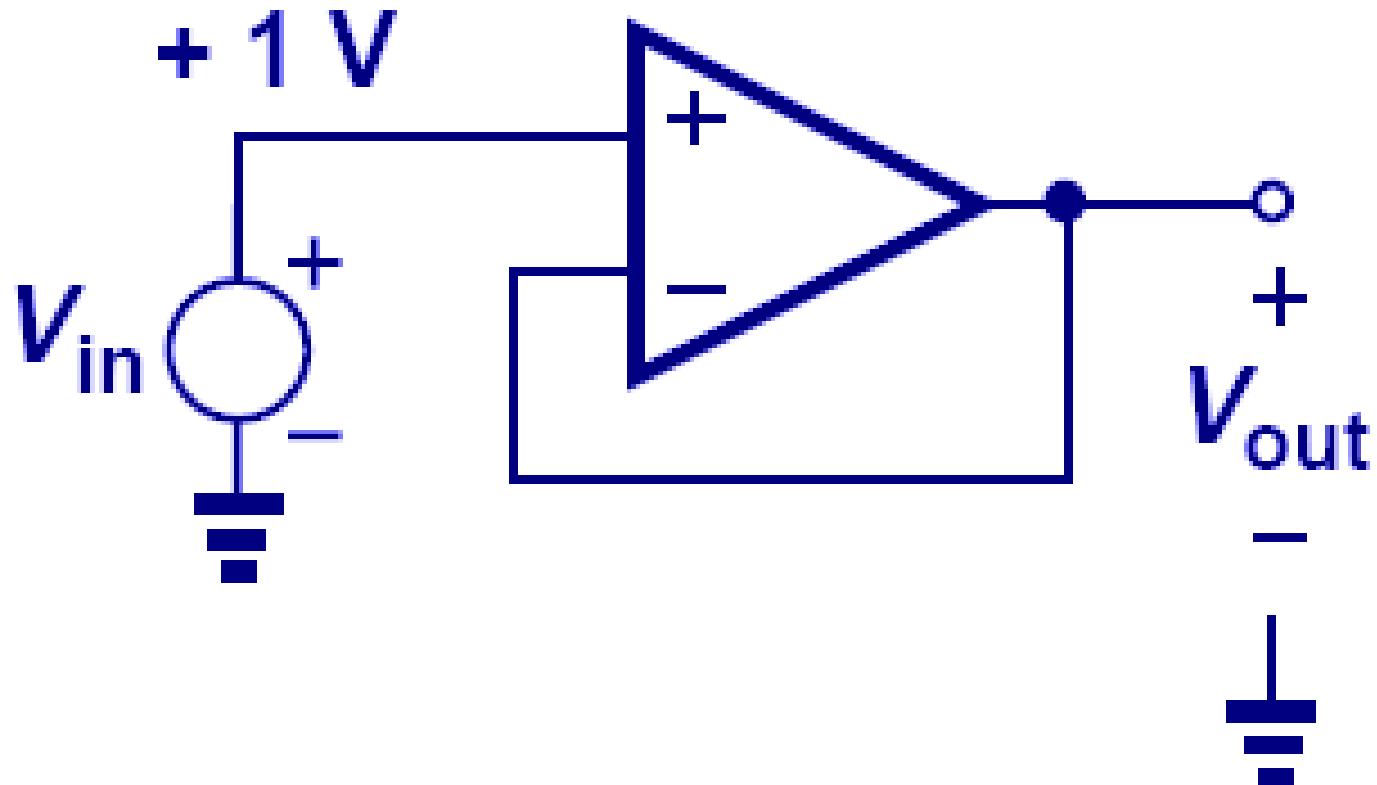
Due to infinite gain of op amp, the circuit forces  $V_{in2}$  to be close to  $V_{in1}$ , thus creating a virtual short.





# Unity Gain Amplifier

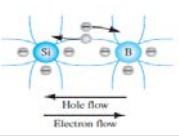
$$A_0 = 1000$$



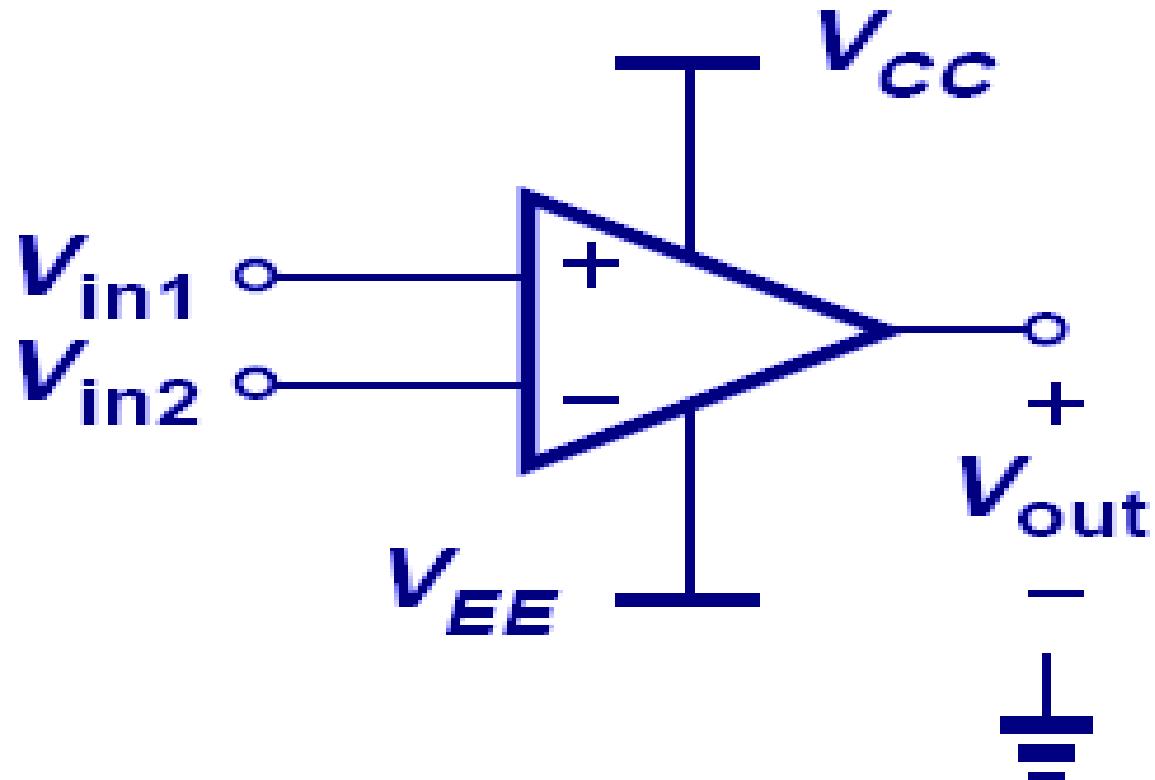
$$V_{out} = A_0(V_{in} - V_{out})$$

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + A_0}$$





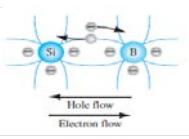
# Op Amp with Supply Rails



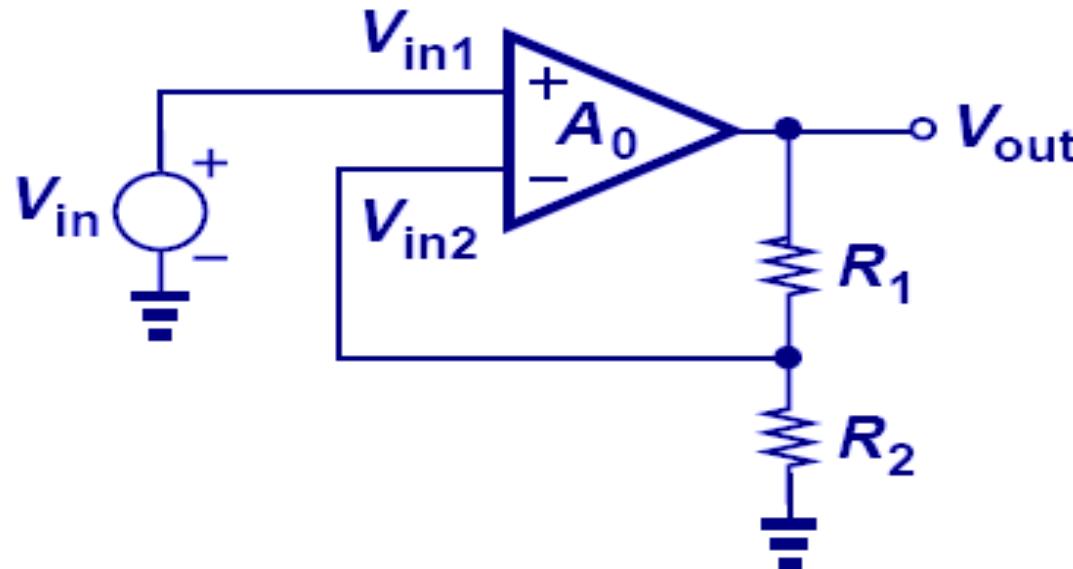
To explicitly show the supply voltages,  $V_{cc}$  and  $V_{ee}$  are shown.

In some cases,  $V_{ee}$  is zero.





# Noninverting Amplifier (Infinite $A_o$ )

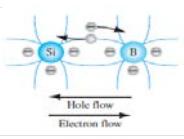


$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_1}{R_2}$$

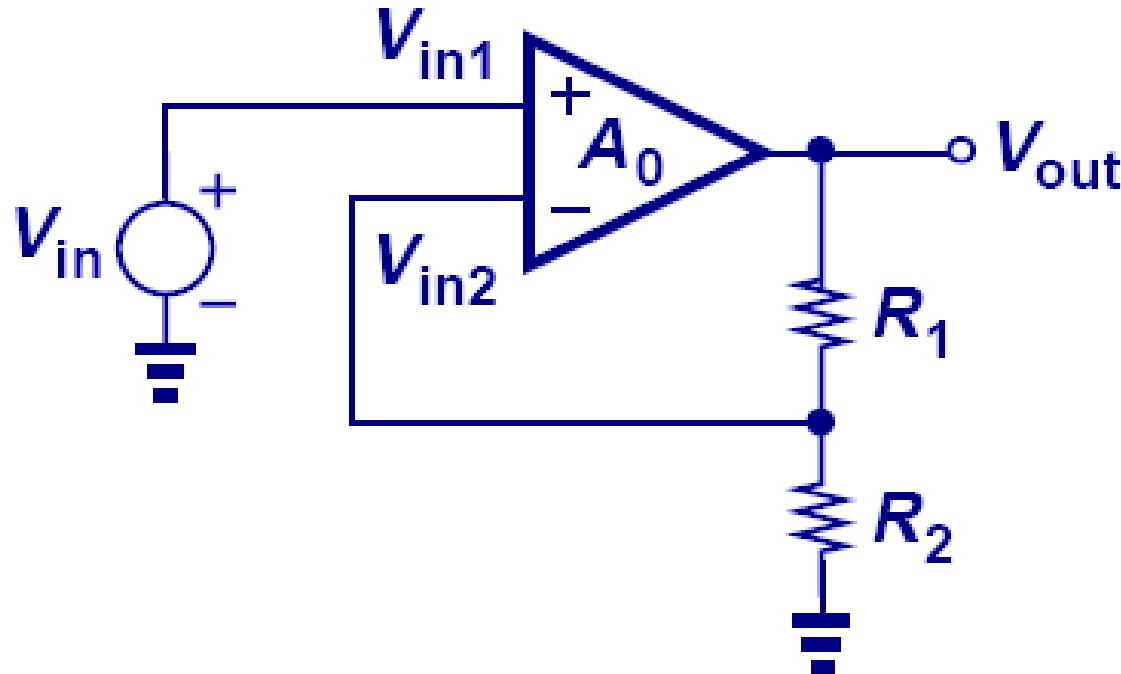
A noninverting amplifier returns a fraction of output signal thru a resistor divider to the negative input.

With a high  $A_o$ ,  $V_{out}/V_{in}$  depends only on ratio of resistors, which is very precise.





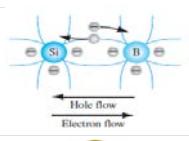
# Noninverting Amplifier (Finite $A_0$ )



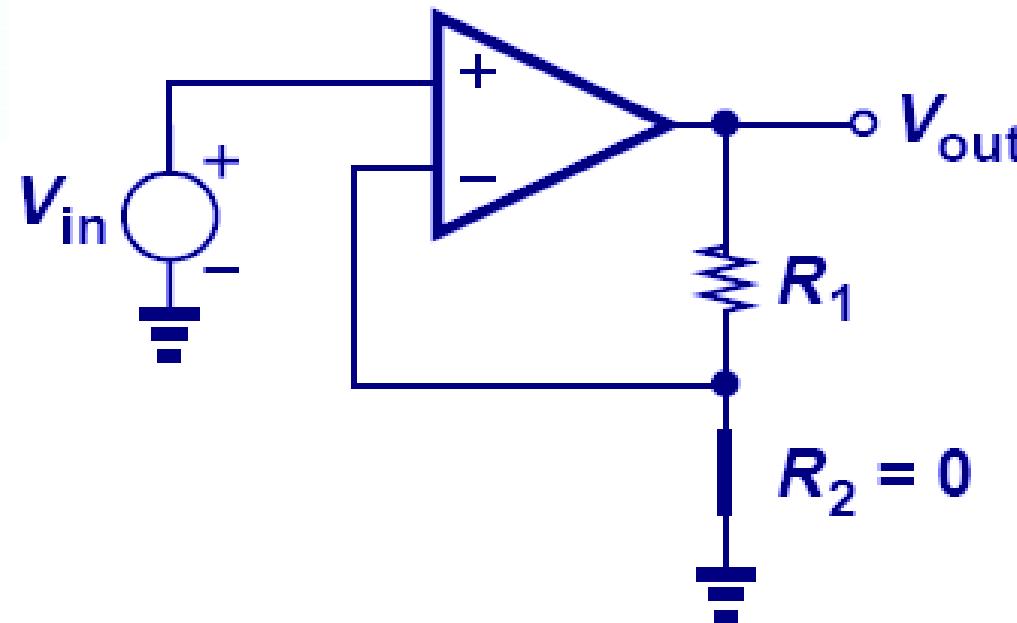
$$\frac{V_{out}}{V_{in}} \approx \left(1 + \frac{R_1}{R_2}\right) \left[ 1 - \left(1 + \frac{R_1}{R_2}\right) \frac{1}{A_0} \right]$$

The error term indicates that the larger the closed-loop gain, the less accurate the circuit becomes.

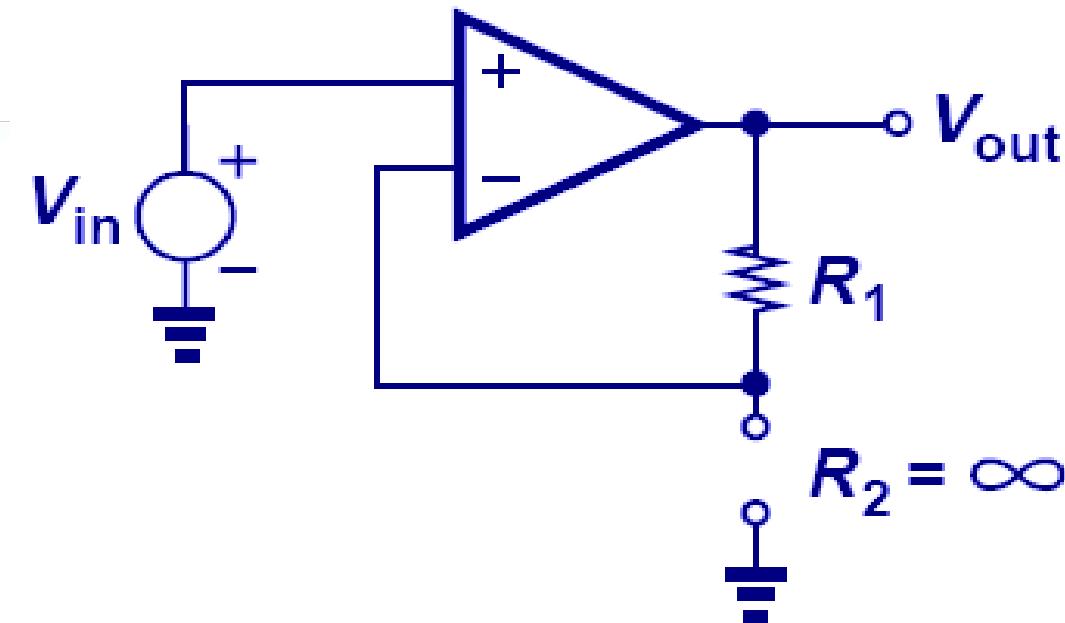




# Extreme Cases of $R_2$ (Infinite $A_0$ )

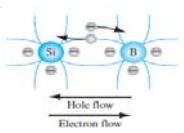


If  $R_2$  is zero, the loop is open and  $V_{\text{out}}/V_{\text{in}}$  is equal to the intrinsic gain of the op amp.

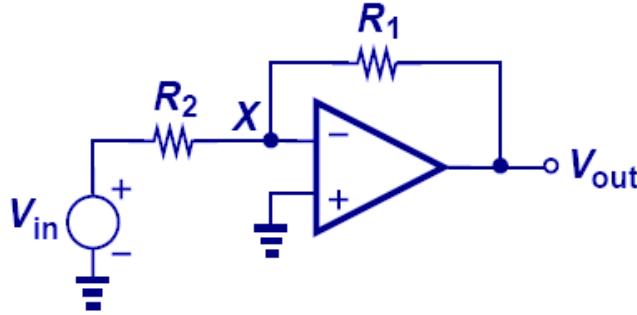


If  $R_2$  is infinite, the circuit becomes a unity-gain amplifier and  $V_{\text{out}}/V_{\text{in}}$  becomes equal to one.

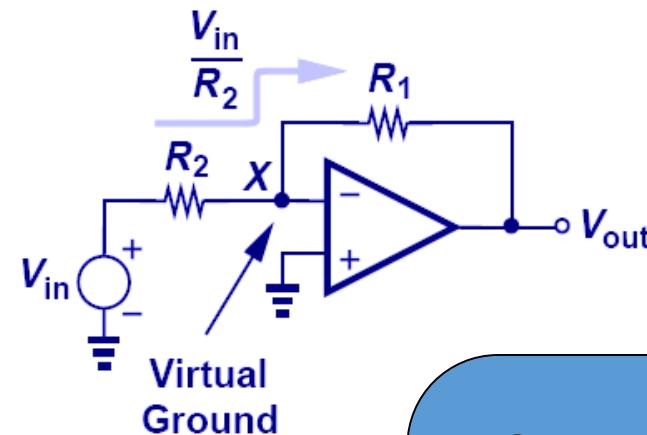




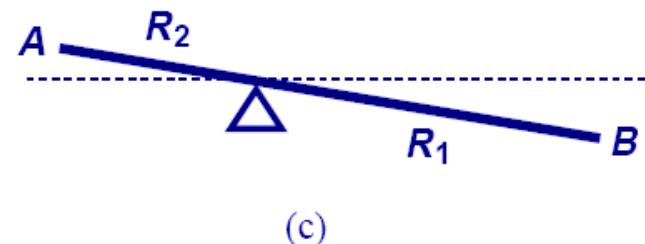
# Inverting Amplifier



(a)



(b)



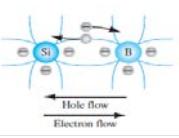
(c)

$$\frac{0 - V_{out}}{R_1} = \frac{V_{in}}{R_2}$$

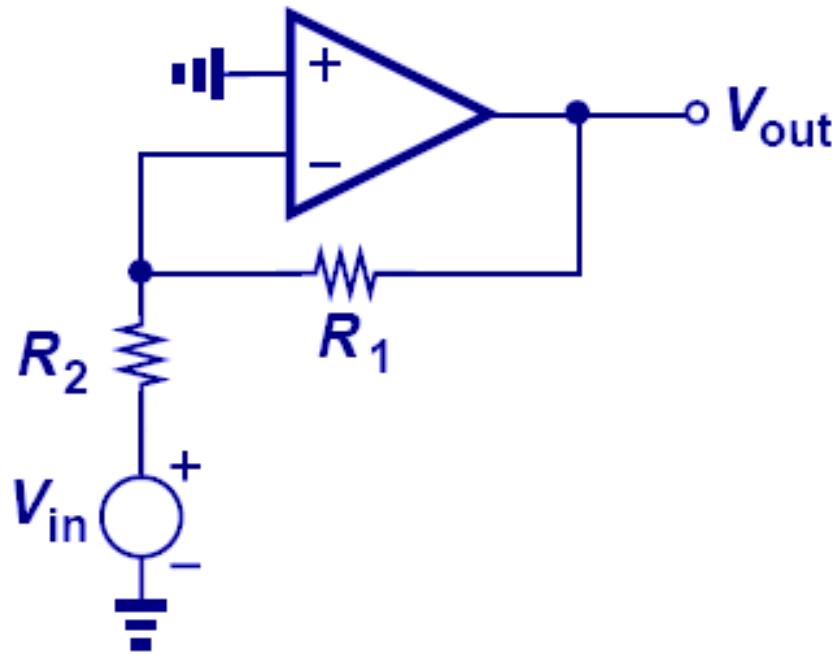
$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{R_2}$$

Infinite  $A_0$  forces the negative input to be a virtual ground.

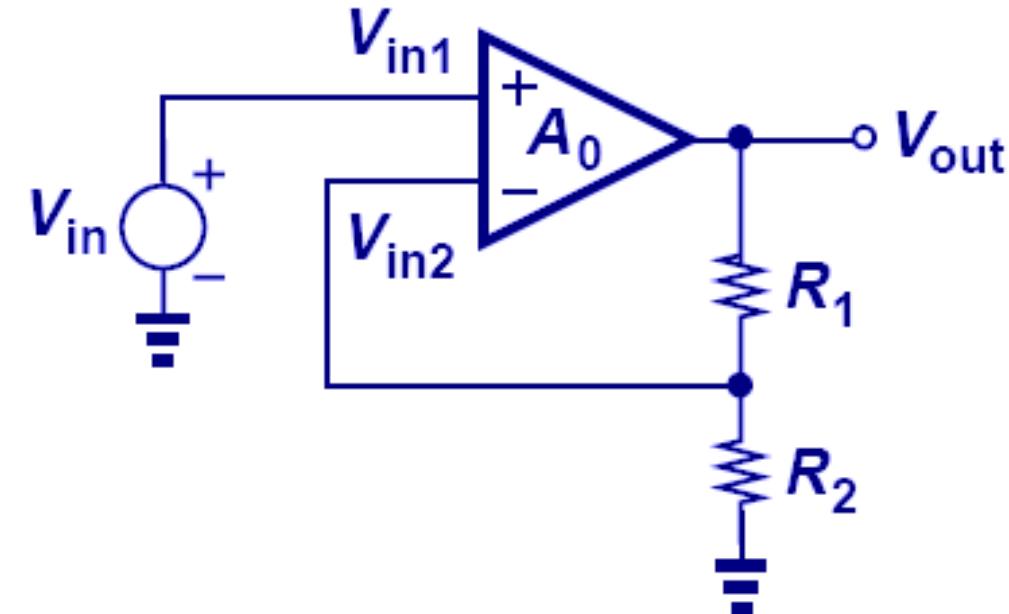




# Another View of Inverting Amplifier

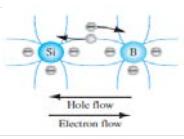


Inverting

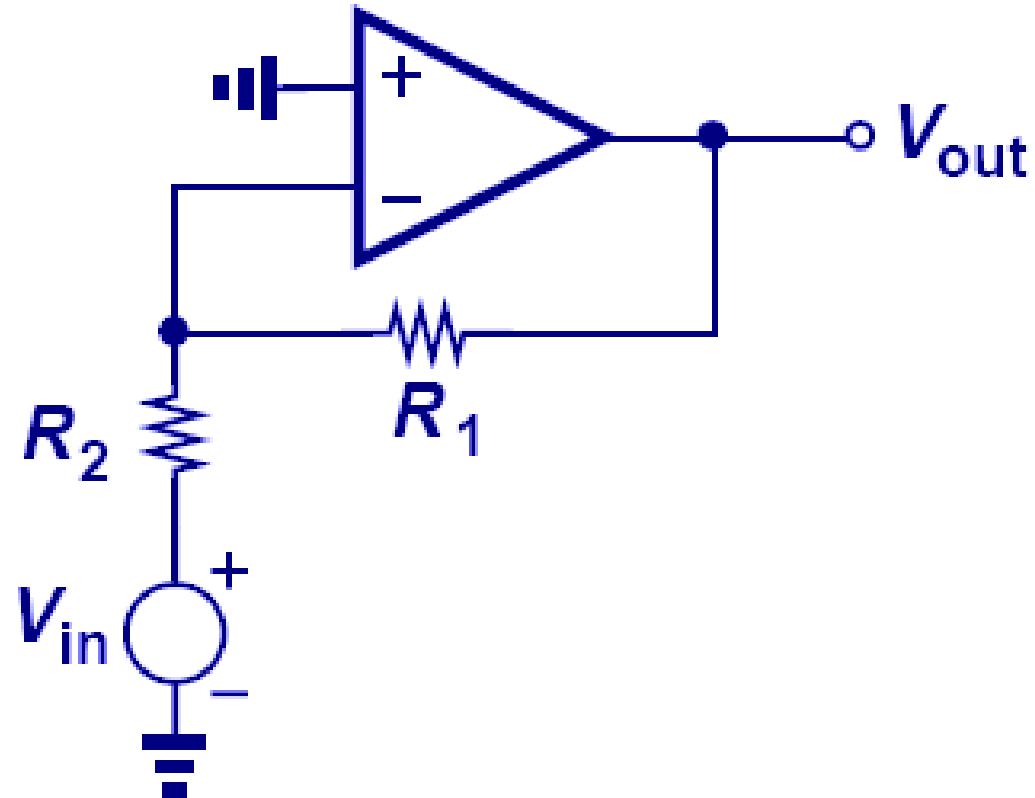


Noninverting





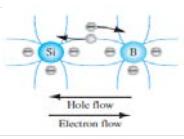
# Gain Error Due to Finite $A_0$



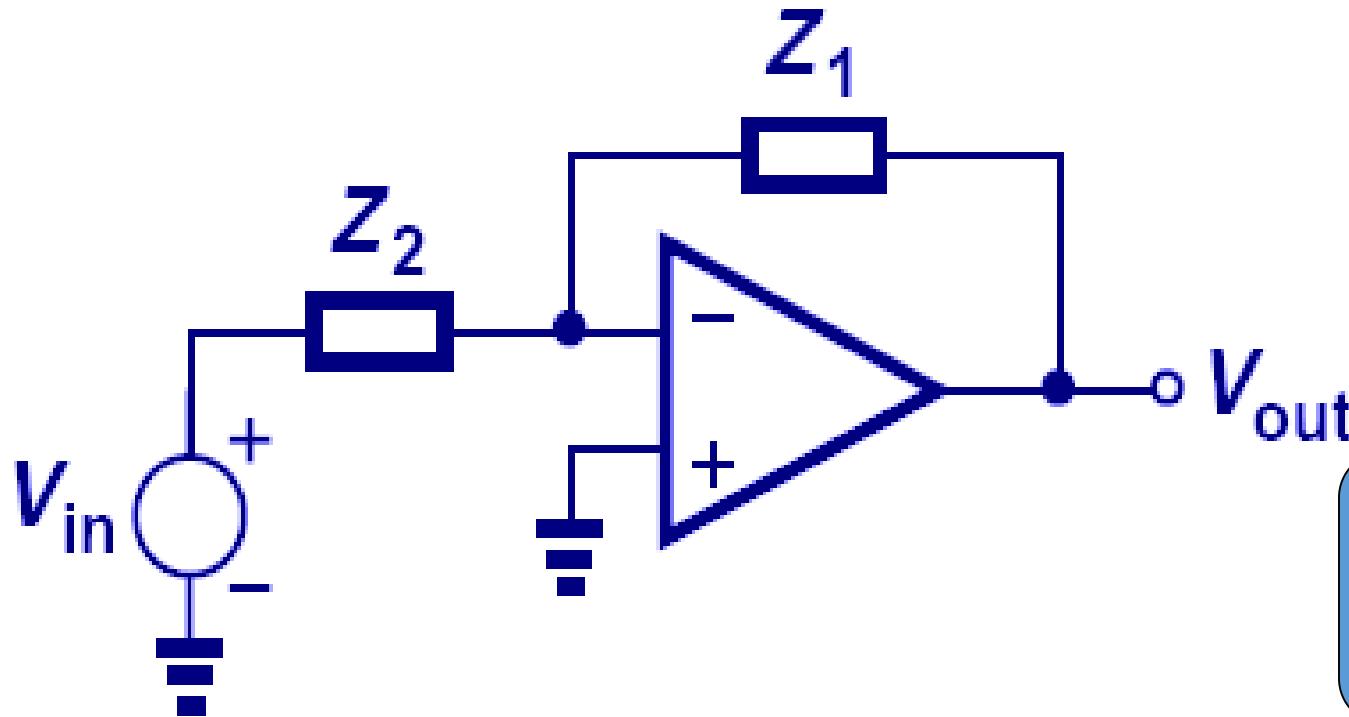
$$\frac{V_{out}}{V_{in}} \approx -\frac{R_1}{R_2} \left[ 1 - \frac{1}{A_0} \left( 1 + \frac{R_1}{R_2} \right) \right]$$

The larger the closed loop gain, the more inaccurate the circuit is.





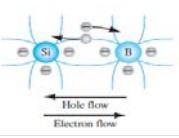
# Complex Impedances Around the Op Amp



$$\frac{V_{out}}{V_{in}} \approx -\frac{Z_1}{Z_2}$$

The closed-loop gain is still equal to the ratio of two impedances.





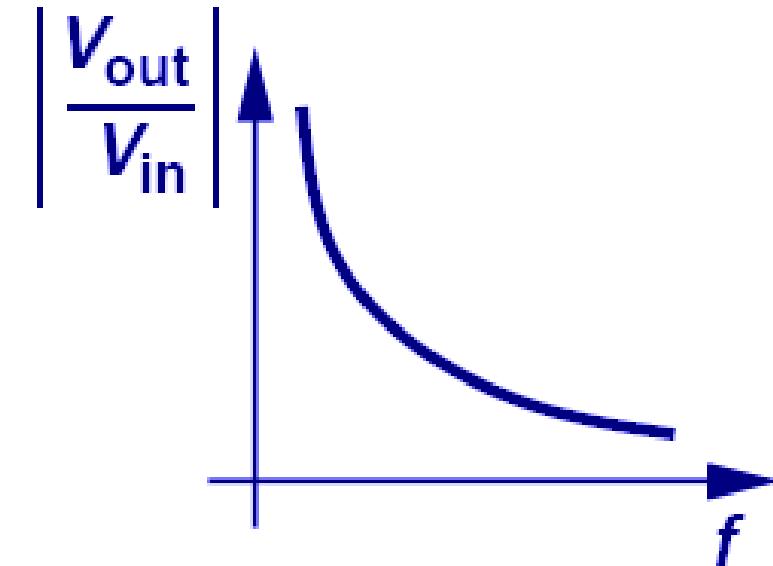
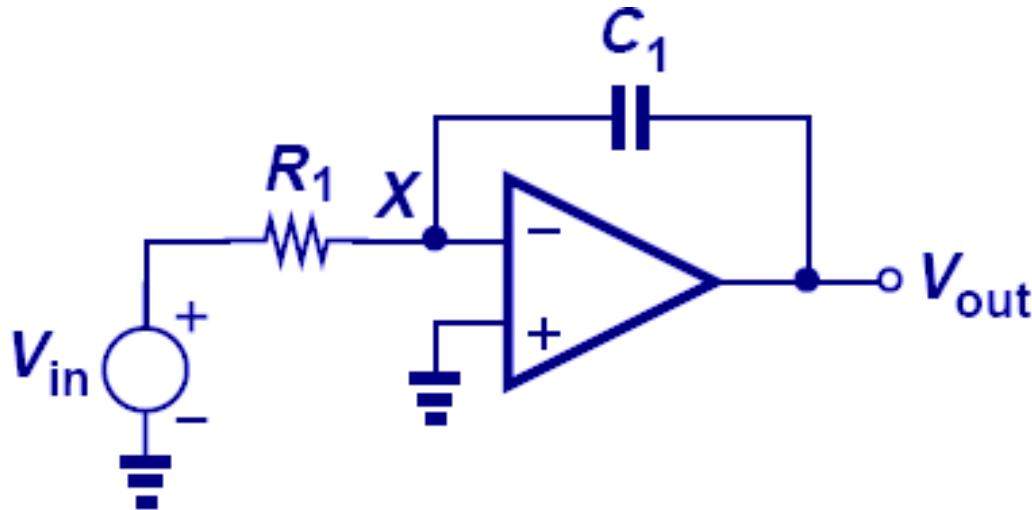
# SEMICONDUCTOR DEVICES

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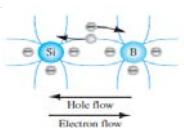
# Integrator



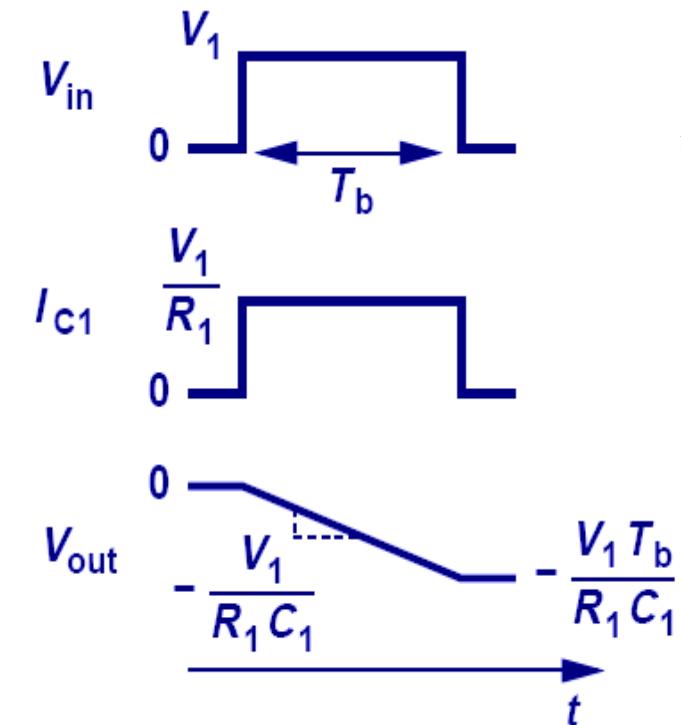
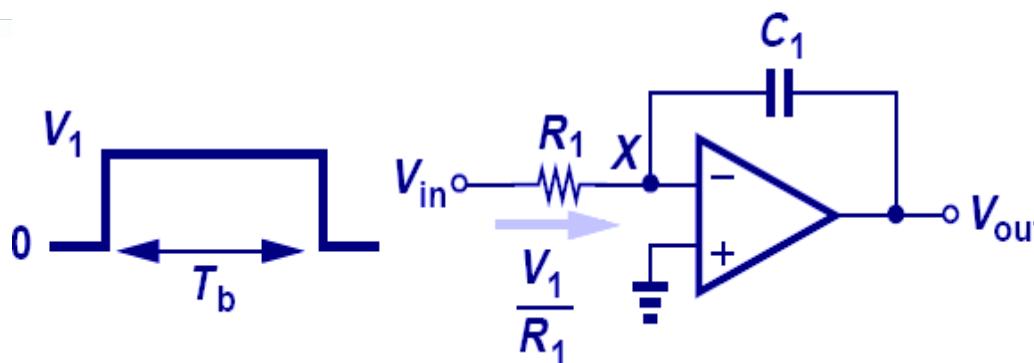
$$\frac{V_{out}}{V_{in}} = -\frac{1}{R_1 C_1 s}$$

$$V_{out} = -\frac{1}{R_1 C_1} \int V_{in} dt$$



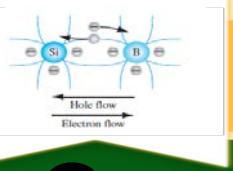


# Integrator with Pulse Input

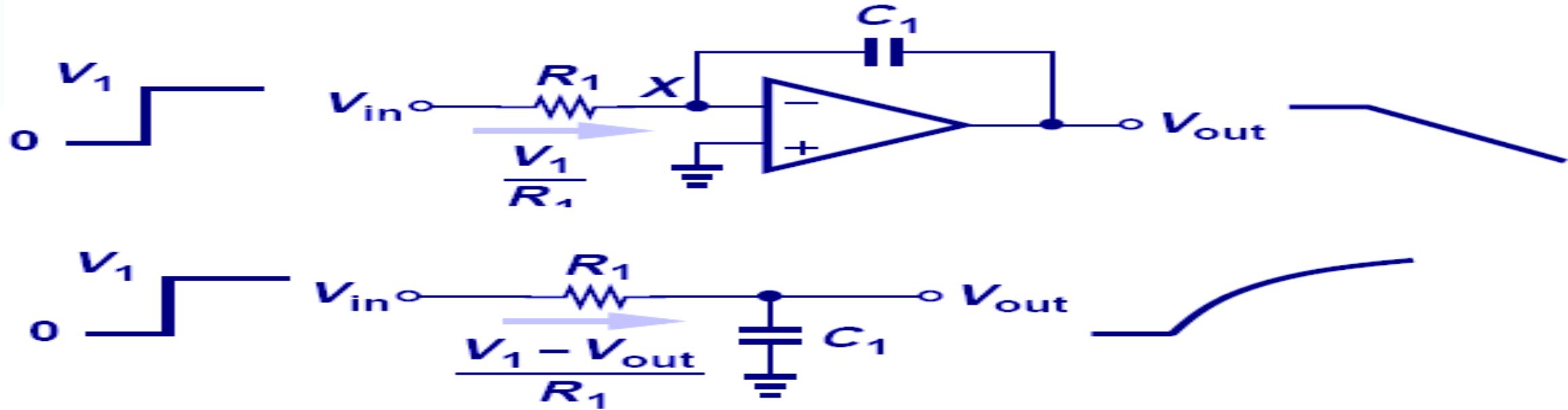


$$V_{out} = -\frac{1}{R_1 C_1} \int V_{in} dt = -\frac{V_1}{R_1 C_1} t \quad 0 < t < T_b$$





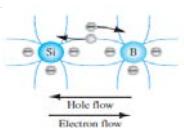
# Comparison of Integrator and RC Lowpass Filter



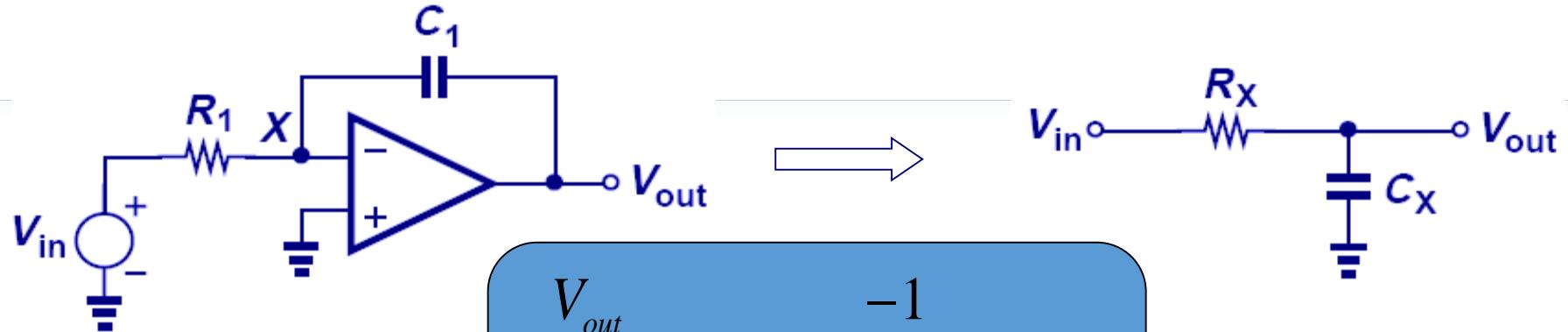
The RC low-pass filter is actually a “passive” approximation to an integrator.

With the RC time constant large enough, the RC filter output approaches a ramp.





# Lossy Integrator

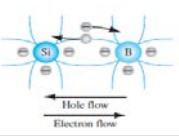


$$\frac{V_{out}}{V_{in}} = \frac{-1}{\frac{1}{A_0} + \left(1 + \frac{1}{A_0}\right)R_1 C_1 s}$$

When finite op amp gain is considered, the integrator becomes lossy as the pole moves from the origin to  $-1/[(1+A_0)R_1C_1]$ .

It can be approximated as an RC circuit with C boosted by a factor of  $A_0+1$ .





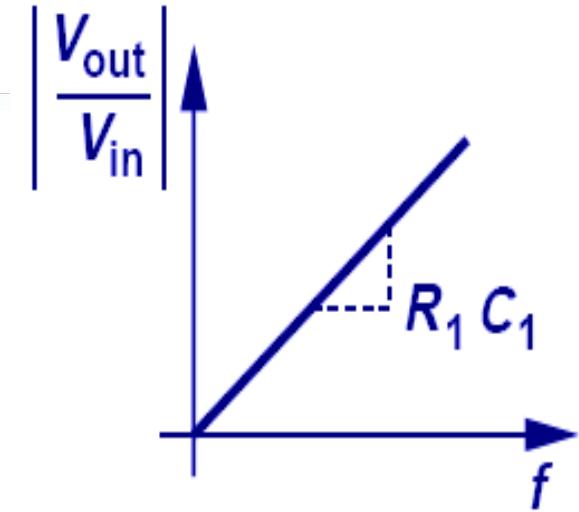
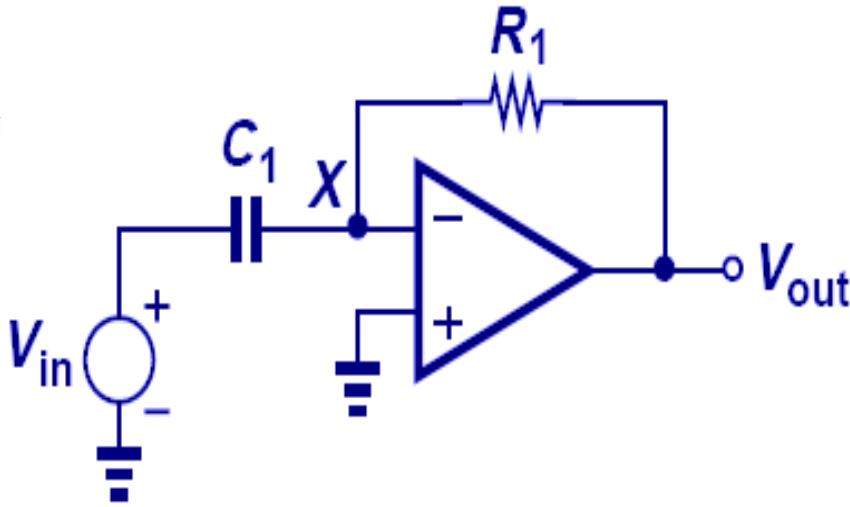
# SEMICONDUCTOR DEVICES

## DEPARTMENT OF COMPUTER ENGINEERING

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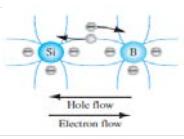
# Differentiator



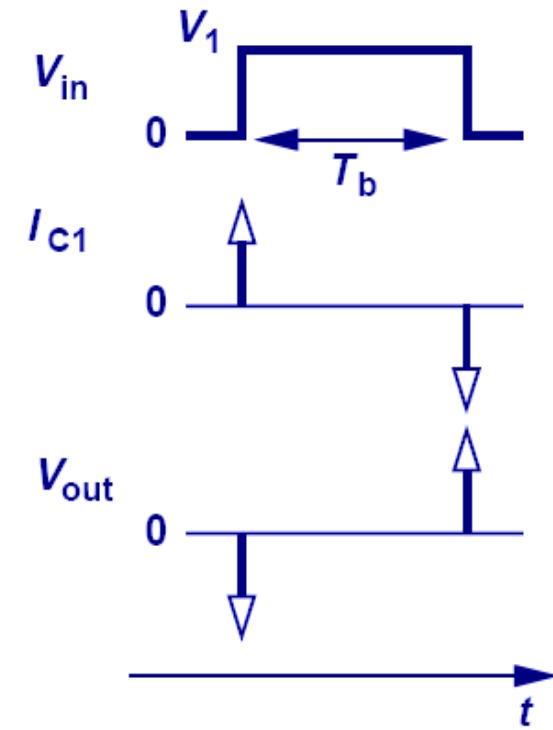
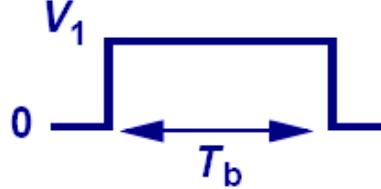
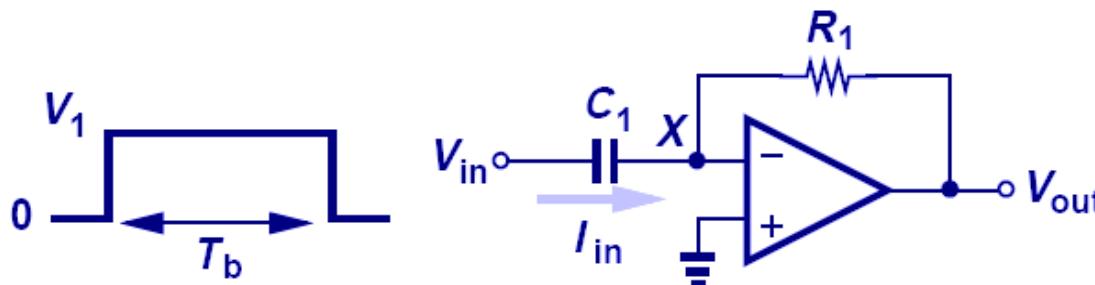
$$V_{out} = -R_1 C_1 \frac{dV_{in}}{dt}$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{1} = -R_1 C_1 s$$



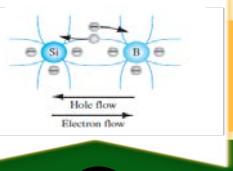


# Differentiator with Pulse Input

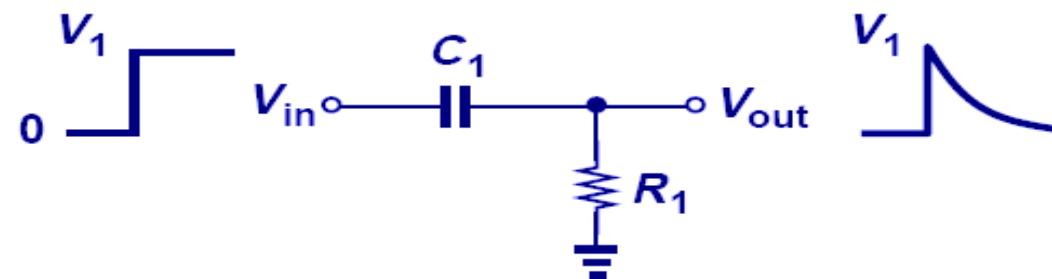
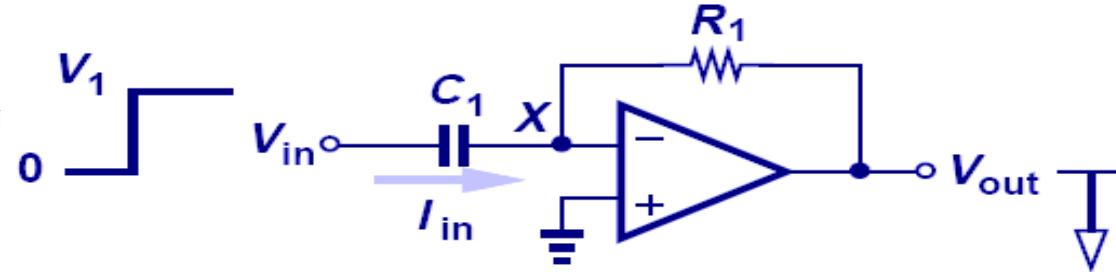


$$V_{out} = \mp R_1 C_1 V_1 \delta(t)$$





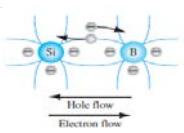
# Comparison of Differentiator and High-Pass Filter



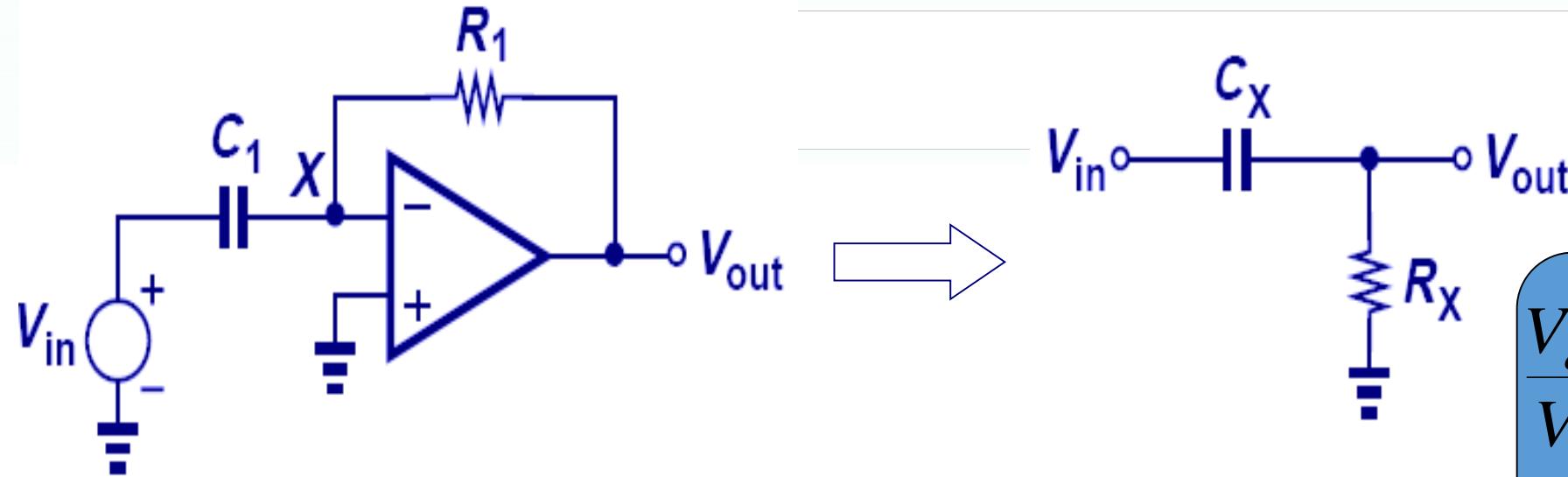
The RC high-pass filter is actually a passive approximation to the differentiator.

When the RC time constant is small enough, the RC filter approximates a differentiator.





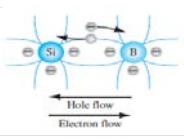
# Lossy Differentiator



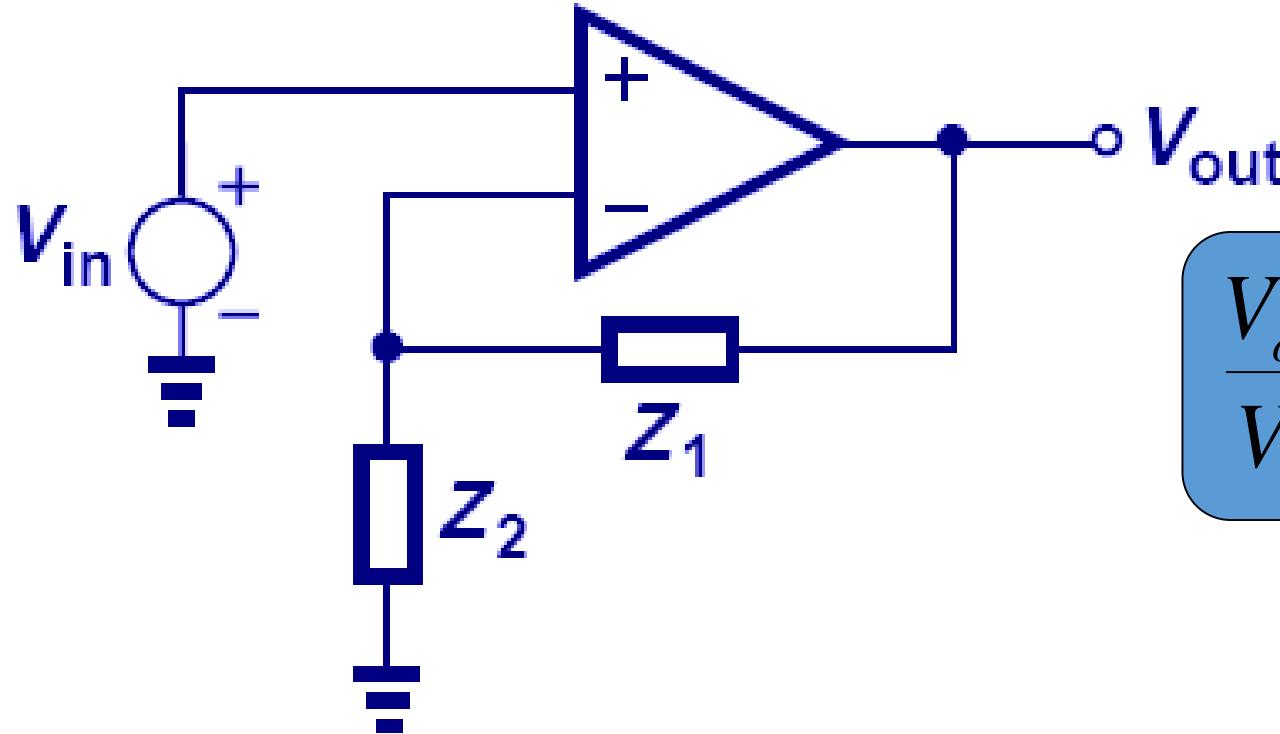
$$\frac{V_{out}}{V_{in}} = \frac{-R_1 C_1 s}{1 + \frac{1}{A_0} + \frac{R_1 C_1 s}{A_0}}$$

When finite op amp gain is considered, the differentiator becomes lossy as the zero moves from the origin to  $-(A_0+1)/R_1 C_1$ . It can be approximated as an RC circuit with R reduced by a factor of  $(A_0+1)$ .





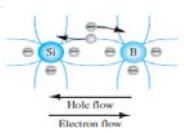
# Op Amp with General Impedances



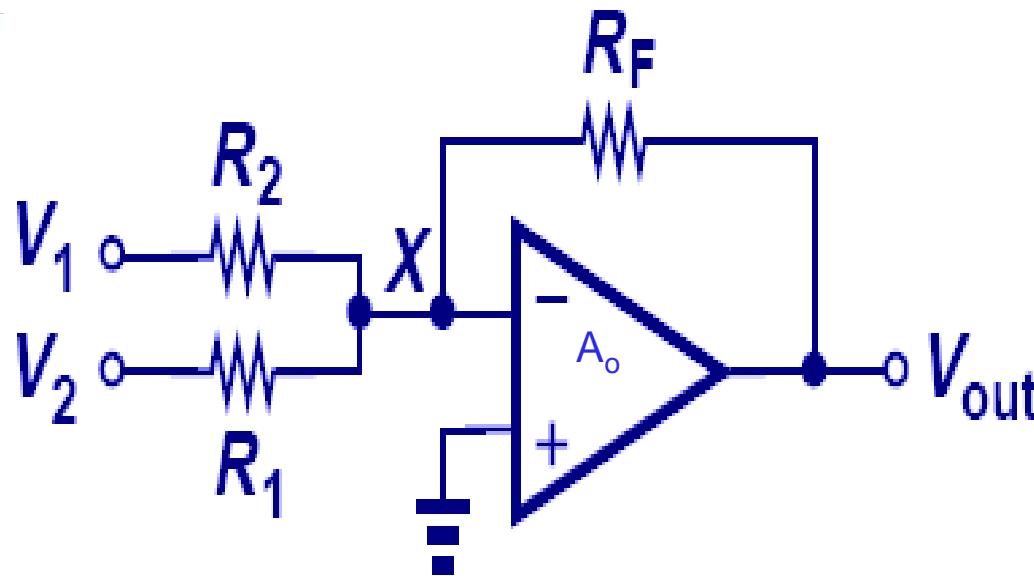
$$\frac{V_{out}}{V_{in}} = 1 + \frac{Z_1}{Z_2}$$

This circuit cannot operate as ideal integrator or differentiator.





# Voltage Adder



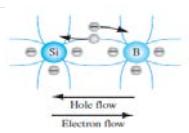
$$V_{out} = -R_F \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} \right)$$

$$V_{out} = -\frac{R_F}{R} (V_1 + V_2)$$

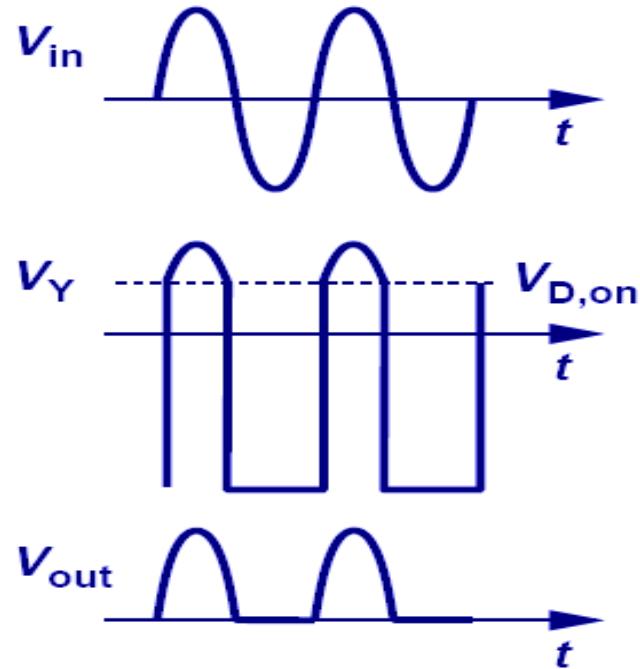
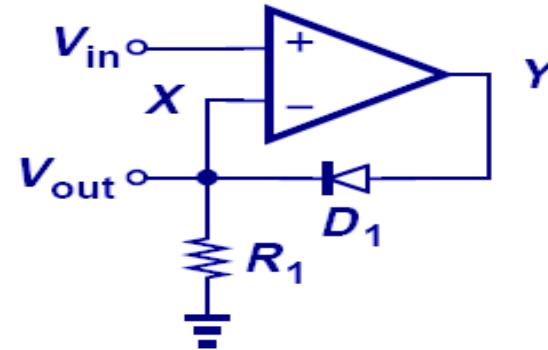
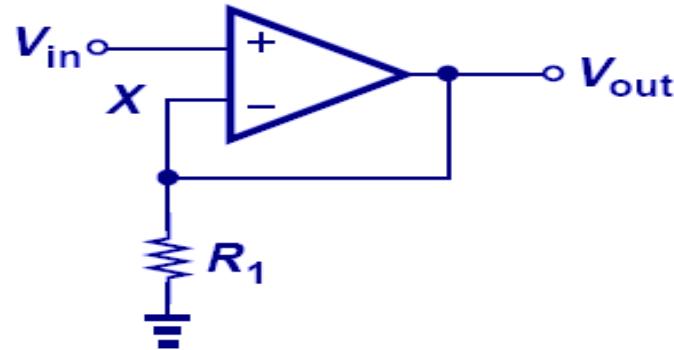
If  $R_1 = R_2 = R$

If  $A_o$  is infinite, X is pinned at ground, currents proportional to  $V_1$  and  $V_2$  will flow to X and then across  $R_F$  to produce an output proportional to the sum of two voltages.





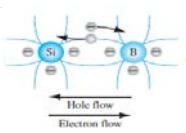
# Precision Rectifier



When  $V_{in}$  is positive, the circuit in b) behaves like that in a), so the output follows input.

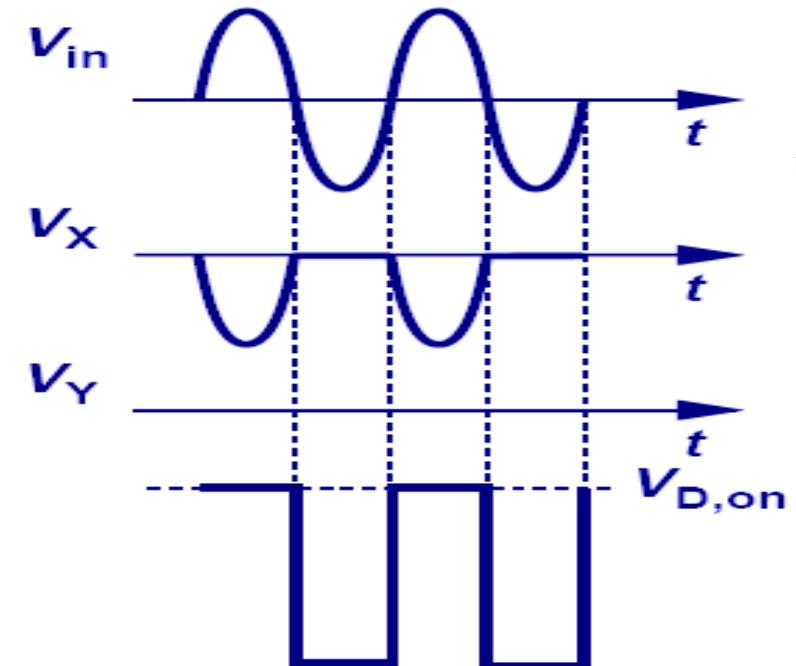
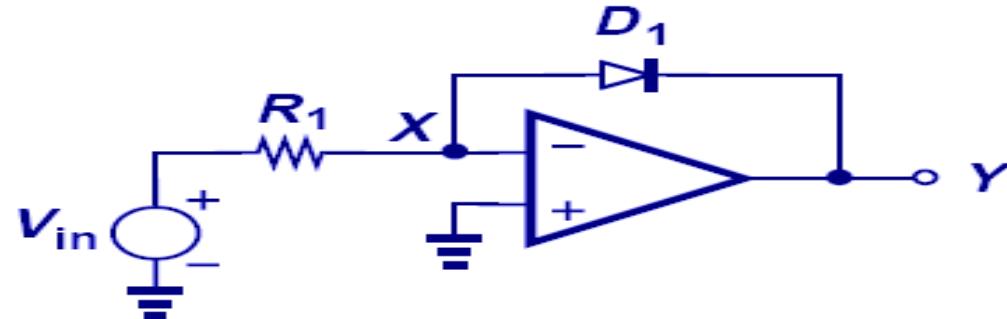
When  $V_{in}$  is negative, the diode opens, and the output drops to zero. Thus performing rectification.





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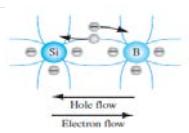
# Inverting Precision Rectifier



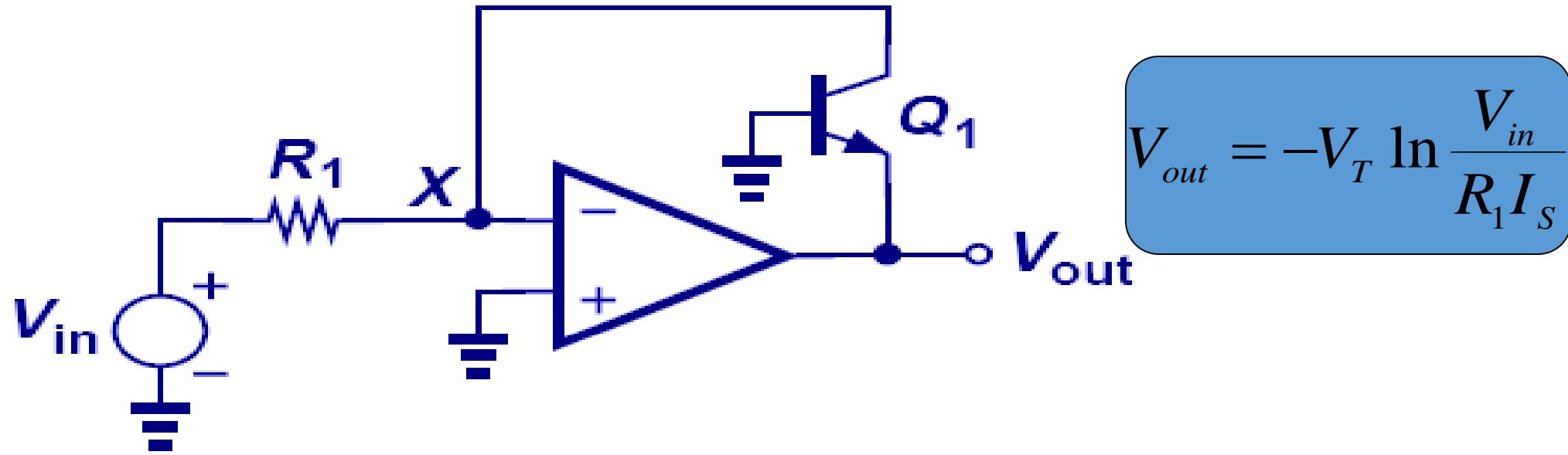
When  $V_{in}$  is positive, the diode is on,  $V_y$  is pinned around  $V_{D,on}$ , and  $V_x$  at virtual ground.

When  $V_{in}$  is negative, the diode is off,  $V_y$  goes extremely negative, and  $V_x$  becomes equal to  $V_{in}$ .





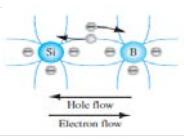
# Logarithmic Amplifier



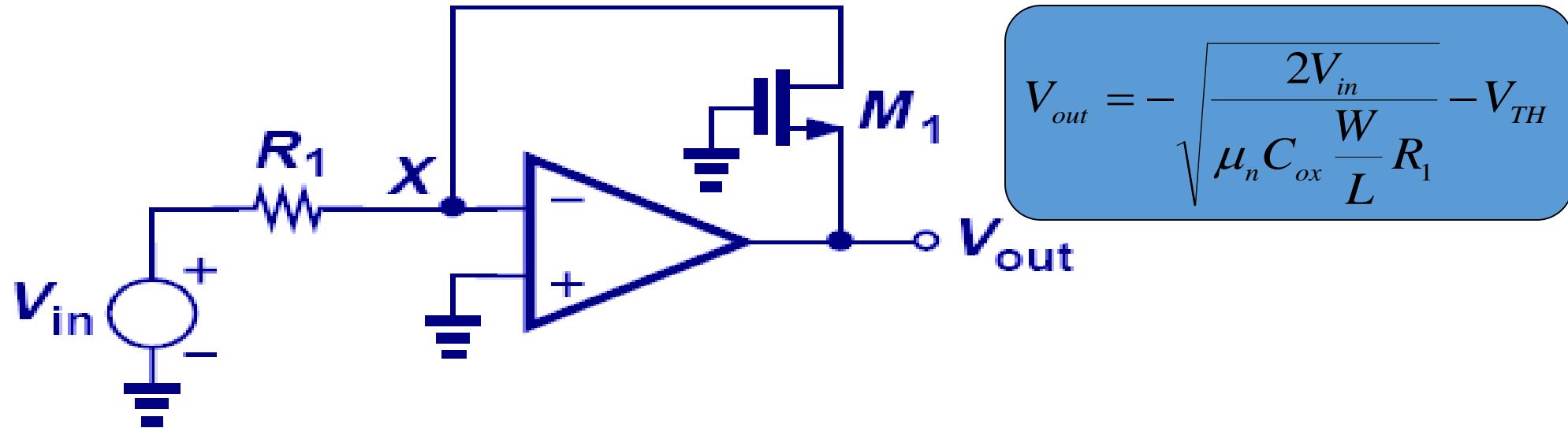
By inserting a bipolar transistor in the loop, an amplifier with logarithmic characteristic can be constructed.

This is because the current to voltage conversion of a bipolar transistor is a natural logarithm.



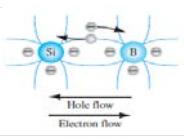


# Square-Root Amplifier

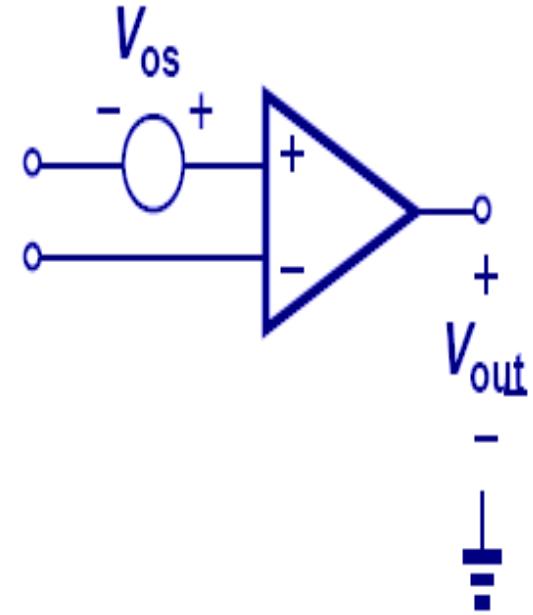
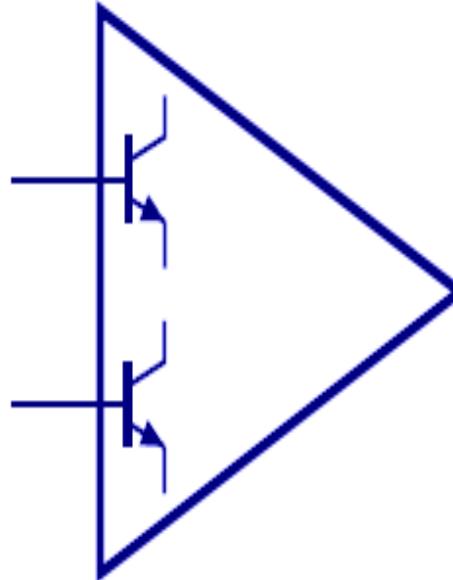
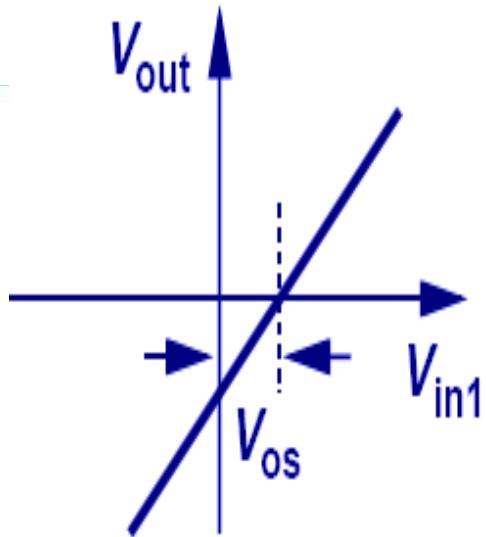


By replacing the bipolar transistor with a MOSFET, an amplifier with a square-root characteristic can be built. This is because the current to voltage conversion of a MOSFET is square-root.



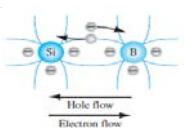


# Op Amp Nonidealities: DC Offsets

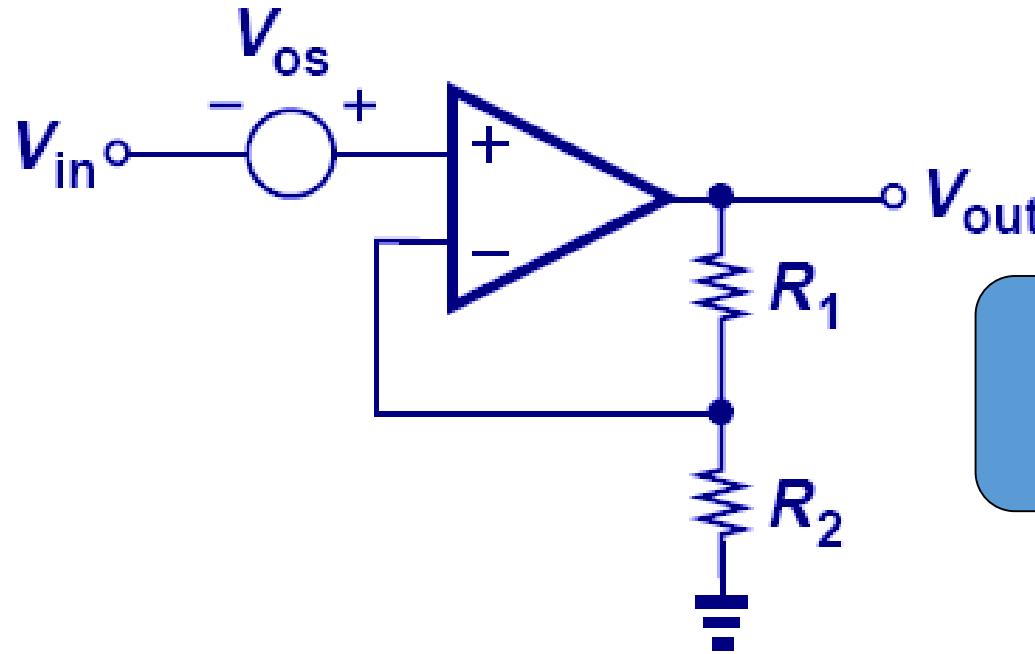


Offsets in an op amp that arise from input stage mismatch cause the input-output characteristic to shift in either the positive or negative direction (the plot displays positive direction).





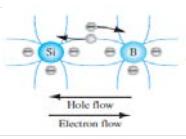
# Effects of DC Offsets



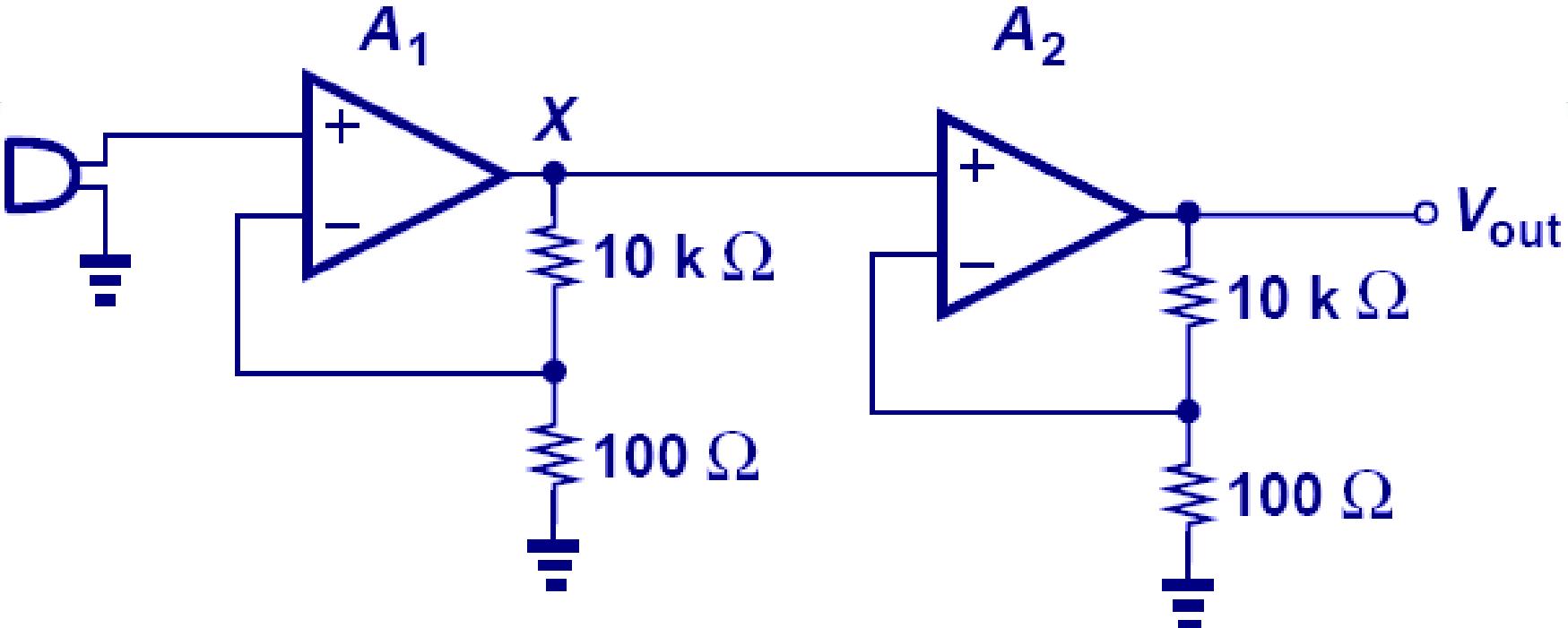
$$V_{out} = \left(1 + \frac{R_1}{R_2}\right)(V_{in} + V_{os})$$

As it can be seen, the op amp amplifies the input as well as the offset, thus creating errors.



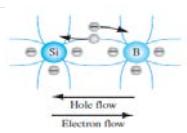


# Saturation Due to DC Offsets

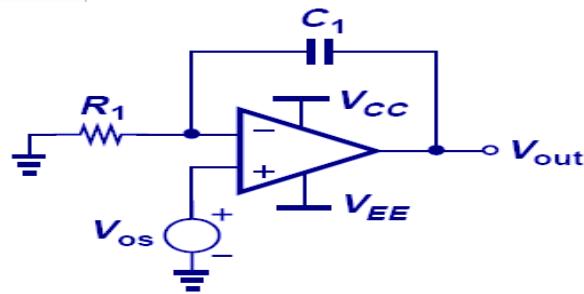


Since the offset will be amplified just like the input signal, output of the first stage may drive the second stage into saturation.

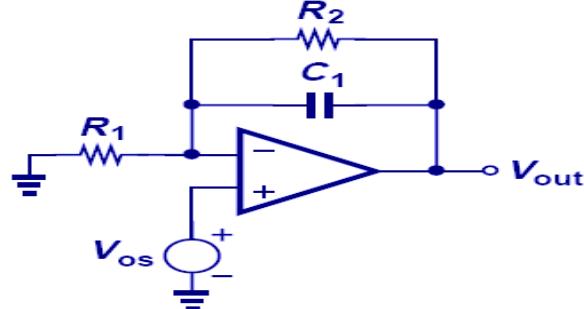




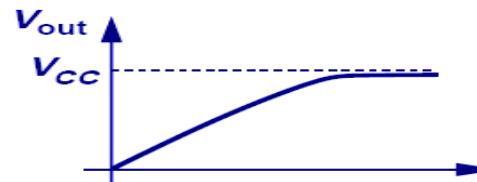
# Offset in Integrator



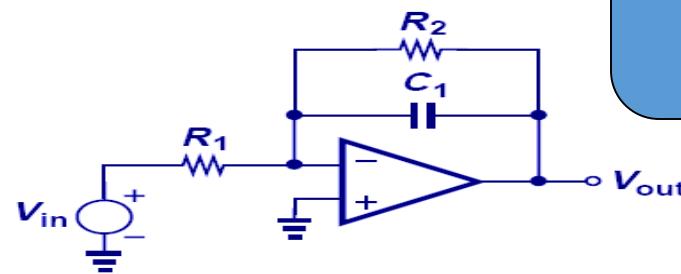
(a)



(c)



(b)

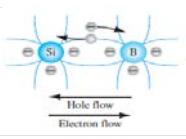


(d)

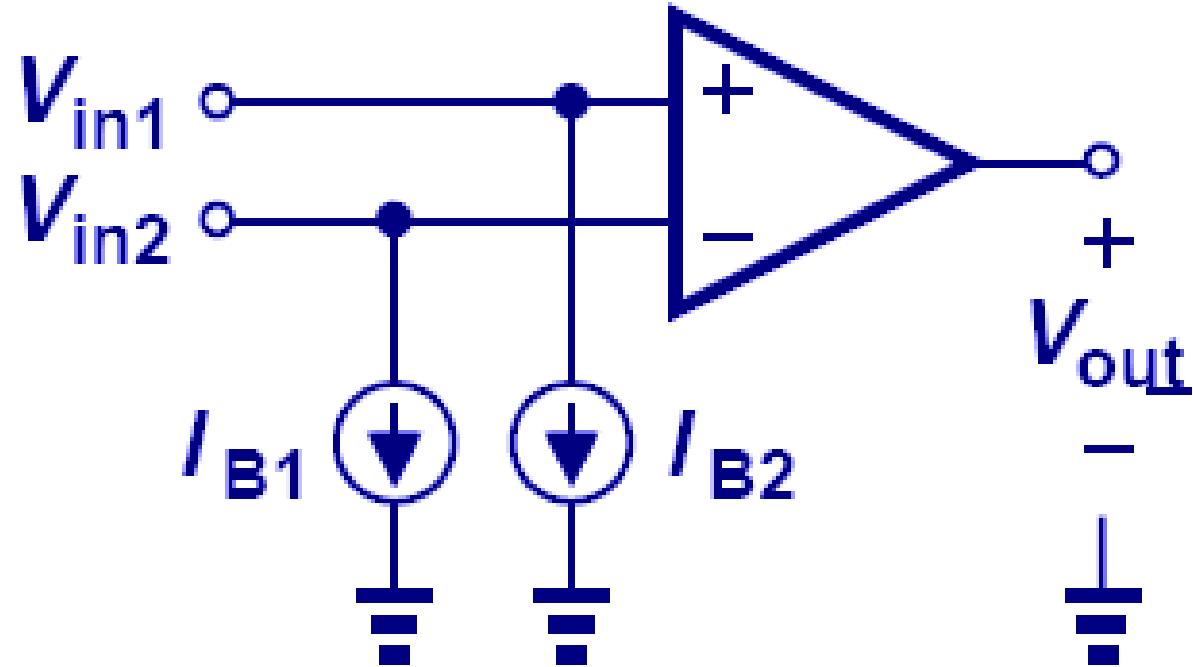
$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \frac{1}{R_2 C_1 s + 1}$$

A resistor can be placed in parallel with the capacitor to “absorb” the offset. However, this means the closed-loop transfer function no longer has a pole at origin.



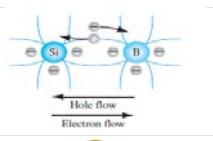


# Input Bias Current

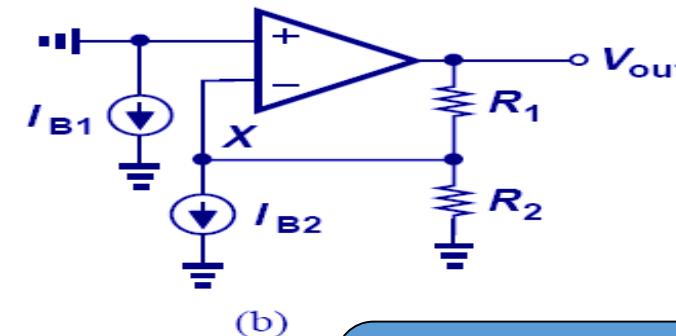
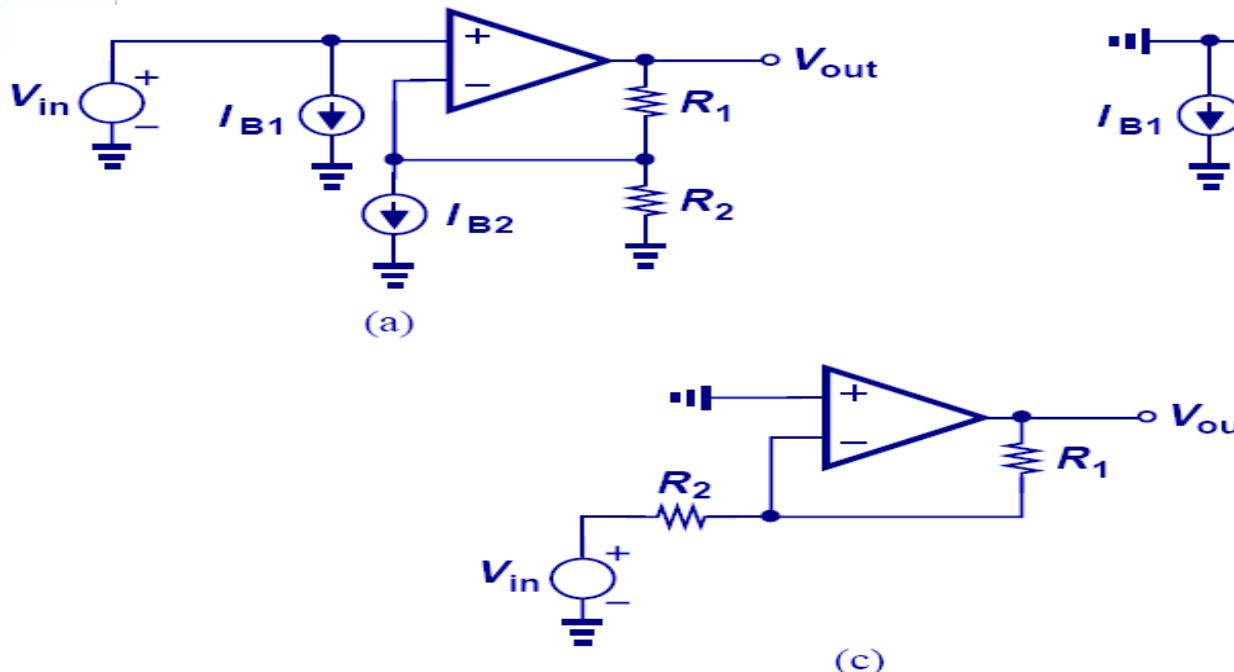


The effect of bipolar base currents can be modeled as current sources tied from the input to ground.





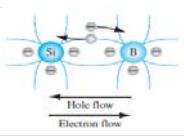
# Effects of Input Bias Current on Noninverting Amplifier



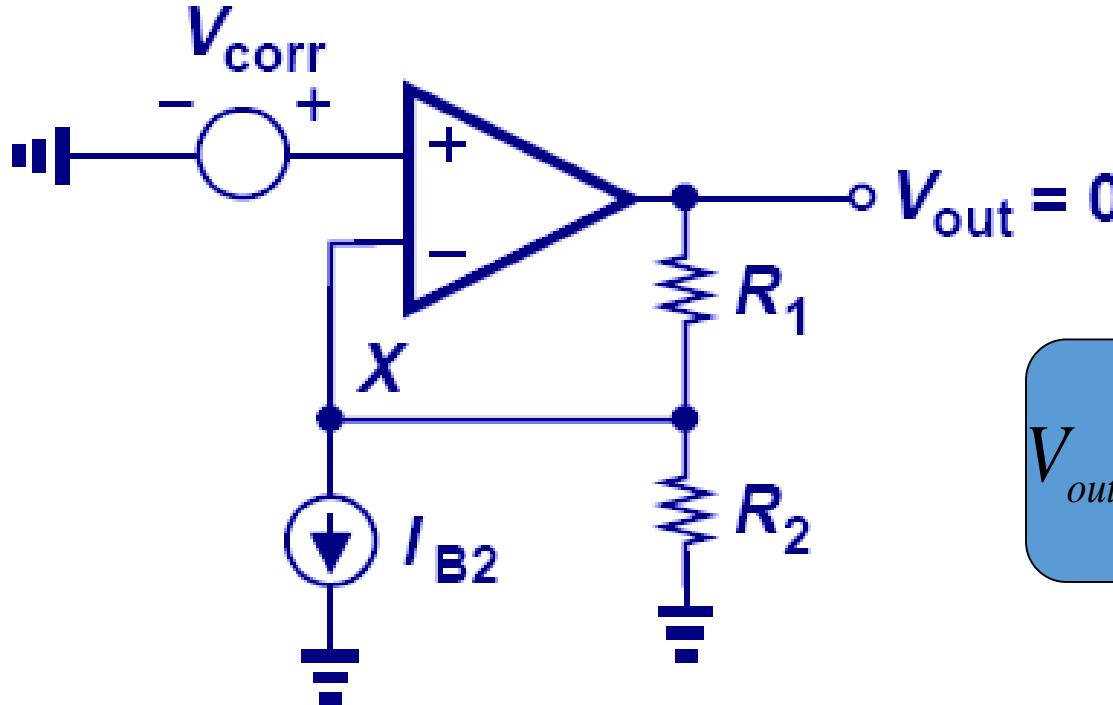
$$V_{out} = -R_2 I_{B2} \left( -\frac{R_1}{R_2} \right) = R_1 I_{B2}$$

It turns out that  $I_{B1}$  has no effect on the output and  $I_{B2}$  affects the output by producing a voltage drop across  $R_1$ .





# Input Bias Current Cancellation

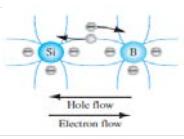


$$V_{out} = V_{corr} \left( 1 + \frac{R_1}{R_2} \right) + I_{B2} R_1$$

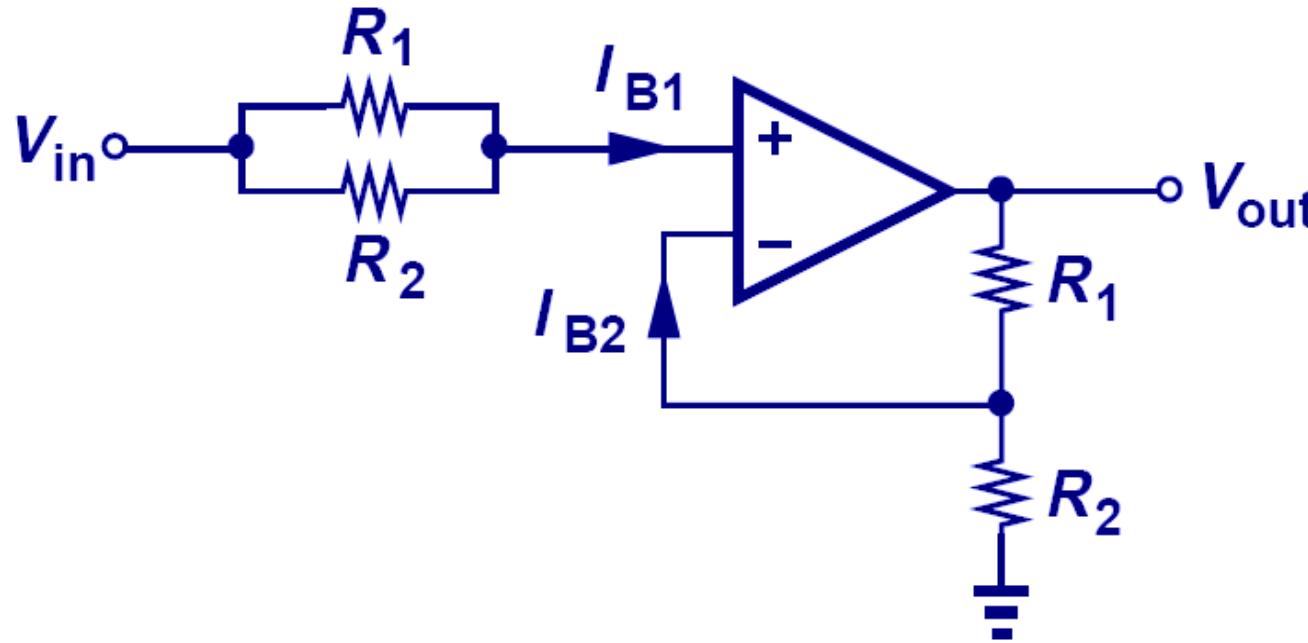
We can cancel the effect of input bias current by inserting a correction voltage in series with the positive terminal.

In order to produce a zero output,  $V_{corr} = -I_{B2}(R_1 || R_2)$ .





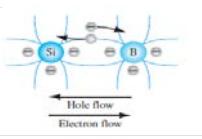
# Correction for $\beta$ Variation



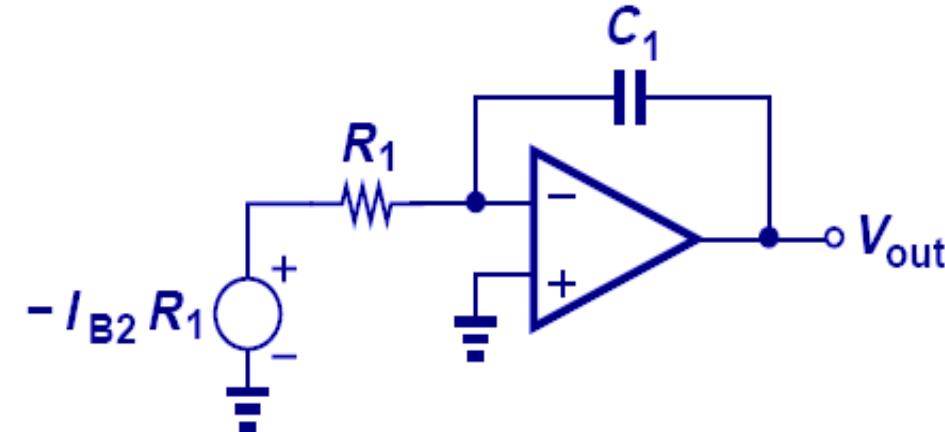
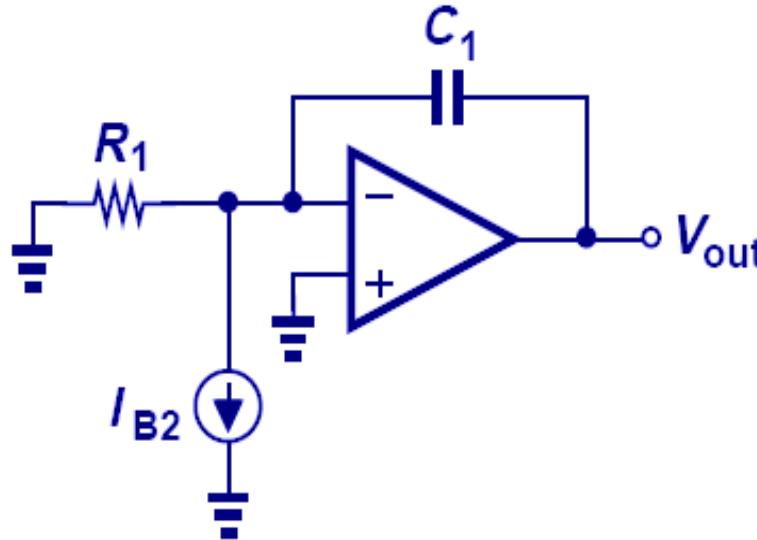
$$I_{B1} = I_{B2}$$

Since the correction voltage is dependent upon  $\beta$ , and  $\beta$  varies with process, we insert a parallel resistor combination in series with the positive input. As long as  $I_{B1} = I_{B2}$ , the correction voltage can track the  $\beta$  variation.





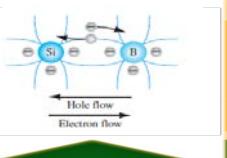
# Effects of Input Bias Currents on Integrator



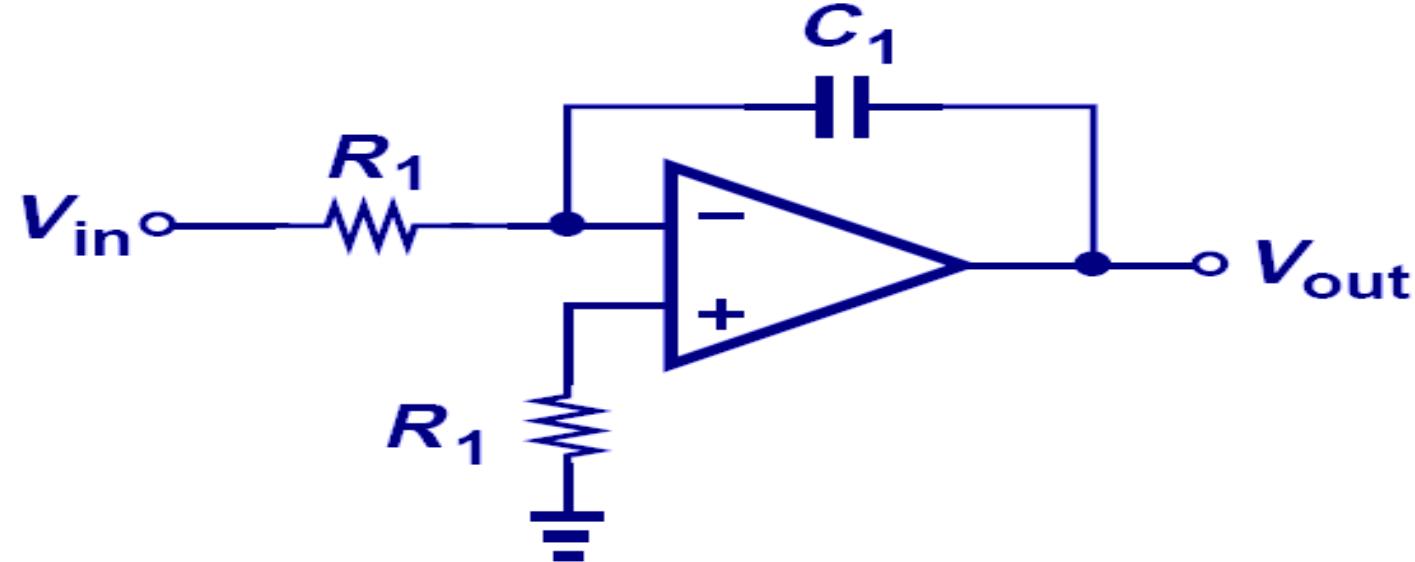
$$V_{out} = -\frac{1}{R_1 C_1} \int (-I_{B2} R_1) dt$$

Input bias current will be integrated by the integrator and eventually saturate the amplifier.





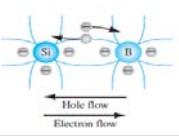
# Integrator's Input Bias Current Cancellation



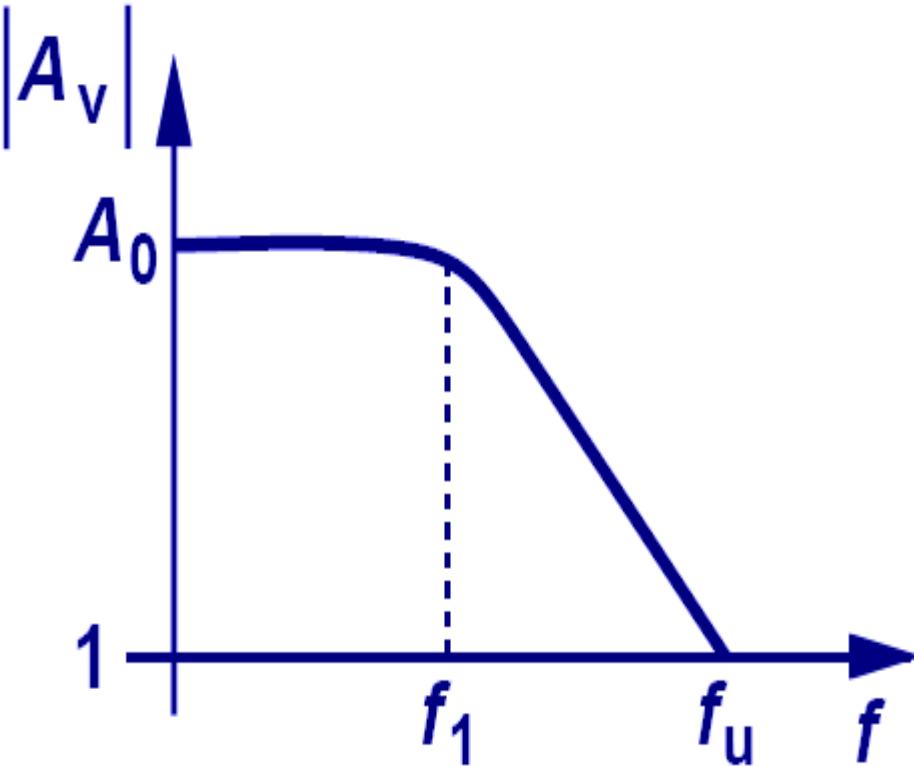
By placing a resistor in series with the positive input, integrator input bias current can be cancelled.

However, the output still saturates due to other effects such as input mismatch, etc.





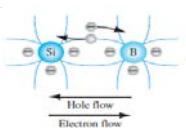
# Speed Limitation



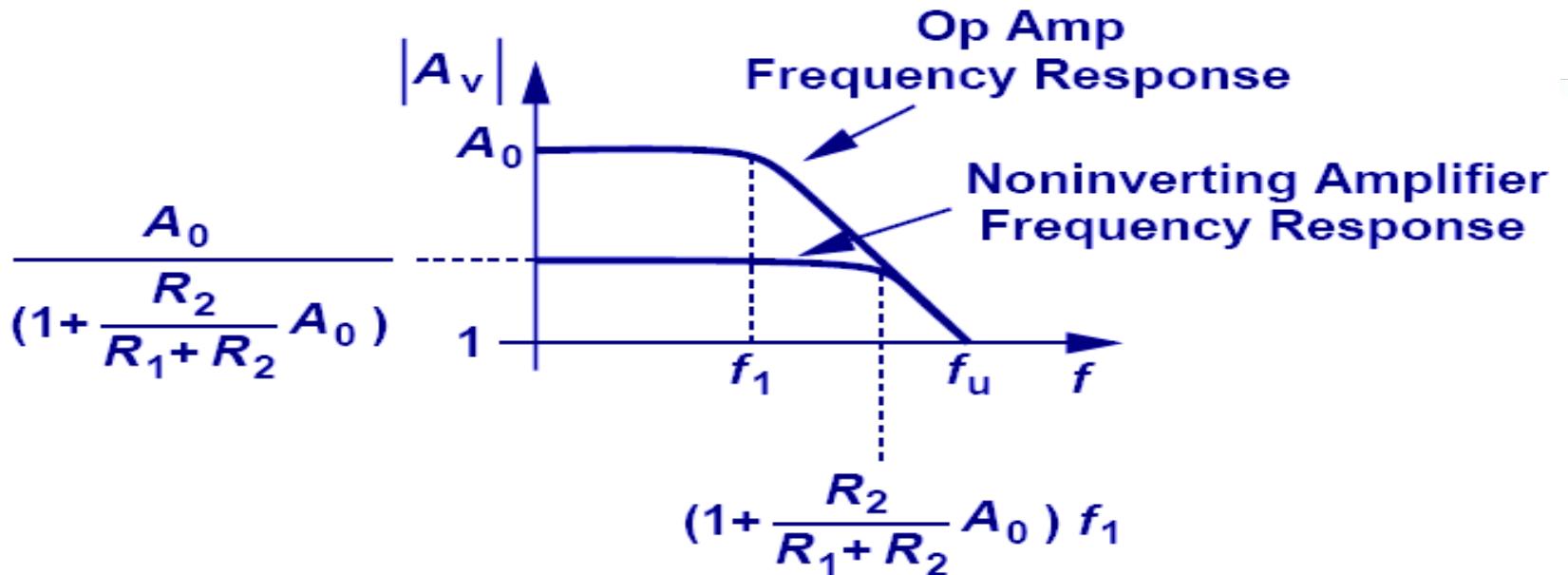
$$\frac{V_{out}}{V_{in1} - V_{in2}}(s) = \frac{A_0}{1 + \frac{s}{\omega_1}}$$

Due to internal capacitances, the gain of op amps begins to roll off.





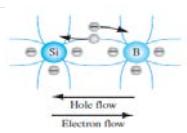
# Bandwidth and Gain Tradeoff



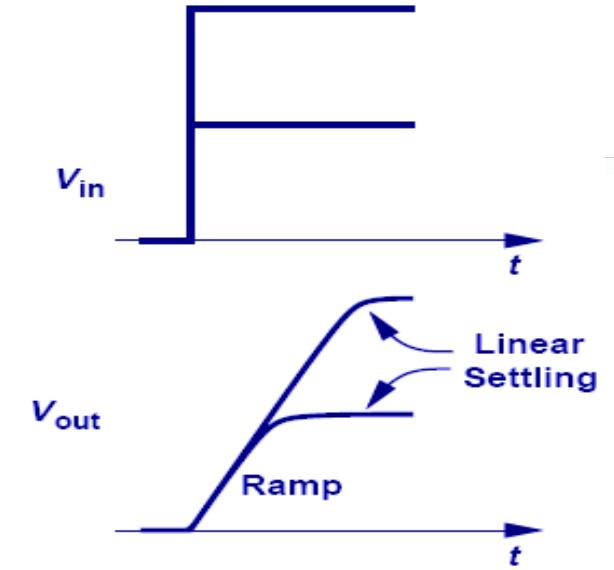
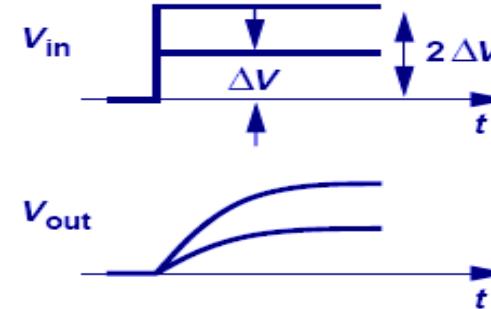
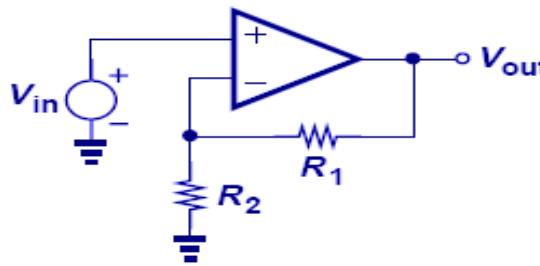
Having a loop around the op amp (inverting, noninverting, etc) helps to increase its bandwidth.

However, it also decreases the low frequency gain.





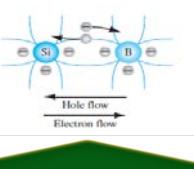
# Slew Rate of Op Amp



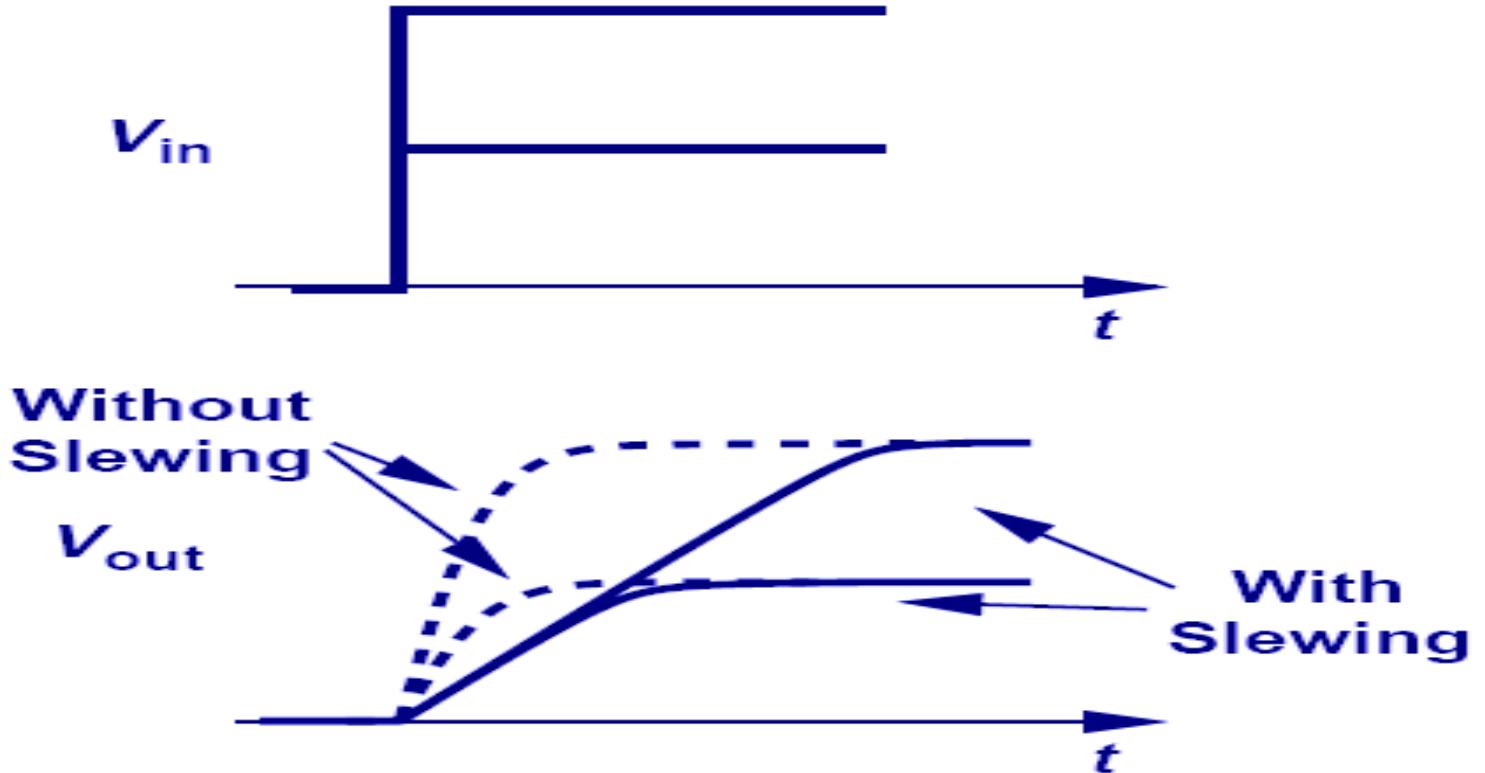
In the linear region, when the input doubles, the output and the output slope also double. However, when the input is large, the op amp slews so the output slope is fixed by a constant current source charging a capacitor.

This further limits the speed of the op amp.



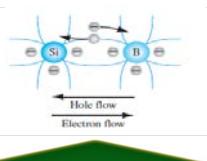


# Comparison of Settling with and without Slew Rate

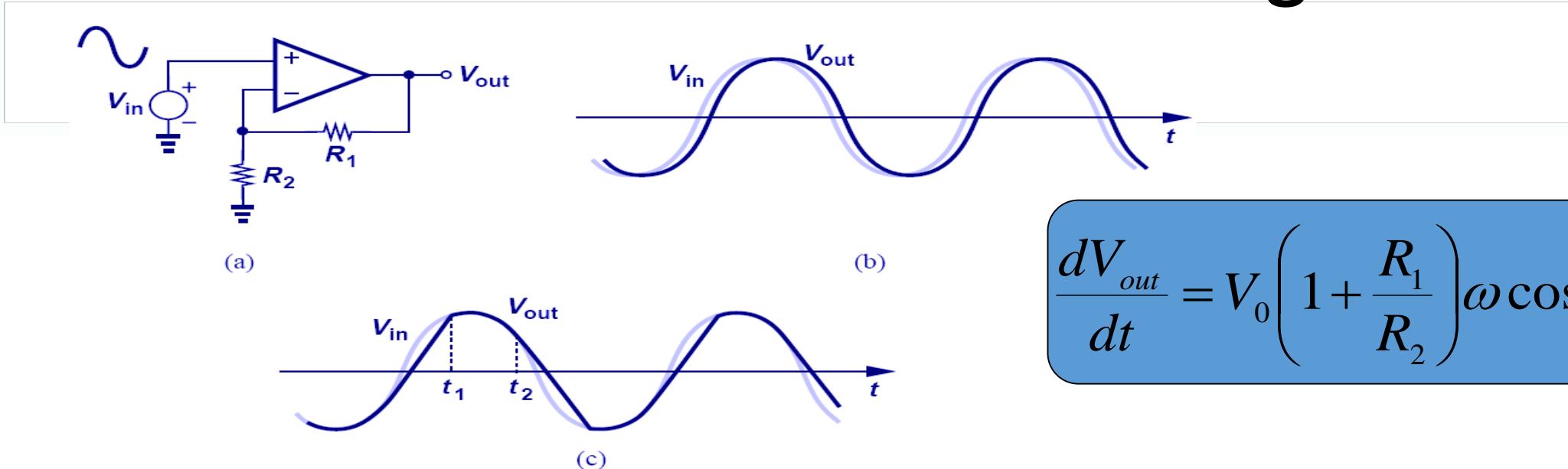


As it can be seen, the settling speed is faster without slew rate (as determined by the closed-loop time constant).





# Slew Rate Limit on Sinusoidal Signals

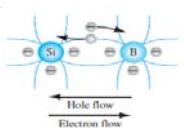


$$\frac{dV_{out}}{dt} = V_0 \left( 1 + \frac{R_1}{R_2} \right) \omega \cos \omega t$$

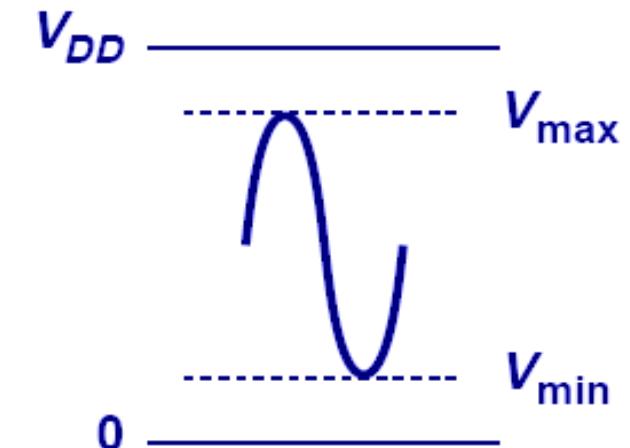
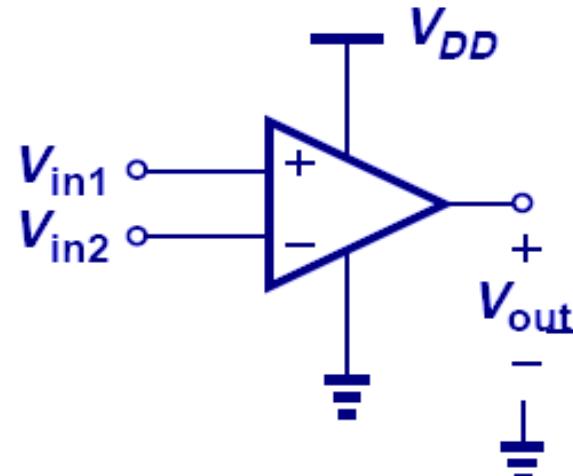
As long as the output slope is less than the slew rate, the op amp can avoid slewing.

However, as operating frequency and/or amplitude is increased, the slew rate becomes insufficient and the output becomes distorted.





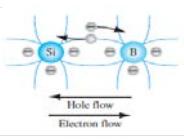
# Maximum Op Amp Swing



$$V_{out} = \frac{V_{max} - V_{min}}{2} \sin \omega t + \frac{V_{max} + V_{min}}{2}$$
$$\omega_{FP} = \frac{SR}{\frac{V_{max} - V_{min}}{2}}$$

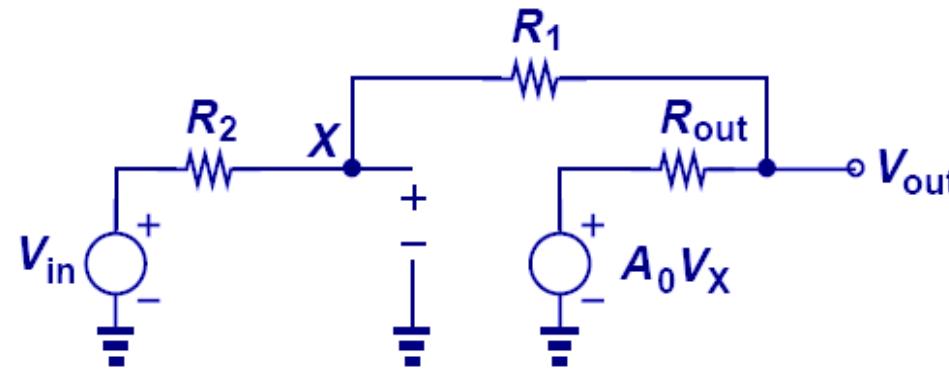
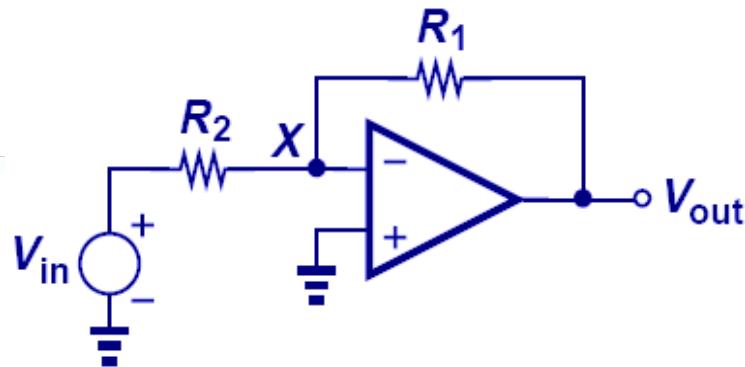
To determine the maximum frequency before op amp slews, first determine the maximum swing the op amp can have and divide the slew rate by it.





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# Nonzero Output Resistance

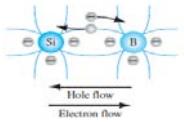


$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{R_2} \frac{A_0 - \frac{R_{out}}{R_1}}{1 + \frac{R_{out}}{R_2} + A_0 + \frac{R_1}{R_2}}$$

In practical op amps, the output resistance is not zero.

It can be seen from the closed loop gain that the nonzero output resistance increases the gain error.





SEMICONDUCTOR DEVICES  
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# Thank You Very Much

Benjamin Kommey

[bkommey.coe@knust.edu.gh](mailto:bkommey.coe@knust.edu.gh)

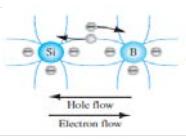
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

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Whatsup: 0049 172 4444 765

Skype\_id: calculus.affairs





SEMICONDUCTOR DEVICES  
DEPARTMENT OF COMPUTER ENGINEERING

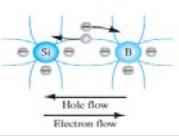
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“Logic will get you from A to Z;  
imagination will get you  
everywhere”

**Albert Einstein**





# SEMICONDUCTOR DEVICES

## DEPARTMENT OF COMPUTER ENGINEERING

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# Overview

## Other Two Terminal Devices

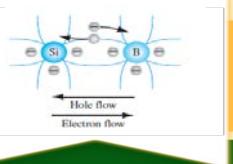
**Schottky  
Barrier Diodes**

**Solar Cells**

**Photodetectors**

**Thermistors**



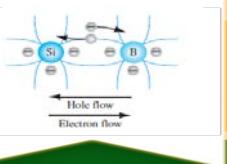


# Other Two Terminal Devices



Like the semiconductor diode,  
there are other two terminal devices having a single p-n  
junction,  
but with different mode of operation,  
terminal characteristics and areas of application





# Other Two Terminal Devices

These include:

Schottky barrier diode

Photodiode

Photoconductive cell

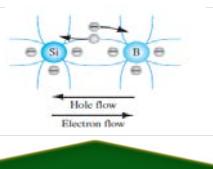
Solar cell

IR emitter

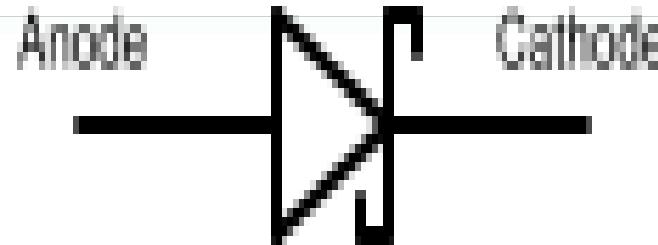
Tunnel diodes

Thermistors





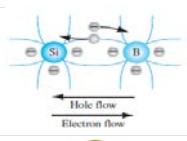
# Schottky Barrier Diode



The Schottky diode (named after German physicist Walter H. Schottky; also known as hot carrier diode) is a semiconductor diode with a low forward voltage drop and a very fast switching action.

When current flows through a diode there is a small voltage drop across the diode terminals.



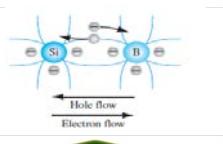


# Schottky Barrier Diode

A normal silicon diode has a voltage drop between 0.6–1.7 volts, while a Schottky diode voltage drop is between approximately 0.15–0.45 volts.

This lower voltage drop can provide higher switching speed and better system efficiency.





# Construction of Schottky Barrier Diode

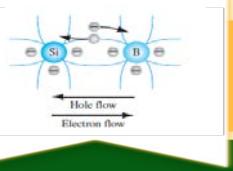
A metal–semiconductor junction is formed between a metal and a semiconductor, creating a Schottky barrier (instead of a semiconductor–semiconductor junction as in conventional diodes).

Typical metals used are **molybdenum, platinum, chromium or tungsten**; and the semiconductor would typically be N-type silicon.

The metal side acts as the anode and N-type semiconductor acts as the cathode of the diode.

This Schottky barrier results in both very fast switching and low forward voltage drop.



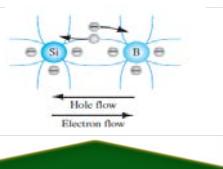


# Reverse Recovery Time

The most important difference between the p-n and Schottky diode is reverse recovery time, when the diode switches from conducting to non-conducting state.

Where in a p-n diode the reverse recovery time can be in the order of hundreds of nanoseconds and less than 100 ns for fast diodes, Schottky diodes do not have a recovery time, as there is nothing to recover from (i.e. no charge carrier depletion region at the junction).



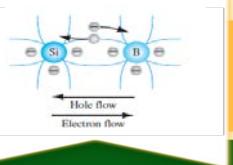


## Reverse Recovery Time

The switching time is  $\sim 100$  ps for the small signal diodes, and up to tens of nanoseconds for special high-capacity power diodes. With p-n junction switching, there is also a reverse recovery current, which in high-power semiconductors brings **increased EMI (electromagnetic interference) noise**.

With Schottky diodes switching essentially instantly with only **slight capacitive loading**, this is much less of a concern.





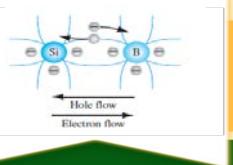
# Schottky Barrier Diode

Schottky diode is a "majority carrier" semiconductor device.

This means that if the semiconductor body is doped n-type, only the n-type carriers (mobile electrons) play a significant role in normal operation of the device.

The majority carriers are quickly injected into the conduction band of the metal contact on the other side of the diode to become free moving electrons.



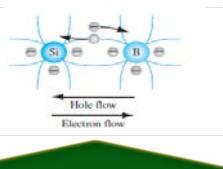


## Schottky Barrier Diode

Therefore no slow, random recombination of n- and p- type carriers is involved, so that this diode can cease conduction faster than an ordinary p-n rectifier diode.

This property in turn allows a smaller device area, which also makes for a faster transition.





# Schottky Barrier Diodes

Schottky barrier or hot-carrier diodes are used mostly in

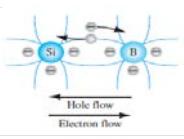
radar systems,

Schottky TTL (transistor-transistor logic) for computers,

Mixers and detectors in communication equipment,

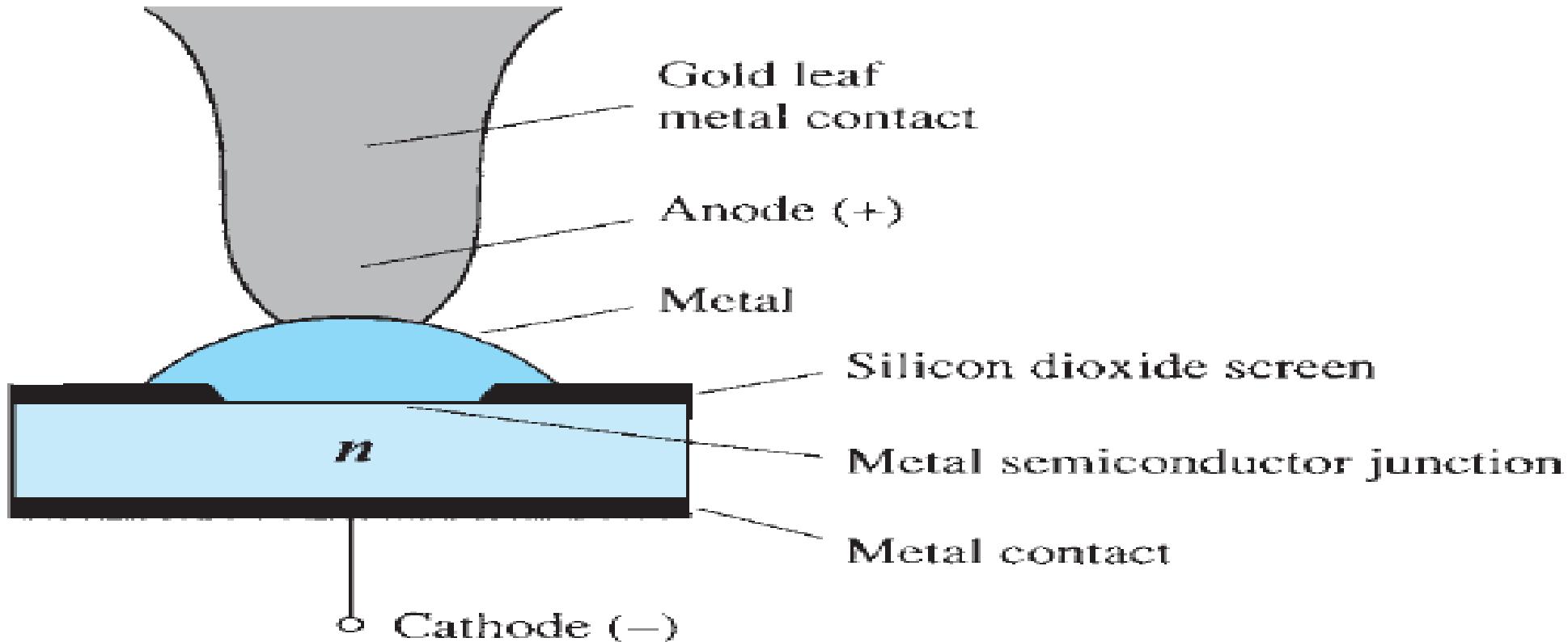
Instrumentation and Analog-digital converters

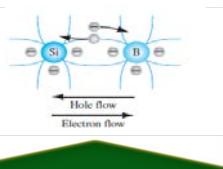




# Schottky Barrier Diodes

Schottky barrier is created by joining a n- or p-type silicon to a host of different metal





# Schottky Barrier Diodes

Electron is the majority carrier in both materials

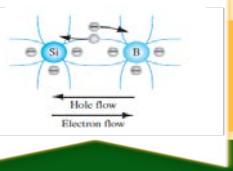
When the materials are joined, the electrons in the n-type silicon material flow immediately into the adjoining metal, establishing a heavy flow of majority carriers

Schottky barrier diode are also called hot-carrier because the injected carriers have a very high kinetic energy level compared to the electrons of the metal

Electrons are injected into a region of the same electron plurality.

Schottky diodes are therefore unique in that conduction is entirely by majority carriers.





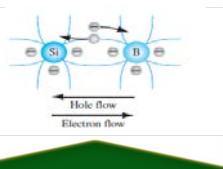
# Schottky Barrier Diodes

The heavy flow of electrons into the metal creates a region near the junction surface depleted of carriers in the silicon material—much like the depletion region in the  $p - n$  junction diode.

The additional carriers in the metal establish a “negative wall” in the metal at the boundary between the two materials.

The net result is a “surface barrier” between the two materials, preventing any further current. That is, any electrons (negatively charged) in the silicon material face a carrier-free region and a “negative wall” at the surface of the metal





# Solar Cells

Solar cells are useful both for space and terrestrial applications

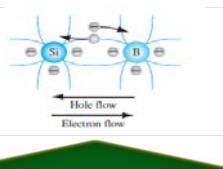
Solar cell provide the long-duration power supply for satellites

Solar cell is an important candidate for an alternative terrestrial energy because it converts sunlight directly to electricity with good conversion efficiency

Solar cell provides nearly permanent power at low operating cost

Solar cell is virtually non-polluting





# Solar Cells

Solar constant is defined as the intensity of solar radiation outside the earth's atmosphere, at the average distance of its orbit around the sun

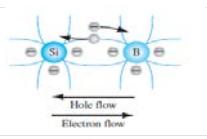
$$\text{Solar constant} = 1367 \text{ W/m}^2$$

Terrestrially, the sunlight is attenuated by clouds and by atmospheric scattering and absorption.

The attenuation depends primarily on the length of the light's path through the atmosphere, or the mass of air through which it passes.

This “air mass” is defined as  $l/\cos \varphi$ , where  $\varphi$  is the angle between the vertical and the sun's position.

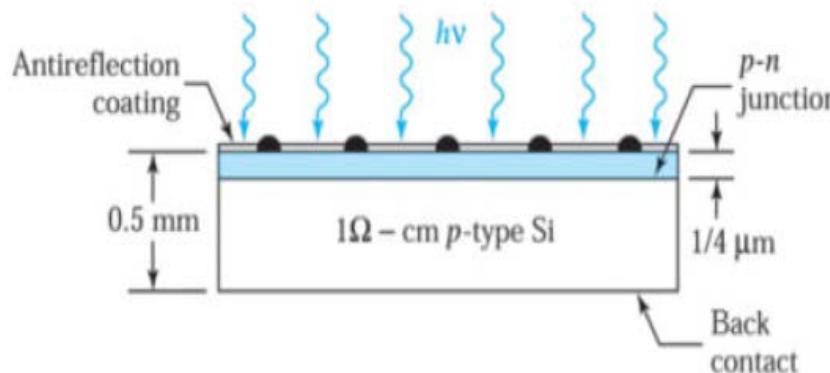




# p-n Junction Solar Cells

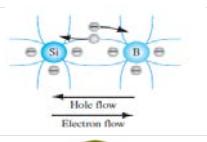
A *p-n* junction solar cell consists of :

- a shallow *p-n* junction formed on the surface,
- a front ohmic contact stripe and fingers,
- a back ohmic contact that covers the entire back surface, and an

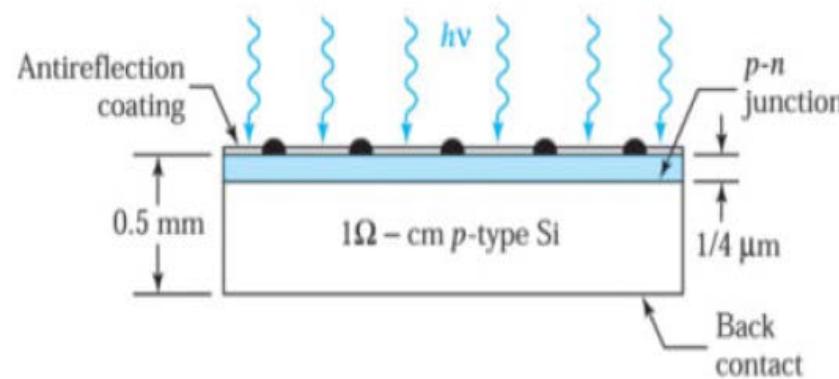
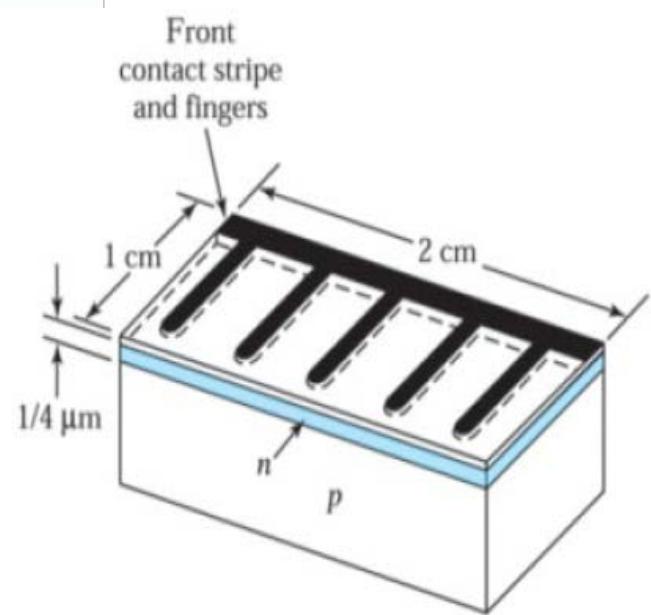


**antireflection coating on the front surface.**





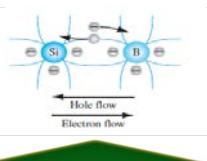
# p-n Junction Solar Cells



The surface reflection of the incident light from air ( $n = 1$ ) into semiconductor silicon ( $n = 3.5$ ) is about 0.31.

This means that 31% of incident light is reflected and is not available for conversion to electrical energy in a silicon solar cell.





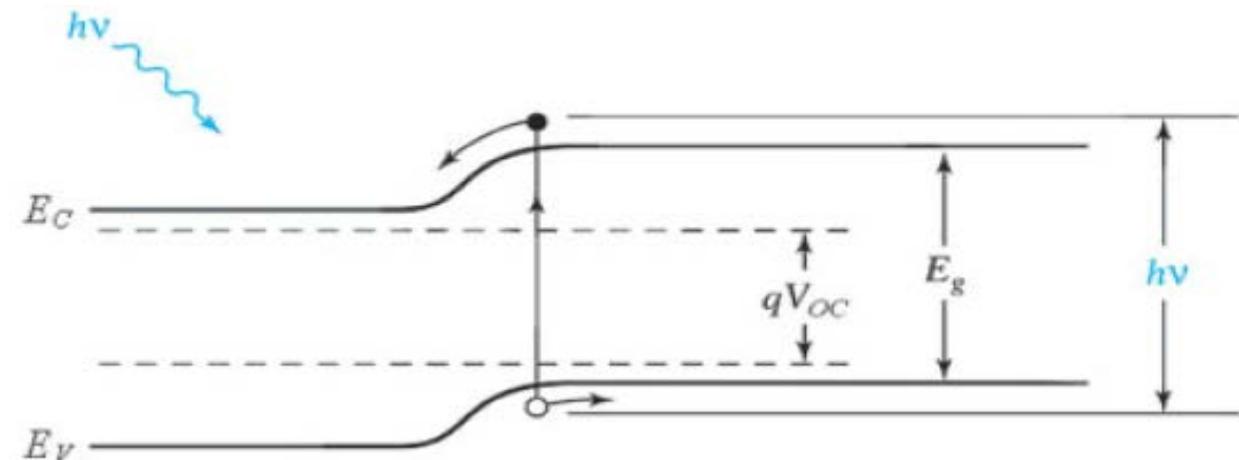
# Solar Cells

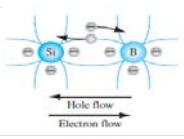
When the cell is exposed to the solar spectrum, a photon that has an energy less than the bandgap  $Eg$  makes no contribution to the cell output.

A photon that has energy greater than  $Eg$  contributes an energy  $Eg$  to the cell output.

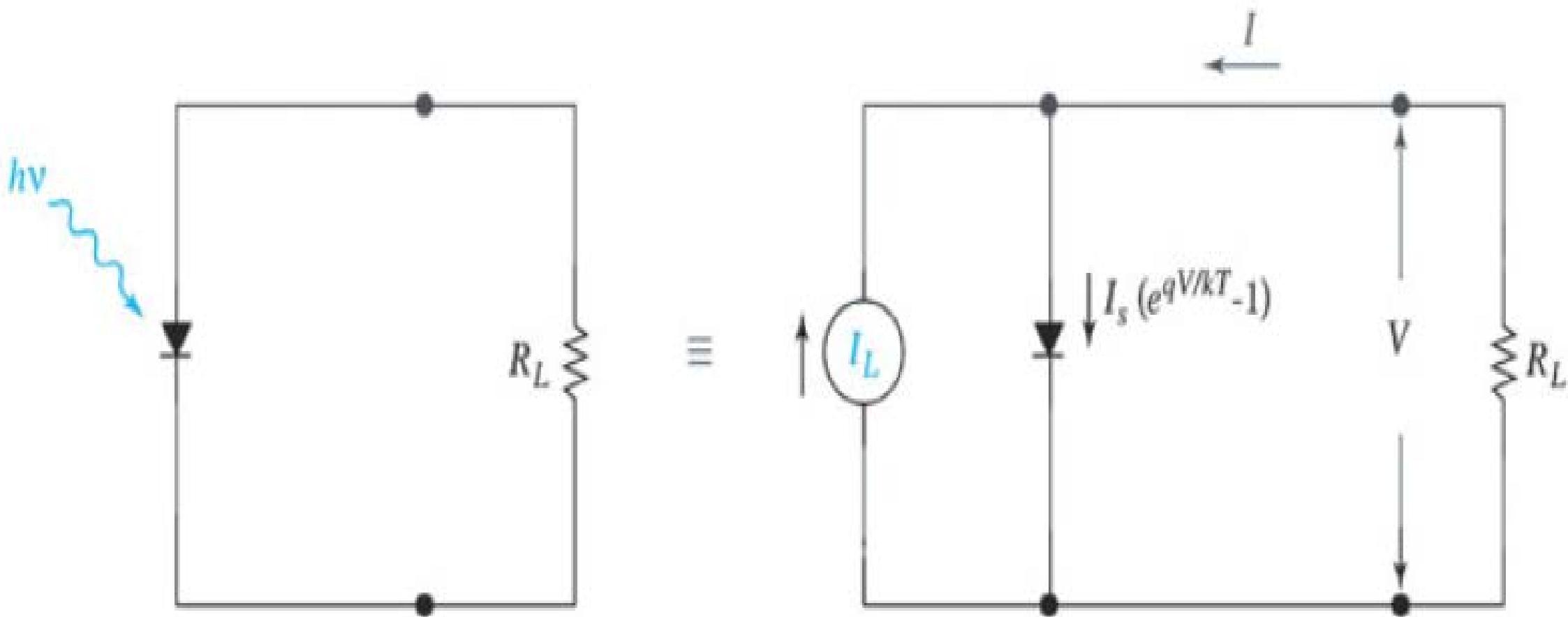
Energy greater than  $Eg$  is wasted as heat

Energy band diagram of a p-n junction solar cell under solar radiation



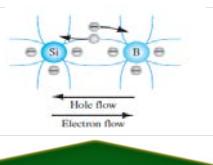


# Conversion Efficiency



**Idealized equivalent circuit of a solar cell**





# Conversion Efficiency

From the equivalent circuit above the constant-current source is in parallel with the junction.

The source current  $I_L$  results from the excitation of excess carriers by solar radiation

$I_s$  is the diode saturation current and  $R_L$  is the load resistance

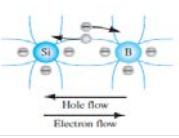
The ideal I-V characteristics of device is given by

$$I = I_s(e^{qV/kT} - 1) - I_L,$$

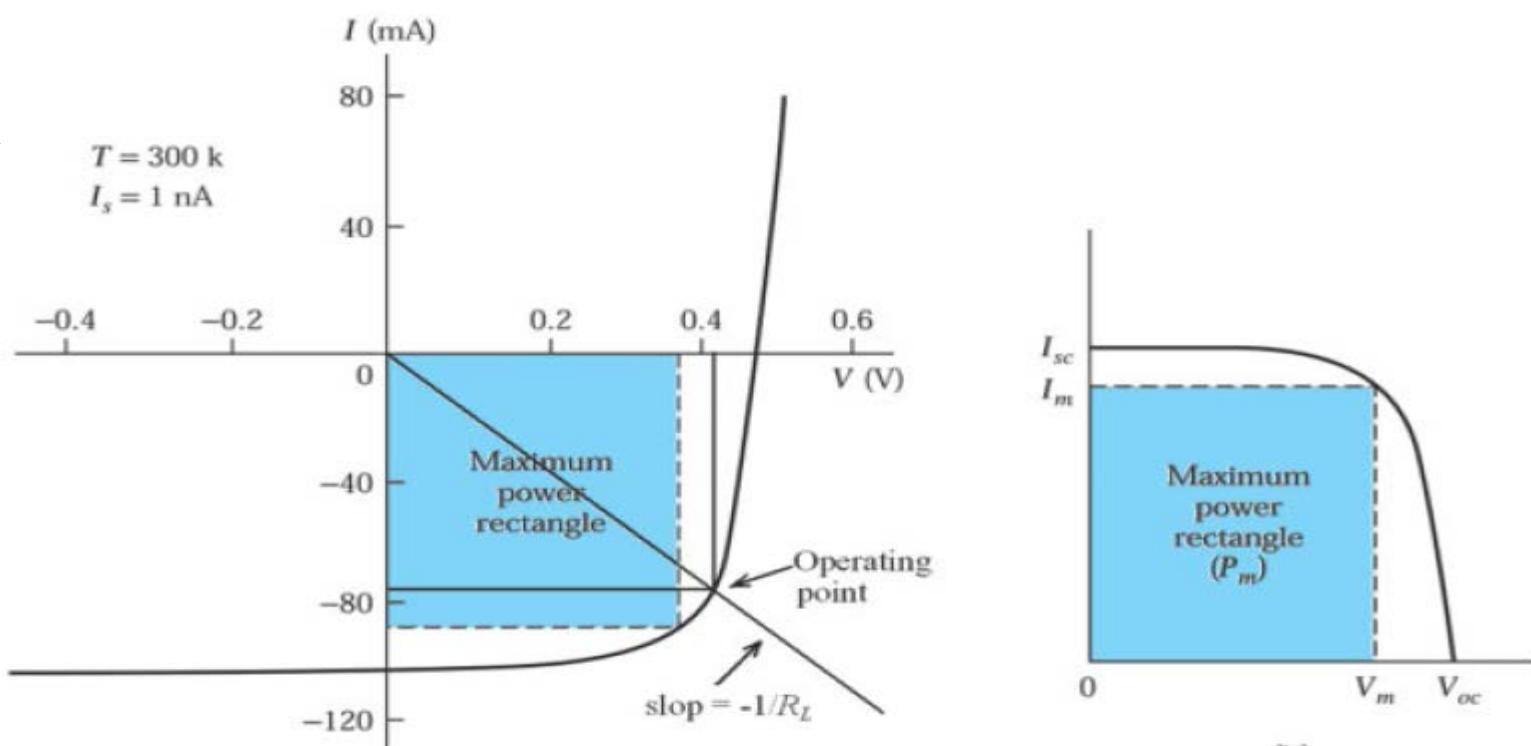
where A is the device area

$$J_s = \frac{I_s}{A} = qN_C N_V \left( \frac{1}{N_A} \sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_D} \sqrt{\frac{D_p}{\tau_p}} \right) \cdot e^{-E_g/kT},$$
$$V_{OC} = \frac{kT}{q} \ln \left( \frac{I_L}{I_s} + 1 \right) \cong \frac{kT}{q} \ln \left( \frac{I_L}{I_s} \right)$$





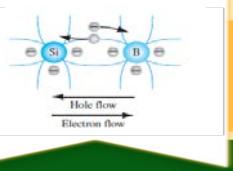
# I-V Characteristics of Solar Cell



For a given  $I_L$ ,  $V_{oc}$  increases logarithmically with decreasing saturation current  $I_s$

The maximum output power  $P_m = I_m V_m \cong I_L \left[ V_{oc} - \frac{kT}{q} \ln \left( 1 + \frac{qV_m}{kT} \right) - \frac{kT}{q} \right]$





# Solar Cell Types

Thin film solar cells

Inverted thin film solar cells

Tandem cells

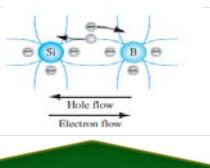
Multiband cells

Multi quantum well

Thermophotonic cells

Thermophotovoltaic cell





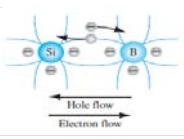
# Thin Film Solar Cells

Produced from cheaper polycrystalline materials and glass

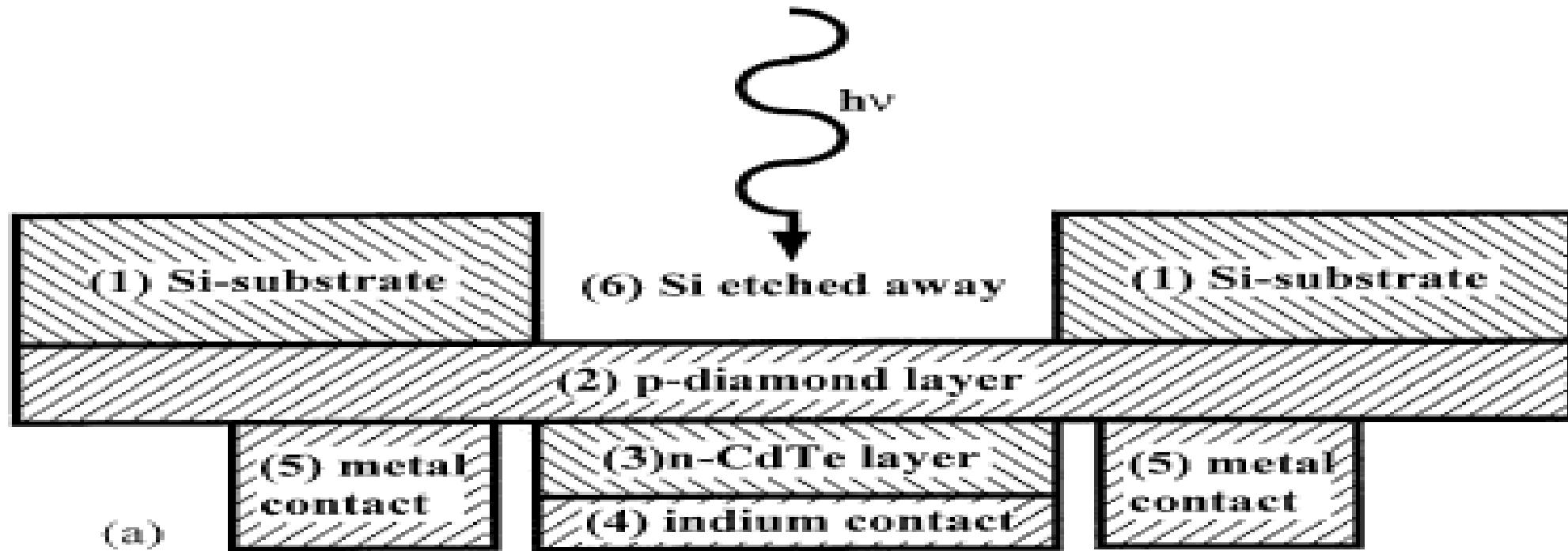
High optical absorption coefficients

Bandgap suited to solar spectrum





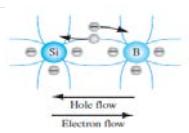
# Inverted Thin Film Cell



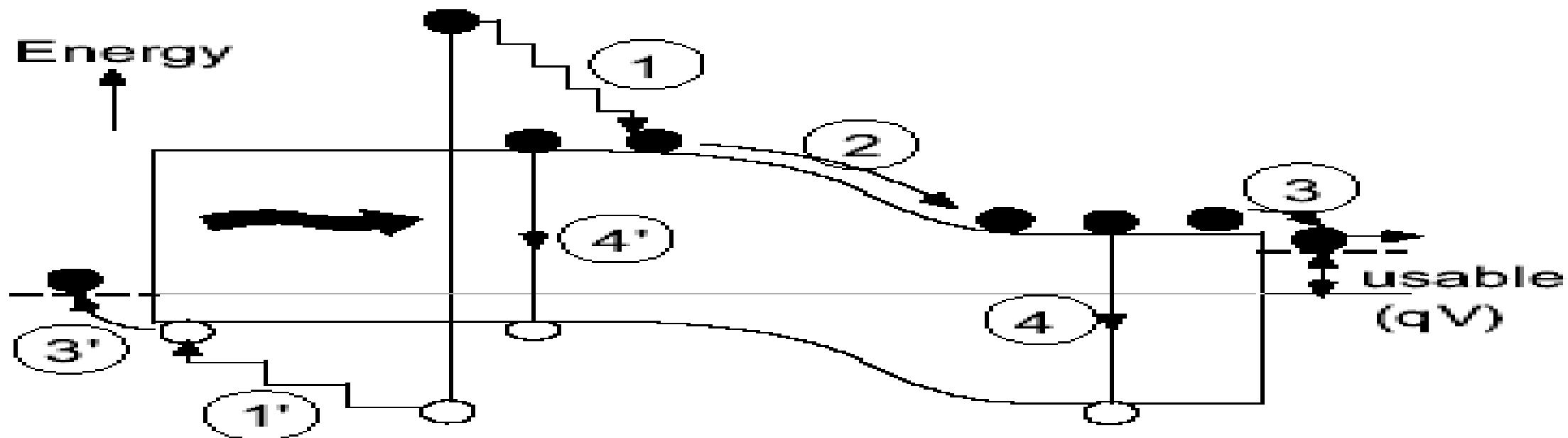
p-diamond (Bandgap 5.5 eV) as a window layer

n-CdTe layer as an absorption layer





# Efficiency Losses in Solar Cell

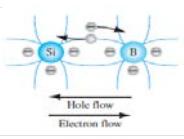


1 = Thermalization loss

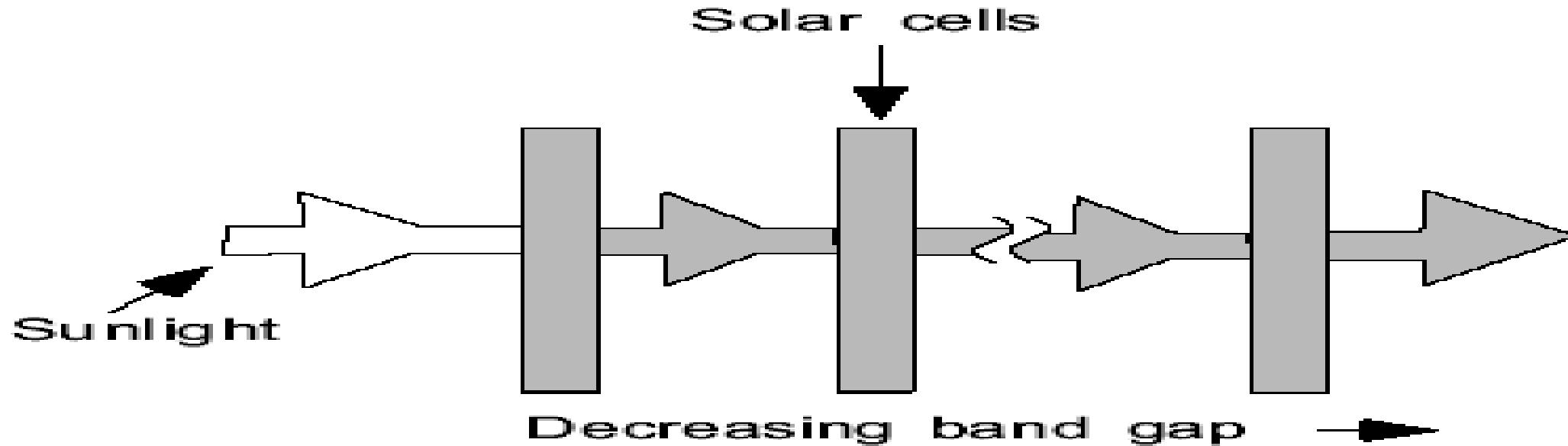
2 and 3 = Junction and contact voltage loss

4 = Recombination loss





# Tandem Cells

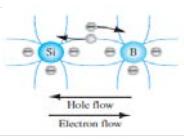


Current output matched for individual cells

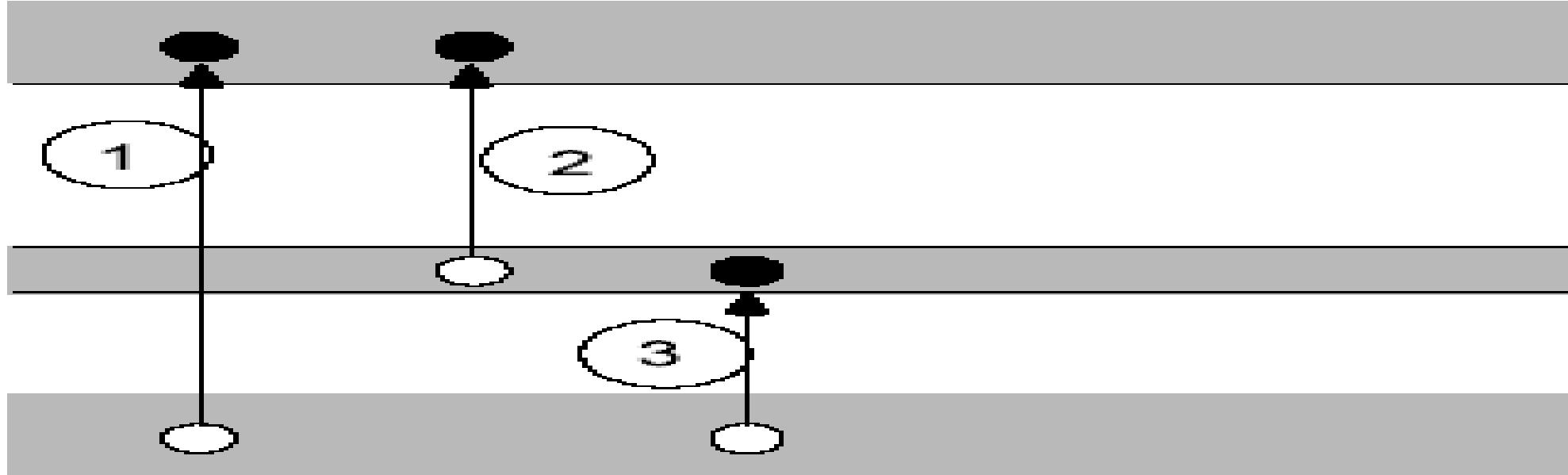
Ideal efficiency for infinite stack is 86.8%

GalnP/GaAs/Ge tandem cells (efficiency 40%)





# Multiband Cells

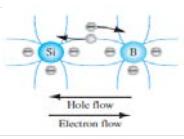


Intermediate band formed by impurity levels.

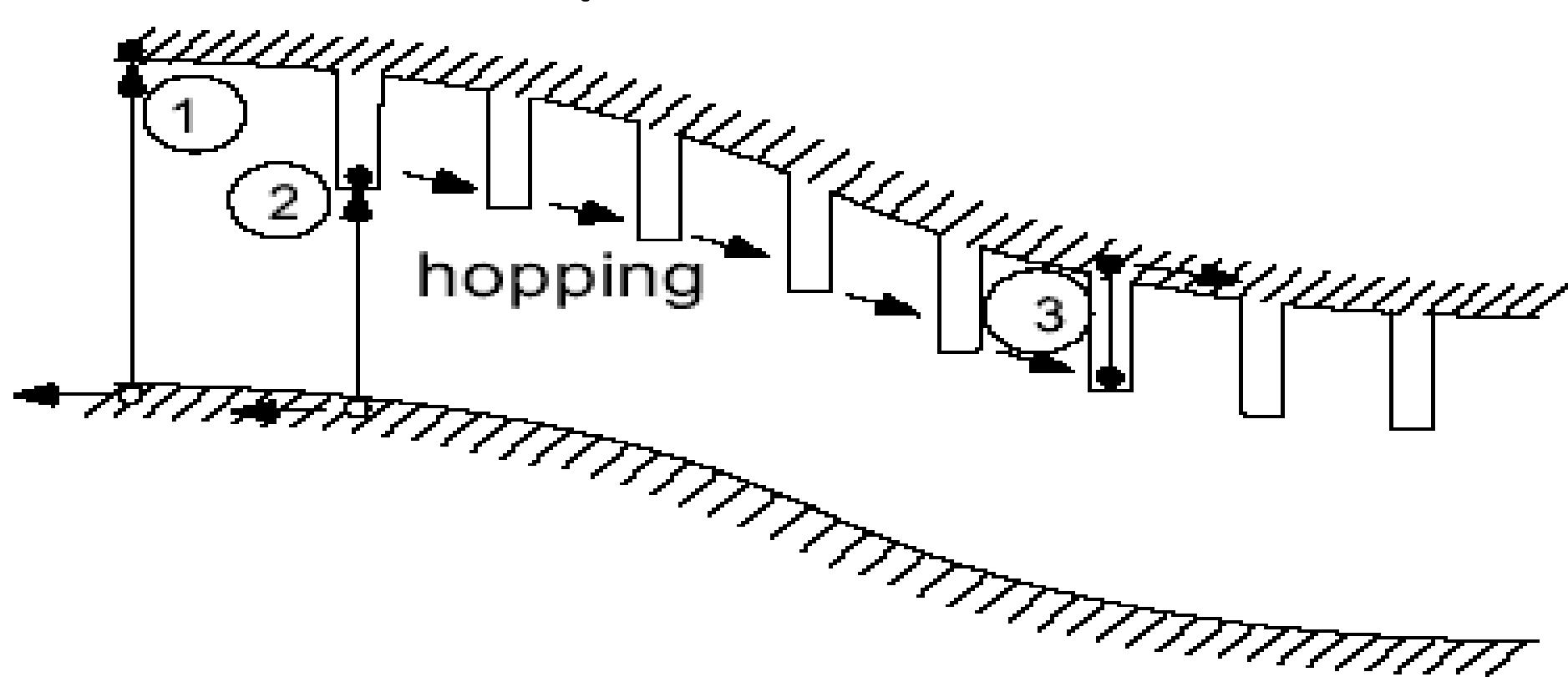
Process 3 also assisted by phonons

Limiting efficiency is 86.8%



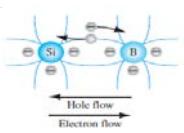


# Multiple Quantum Well

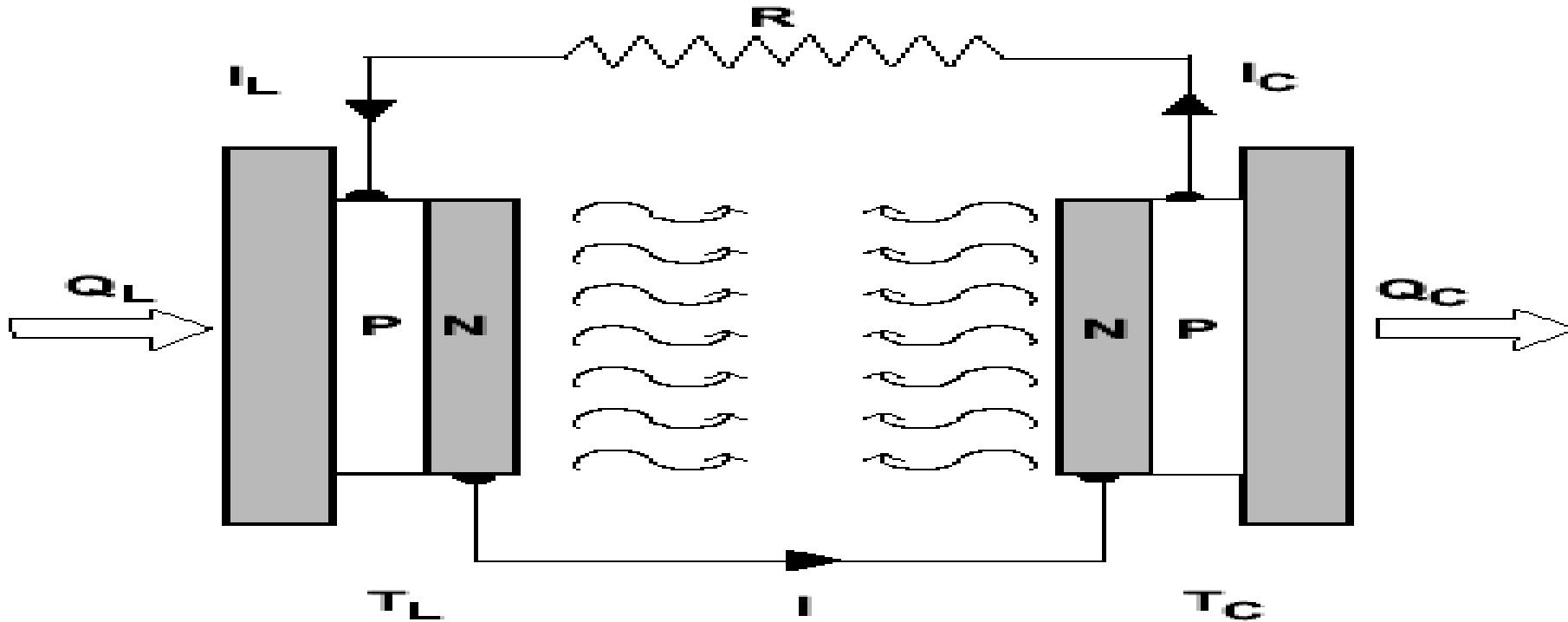


Principle of operation similar to multiband cells



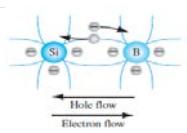


# Thermophotonic Cells

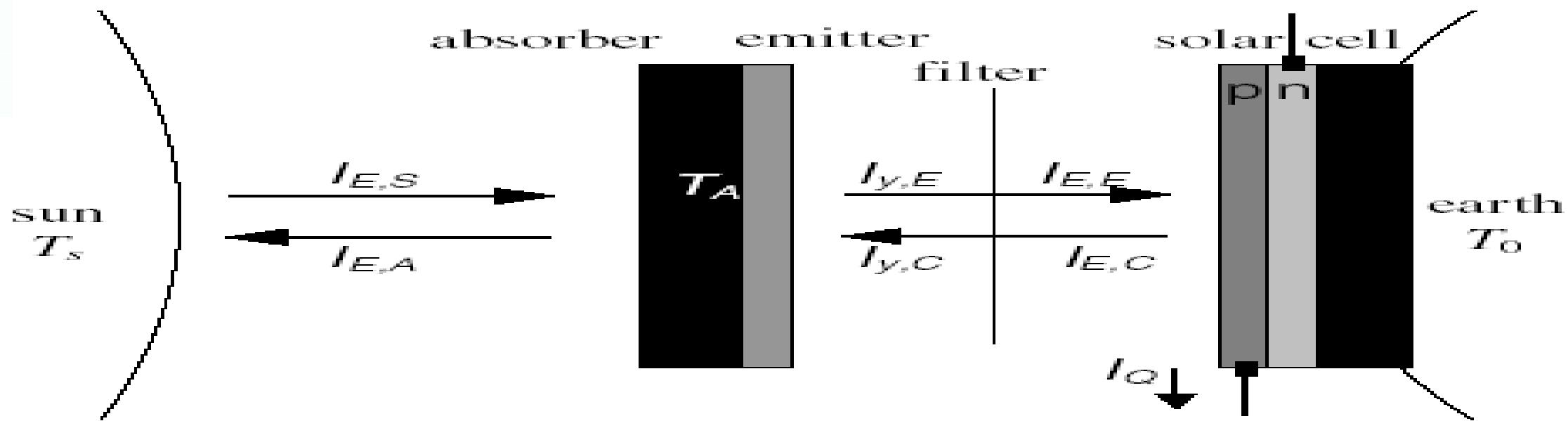


Heated semiconductor emits narrow bandwidth radiations  
Diode with higher temperature has lower voltage





# Thermophotovoltaic Cell

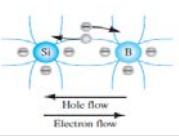


Filter passes radiations of energy equal to bandgap of solar cell material

Emitter radiation matched with spectral sensitivity of cell

High Illumination Intensity ( $\sim 10 \text{ kW/m}^2$ )





# Photodetectors - Overview

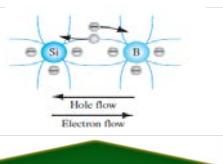
## Photodetectors

P-Intrinsic N (Pin)

Avalanche Photo Diode  
(APD)

Characteristics





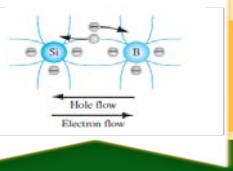
# Photodetectors

These are Opto-electric devices i.e. to convert the optical signal back into electrical impulses.

The light detectors are commonly made up of semiconductor material.

When the light strikes the light detector a current is produced in the external circuit proportional to the intensity of the incident light.

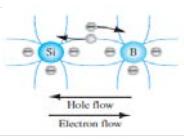




# Photodetectors

- A **high sensitivity** to the emission wavelength range of the received light signal
- A **minimum** addition of **noise** to the signal
- A **fast response** speed to handle the desired data rate
- Be **insensitive** to **temperature** variations
- Be **compatible** with the physical dimensions of the **fiber**
- Have a **Reasonable cost** compared to other system components
- Have a long **operating lifetime**





# Type of Photodetectors

PIN Photodiode

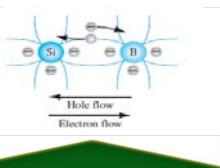


Avalanche Photodiode



PIN photodiode





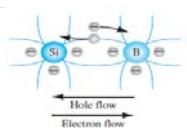
# *p-intrinsic-n* pin Photodetector

The **device structure** consists of p and n semiconductor regions separated by a very lightly n-doped intrinsic (i) region.

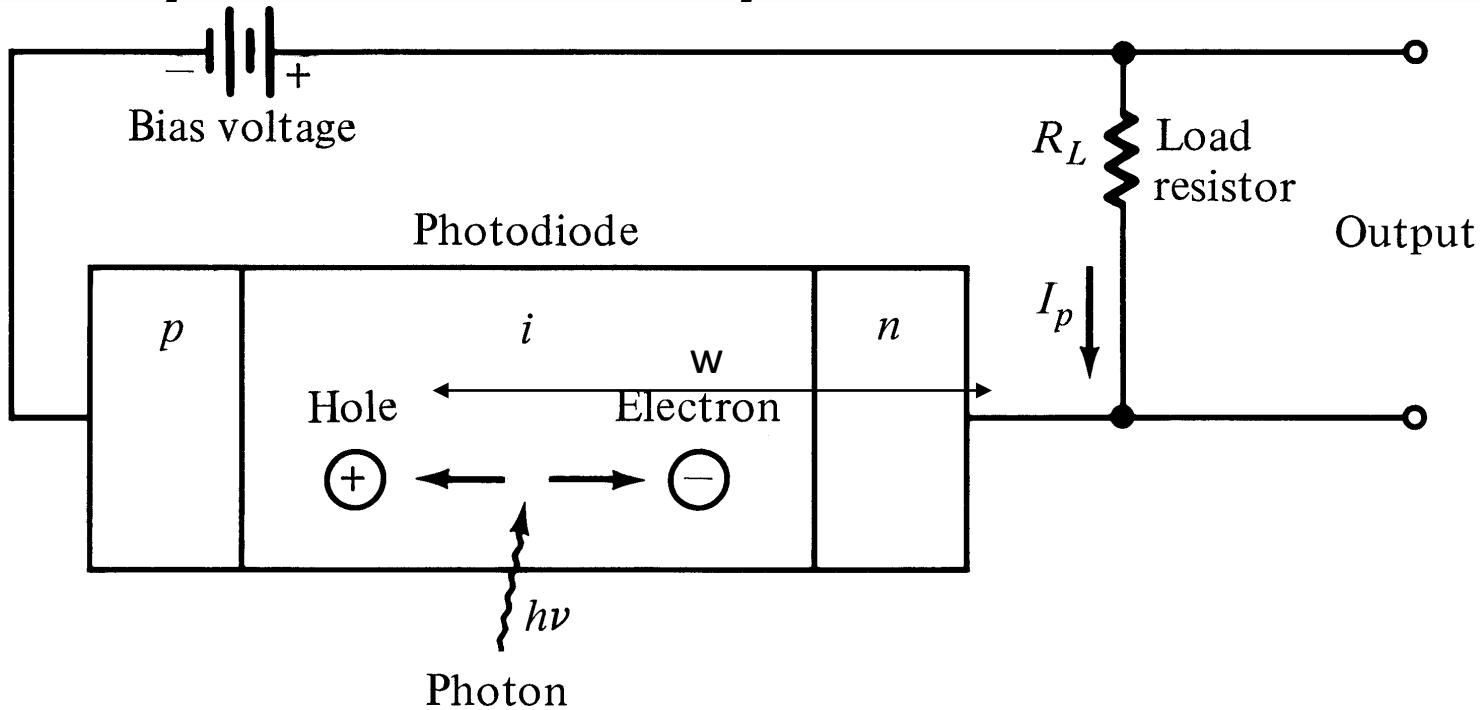
In **normal operation** a reverse-bias voltage is applied across the device so that no free electrons or holes exist in the **intrinsic region**.

**Incident photon** having energy **greater than or equal** to the **bandgap energy** of the semiconductor material, **give up its energy** and **excite an electron** from the valence band to the conduction band



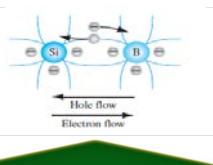


# *p-intrinsic-n* pin Photodetector



The high electric field present in the depletion region causes photo-generated carriers to separate and be collected across the reverse -biased junction. This give rise to a current flow in an external circuit, known as **photocurrent**.





# *p-intrinsic-n* pin Photodetector

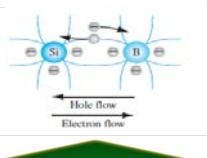
## Photocarriers:

Incident photon, generates free (mobile) **electron-hole pairs in the intrinsic region**. These charge carriers are known as **photocarriers**, since they are generated by a photon.

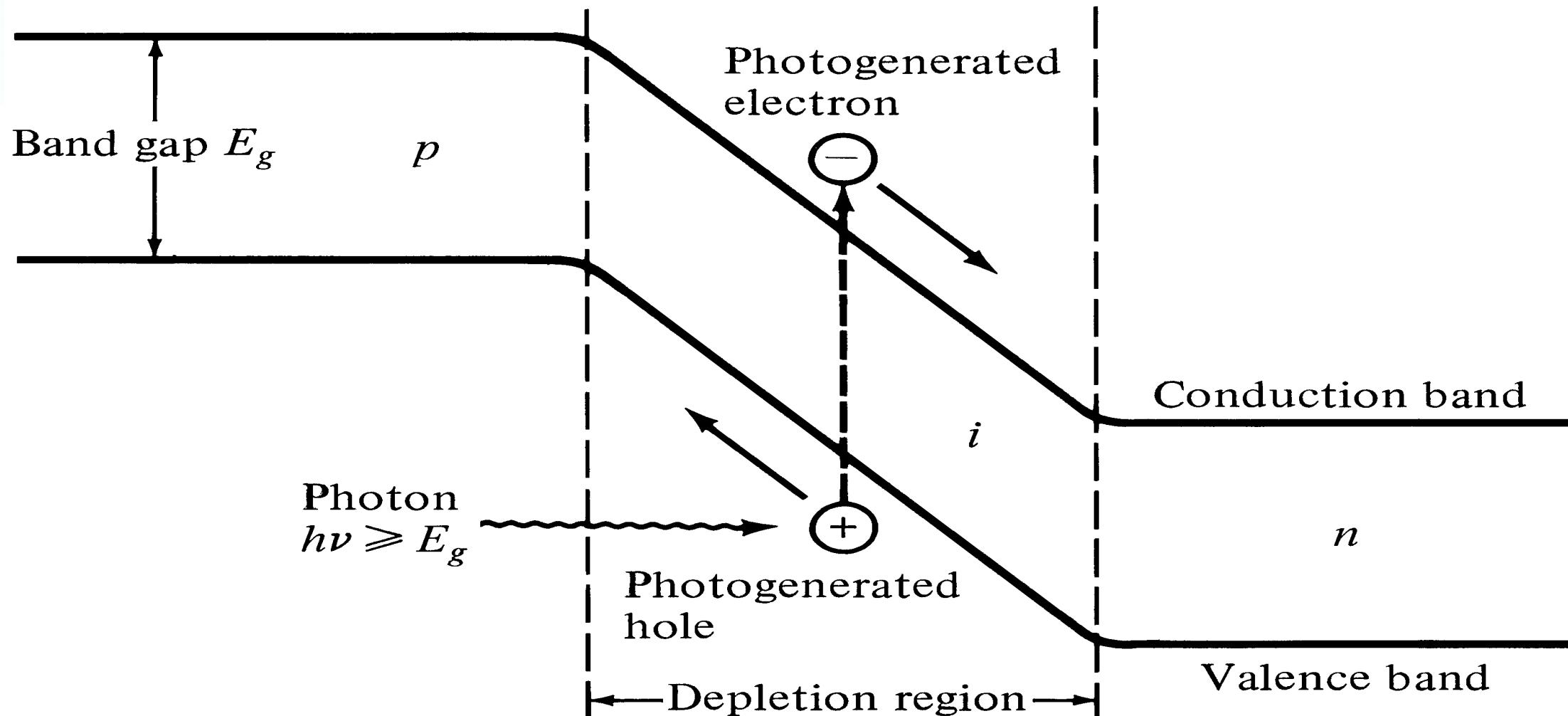
## Photocurrent:

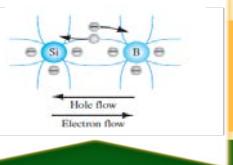
The electric field across the device causes the **photocarriers to be swept out of the intrinsic region**, thereby giving rise to a **current flow in an external circuit**. This current flow is known as the **photocurrent**.





# Energy-Band Diagram for a *pin* Photodiode





# Avalanche Photodiode (APD)

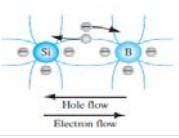
APD has an internal gain  $M$ , which is obtained by having a high electric field that energizes photo-generated electrons.

These electrons ionize bond electrons in the valence band upon colliding with them which is known as *impact ionization*

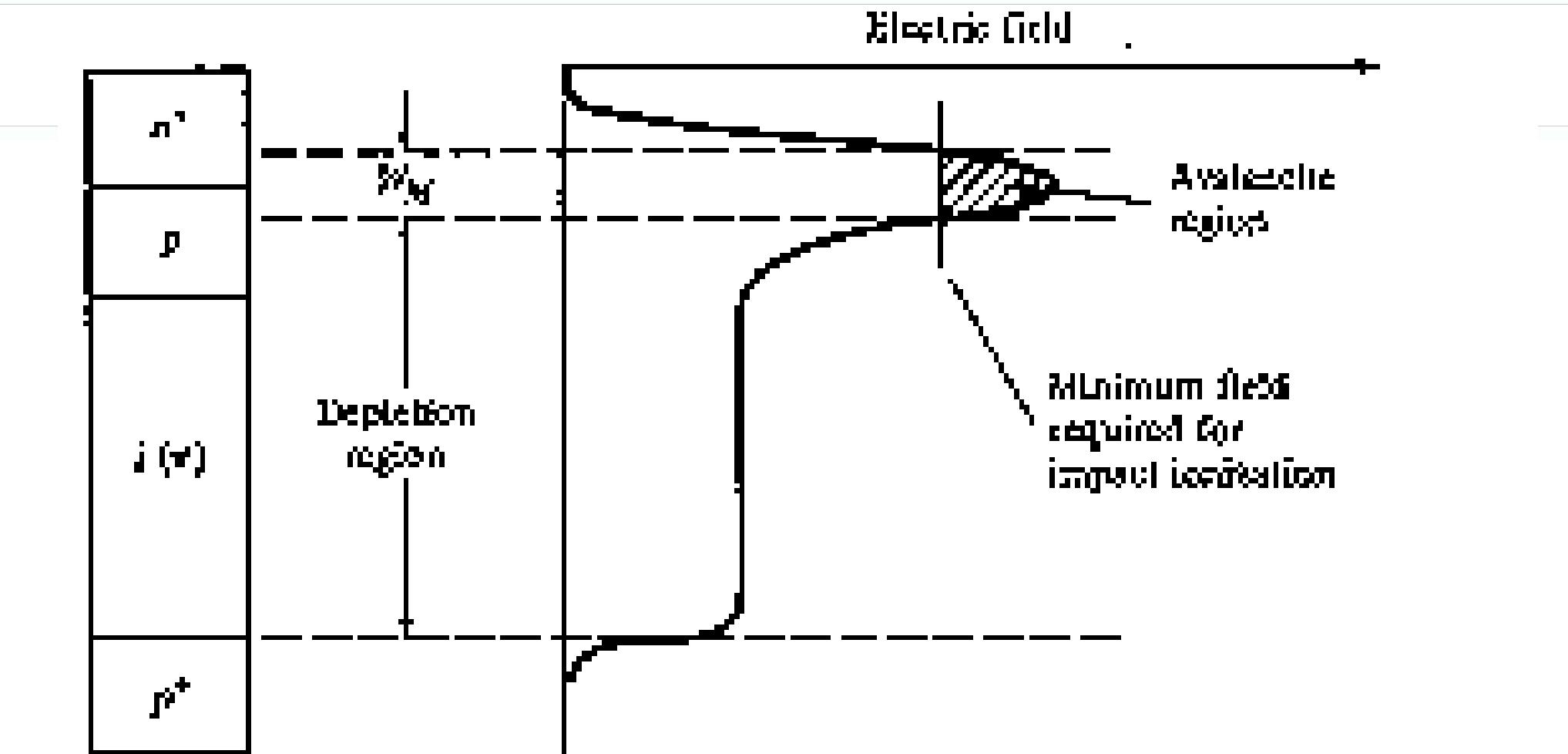
The newly generated electrons and holes are also accelerated by the high electric field and gain energy to cause further impact ionization

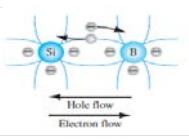
This phenomena is the avalanche effect





# Avalanche Photodiode (APD)





# Photocurrent

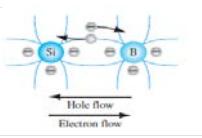
Optical power absorbed,  $P(x)$

in the depletion region  $P_0$

can be written in terms of incident optical power, :

$$P(x) = P_0 (1 - e^{-\alpha_s(\lambda)x})$$



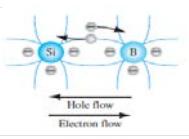


# Photocurrent

Absorption coefficient  $\alpha_s(\lambda)$  strongly depends on wavelength. The upper wavelength cutoff for any semiconductor can be determined by its energy gap as follows:

$$\lambda_c (\mu\text{m}) = \frac{1.24}{E_g (\text{eV})}$$



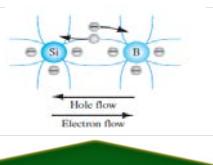


# Photocurrent

Taking entrance face reflectivity into consideration, the absorbed power in the width of depletion region,  $w$ , becomes:

$$(1 - R_f)P(w) = P_0(1 - e^{-\alpha_s(\lambda)w})(1 - R_f)$$





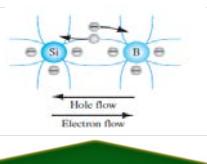
# Noise Sources in Photodetectors

The principal noises associated with photodetectors are :

**1- Quantum (Shot) noise:** arises from statistical nature of the production and collection of photo-generated electrons upon optical illumination. It has been shown that the statistics follow a Poisson process.

**2- Dark current noise:** is the current that continues to flow through the bias circuit in the absence of the light. This is the combination of **bulk dark current**, which is due to thermally generated e and h in the *pn* junction, and the **surface dark current**, due to surface defects, bias voltage and surface area.



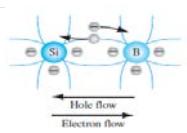


# Noise Sources in Photodetectors

In order to calculate the total noise presented in photodetector, we should sum up the root mean square of each noise current by assuming that those are uncorrelated.

**Total photodetector noise current = quantum noise current + bulk dark current noise + surface current noise**





# SEMICONDUCTOR DEVICES

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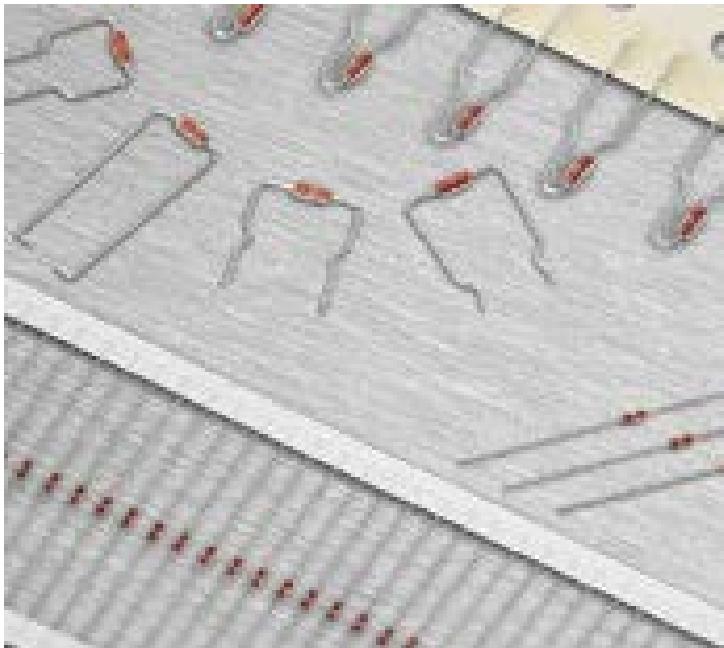
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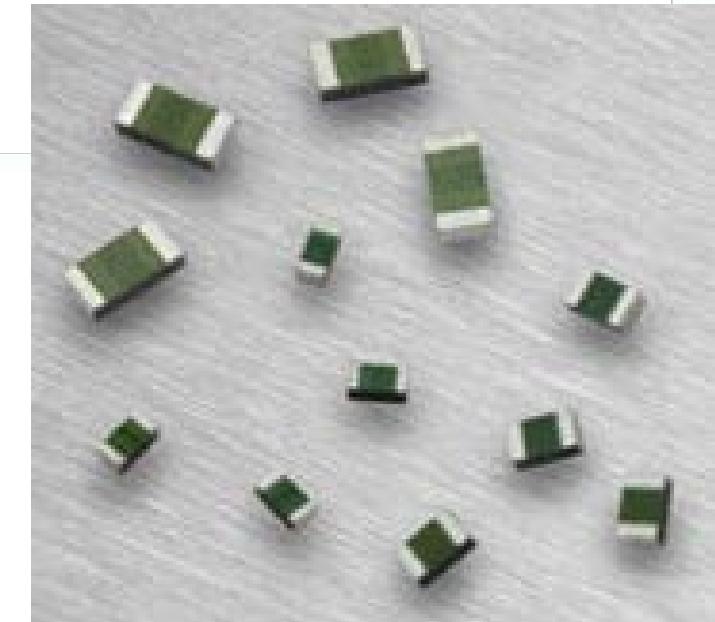
# Thermistors



Leads, coated



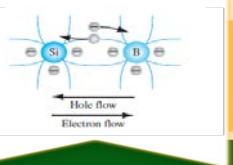
Glass encased



Surface mount

Thermistors are made of semiconductor materials (metallic compounds including oxides such as manganese, copper, cobalt, and nickel, as well as single-crystal semiconductors silicon and germanium).



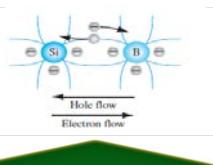


# Thermistors

*Thermistors* are sensors whose resistance changes as a function of temperature

Thermistors are classified as either  
*NTC* (negative temperature coefficient) or  
*PTC* (positive temperature coefficient)





# Thermistors

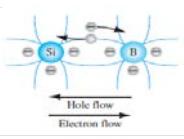
Resistance increases with temperature for PTCs;

Resistance decreases with temperature for NTCs

A resistance variation is generally not directly useful; information is generally relayed with voltage

We need to convert the resistance change to a voltage change

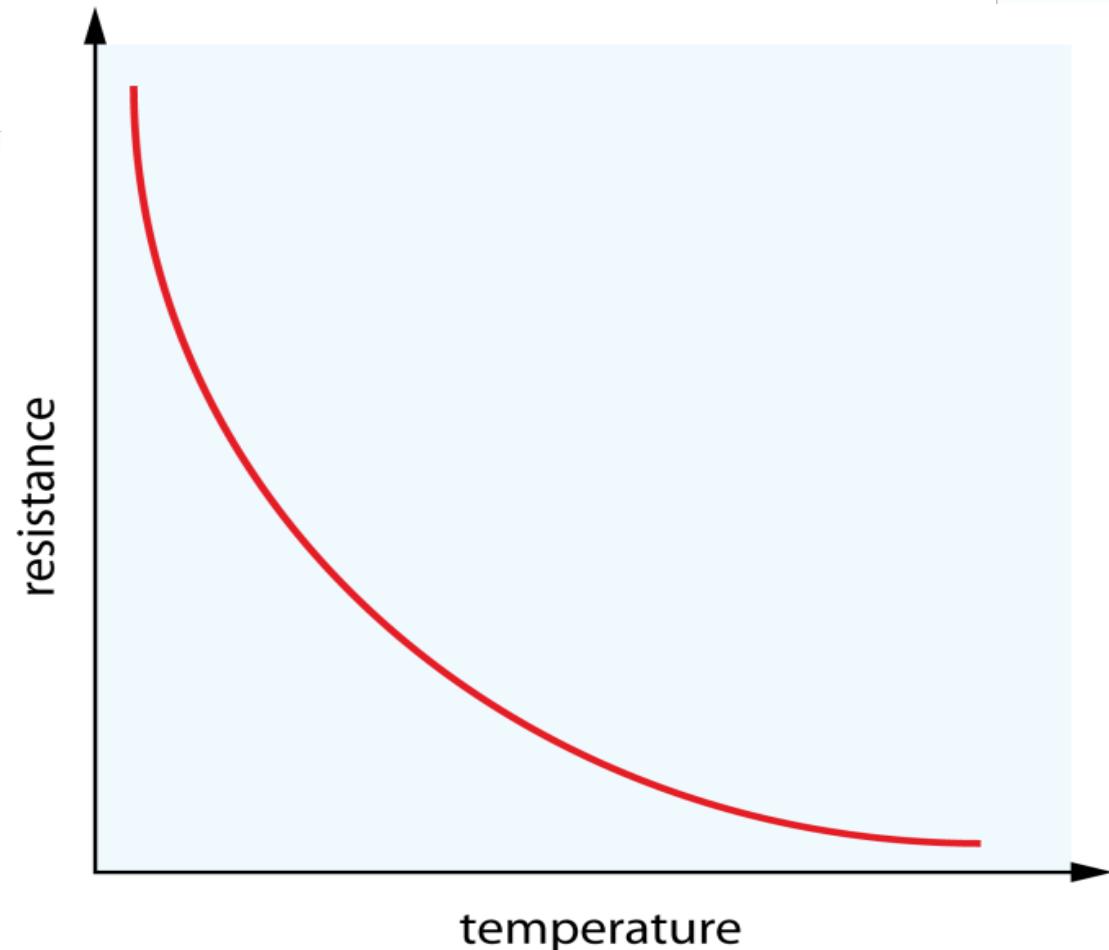


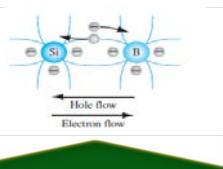


# Thermistors

This graph shows the thermistor's resistance against temperature.

Remember, the resistance of a thermistor decreases as the temperature increases.





# Thermistors Applications

Air conditioning and seat temperature controls.

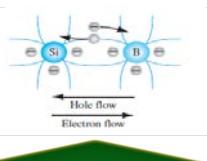
Electronic fuel injection, in which air-inlet, air/fuel mixture and cooling water temperatures are monitored to help determine the fuel concentration for optimum injection.

Warning indicators such as oil and fluid temperatures, oil level and turbo-charger switch off.

Fan motor control, based on cooling water temperature

Frost sensors, for outside temperature measurement





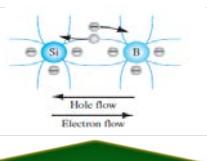
# Thermistors Advantages

High sensitivity to small temperature changes

Temperature measurements become more stable with use

Copper or nickel extension wires can be used





# Thermistors Disadvantages

Limited temperature range

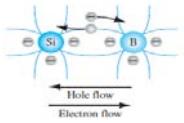
Fragile

Some initial accuracy “drift”

Decalibration if used beyond the sensor’s temperature ratings

Lack of standards for replacement





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# Thank You Very Much

Dipl.-Ing. B. Kommey

[bkommey.coe@knust.edu.gh](mailto:bkommey.coe@knust.edu.gh)

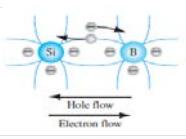
[nii\\_kommey@msn.com](mailto:nii_kommey@msn.com)

Tel: 050 770 32 86

Whatsup: 0049 172 4444 765

Skype\_id: calculus.affairs





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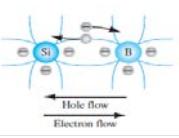
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**“The person who reads too much  
and uses his brain too little will  
fall into lazy habits of thinking”**

**Albert Einstein**





# SEMICONDUCTOR DEVICES

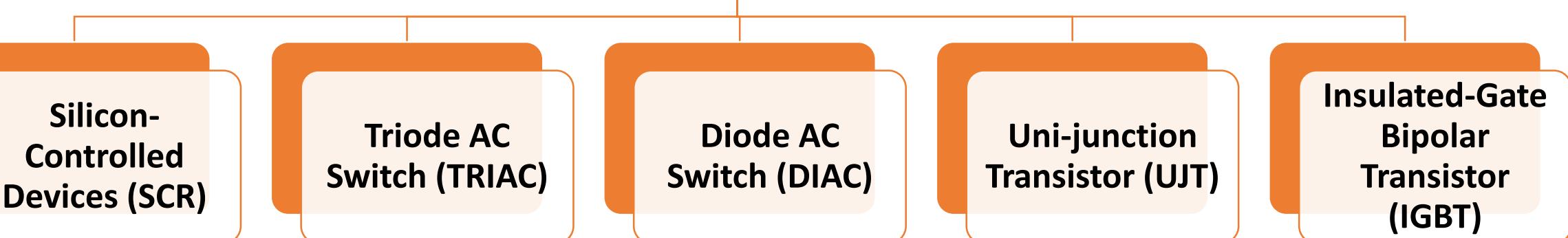
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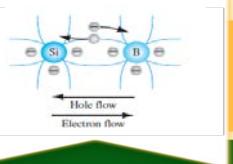
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# Overview

## PNPN Devices



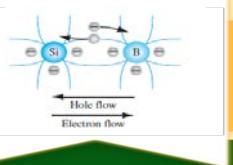


# Silicon-Controlled Rectifier (SCR)

The *silicon-controlled rectifier or semiconductor controlled rectifier* is a two-state device used for efficient power control.

**SCR** is the parent member of the *thyristor family* and is used in *high-power electronics*.





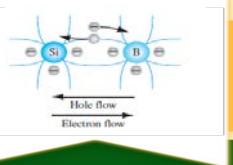
# Silicon-Controlled Rectifier (SCR)

The SCR is the most important special semiconductor device. This device is popular for its *Forward-Conducting* and *Reverse-blocking characteristics*.

SCR can be used in *high-power devices*.

For example, in the central processing unit of the computer, the SCR is used in *switch mode power supply (SMPS)*.





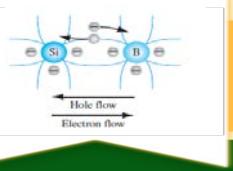
# SCR Constructional Features

The SCR is a ***four-layer structure***,  
either ***p–n–p–n or n–p–n–p***,  
*that effectively blocks current through two terminals until it is turned ***ON*** by a small-signal at a third terminal.*

SCR has ***two states***:  
a ***high-current low-impedance ON state*** and  
***a low-current high-impedance OFF state***.

The basic transistor action in a ***four-layer p–n–p–n structure is analysed first with only two terminals***, and then the third control input is introduced.



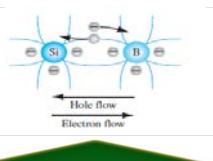


# Physical Operation and Characteristics:

The physical operation of the SCR can be explained clearly with reference to the current-voltage characteristics.

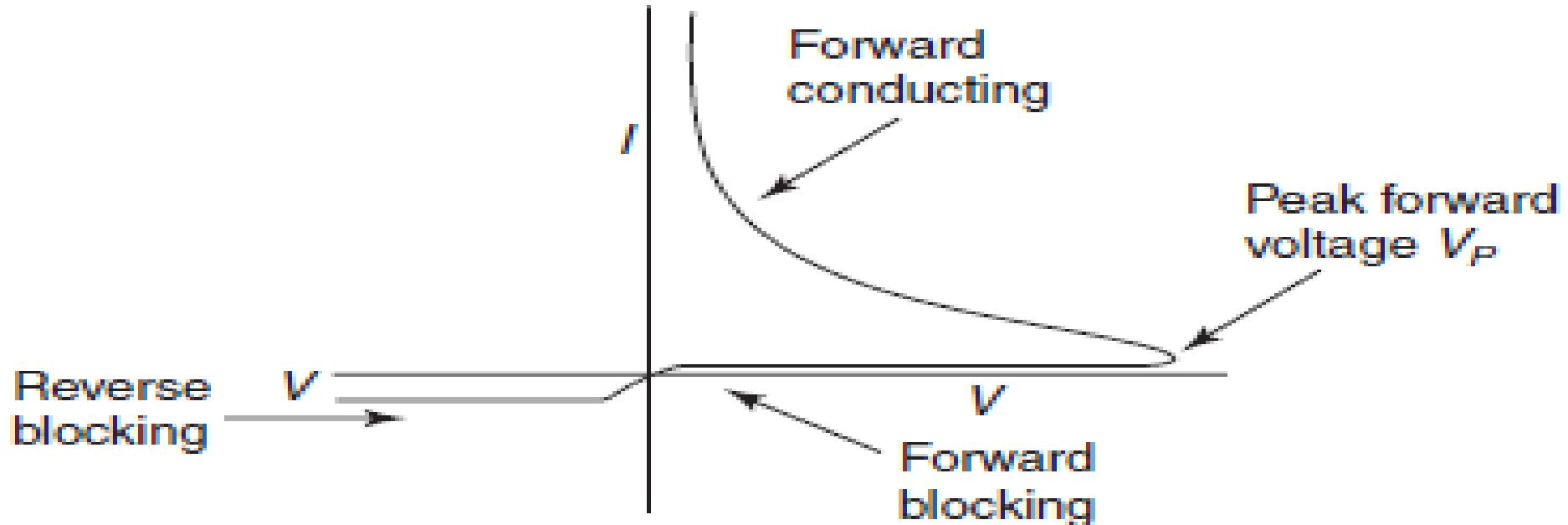
The forward-bias condition and reverse-bias condition illustrate the conducting state and the reverse blocking state respectively.





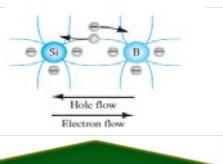
# Physical Operation and Characteristics:

Based on these two states a typical I –V characteristic of the SCR is as shown



I–V characteristics of a two terminal  $p-n-p-n$  device



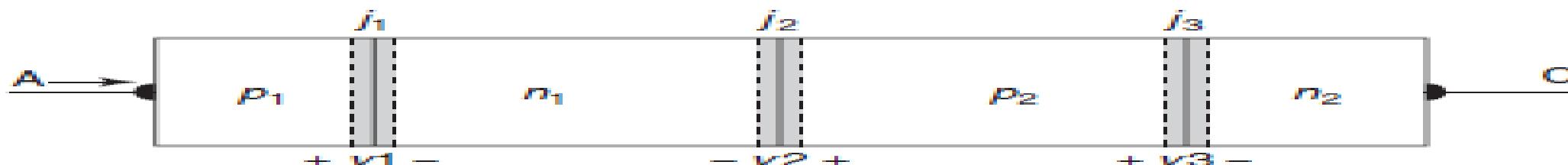


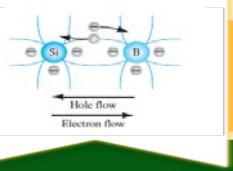
# SCR in Forward Bias

There are two different states in which we can examine the SCR in the forward-biased condition:

- (i) The high- impedance or forward-blocking state
- (ii) The low-impedance or forward-conducting state

At a critical peak forward voltage  $V_p$ , the SCR switches from the blocking state to the conducting state, as shown in slide before.





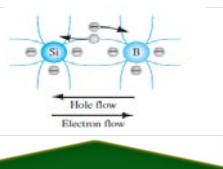
## SCR in Forward Bias

A positive voltage places junction  $j_1$  and  $j_3$  under forward-bias, and the centre junction  $j_2$  under reverse-bias.

The forward voltage in the blocking state appears across the reverse-biased junction  $j_2$  as the applied voltage  $V$  is increased.

The voltage from the anode  $A$  to cathode  $C$ , as shown in Figure, is very small after switching to the forward-conducting state, and all three junctions are forward-biased. The junction  $j_2$  switches from reverse-bias to forward-bias..





## SCR in Reverse Bias:

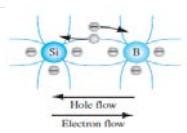
In the reverse-blocking state the junctions  $j_1$  and  $j_3$  are reverse-biased, and  $j_2$  is forward-biased.

The supply of electrons and holes to junction  $j_2$  is restricted, and due to the thermal generation of electron–hole pairs near junctions  $j_1$  and  $j_2$  the device current is a small saturation current.

In the reverse blocking condition the current remains small until avalanche breakdown occurs at a large reverse-bias of several thousand volts.

An SCR  $p\text{--}n\text{--}p\text{--}n$  structure is equivalent to one  $p\text{--}n\text{--}p$  transistor and one  $n\text{--}p\text{--}n$  transistor sharing some common terminals.





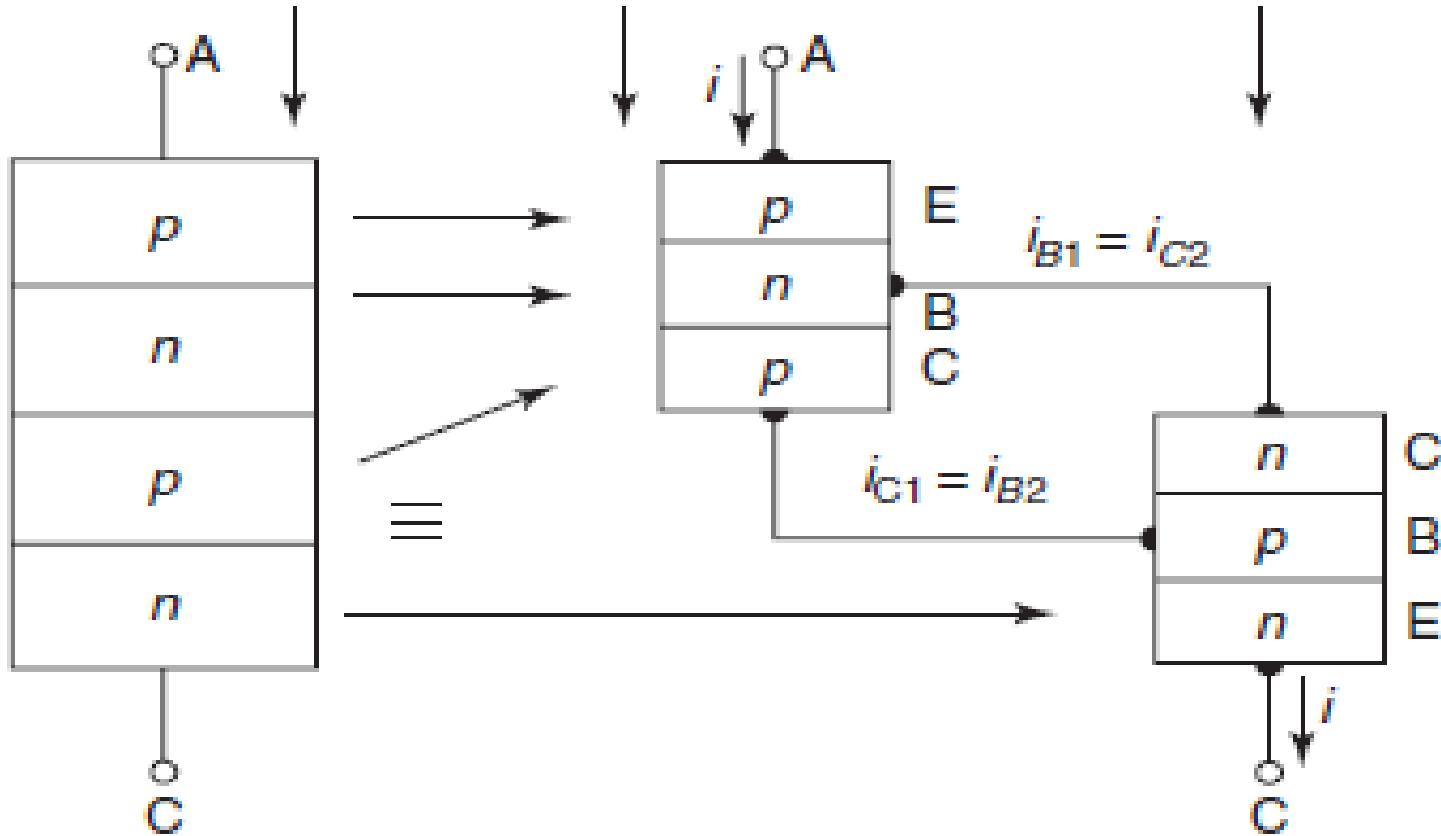
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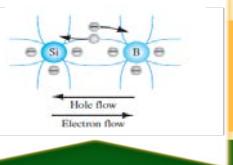
# SCR in Reverse Bias

SCR =  $p-n-p$  transistor +  $n-p-n$  transistor



An SCR  $p-n-p-n$ : a combination of one  $p-n-p$  transistor and one  $n-p-n$  transistor





## SCR in Reverse Bias:

Collector current  $I_{C1} = \alpha_1 i + I_{CO1}$  having a transfer ratio  $\alpha_1$  for the p-n-p.

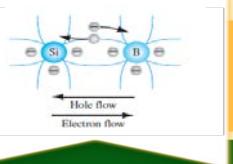
Collector current  $I_{C2} = \alpha_2 i + I_{CO2}$  having a transfer ratio  $\alpha_2$  for the n-p-n.

$I_{CO1}$  and  $I_{CO2}$  stand for the respective collector-saturation currents.

$$I_{C1} = \alpha_1 i + I_{CO1} = I_{B2}$$

$$I_{C2} = \alpha_2 i + I_{CO2} = I_{B1}$$



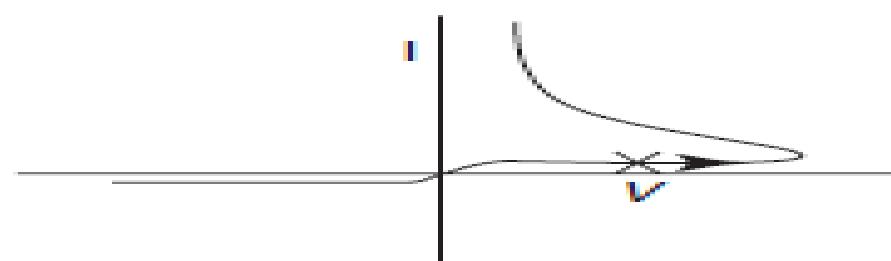


# I-V Characteristics of the SCR

## Forward-Blocking State:

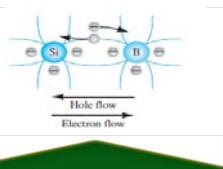
When the device is biased in the forward-blocking state, as shown in the figure below, the applied voltage appears primarily across the reverse-biased junction  $j_2$ .

*Although the junctions  $j_1$  and  $j_3$  are forward-biased, the current is small.*



The forward-blocking state of the SCR





# I-V Characteristics of the SCR

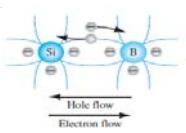
## Forward-Conducting State of the SCR:

As the value of  $(\alpha_1 + \alpha_2)$  approaches unity through one of the mechanisms ,many holes injected at  $j_1$  survive to be swept across  $j_2$  into  $p_2$ .

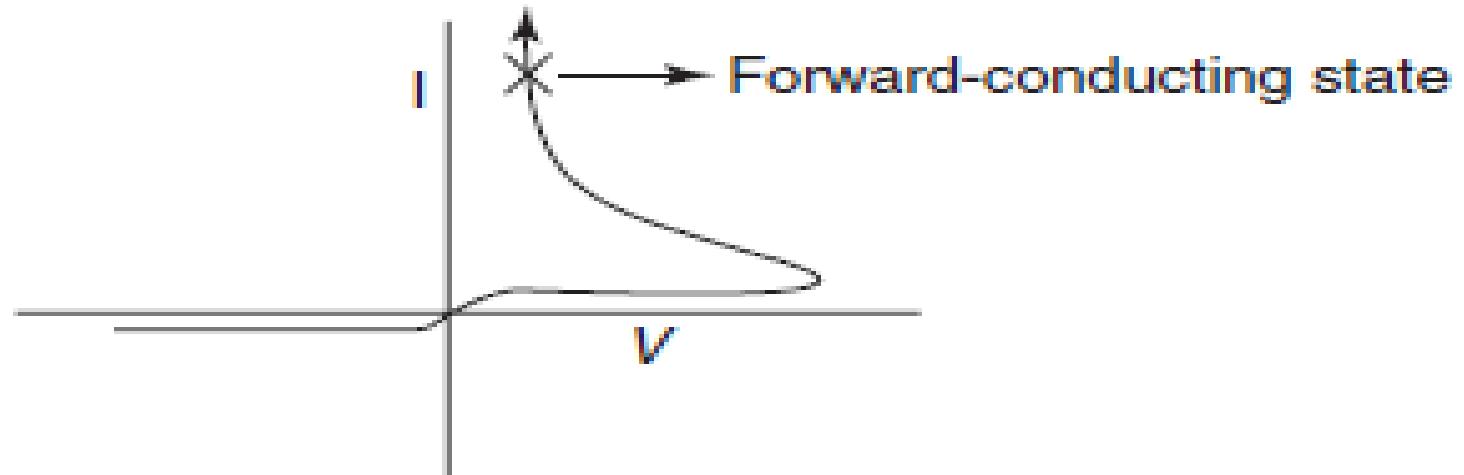
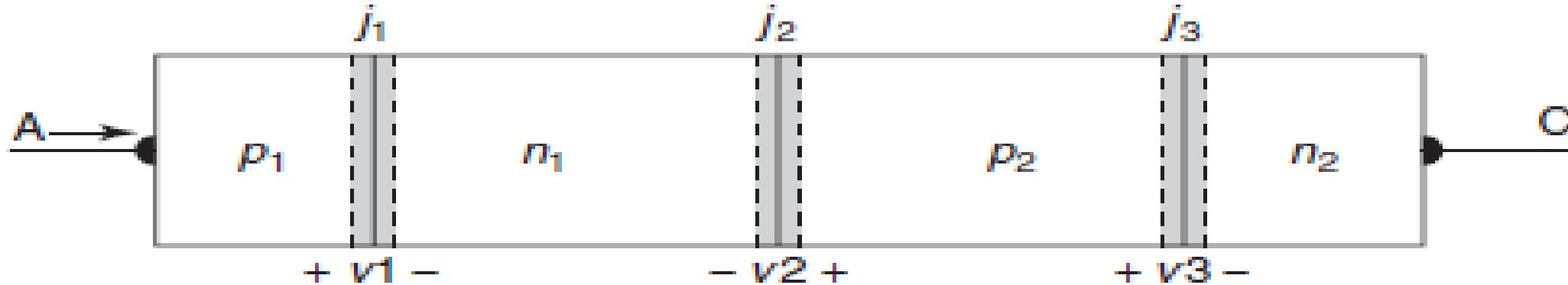
*This process helps feed the recombination in  $p_2$  and support the injection of holes into  $n_2$ . In a similar manner, the transistor action of electrons injected at  $j_3$  and collected at  $j_2$  supplies electrons for  $n_1$ .*

*The current through the device can be much larger.*



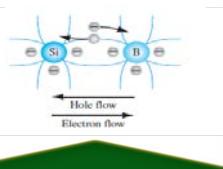


# I-V Characteristics of the SCR



Forward-conducting state of the SCR





# Reverse-Blocking State of the SCR

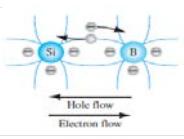
The SCR in reverse-biased condition allows almost negligible current to flow through it.

In the reverse-blocking state of the SCR, a small saturation current flows from anode to cathode.

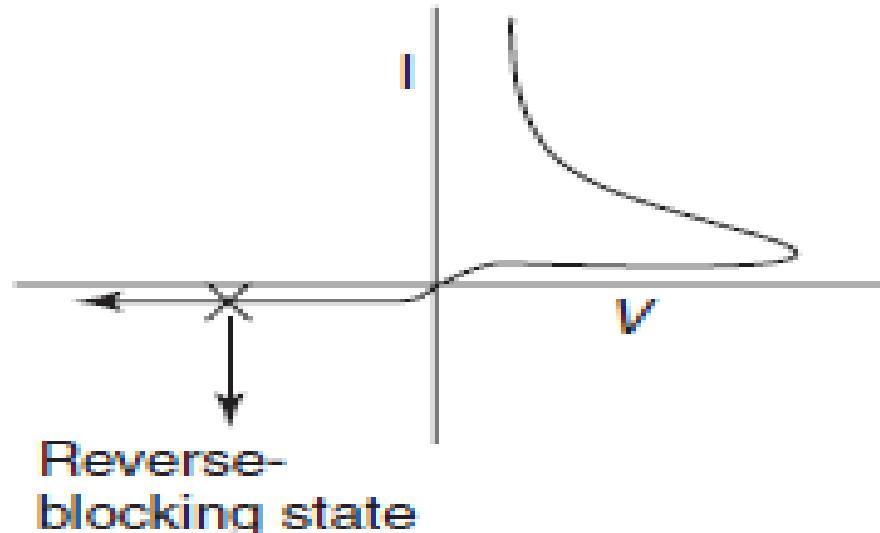
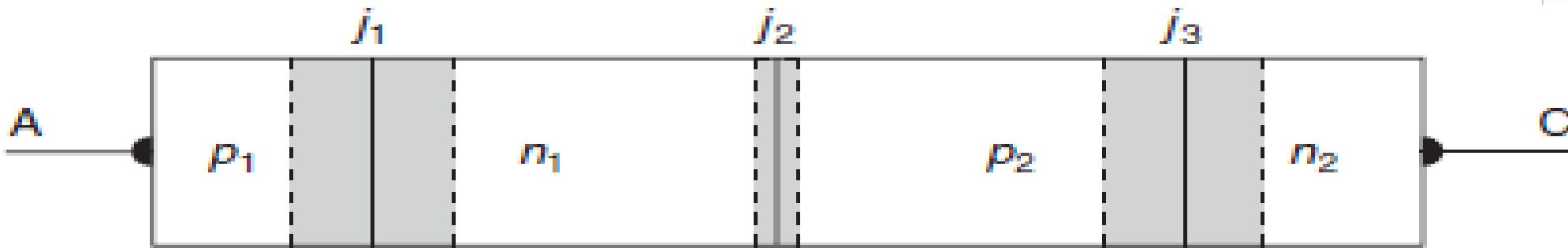
Holes will flow from the gate into  $p_2$ , *the base of the  $n-p-n$  transistor, due to positive gate current.*

The required gate current for turn-on is only a few milliamperes, therefore, the SCR can be turned on by a very small amount of power in the gate.



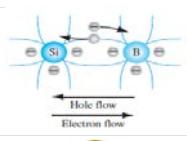


# Reverse-Blocking State of the SCR



Reverse-blocking state of the SCR



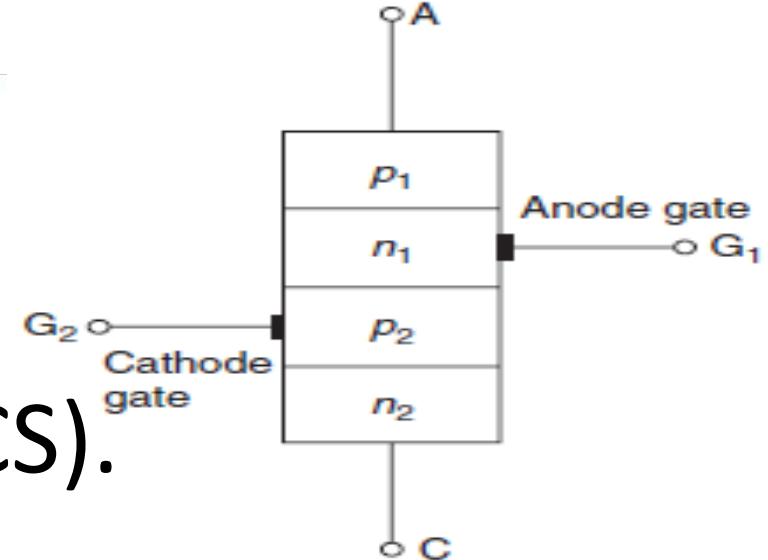


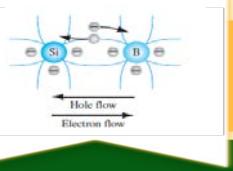
# Semiconductor-controlled switch (SCS)

Few SCRs have two gate leads,  $G_2$  attached to  $p_2$  and  $G_1$  attached to  $n_1$ .

*This configuration is called the semiconductor-controlled switch (SCS).*

The SCS, biased in the forward-blocking state, can be switched to the conducting state by a negative pulse at the anode gate  $n_1$  or by a positive current pulse applied to the cathode gate at  $p_2$ .



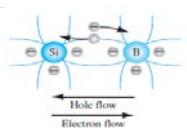


# Triode AC Switch (TRIAC)

The term TRIAC is derived by combining the first three letters of the word “TRIODE” and the word “AC”.

A TRIAC is capable of conducting in both the directions. The TRIAC, is thus, a bidirectional thyristor with three terminals. It is widely used for the control of power in ac circuits.



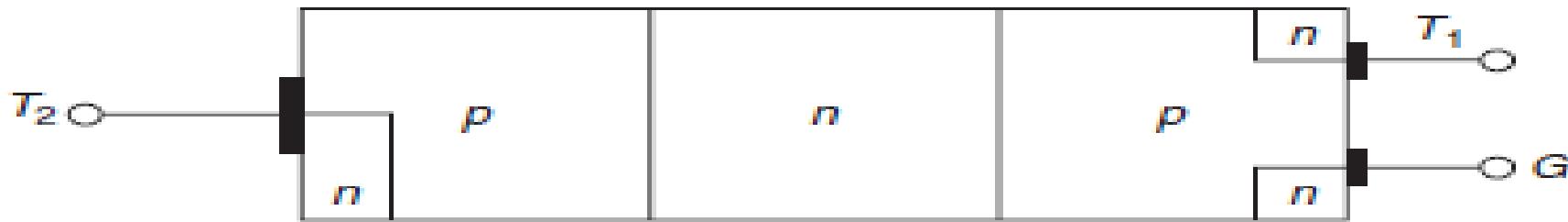


SEMICONDUCTOR DEVICES  
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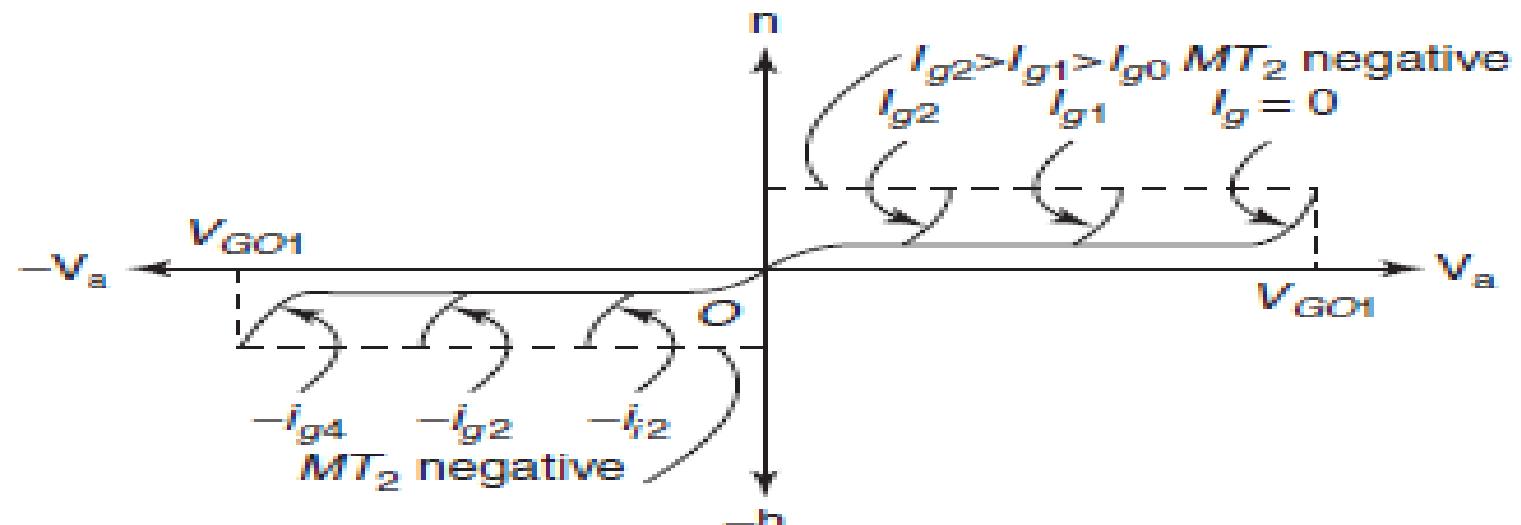
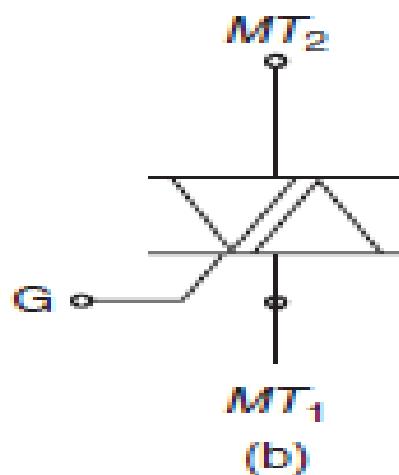
KWAME NKRUMAH UNIVERSITY OF SCIENCE  
AND TECHNOLOGY, KUMASI, GHANA



# Triode AC Switch (TRIAC)

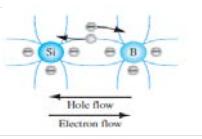


(a)



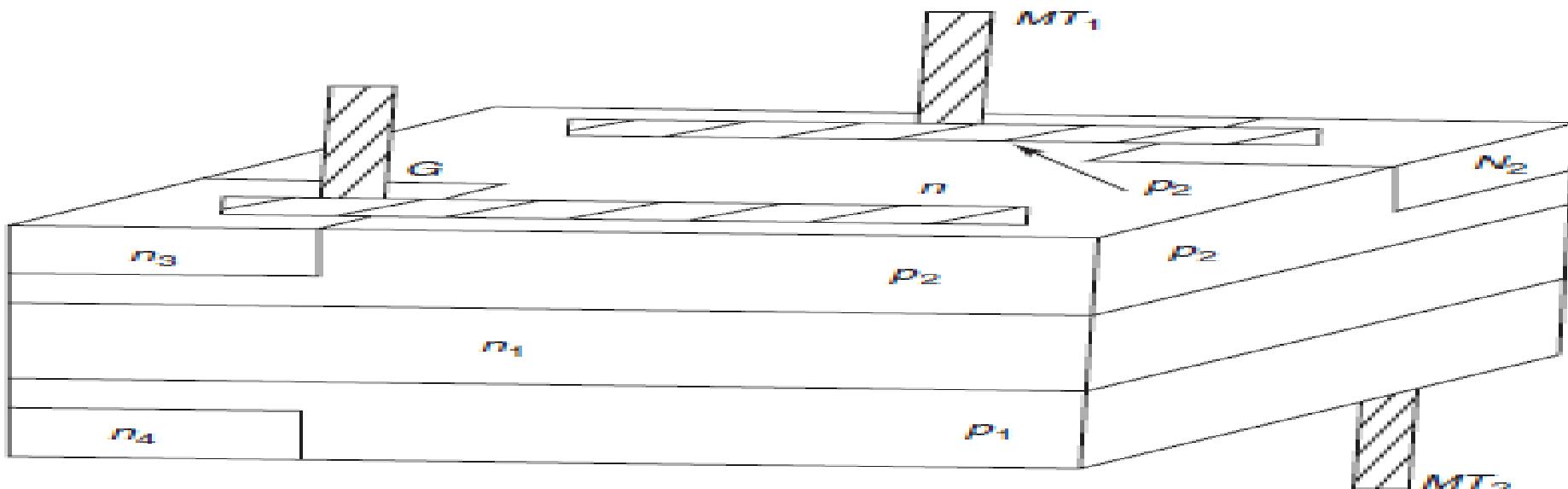
(a) Structure of TRIAC (b) Circuit symbol (c) Static I-V characteristics





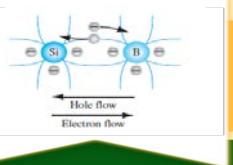
# Constructional Features

Depending upon the polarity of the gate pulse and the biasing conditions, the main four-layer structure that turns ON by a regenerative process could be one of  $p_1 n_1$ ,  $p_2 n_2$ ,  $p_1 n_1 p_2 n_3$ , or  $p_2 n_1 p_1 n_4$



Cross-sectional view of the TRIAC



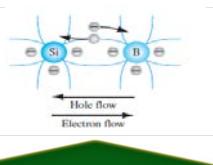


# Advantages of the TRIAC

The TRIAC has the following advantages

- (i) They can be triggered with positive- or negative-polarity voltage.
- (ii) They need a single heat sink of slightly larger size.
- (iii) They need a single fuse for protection, which simplifies their construction.
- (iv) In some dc applications, the SCR has to be connected with a parallel diode for protection against reverse voltage, whereas a TRIAC may work without a diode, as safe breakdown in either direction is possible.



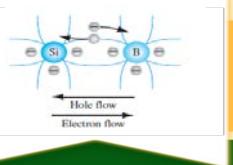


# Disadvantages of the TRIAC

The TRIAC has the following disadvantages

- (i) TRIACs have low  $dv/dt$  ratings compared to SCRs.
- (ii) Since TRIACs can be triggered in either direction, the trigger circuits with TRIACs needs careful consideration.
- (iii) Reliability of TRIACs is less than that of SCRs.





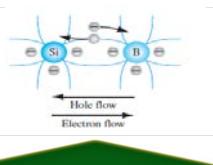
# Simple Applications of the TRIAC

The TRIAC as a bidirectional thyristor has various applications.

Some of the popular applications of the TRIAC are as follows:

- (i) In speed control of single-phase ac series or universal motors.
- (ii) In food mixers and portable drills.
- (iii) In lamp dimming and heating control.
- (iv) In zero-voltage switched ac relay.

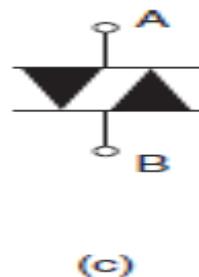
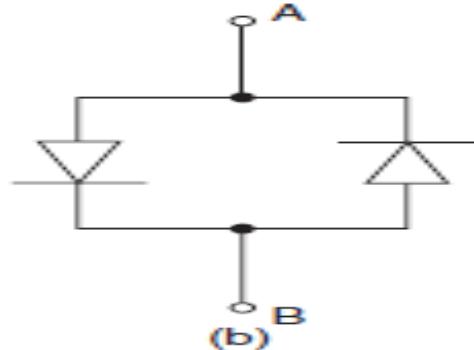




# Diode AC Switch (DIAC)

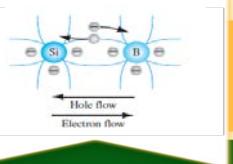
The DIAC is a combination of two diodes. Diodes being unidirectional devices, conduct current only in one direction.

If bidirectional (ac) operation is desired, two Shockley diodes may be joined in parallel facing different directions to form the DIAC.



(a) Basic structure of the DIAC (b) Equivalent circuit of the DIAC (c) Symbol of the DIAC





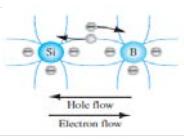
# DIAC Constructional Features

The construction of DIAC looks like a transistor but there are major differences.

## They are as follows

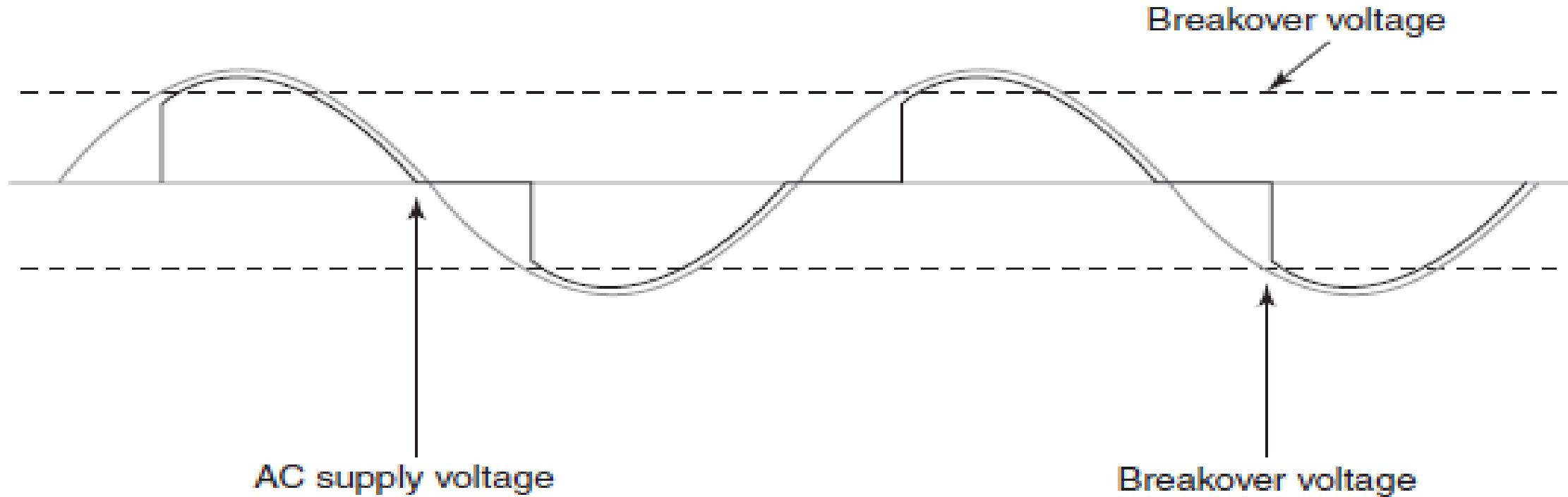
All the three layers,  $p-n-p$  or  $n-p-n$ , are *equally doped* in the DIAC, whereas in the BJT there is a *gradation* of doping. The emitter is highly doped, the collector is lightly doped, and the base is moderately doped.





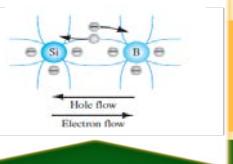
## DIAC Constructional Features

The DIAC is a two-terminal diode as opposed to the BJT, which is a three-terminal device.



Current waveform in the DIAC





# Physical Operation and Characteristics

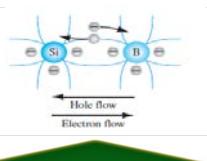
The main characteristics of the DIAC are as follows

- (i) Break over voltage
- (ii) Voltage symmetry
- (iii) Break-back voltage
- (iv) Break over current
- (v) Lower power dissipation

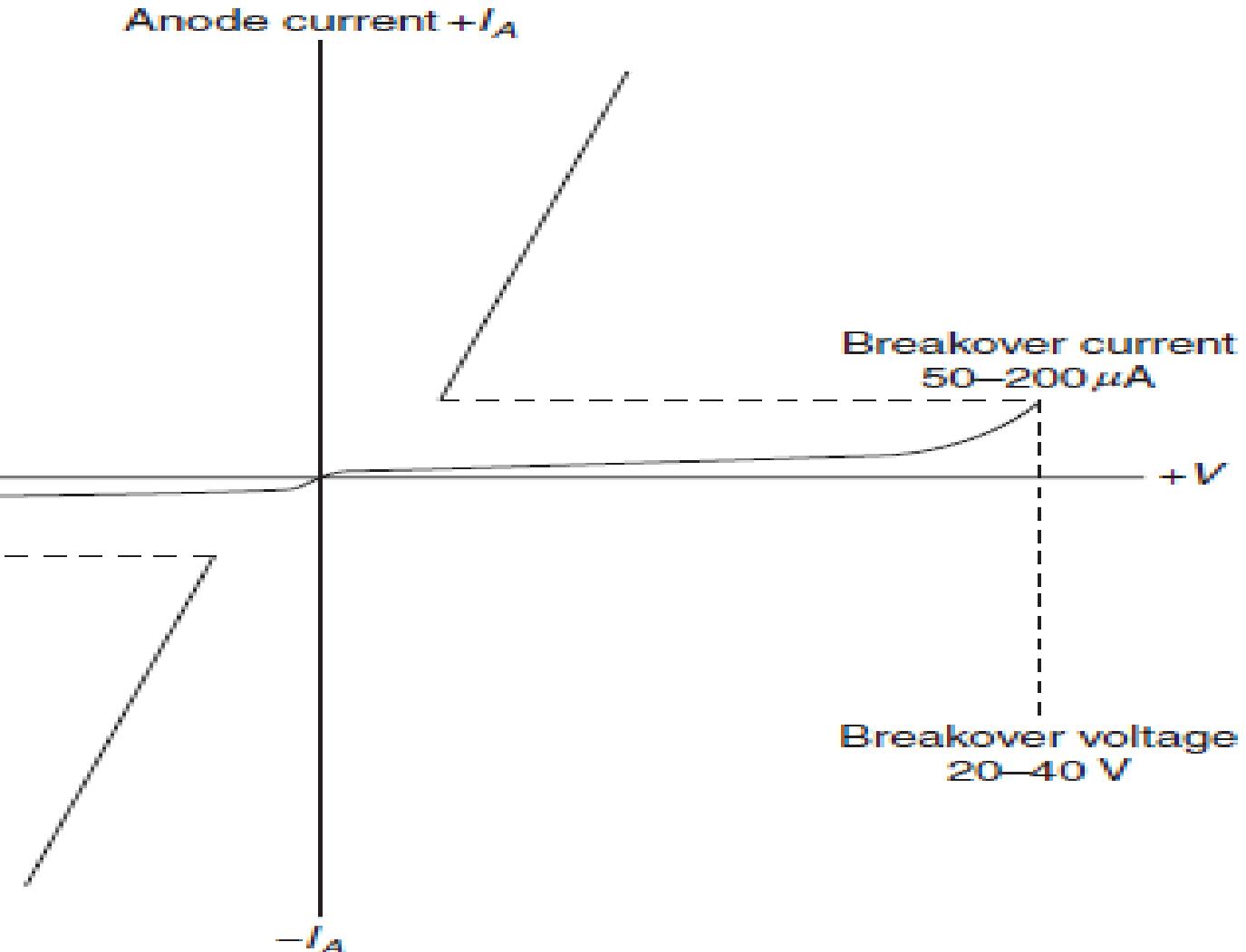
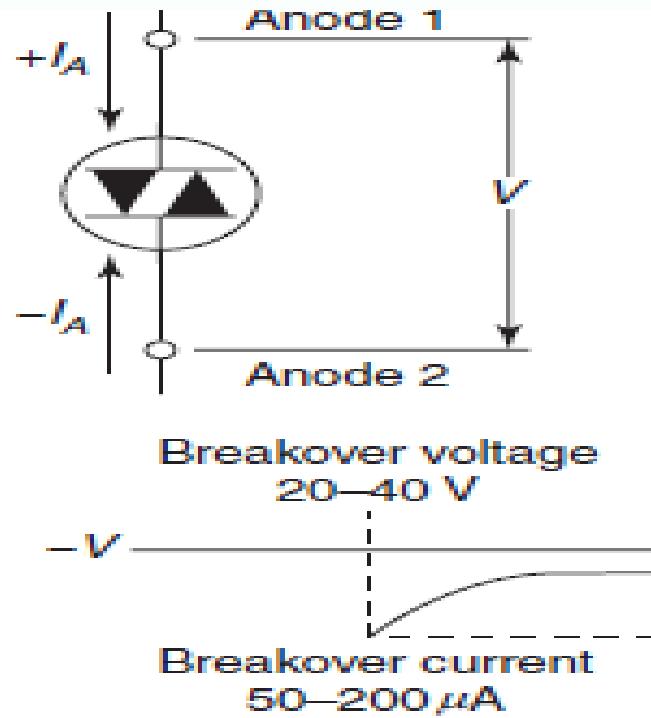
Although most DIACs have symmetric switching voltages, asymmetric DIACs are also available.

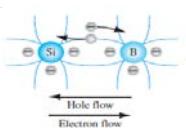
Typical DIACs have a power dissipations ranging from 1/2 to 1 watt.





# I-V Characteristics of the DIAC

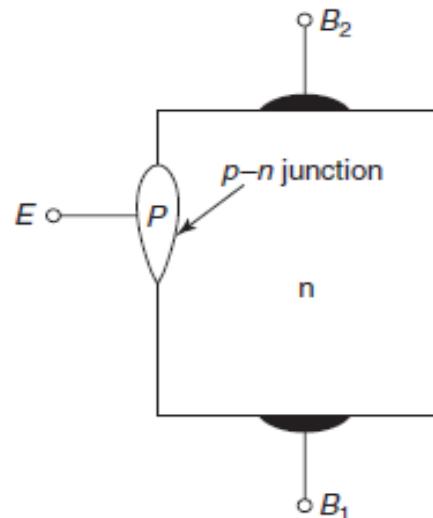




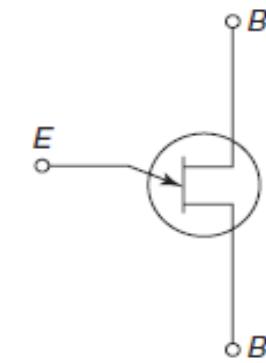
# Unijunction Transistor (UJT)

The uni-junction transistor is a three-terminal single-junction device. The switching voltage of the UJT can be easily varied.

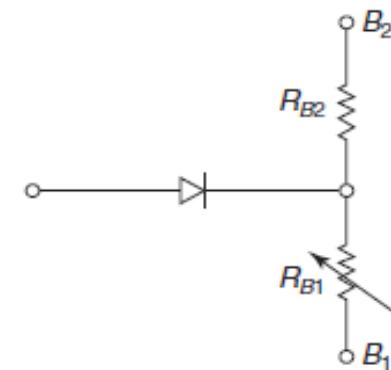
The UJT is always operated as a switch in oscillators, timing circuits and in SCR/TRIAC trigger circuits.

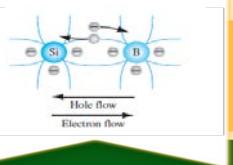


(a)



(b)





# Constructional Features

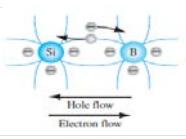
The UJT structure consists of a lightly doped *n*-type silicon bar provided with ohmic contacts on either side.

The two end connections are called base *B*<sub>1</sub> and base *B*<sub>2</sub>. A small heavily doped *p*-region is alloyed into one side of the bar.

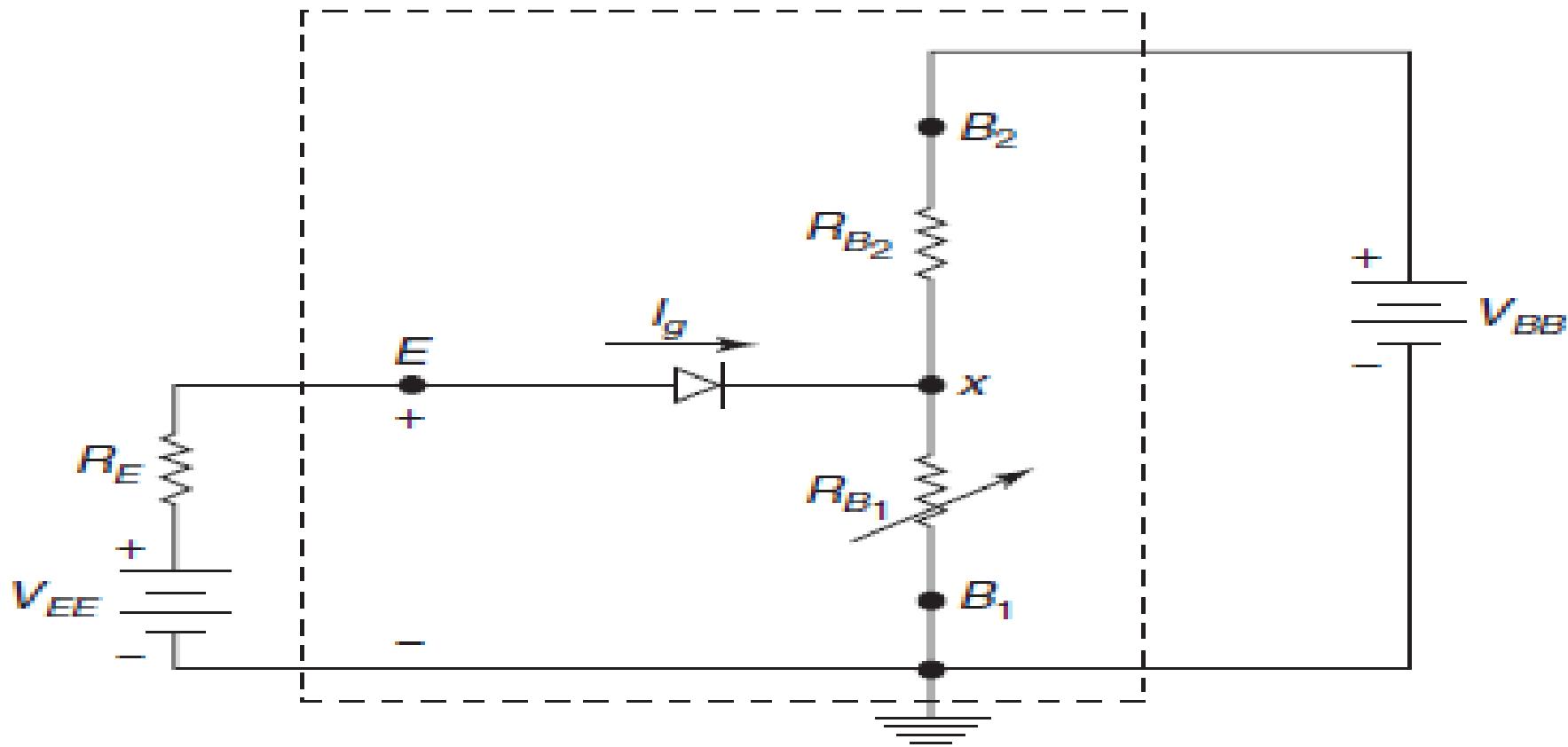
*This p-region is the UJT emitter (E) that forms a p–n junction with the bar.*

*Between base *B*<sub>1</sub> and base *B*<sub>2</sub>, the resistance of the *n*-type bar called inter-base resistance (*R*<sub>B</sub>) and is in the order of a few kilo ohm.*



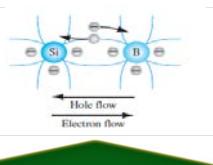


# Equivalent circuit for UJT



Equivalent circuit for UJT analysis





## Constructional Features

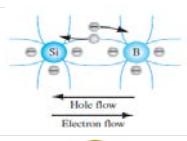
This inter-base resistance can be broken up into two resistances—the resistance from  $B_1$  to the emitter is  $RB_1$  and the resistance from  $B_2$  to the emitter is  $RB_2$ .

*Since the emitter is closer to  $B_2$  the value of  $RB_1$  is greater than  $RB_2$ .*

Total resistance is given by:

$$RB = RB_1 + RB_2$$



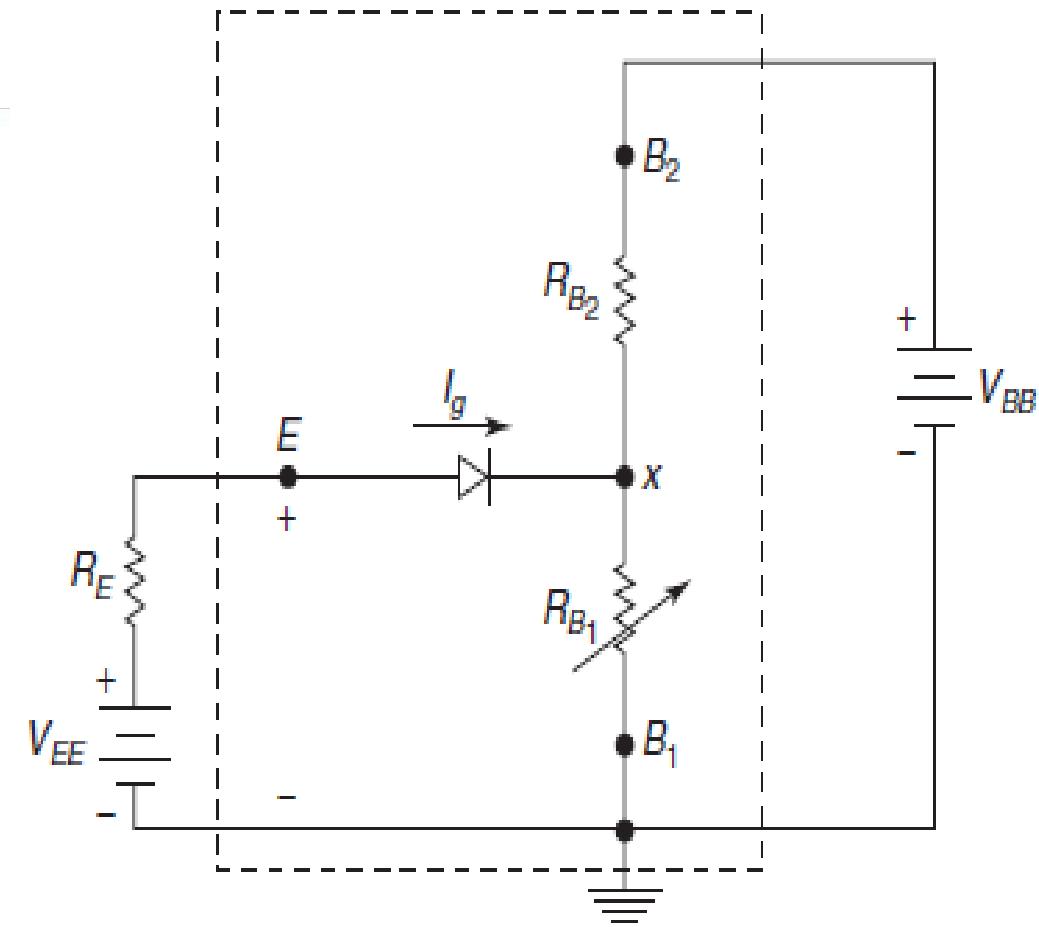


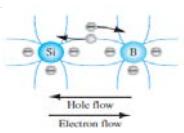
# Equivalent circuit for UJT

The  $V_{BB}$  source is generally fixed and provides a constant voltage from  $B_2$  to  $B_1$ .

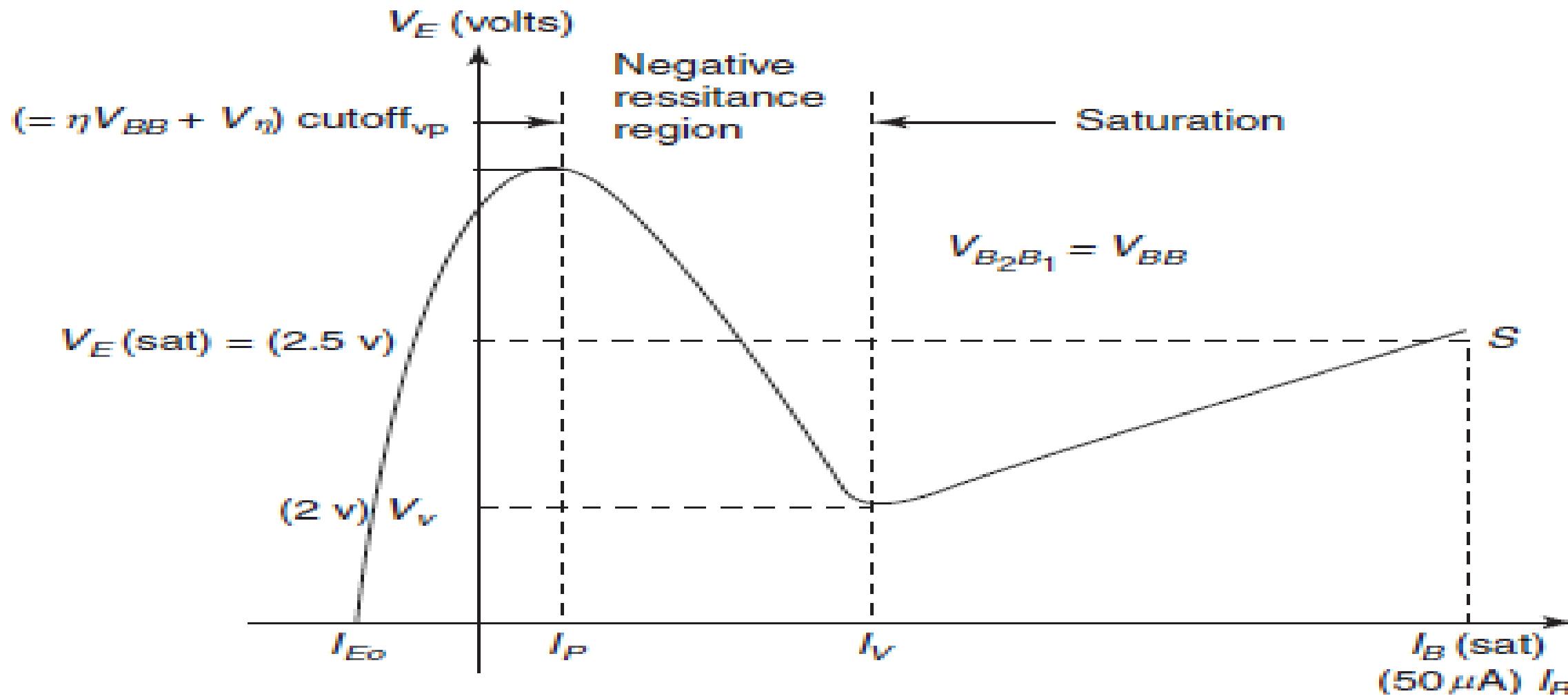
The UJT is normally operated with both  $B_2$  and  $E$  positive biased relative to  $B_1$ .

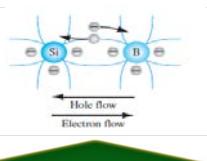
$B_1$  is always the UJT reference terminal and all voltages are measured relative to  $B_1$ .  $V_{EE}$  is a variable voltage source.





# UJT V-I Characteristic Curves



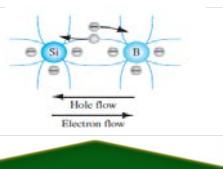


## ON State of the UJT Circuit

*As  $V_{EE}$  increases, the UJT stays in the OFF state until  $V_E$  approaches the peak point value  $V_P$ . As  $V_E$  approaches  $V_P$  the p–n junction becomes forward-biased and begins to conduct in the opposite direction.*

*As a result  $I_E$  becomes positive near the peak point  $P$  on the  $V_E$ -  $I_E$  curve. When  $V_E$  exactly equals  $V_P$  the emitter current equals  $I_P$ .*





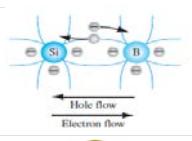
## ON State of the UJT Circuit

*At this point holes from the heavily doped emitter are injected into the n-type bar, especially into the B1 region. The bar, which is lightly doped, offers very little chance for these holes to recombine.*

The lower half of the bar becomes replete with additional current carriers (holes) and its resistance  $RB$  is drastically reduced; the decrease in  $BB1$  causes  $Vx$  to drop.

*This drop, in turn, causes the diode to become more forward-biased and  $IE$  increases even further.*





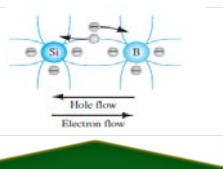
## OFF State of the UJT Circuit

When a voltage  $V_{BB}$  is applied across the two base terminals  $B_1$  and  $B_2$ , the potential of point  $p$  with respect to  $B_1$  is given by:

$$V_P = [V_{BB} / (R_{B1} + R_{B2})] * R_{B1} = \eta * R_{B1}$$

$\eta$  is called the intrinsic stand off ratio with its typical value lying between 0.5 and 0.8.



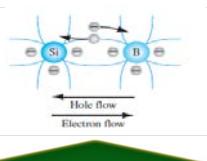


## OFF State of the UJT Circuit

The  $V_{EE}$  source is applied to the emitter which is the p-side. Thus, the emitter diode will be reverse-biased as long as  $V_{EE}$  is less than  $V_x$ . This is OFF state and is shown on the  $V_E$  -  $I_E$  curve as being a very low current region.

In the OFF the UJT has a very high resistance between E and  $B_1$ , and  $I_E$  is usually a negligible reverse leakage current. With no  $I_E$ , the drop across  $R_E$  is zero and the emitter voltage equals the source voltage.





# UJT Ratings

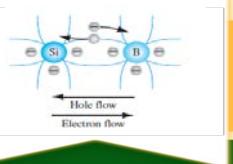
## Maximum peak emitter current

This represents the maximum allowable value of a pulse of emitter current.

## Maximum reverse emitter voltage

This is the maximum reverse-bias that the emitter base junction  $B_2$  can tolerate before breakdown occurs.





## UJT Ratings

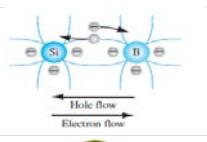
### Maximum inter base voltage

This limit is caused by the maximum power that the *n-type base bar* can safely dissipate.

### Emitter leakage current :

This is the emitter current which flows when  $V_E$  is less than  $V_p$  and the UJT is in the OFF state.





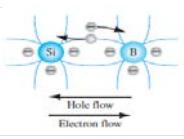
# Applications

The UJT is very popular today mainly due to its high switching speed.

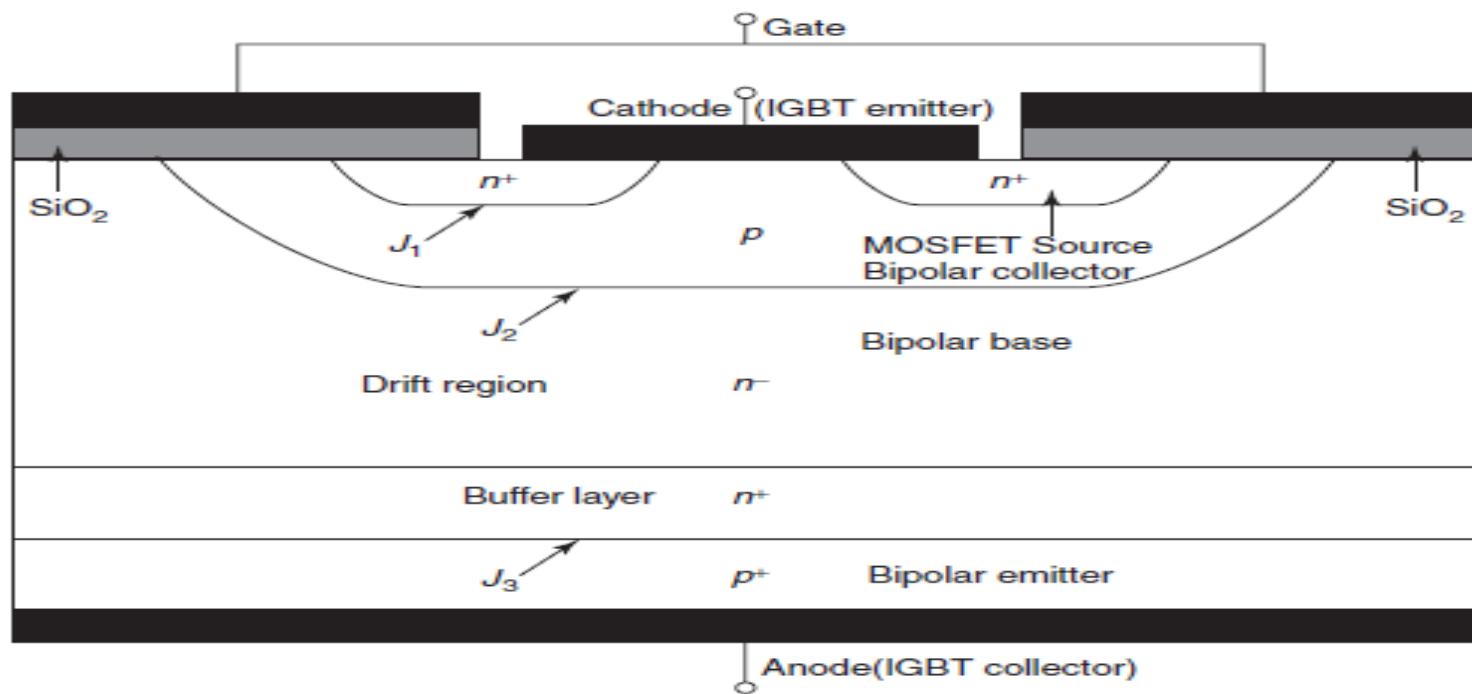
**A few select applications of the UJT are as follows**

- (i) It is used to trigger SCRs and TRIACs
- (ii) It is used in non-sinusoidal oscillators
- (iii) It is used in phase control and timing circuits
- (iv) It is used in saw tooth generators
- (v) It is used in oscillator circuit design





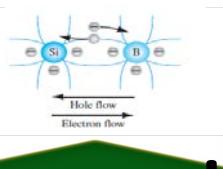
# Insulated-Gate Bipolar Transistor (IGBT)



The insulated-gate bipolar transistor is a recent model of a power-switching device that combines the advantages of a power BJT and a power MOSFET.

Both power MOSFET and IGBT are the continuously controllable voltage-controlled switch.





# Insulated-Gated Bipolar Transistor (IGBT)

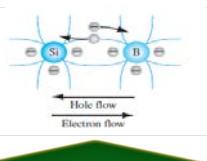
## Constructional Features

The *p* region acts as a substrate which forms the anode region, i.e., the collector region of the IGBT. Then there is a buffer layer of *n* region and a bipolar-base drift region.

The *p*-region contains two *n* regions and acts as a MOSFET source. An inversion layer can be formed by applying proper gate voltage.

The cathode, i.e., the IGBT emitter is formed on the *n* source region.



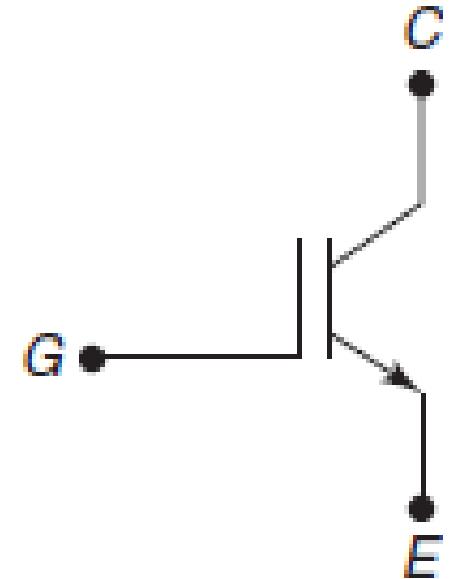


# Physical Operation

The principle behind the operation of an IGBT is similar to that of a power MOSFET.

**The IGBT operates in two modes:**

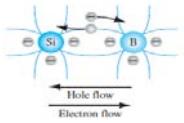
- (i) The blocking or non-conducting mode
- (ii) The ON or conducting mode.



The **circuit symbol** for the IGBT is shown beside

It is similar to the symbol for an *n–p–n bipolar-junction power transistor* with the insulated-gate terminal replacing the base.





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# Thank You Very Much

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