



EE/COE 152: Basic Electronics

Lecture 3

A.S Agbemenu

<https://sites.google.com/site/agbemenu/courses/ee-coe-152>

Books:

Microelectronic Circuit Design (Jaeger/Blalock)

Microelectronic Circuits (Sedra/Smith)



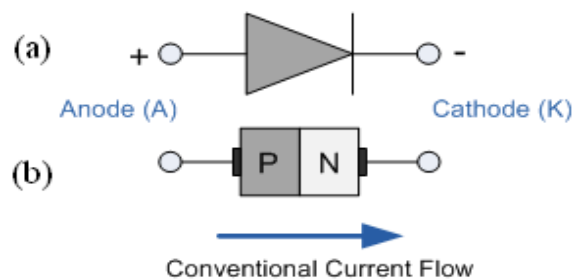
Outline

- PN Junction
- Diode Operation Modes
- Diode Models
- Diode Circuit Analysis
- Rectifier Circuits

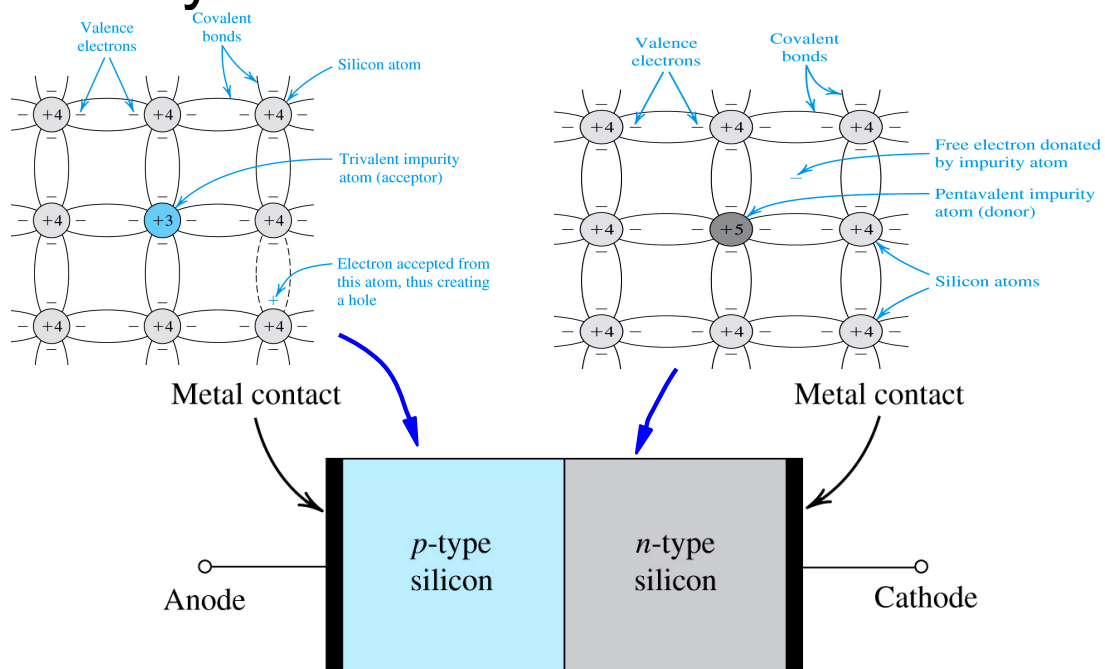


PN Junction

- A PN junction is formed when a P-type (acceptor) semiconductor is joined to a N-type (donor) semiconductor such that the crystal structure remains continuous at the boundary
- This type of semiconductor configuration is called a **diode**



Physical Structure of the Diode





The PN Characteristics

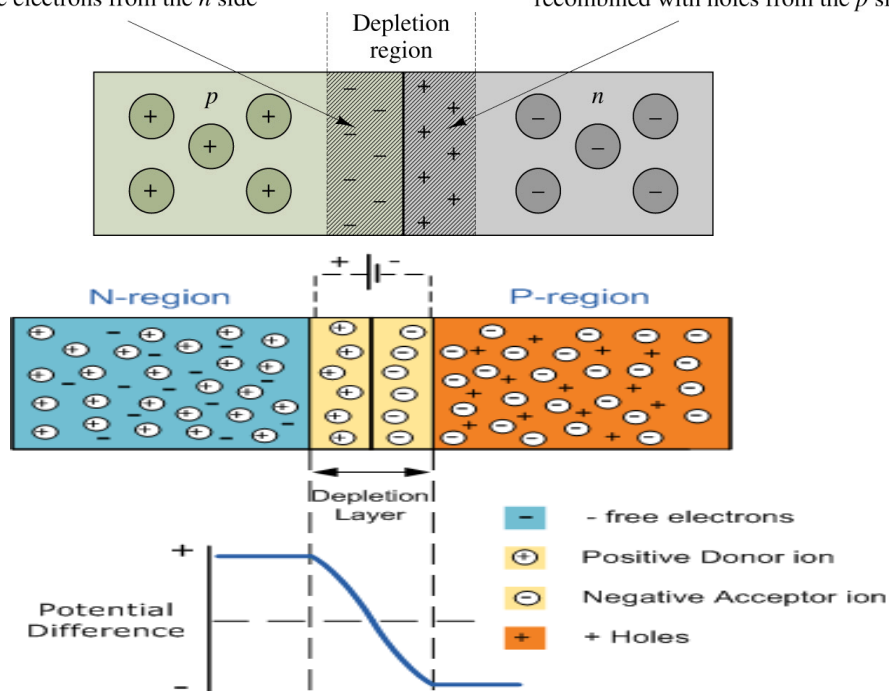
- Electrons diffuse from the n-region junction to the p-region junction
- This diffusion created negative ions at the p-side of the junction and positive ions at the n-side of the junction
- Enough potential is built up to prevent any further diffusion of charge carriers
- This potential is **Barrier/Junction Potential** and the charged region **Depletion region/layer**



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The *p*-side depletion region is negatively charged because its holes have recombined with free electrons from the *n* side

The *n*-side depletion region is positively charged because its free electrons have recombined with holes from the *p* side





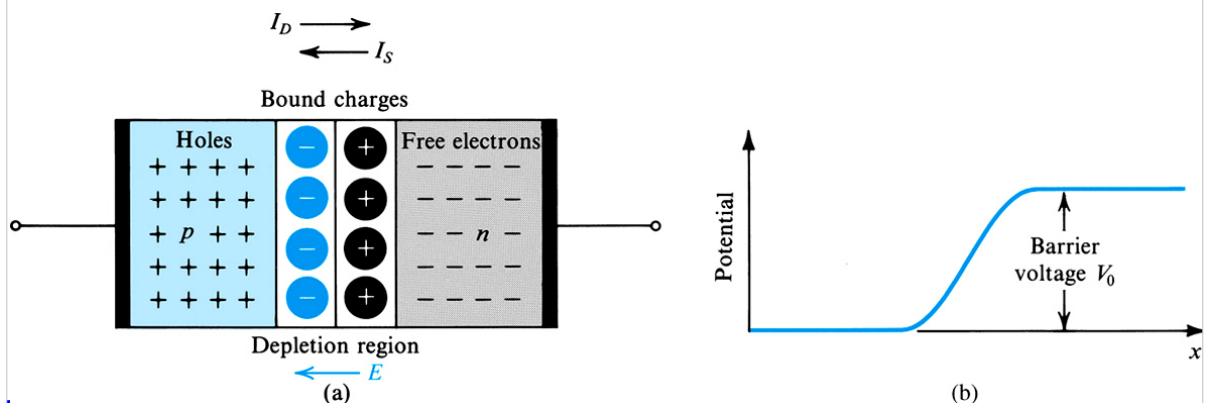
The Diode

- The diode operates in three modes
 - No Bias Mode
 - When no external voltage is applied to the terminals
 - Forward Bias Mode
 - When the terminals are connected such that the positive terminal is connected to the P-region and the negative terminal is connected to the N-region
 - Reverse Bias Mode
 - When the negative terminal is connected to the P-region and the positive terminal to the N-region



No Bias Mode

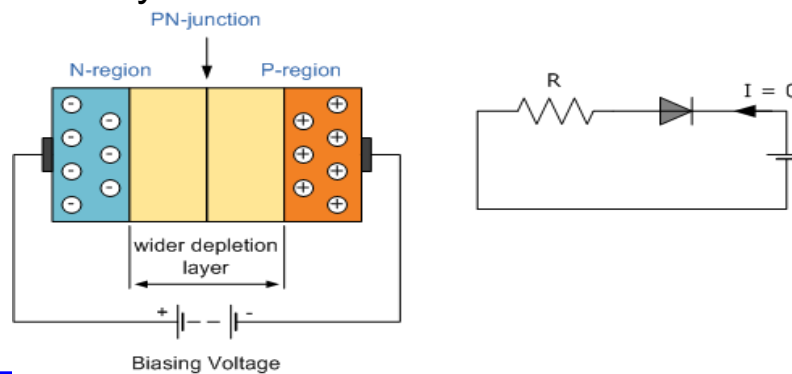
- Majority carriers diffuse into other region causing diffusion current, I_D
- Thermally generated minority charge carriers drift (generate drift current, I_S) across the junction due to electric field generated by the depletion region.





Reverse Bias Mode

- In this mode the junction potential is effectively reinforced widening the depletion layer
- Free electrons from the n-region are attracted towards the positive terminal and electrons from the negative terminal enter the p-region widening the depletion layer

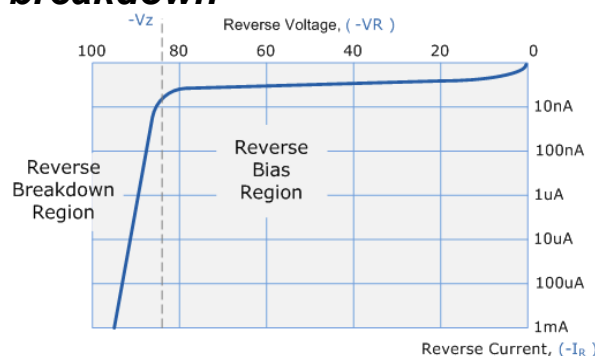


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Reverse Bias Mode

- In reverse bias mode a small **leakage current** flows through the junction
- Increasing the reverse voltage sufficiently will overheat the junction. This voltage is the **breakdown voltage**
- The thermal energy created large electron-hole pair causing large currents to flow in a phenomenon called **avalanche breakdown**

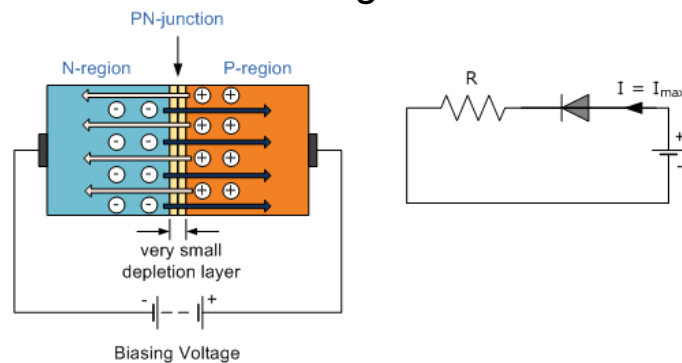


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Forward Bias Mode

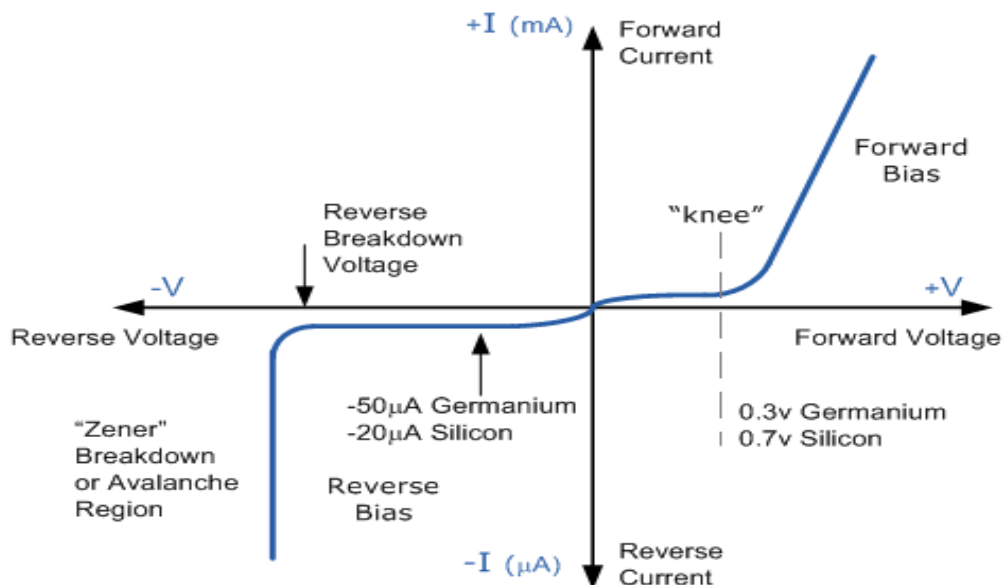
- In this mode, the electric field is applied in the opposite direction to the barrier potential which results in the depletion layer becoming very thin
- When the applied voltage is greater than the barrier potential($0.7V$ for silicon and $0.3V$ for germanium) , the diode starts conducting



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Diode Characteristics Curve

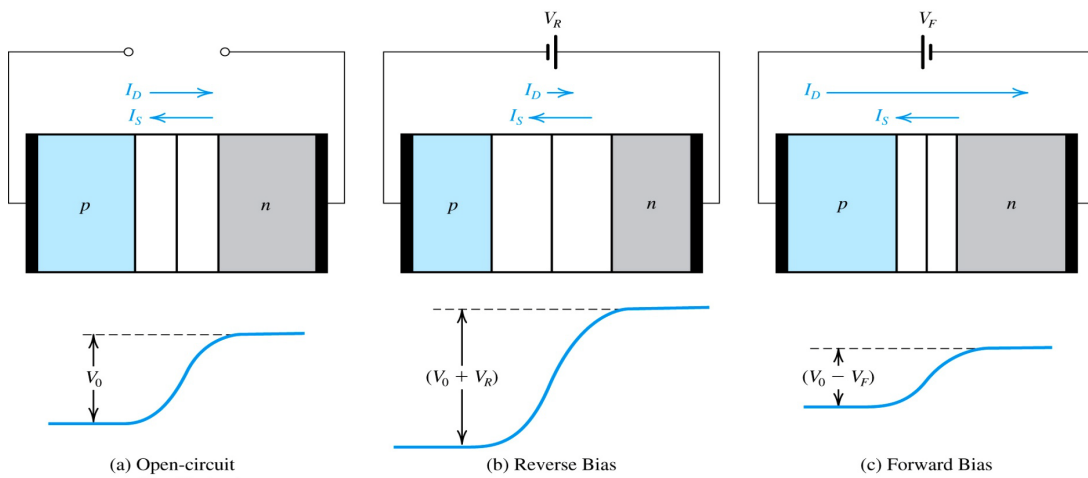


I - V characteristic curve of a diode

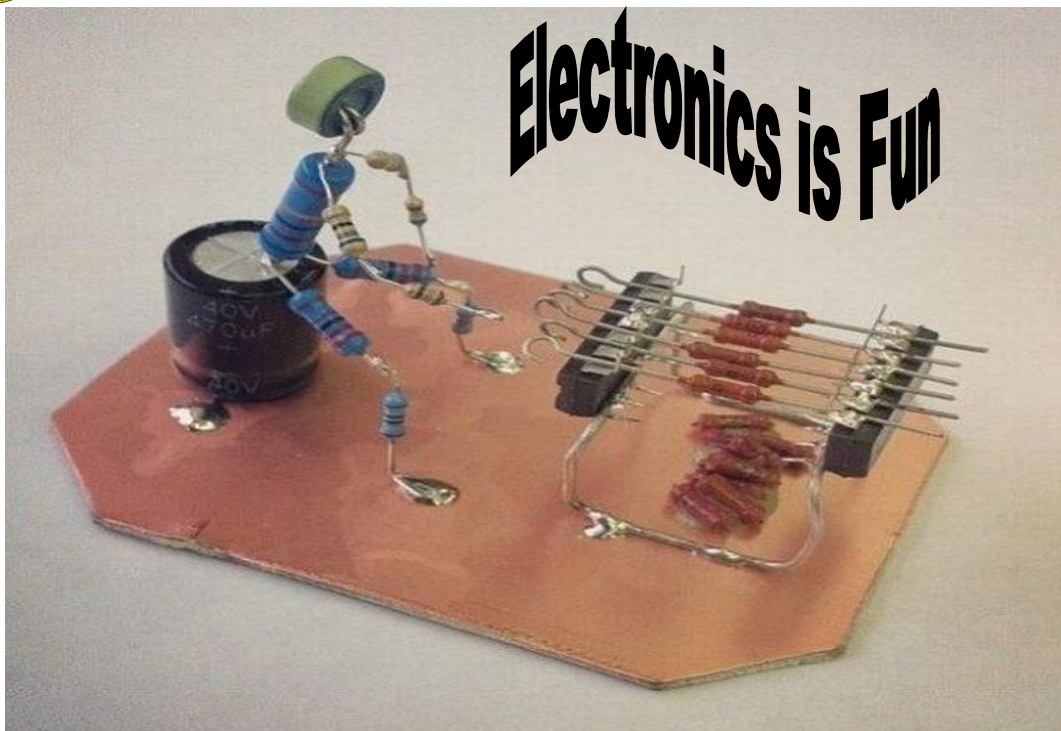
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Generalized Diode Operation



Open Circuit, $I_D = I_S$
Reverse Biased, $I_D < I_S$
Forward Biased, $I_D \gg I_S$



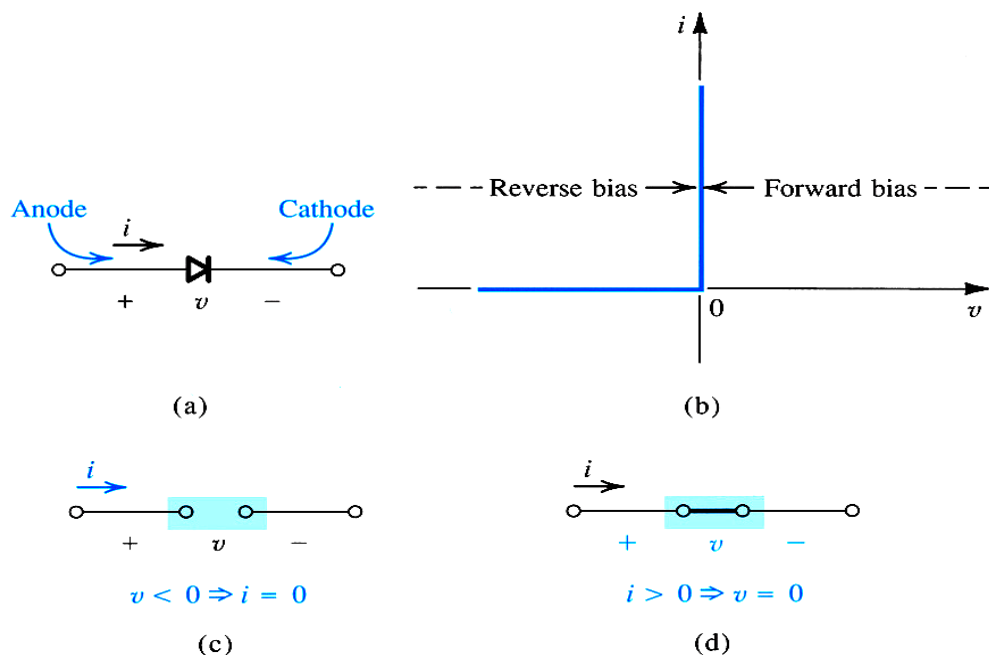


Diode Models

- In the forward bias mode, the diode can be modeled with
 - Ideal Model
 - The diode is modeled as a switch with no resistance
 - Constant Voltage Drop Model
 - The diode is modeled as having a constant voltage drop after which it behaves as a switch
 - Exponential I - V Model
 - The diode equation defines the operation of the diode

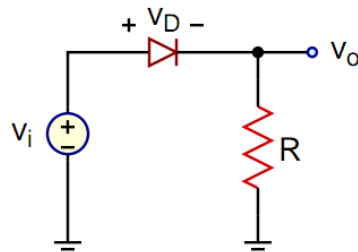


Ideal Diode Model

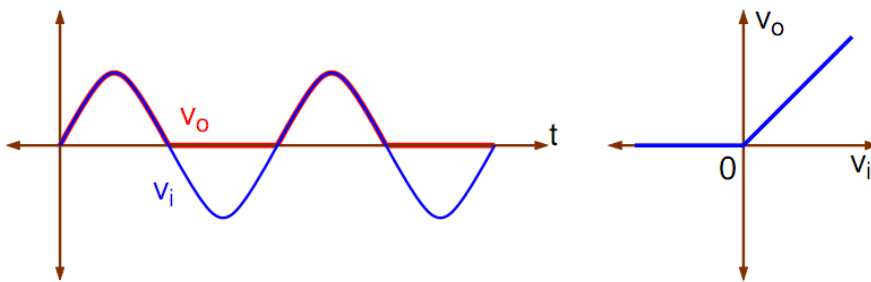




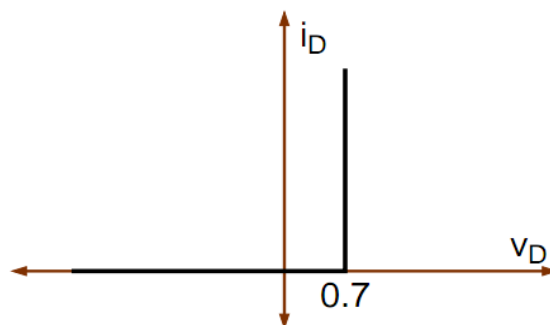
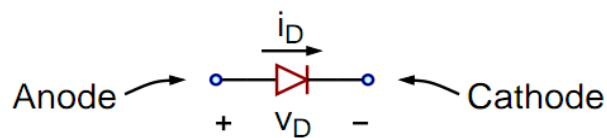
Ideal Diode Model



Diode does not drop any voltage across the terminal



Constant Voltage Drop Model

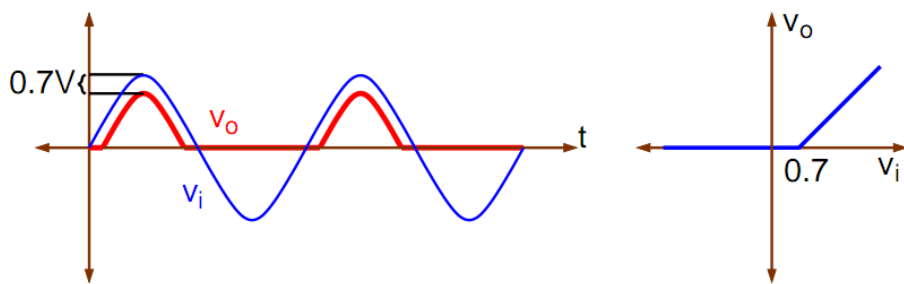
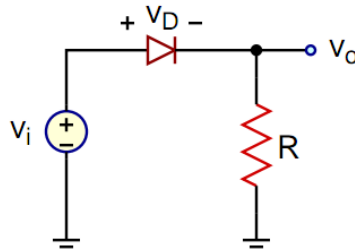


$$v_D < 0.7 \Rightarrow i_D = 0$$

$$i_D > 0 \Rightarrow v_D = 0.7$$



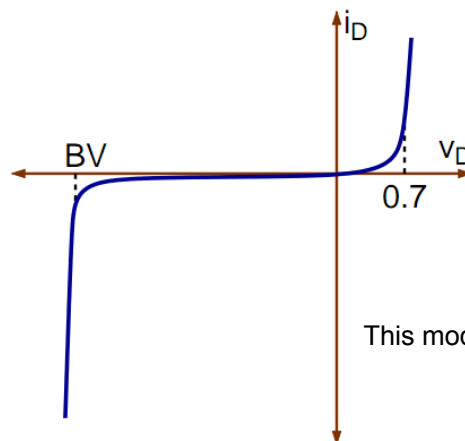
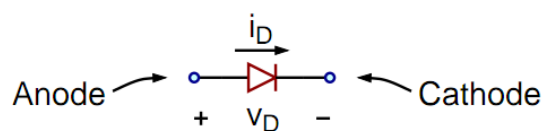
Constant Voltage Drop Model



Diode drop constant voltage across it's terminal
(typically 0.7V for silicon)



Exponential I-V Model



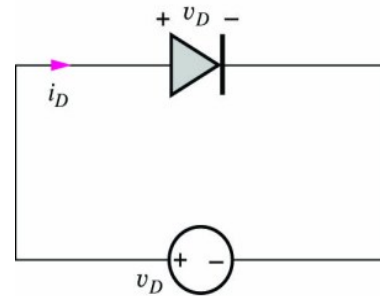
This model is defined by the diode equation



Diode Equation

$$i_D = I_S \left[\exp\left(\frac{qv_D}{nkT}\right) - 1 \right] = I_S \left[\exp\left(\frac{v_D}{nV_T}\right) - 1 \right]$$

where I_S = reverse saturation current (A)
 v_D = voltage applied to diode (V)
 q = electronic charge (1.60×10^{-19} C)
 k = Boltzmann's constant (1.38×10^{-23} J/K)
 T = absolute temperature
 n = nonideality factor (dimensionless)
 $V_T = \frac{kT}{q}$ = thermal voltage (V) (25 mV at room temp.)



I_S is typically between 10^{-18} and 10^{-9} A, and is strongly temperature dependent due to its dependence on n_i^2 . The nonideality factor is typically close to 1, but approaches 2 for devices with high current densities. It is assumed to be 1 in this text.



Diode Equation

I_S , the reverse bias saturation current for an ideal p-n diode is

$$I_S = eA \left(\sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}} \frac{n_i^2}{N_A} \right), \quad (\text{Schubert 2006, 61})$$

where

I_S is the reverse bias saturation current,

e is elementary charge

A is the cross-sectional area

$D_{p,n}$ are the diffusion coefficients of holes and electrons, respectively,

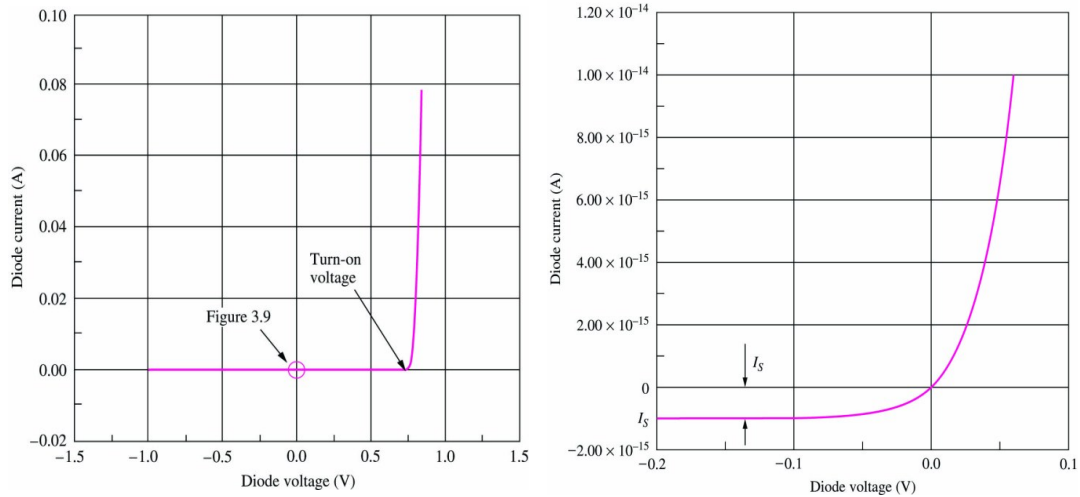
$N_{D,A}$ are the donor and acceptor concentrations at the n side and p side, respectively,

n_i is the intrinsic carrier concentration in the semiconductor material,

$\tau_{p,n}$ are the carrier lifetimes of holes and electrons, respectively.



Diode Equation



Diode I - V characteristics curve showing I_s



Diode Models

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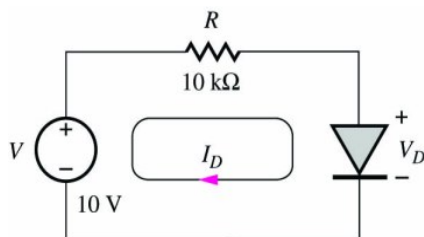


Diode Equations

- Reverse Bias:
$$i_D = I_S \left[\exp\left(\frac{v_D}{nV_T}\right) - 1 \right] \cong I_S [0 - 1] \cong -I_S$$
- No Bias:
$$i_D = I_S \left[\exp\left(\frac{v_D}{nV_T}\right) - 1 \right] \cong I_S [1 - 1] \cong 0$$
- Forward Bias:
$$i_D = I_S \left[\exp\left(\frac{v_D}{nV_T}\right) - 1 \right] \cong I_S \exp\left(\frac{v_D}{nV_T}\right)$$



Diode Circuit Analysis



V and R may represent the Thévenin equivalent of a more complex 2-terminal network. The objective of diode circuit analysis is to find the **quiescent operating point** for the diode.

Q-Point = (I_D , V_D)

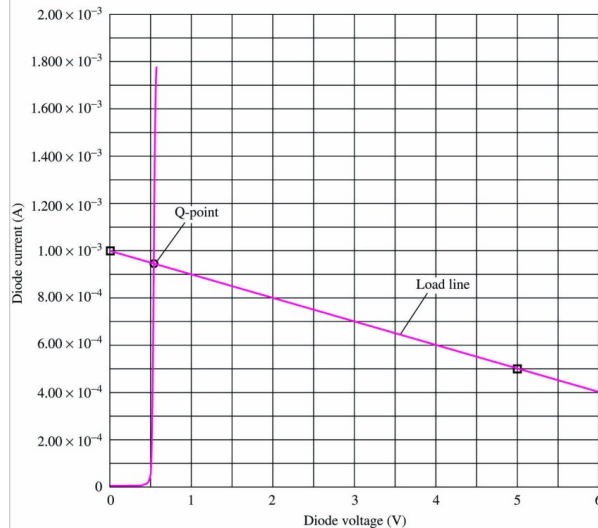
The loop equation for the diode circuit is:

$$V = I_D R + V_D$$

- This is also called the **load line** for the diode. The solution to this equation can be found by:
- Graphical analysis using the load-line method.
- Analysis with the diode's exponential model.
- Simplified analysis with the ideal diode model.
- Simplified analysis using the constant voltage drop (CVD) model.



Graphical Analysis Example



Problem: Find diode Q-point

Given data: $V = 10\text{ V}$, $R = 10\text{ k}\Omega$.

Analysis:

$$10 = I_D 10^4 + V_D$$

To define the load line we use,

$$\text{For } V_D = 0, I_D = (10\text{ V} / 10\text{ k}\Omega) = 1\text{ mA}$$

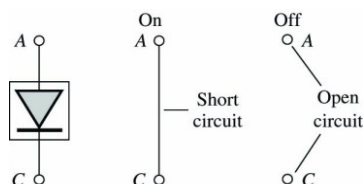
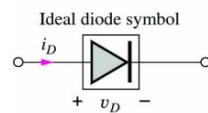
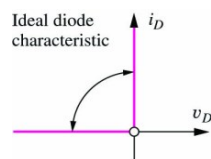
$$\text{For } V_D = 5\text{ V}, I_D = (5\text{ V} / 10\text{ k}\Omega) = 0.5\text{ mA}$$

- These points and the resulting load line are plotted. Q-point is given by intersection of load line and diode characteristic:

Q-point = (0.95 mA, 0.6 V)



Analysis Using Ideal Model



If an ideal diode is forward-biased, the voltage across the diode is zero. If an ideal diode is reverse-biased, the current through the diode is zero.

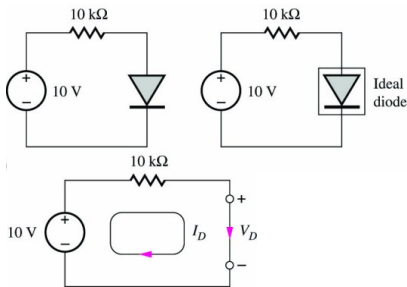
$$v_D = 0 \text{ for } i_D > 0 \text{ and } i_D = 0 \text{ for } v_D < 0$$

Thus, the diode is assumed to be either on or off. Analysis is conducted in following steps:

- Select a diode model.
- Identify anode and cathode of the diode and label v_D and i_D .
- Guess diode's region of operation from circuit.
- Analyze circuit using diode model appropriate for assumed region of operation.
- Check results to check consistency with assumptions.



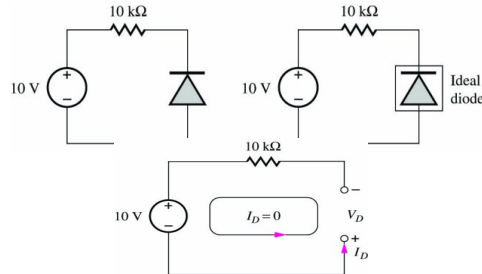
Analysis using Ideal Model



Since source appears to force positive current through diode, assume diode is on.

$$I_D = \frac{(10-0)V}{10k\Omega} = 1 \text{ mA} \quad | \quad I_D \geq 0$$

Our assumption is correct, and the **Q-Point = (1 mA, 0V)**



Since source is forcing current backward through diode assume diode is off. Hence $I_D = 0$. Loop equation is:

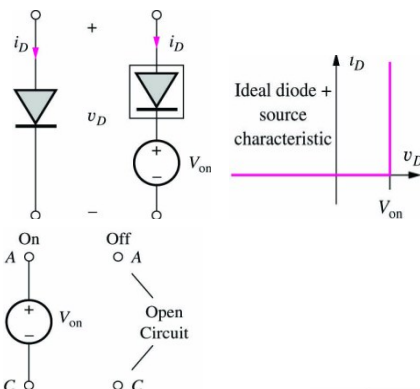
$$10 + V_D + 10^4 I_D = 0$$

$$V_D = -10V \quad | \quad V_D < 0$$

Our assumption is correct and the **Q-Point = (0, -10 V)**

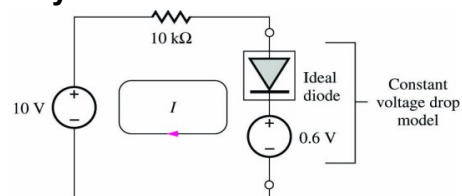


Analysis using Constant Voltage Drop Model

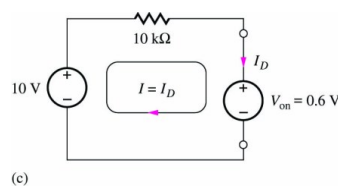


$v_D = V_{on}$ for $i_D > 0$
and $v_D = 0$ for $v_D < V_{on}$.

Analysis:



Since the 10-V source appears to force positive current through the diode, assume diode is on.

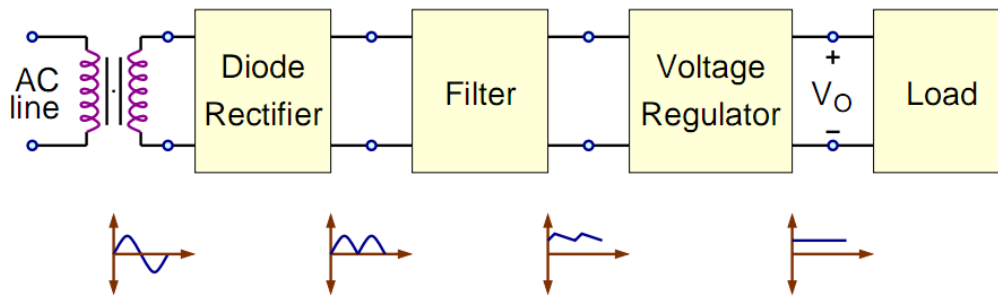


$$I_D = \frac{(10 - V_{on})V}{10k\Omega}$$

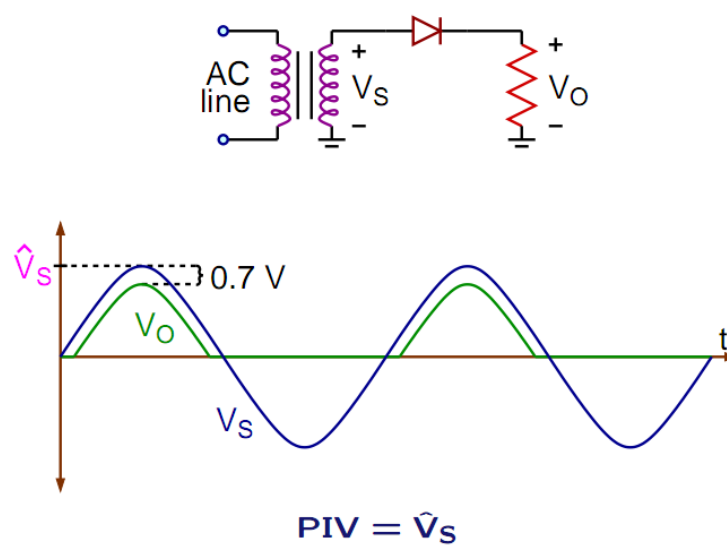
$$= \frac{(10 - 0.6)V}{10k\Omega} = 0.940 \text{ mA}$$



Rectifier Circuits

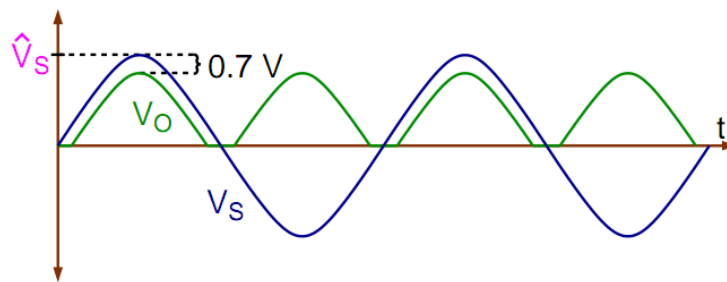
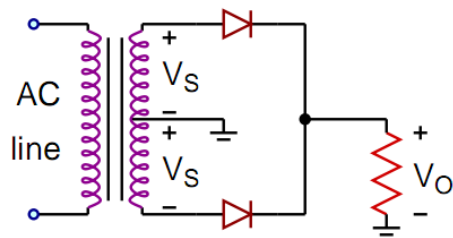


Half-Wave Rectifier





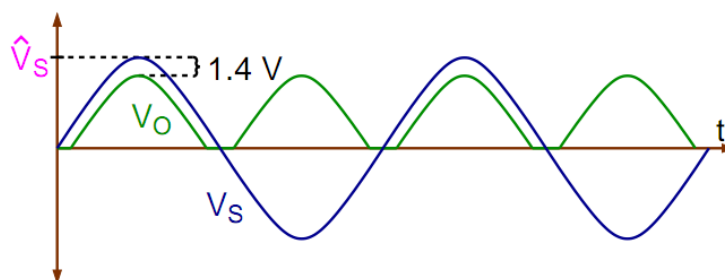
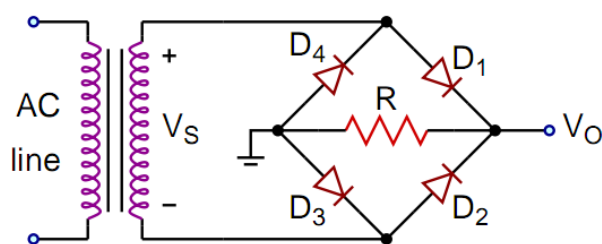
Full-Wave Rectifier



$$PIV = 2\hat{V}_S - 0.7$$



Bridge Rectifier



$$PIV = \hat{V}_S - 0.7$$



Next Lecture

- Diode Rectifier Circuit Analysis
- BJT

