TYPICAL QUESTIONS & ANSWERS

PART - I

OBJECTIVE TYPE QUESTIONS

Each Question carries 2 marks.

Choose correct or the best alternative in the following:

Q.1 The breakdown mechanism in a lightly doped p-n junction under reverse biased condition is called
- **(A)** avalanche breakdown.
- **(B)** zener breakdown.
- **(C)** breakdown by tunnelling.
- **(D)** high voltage breakdown.

Ans: A

Q.2 In a CE – connected transistor amplifier with voltage – gain A_v, the capacitance C_{bc} is amplified by a factor

(A) A_v **(B)** $1 + A_v$

(C) $\sqrt{1 + A_v}$ **(D)** A_v^2

Ans: B

Q.3 For a large values of $|V_{DS}|$, a FET – behaves as
- **(A)** Voltage controlled resistor.
- **(B)** Current controlled current source.
- **(C)** Voltage controlled current source.
- **(D)** Current controlled resistor.

Ans: C

Q.4 Removing bypass capacitor across the emitter-leg resistor in a CE amplifier causes
- **(A)** increase in current gain. **(B)** decrease in current gain.
- **(C)** increase in voltage gain. **(D)**decrease in voltage gain.

Ans: D

Q.5 For an op-amp having differential gain A_v and common-mode gain A_c the CMRR is given by

(A) $A_v + A_c$ **(B)** A_v / A_c

(C) $\frac{A_v}{A_c} + 1$ **(D)** A_c / A_v

Ans: B

Q.6 When a step-input is given to an op-amp integrator, the output will be
- **(A)** a ramp.
- **(B)** a sinusoidal wave.
- **(C)** a rectangular wave.
- **(D)** a triangular wave with dc bias.

Ans: A

Q.7 Hysteresis is desirable in Schmitt-trigger, because
- **(A)** energy is to be stored/discharged in parasitic capacitances.
- **(B)** effects of temperature would be compensated.
- **(C)** devices in the circuit should be allowed time for saturation and desaturation.
- **(D)** it would prevent noise from causing false triggering.

Ans: C

Q.8 In a full-wave rectifier without filter, the ripple factor is
- **(A)** 0.482
- **(B)** 1.21
- **(C)** 1.79
- **(D)** 2.05

Ans: A

Q.9 A minterm of the Boolean-function, f(x, y, x) is
- **(A)** $x' + y + z$
- **(B)** $x\ y\ z'$
- **(C)** $x\ z$
- **(D)** $(y + z)\ x$

Ans: B

Q.10 The minimum number of flip-flops required to construct a mod-75 counter is
- **(A)** 5
- **(B)** 6
- **(C)** 7
- **(D)** 8

Ans: C

Q.11 Space charge region around a p-n junction
- **(A)** does not contain mobile carriers
- **(B)** contains both free electrons and holes
- **(C)** contains one type of mobile carriers depending on the level of doping of the p or n regions
- **(D)** contains electrons only as free carriers

Ans: A

Q.12 The important characteristic of emitter-follower is
- **(A)** high input impedance and high output impedance
- **(B)** high input impedance and low output impedance
- **(C)** low input impedance and low output impedance
- **(D)** low input impedance and high output impedance

Ans: B

Q.13 In a JFET, at pinch-off voltage applied on the gate
- **(A)** the drain current becomes almost zero
- **(B)** the drain current begins to decrease
- **(C)** the drain current is almost at saturation value.
- **(D)** the drain-to-source voltage is close to zero volts.

Ans: C

Q.14 When an amplifier is provided with current series feedback, its
- **(A)** input impedance increases and output impedance decreases
- **(B)** input and output impedances both decrease
- **(C)** input impedance decreases and output impedance increases
- **(D)** input and output impedances both increase

Ans: D

Q.15 The frequency of oscillation of a tunnel-collector oscillator having L= 30μH and C = 300pf is nearby
- **(A)** 267 kHz
- **(B)** 1677 kHz
- **(C)** 1.68 kHz
- **(D)** 2.67 MHz

Ans: B $$fo = \frac{1}{2\pi\sqrt{Lc}} = \frac{1}{2\pi\sqrt{30\mu \times 300 \times 10^{-12}}} = 1677.42\,KHz$$

Q.16 The open-loop gain of an op-amp available in the market may be around.
- **(A)** 10^{-1}
- **(B)** 10
- **(C)** 10^{5}
- **(D)** 10^{2}

Ans: C

Q.17 The control terminal (pin5) of 555 timer IC is normally connected to ground through a capacitor (~ 0.01μF). This is to
- **(A)** protect the IC from inadvertent application of high voltage
- **(B)** prevent false triggering by noise coupled onto the pin
- **(C)** convert the trigger input to sharp pulse by differentiation
- **(D)** suppress any negative triggering pulse

Ans: B

Q.18 The value of ripple factor of a half-wave rectifier without filter is approximately
- **(A)** 1.2
- **(B)** 0.2
- **(C)** 2.2
- **(D)** 2.0

Ans: A

Q.19 The three variable Boolean expression xy + xyz + $\bar{x}$ y + x $\bar{y}$ z

(A) $\bar{y} + x\bar{z}$ **(B)** $\bar{x} + \bar{y}z$

(C) $y + xz$ **(D)** $y + \bar{x}z$

Ans: C

$$y(x + \bar{x}) + xz(y + \bar{y}) = y + xz$$

Q.20 The fan-out of a MOS-logic gate is higher than that of TTL gates because of its

(A) low input impedance **(B)** high output impedance

(C) low output impedance **(D)** high input impedance

Ans: D

Q.21 In an intrinsic semiconductor, the Fermi-level is

(A) closer to the valence band

(B) midway between conduction and valence band

(C) closer to the conduction band

(D) within the valence band

Ans: C

Q.22 The reverse – saturation current of a silicon diode

(A) doubles for every 10°C increase in temperature

(B) does not change with temperature

(C) halves for every 1°C decrease in temperature

(D) increases by 1.5 times for every 2°C increment in temperature

Ans: A

Q.23 The common collector amplifier is also known as

(A) collector follower **(B)** Base follower

(C) Emitter follower **(D)** Source follower

Ans: C

Q.24 In class–A amplifier, the output current flows for

(A) a part of the cycle or the input signal.

(B) the full cycle of the input signal.

(C) half the cycle of the input signal.

(D) $3/4^{th}$ of the cycle of the input signal.

Ans: B

Q.25 In an amplifier with negative feedback

(A) only the gain of the amplifier is affected

(B) only the gain and bandwidth of the amplifier are affected

(C) only the input and output impedances are affected

(D) All of the four parameters mentioned above would be affected

Ans: D

Q.26 Wien bridge oscillator can typically generate frequencies in the range of
- **(A)** 1KHz – 1MHz
- **(B)** 1 MHz – 10MHz
- **(C)** 10MHz – 100MHz
- **(D)** 100MHz – 150MHz

Ans: A

Q.27 A differential amplifier, amplifies
- **(A)** and mathematically differentiates the average of the voltages on the two input lines
- **(B)** and differentiates the input waveform on one line when the other line is grounded
- **(C)** the difference of voltages between the two input lines
- **(D)** and differentiates the sum of the two input waveforms

Ans: C

Q.28 The transformer utilization factor of a half-wave rectifier is approximately
- **(A)** 0.6
- **(B)** 0.3
- **(C)** 0.9
- **(D)** 1.1

Ans: B

$0.286 \approx 0.3$

Q.29 The dual of the Boolean expression: x + y + z is
- **(A)** x .y + z
- **(B)** x + yz
- **(C)** $\bar{x} . \bar{y} . \bar{z}$
- **(D)** x.y.z

Ans: C

$\overline{x + y + z} = \bar{x}.\bar{y}.\bar{z}$

Q.30 It is required to construct a counter to count upto 100(decimal). The minimum number of flip-flops required to construct the counter is

- **(A)** 8
- **(B)** 7
- **(C)** 6
- **(D)** 5

Ans: A

Q.31 The power conversion efficiency of an output stage is defined as_____.
- **(A)** (Load power + supply power) / supply power
- **(B)** (Load power + supply power) / (load power-supply power)
- **(C)** Load power / supply power
- **(D)** Supply power / load power

Ans. (C)
Power gain is defined as the ratio of output signal power to that of input signal power.

Q.32 A highly stable resonance characteristic is the property of a ____ oscillator.
(A) Hartley **(B)** Colpitts
(C) Crystal **(D)** Weinbridge

Ans. (C)

Q.33 The gate that assumes the 1 state, if and only if the input does not take a 1 state is called_____.
(A) AND gate **(B)** NOT gate
(C) NOR gate **(D)** Both **(B)** & **(C)**

Ans. (D)
Y= $\overline{A+B}$ therefore output is high only when the values of both A and B are 0.

Q.34 The width of depleted region of a PN junction is of the order of a few tenths of a _____.
(A) millimeter **(B)** micrometer
(C) meter **(D)** nanometer

Ans. (B)

Q.35 For NOR circuit SR flip flop the not allowed condition is _____.
(A) S=0, R=0. **(B)** S=0, R=1.
(C) S=1, R=1. **(D)** S=1, R=0.

Ans. (C)
When S=R=1 the output is subject to unpredictable behaviour when S and R return to 0 simultaneously.

Q.36 In negative feedback the return ratio is _____.
(A) 0 **(B)** 1
(C) greater than 0 **(D)** greater than 1

Ans. (C)
In a negative feed back circuit, always the return ratio will be in the range of 0 to 1.

Q.37 A phase shift oscillator uses _____.
(A) LC tuning **(B)** Piezoelectric crystal
(C) Balanced bridge **(D)** Variable frequency operation

Ans. (C)

Q.38 The voltage gain of basic CMOS is approximately _____.
(A) $(g_m r_o)/2$ **(B)** $2g_m r_o$

(C) $1 / (2g_m r_o)$ **(D)** $2r_o / g_m$

Ans. (A)

Q.39 Transistor is a

(A) Current controlled current device.
(B) Current controlled voltage device.
(C) Voltage controlled current device.
(D) Voltage controlled voltage device.

Ans. (A)
The output current depends on the input current.

Q.40 A bistable multivibrator is a

(A) Free running oscillator. **(B)** Triggered oscillator.
(C) Saw tooth wave generator. **(D)** Crystal oscillator.

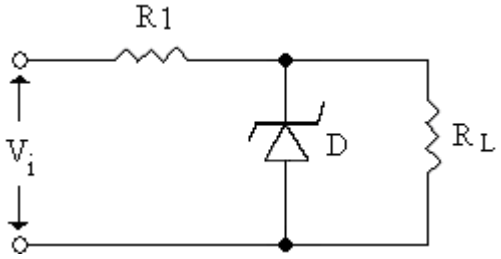
Ans. (B)
The transistors would change their state of operation from ON to OFF and vice versa depending on the external trigger provided.

Q.41 If the output voltage of a bridge rectifier is 100V, the PIV of diode will be

(A) $100\sqrt{2}$V **(B)** $200/\pi$ V
(C) 100πV **(D)** $100\pi/2$ V

Ans. (D)
Peak inverse voltage = max secondary voltage
$V_{dc}=2V_m/\pi=100$
$V_m=100\pi/2$

Q.42 In the voltage regulator shown below, if the current through the load decreases,



(A) The current through R1 will increase.
(B) The current through R1 will decrease.
(C) zener diode current will increase.
(D) zener diode current will decrease.

Ans. (C)

Q.43 In Boolean algebra A + AB

(A) A + B

(B) A + B
(C) A + B
(D) A +B

Ans. (A)
A.1+A B= A (1+B) +A B = A + AB +A B = A+B (A +A) = A+B

Q.44 For a JFET, when V_{DS} is increased beyond the pinch off voltage, the drain current
(A) Increases
(B) decreases
(C) remains constant.
(D) First decreases and then increases.

Ans. (C)
At pinch off voltage drain current reaches its maximum off. Now if we further increase V_{DS} above Vp the depletion layer expands at the top of the channel. The channel acts as a current limiter & holds drain current constant

Q.45 The type of power amplifier which exhibits crossover distortion in its output is
(A) Class A **(B)** Class B
(C) Class AB **(D)** Class C

Ans. (B)
The transistors do not conduct until the input signal is more than cut-in voltage of the B-A junction. In class B, the devices being biased at cut-off, one device stops conducting before the other device starts conducting leaving to Cross-over distortion.

Q.46 The main advantage of a crystal oscillator is that its output is
(A) 50Hz to 60Hz **(B)** variable frequency
(C) a constant frequency. **(D)** d.c

Ans. (C)
The quality factor (Q) of a crystal as a resonating element is very high, of the order of thousands. Hence frequency of a crystal oscillator is highly stable.

Q.47 The lowest output impedance is obtained in case of BJT amplifiers for
(A) CB configuration.
(B) CE configuration.
(C) CC configuration.
(D) CE with R_E configuration.

Ans. (C)
The output impedance in case of CC configuration is on the order of a few ohms. (In case of CB $\approx$ 450kΩ and in case of CE $\approx$ 45kΩ)

Q.48 N-channel FETs are superior to P-channel FETs, because
(A) They have higher input impedance

(B) They have high switching time
(C) They consume less power
(D) Mobility of electrons is greater than that of holes

Ans. (D)

Q.49 The upper cutoff frequency of an RC coupled amplifier mainly depends upon
(A) Coupling capacitor
(B) Emitter bypass capacitor
(C) Output capacitance of signal source
(D) Inter-electrode capacitance and stray shunt capacitance

Ans. (D)

Q.50 Just as a voltage amplifier amplifies signal-voltage, a power amplifier
(A) Amplifies power
(B) Amplifies signal current
(C) Merely converts the signal ac power into the dc power
(D) Merely converts the dc power into useful ac power

Ans. (D)

Q.51 A radio frequency signal contains three frequency components, 870 KHz, 875 KHz and 880 KHz. The signal needs to be amplified. The amplifier used should be
(A) audio frequency amplifier **(B)** wide band amplifier
(C) tuned voltage amplifier **(D)** push-pull amplifier

Ans. (C)
We need to amplify 3 signal frequencies i.e., 870 kHz, 875 kHz and 880 kHz. These frequencies lie in a bandwidth of 10 kHz and we should use only tuned voltage amplifiers to amplify them.

Q.52 An oscillator of the LC type that has a split capacitor in the circuit is
(A) Hartley oscillator
(B) Colpitts oscillator
(C) Weinbridge oscillator
(D) R-C phase shift oscillator

Ans. (B)
We have two capacitors in the tank circuit, which serve as a simple ac voltage divider.

Q.53 The function of a bleeder resistor in a power supply is
(A) the same as that of load resistor
(B) to ensure a minimum current drain in the circuit
(C) to increase the output dc voltage
(D) to increase the output current

Ans. (B)

Q.54 In a bistable multivibrator circuit, commutating capacitor is used

(A) to increase the base storage charge
(B) to provide ac coupling
(C) to increase the speed of response
(D) to provide the speed of oscillations

Ans. (C)

The commutating capacitor is used for the speedy transition of the state of the bistable.

Q.55 n-type silicon is obtained by

(A) Doping with tetravalent element
(B) Doping with pentavalent element
(C) Doping with trivalent element
(D) Doping with a mixture of trivalent and tetravalent element

Ans: (B)

The pentavalent atom provides an excess electron while the other four form the covalent bond with the neighbouring atoms. This excess free electron provides the n type conductivity.

Q.56 The forward characteristic of a diode has a slope of approximately 50mA/V at a desired point. The approximate incremental resistance of the diode is

(A) 50Ω **(B)** 35Ω
(C) 20Ω **(D)** 10Ω

Ans: (C)

Resistance at any point in the forward characteristics is given by $R = \Delta V / \Delta I = 1/50mA = 20\Omega$

Q.57 Two stages of BJT amplifiers are cascaded by RC coupling. The voltage gain of the first stage is 10 and that of the second stage is 20. The overall gain of the coupled amplifier is

(A) 10x20
(B) 10+20
(C) $(10+20)^2$
(D) (10x20)/2

Ans: (A)

The voltage gain of a multistage amplifier is equal to the product of the gains of the individual stages.

Q.58 In the voltage range, $Vp < V_{DS} < BV_{DSS}$ of an ideal JFET or MOSFET

(A) The drain current varies linearly with V_{DS}.
(B) The drain current is constant.
(C) The drain current varies nonlinearly with V_{DS}.
(D) The drain current is cut off.

Ans: (B)

It is the saturation region or pinch off region, and drain current remains almost constant at its maximum value, provided V_{GS} is kept constant.

Q.59 In a voltage shunt negative feedback amplifier system, the input resistance Ri and the output resistance Ro of the basic amplifier are modified as follows:

(A) Ri is decreased and Ro increased.
(B) Both Ri and Ro are decreased.
(C) Both Ri and Ro are increased
(D) Ri is increased and Ro is decreased.

Ans: (B)

Here, a fraction of output voltage obtained by parallel sampling is applied in parallel with the input voltage through feedback and both input and output resistance decrease by a factor equal to $(1+ \beta Av)$.

Q.60 The use of crystal in a tunable oscillator

(A) Improves frequency stability.
(B) Increases the gain of the oscillator.
(C) Helps to obtain optimum output impedance.
(D) Facilitates generation of wide range of frequencies.

Ans: (A)

Piezoelectric crystal is used as a resonant tank circuit. The crystal is made of quartz material and provides a high degree of frequency stability.

Q.61 The large signal bandwidth of an opamp is limited by its

(A) Loop gain **(B)** slew rate
(C) output impedance **(D)** input frequency

Ans: (B)

Q.62 Rectification efficiency of a full wave rectifier without filter is nearly equal to

(A) 51% **(B)** 61%
(C) 71% **(D)** 81%

Ans: (D)

Efficiency of a full wave rectifier is given by
$[(2I_m / \pi)\ 2 \times R_L] / [(I_m / \sqrt{2})\ 2 \times (R_f + R_L)] = 81\%$, when Rg is zero.

Q.63 When the temperature of a doped semiconductor is increased, its conductivity

(A) decreases.
(B) increases.
(C) does not change.
(D) increases or decreases depending on whether it is p- or n-type.

Ans: B

Q.64 The main characteristics of a Darlington Amplifier are

(A) High input impedance, high output impedance and high current gain.
(B) Low input impedance, low output impedance and low voltage gain.
(C) High input impedance, low output impedance and high current gain.
(D) Low input impedance, low output impedance and high current gain.

Ans: C

Q.65 The transconductance, g_m, of a JFET is computed at constant V_{DS}, by the following:

(A) $\frac{\Delta I_D}{\Delta V_{GS}}$ **(B)** $\frac{\Delta V_{GS}}{\Delta I_D}$

(C) $\Delta V_{GS} \times \Delta I_D$ **(D)** $\frac{\Delta I_D}{\Delta V_{GS} + \Delta I_{DS}}$

Ans: A

Q.66 The feedback factor β at the frequency of oscillation of a Wien bridge oscillator is

(A) 3 **(B)** $\frac{1}{3}$

(C) $\frac{1}{29}$ **(D)** $-\frac{3}{29}$

Ans: B

Q.67 In an amplifier with negative feedback, the bandwidth is

(A) increased by a factor of β
(B) decreased by a factor of β
(C) increased by a factor of (1+Aβ)
(D) not affected at all by the feedback

where A = gain of the basic amplifier and β = feedback factor

Ans: C

Q.68 The 'slew rate' of an operational amplifier indicates

(A) how fast its output current can change
(B) how fast its output impedance can change
(C) how fast its output power can change
(D) how fast its output voltage can change

when a step input signal is given.

Ans: D

Q.69 In a clamping circuit, the peak-to peak voltage of the waveform being clamped is

(A) affected by the clamping
(B) not affected by the clamping
(C) determined by the clamping voltage value
(D) determined by the ratio of rms voltage of the waveform and the clamping voltage

Ans: B

Q.70 Regulation of a.d.c. power supply is given by
- **(A)** product of no-load output voltage and full-load current
- **(B)** ratio of full-load output voltage and full-load current
- **(C)** change in output voltage from no-load to full-load
- **(D)** change in output impedance from no-load to full-load

Ans: D

Q.71 A 'literal' in Boolean Algebra means
- **(A)** a variable inn its uncomplemented form only
- **(B)** a variable ORed with its complement
- **(C)** a variable in its complemented form only
- **(D)** a variable in its complemented or uncomplemented form

Ans: D

Q.72 In an unclocked R-S flip-flop made of NOR gates, the forbidden input condition is
- **(A)** R = 0, S = 0
- **(B)** R = 1, S = 0
- **(C)** R = 0, S = 1
- **(D)** R = 1, S = 1

Ans: D

Q.73 The current amplification factor in CE configuration is
- **(A)** α
- **(B)** $\beta + 1$
- **(C)** $1/\beta$
- **(D)** β

Ans: D

Q.74 A zener diode
- **(A)** Has a high forward voltage rating.
- **(B)** Has a sharp breakdown at low reverse voltage.
- **(C)** Is useful as an amplifier.
- **(D)** Has a negative resistance.

Ans: B

Q.75 N-channel FETs are superior to P-channel FETs, because
- **(A)** They have a higher input impedance.
- **(B)** They have high switching time.
- **(C)** They consume less power.
- **(D)** Mobility of electrons is greater than that of holes.

Ans:

Q.76 The maximum possible collector circuit efficiency of an ideal class A power amplifier is
- **(A)** 15%
- **(B)** 25%
- **(C)** 50%
- **(D)** 75%

Ans: C

Q.77 Negative feedback in an amplifier
(A) Reduces the voltage gain.
(B) Increases the voltage gain.
(C) Does not affect the voltage gain.
(D) Converts the amplifier into an oscillator.

Ans: A

Q.78 For generating 1 kHz signal, the most suitable circuit is
(A) Colpitts oscillator. **(B)** Hartley oscillator.
(C) Tuned collector oscillator. **(D)** Wien bridge oscillator.

Ans: D

Q.79 Phe output stage of an op-amp is usually a
(A) Complementary emitter follower**.**
(B) Transformer coupled class B amplifier**.**
(C) Class A power amplifier.
(D) Class B amplifier.

Ans: A

Q.80 When a sinusoidal voltage wave is fed to a Schmitt trigger, the output will be
(A) triangular wave. **(B)** asymmetric square wave.
(C) rectangular wave. **(D)** trapezoidal wave.

Ans: B

Q.81 If the peak value of the input voltage to a half wave rectifier is 28.28 volts and no filter is use, the maximum dc voltage across the load will be
(A) $20\sqrt{2}$V . **(B)** 15 V.
(C) 9 V. **(D)** 14.14 V.

Ans: C

Q.82 The logic gate which detects equality of two bits is
(A) EX-OR **(B)** EX-NOR
(C) NOR **(D)** NAND

Ans: B

Q.83 The electron relaxation time of metal A is 2.7×10^{-4} s, that of B is 1.35×10^{-4} s. The ratio of resistivity of B to resistivity of A will be
(A) 4. **(B)** 2.0.

(C) 0.5. **(D)** 0.25.

Ans: B

Q.84 The overall bandwidth of two identical voltage amplifiers connected in cascade will
(A) Remain the same as that of a single stage.
(B) Be worse than that of a single stage.
(C) Be better than that of a single stage.
(D) Be better if stage gain is low and worse if stage gain is high.

Ans: B

Q.85 Field effect transistor has
(A) large input impedance. **(B)** large output impedance.
(C) large power gain. **(D)** large votage gain.

Ans: A

Q.86 Which of the following parameters is used for distinguishing between a small signal and a large-signal amplifier?
(A) Voltage gain **(B)** Frequency response
(C) Harmonic Distortion **(D)** Input/output impedances

Ans: D

Q.87 Which of the following parameters is used for distinguishing between a small signal and a large-signal amplifier?
(A) Instability **(B)** Bandwidth
(C) Overall gain **(D)** Distortion

Ans: B

Q.88 If the feedback signal is returned to the input in series with the applied voltage, the input impedance _____.
(A) decreases **(B)** increases
(C) does not change **(D)** becomes infinity

Ans: B

Q.89 Most of linear ICs are based on the two transistor differential amplifier because of its
(A) input voltage dependent linear transfer characteristic.
(B) High voltage gain.
(C) High input resistance.
(D) High CMRR

Ans: D

Q.90 The waveform of the output voltage for the circuit shown in Fig.1 (RC >> 1) is a

(A) sinusoidal wave **(B)** square wave
(C) series of spikes **(D)** triangular wave.

Ans: D

Q.91 A single phase diode bridge rectifier supplies a highly inductive load. The load current can be assumed to be ripple free. The ac supply side current waveform will be

(A) sinusoidal **(B)** constant dc.
(C) square **(D)** triangular

Ans: C

Q.92 Which of the following Boolean rules is correct?

(A) $A + 0 = 0$ **(B)** $A + 1 = 1$
(C) $A + \overline{A} = A.A$ **(D)** $A + AB = \overline{A} + B$

Ans: B

Q.93 A single phase diode bridge rectifier supplies a highly inductive load. The load current can be assumed to be ripple free. The ac supply side current waveform will be

(A) sinusoidal **(B)** constant dc.
(C) square **(D)** triangular

Ans: C

Q.94 Which of the following Boolean rules is correct?

(A) $A + 0 = 0$ **(B)** $A + 1 = 1$
(C) $A + \overline{A} = A.A$ **(D)** $A + AB = \overline{A} + B$

Ans: B

PART – II

NUMERICALS

Q.1 In a transformer, give the relationship between
(i) turns ratio and its primary and secondary impedances
(ii) turns ratio and primary/secondary voltage.
In a transformer-coupled amplifier, the transformer used has a turns ratio N1:N2 = 10:1. If the source impedance is 8 KΩ what should be the value of load impedance for maximum power transfer to the load? Also find the load voltage if the source voltage is 10 volts. **(6)**

Ans: p. 439 – 40

Given: $N_1 : N_2 - 10:1$; N_2 - load side; N_1 - amplifier side or source side.

$Z_S = 8K\Omega$, $Z_L = ?$ $V_{in} = 10V$; $V_o = ?$

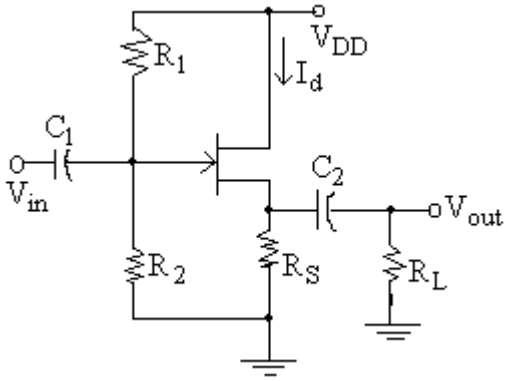
Turns ratio and impedances: $\frac{N_1}{N_2} = \sqrt{\frac{Z_S}{Z_L}}$

Turns ration and voltages: $\frac{N_1}{N_2} = \frac{V_1}{V_2}$

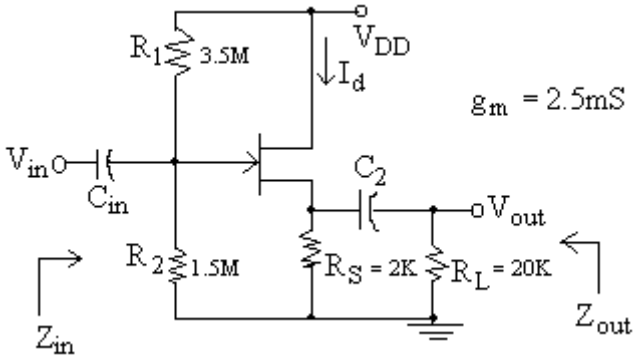
$\frac{Z_S}{Z_l} = \left(\frac{N_1}{N_2}\right)^2$; i.e. $Z_L = Z_S\left(\frac{N_2}{N_1}\right)^2 = 8\times10^3 \times \frac{1}{100} = 80\Omega$

Load voltage = V_2 ; $V_2 = V_1 \frac{N_2}{N_1} = 10\times\frac{1}{10} = 1$ volt .

Q.2 The FET circuit given below in Fig.1, has R_1=3.5MΩ, R_2 = 1.5MΩ, R_S = 2KΩ, R_L = 20KΩ and g_m = 2.5mS. Find its input impedance, output impedance and voltage gain. **(8)**



Ans:



(i) $Z_{in} = R_1 \parallel R_2 = 3.5M\Omega \parallel 1.5M\Omega = 1.05M\Omega$

(ii) $Z_{out} = R_s \parallel \dfrac{1}{g_m} = 2K\Omega \parallel \dfrac{1}{2.5\times10^{-3}} = 333.33\Omega$

(iii) Voltage gain $A_v = \dfrac{g_m(R_S \parallel R_L)}{1+g_m(R_S \parallel R_L)} = \dfrac{2.5\times10^{-3}(2 \parallel 20)\times10^3}{1+2.5\times10^{-3}(2 \parallel 20)\times10^3} = 0.819 \tilde{-} 0.82$

Q.3 In an amplifier with negative feedback, the gain of the basic amplifier is 100 and it employs a feedback factor of 0.02. If the input signal is 40mV, determine

(i) voltage gain with feedback and

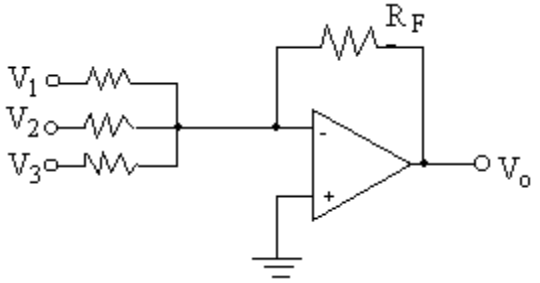
(ii) value of output voltage. **(3)**

Ans:

(i) $A_f = \dfrac{A}{1+AB} = \dfrac{100}{1+100\times0.02} = 33.33$

(ii) $V_o = A_f V_{in} = 33.33\times40\times10^{-3} = 1.33$ volts

Q.4 In the circuit shown below in Fig.2, R_1=12KΩ, R_2 = 5KΩ, R_3 = 8KΩ, R_F = 12KΩ. The inputs are: V_1 = 9V, V_2 = -3V and V_3 = -1V. Compute the output voltage. **(4)**



Ans:

$$V_o = -R_F\left[\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}\right] = -12\left[\frac{9}{12}+\frac{-3}{5}+\frac{-1}{8}\right]$$

$= -12(0.75 - 0.6 - 0.125) = -0.3$ V.

Q.5 A half-wave rectifier has a load resistance of 3.5 KΩ. If the diode and secondary of the transformer have a total resistance of 800KΩ and the ac input voltage has 240 V (peak value), determine:

(i) peak, rms and average values of current through load
(ii) DC power output
(iii) AC power input
(iv) rectification efficiency **(7)**

Ans:

(i) $I_m = \frac{V_m}{R_L + R_f} = \frac{240}{3.5X\ 103 + 800} = 55.8\text{mA} =$ peak current.

$I_{dc} = \frac{I_m}{\pi} = 17.77\text{mA} =$ average current.

$I_{rms} = \frac{I_m}{2} = 27.91\text{mA}$.

(ii) DC power output = $I_{d2}{}^2 R_L = 1.1$ watts.

(iii) AC power input = $I_{rms}{}^2 (R_L + R_f) = 3.35$ watts.

(iv) Rectification Effect $= \eta = \frac{P_{dc(out)}}{P_{ac(in)}} = \frac{1.1\text{W}}{3.35\text{W}} = 32.84\%$.

Q.6 A BJT has a base current of 250 μA and emitter current of 15mA Determine the collector current gain and β. **(2)**

Ans:

The current relationship in a transistor is given by $I_E = I_B + I_C$

$$\text{i.e. } I_C = I_E - I_B$$

$$\text{Given: } I_B = 250\,\mu\text{A} = 0.25\text{ mA}$$

$$I_E = 15\text{ mA}$$

$$\therefore I_C = 15 - 0.25 = 14.75\text{ mA}$$

$$\text{And} \quad \beta = \frac{I_C}{I_B} = \frac{14.75}{0.25} = 59\,.$$

Q.7 In the circuit shown in Fig.1, $[I_{DSS}] = 4\text{mA}$, $V_p = 4\text{V}$. Find the quiescent values of 1_D, V_{GS} and V_{DS} of the FET. **(6)**

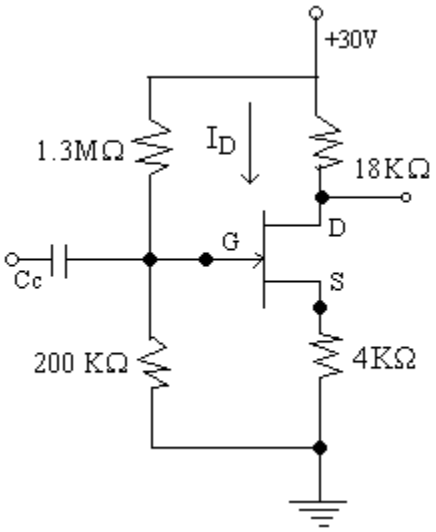
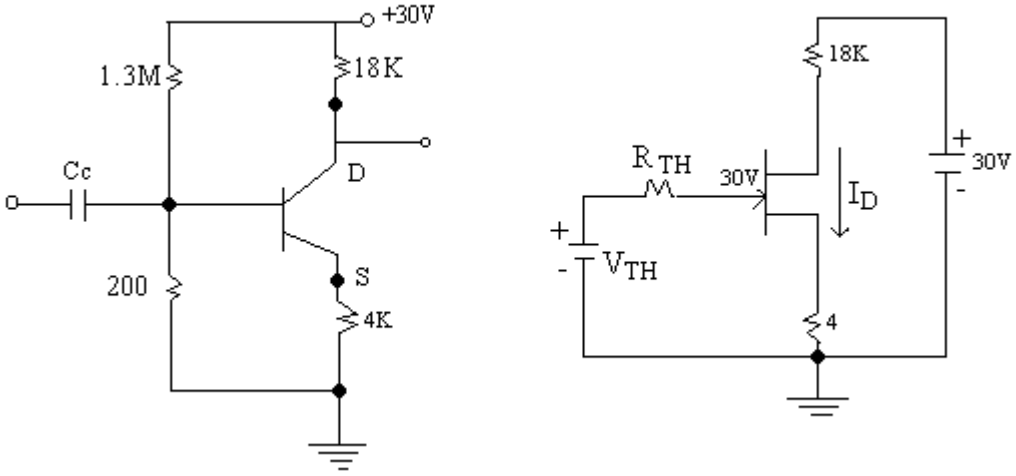


Fig.1

Ans:



The potential divider bias circuit can be replaced by Thevenin equivalent as shown, where

$$R_{TH} = 200K \parallel 1.3M = \frac{200\times1300}{200+1300} = 173.5K$$

$$V_{TH} = \frac{200K}{1500K}(30) = 4V$$

Applying Kirchoff's Voltage law to gate–source circuit gives $V_{GS} = V_{TH} - 4I_D$ as there is no gate current flow.

Hence $I_D = \frac{V_{TH} - V_{GS}}{4} = \frac{4 - V_{GS}}{4} = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2$

Given, I_{DSS} = 4 mA and V_P = 4 V. substituting these values in the equation for I_P

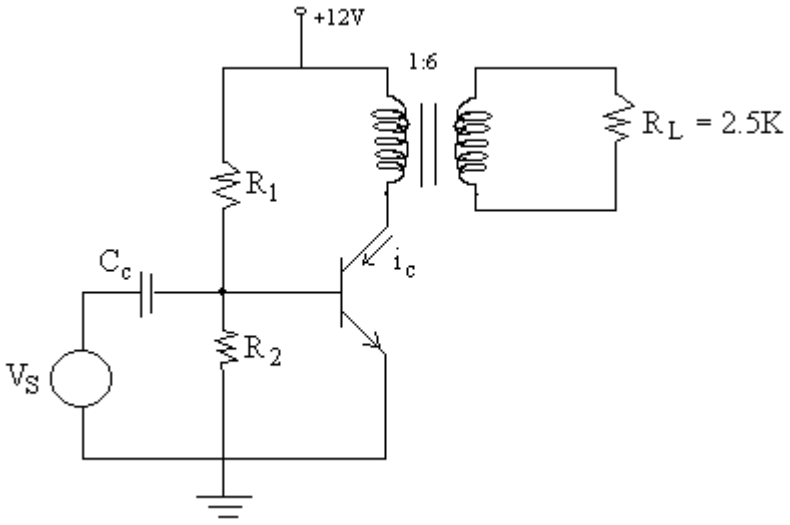
$$I_D = 4\left(\frac{1 - V_{GS}}{4}\right)^2$$

Forming the quadratic equation in V_{GS}.

$$\frac{4-V_{GS}}{4}=4\left(\frac{1-V_{GS}}{4}\right)^2$$

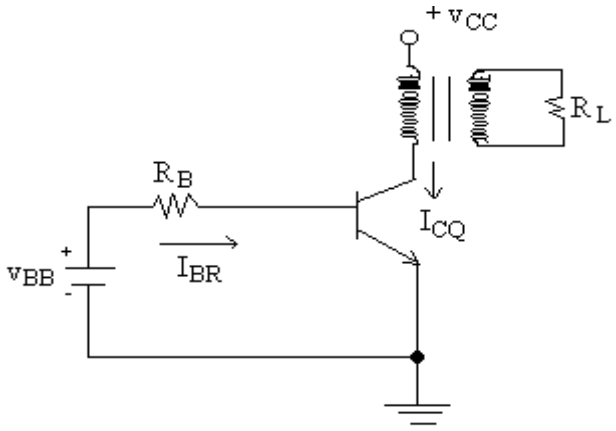
Solving, V_{GS} = 3 V(Solution V_{GS} = 4V is not realistic).
Solving for I_D, I_D = (1 – ¾) = 0.25 mA
Hence, V_{DS} = 30 – 0.25(18 + 4) = 24.5 Volts.

Q.8 In the transformer coupled class A amplifier shown in Fig.2 below, the transistor has $h_{FE} = \beta =$ 40 and h_{ie} = 25Ω. Assume that the transformer is ideal and that $V_{CE(sat)} \simeq 0$ and also $I_{CBO} = 0$. Determine values of R_1 and R_2 to obtain quiescent current I_{CQ} = 100mA. If the collector current swing $\pm 80mA$, find the peak values of load current and load voltage. Transformer turns ratio is primary 1:6 secondary. **(10)**



Ans:

The equivalent circuit replacing R_1, R_2 as part of thevenin source is shown



$$R_B=\frac{R_1R_2}{R_1+R_2} \quad \ldots\ldots(1) \qquad V_{BB}=\frac{R_2}{R_1+R_2}V_{CC} \quad \ldots\ldots\ldots(2)$$

Applying KVL around base-emitter circuit,

$$V_{BB} = V_{BEQ} + I_{BQ}R_B = V_{BEQ} + \frac{I_{CQ}}{\beta}R_B$$

i.e. $V_{BB} = 0.7 + \frac{100\times10^{-3}}{40}R_B = 0.7 + 0.0025(2-2k)$ …….(3)

Any value of R_B by which $V_{BB} \le V_{CC}$ is acceptable. Hence, choosing a reasonable value of 2.2K for R_B, $V_{BB} = 0.7 + 0.0025(2.2\times10^3) = 6.2$ volts.

Use equations (1) and (2) to find R_1 and R_2

From (1) $R_B(R_1 + R_2) = R_1R_2$ or $R_1R_2 - R_BR_1 - R_BR_2 = 0$

i.e. $R_1(R_2 - R_B) - R_BR_2 = 0$, *or* $R_1 = \frac{R_BR_2}{R_2 - R_B}$ ……..(4)

substituting the value of R_1 in equation (2)

$$V_{BB} = \frac{R_2}{\left(\frac{R_BR_2}{R_2 - R_B}\right) + R_2}V_{CC} \text{ i.e. } V_{BB} = \frac{(R_2 - R_B)R_2V_{CC}}{R_BR_2 + (R_2)^2 - R_BR_2} = \frac{(R_2 - R_B)}{R_2}V_{CC} \quad ….(5)$$

simplifying, $R_2 = \frac{R_BV_{CC}}{(V_{CC} - V_{BB})}$ ……(6)

From (4) and (6), we get

$$R_1 = \frac{R_B\frac{R_BV_{CC}}{V_{CC} - V_{BB}}}{\frac{R_BV_{CC}}{(V_{CC} - V_{BB})} - R_B} = \frac{(R_B)^2V_{CC}}{R_BV_{CC}.V_{CC}R_B + R_BV_{BB}} = \frac{V_{CC}R_B}{V_{BB}} \quad ……(7)$$

using equation (6), $R_2 = \frac{2.2\times12}{12-6.2} = 4.55k$

using equation (7), $R_1 = \frac{12\times2.2}{6.2} = 4.23k$

The load R_{ac} at the collector leg of the transistor is reflected load of R_L as per the turns ratio (a) of the transformer.

i.e. $R_{ac} = a^2R_L = \left(\frac{1}{6}\right)^2(2.5k) = 69.4\Omega$

As i_c swings ± 80 mA either side of I_{CQ} = 100 mA on the R_{ac} load line, and V_{CEQ} = 12V (DC load line being almost vertical)

$$V_{CE\,max} = V_{CEQ} + I_{Cm}R_{ac} = 12 + 80\times10^{-3}\times69.4$$

= 12 + 5.55 = 17.55 Volts.

Hence, Maximum Load voltage$_{(secondary)}$:

$$V_{L\,max} = \frac{1}{a}I_{cm}R_{ac} = 6\times(80\times10^{-3})(69.4) = 33.31V$$

Hence, Maximum Load current:

$$I_{L\,max} = aI_{cm} = \frac{1}{6}(80\times10^{-3}) = 13.33mA\,.$$

Q.9 A negative feedback of $\beta = 2.5 \times 10^{-3}$ is applied to an amplifier of open loop gain 1000. Calculate the change in overall gain of the feedback amplifier if the gain of the internal amplifier is reduce by 20%. **(4)**

Ans:

If A is the gain of the basic amplifier, the overall gain A_f of the amplifier with negative f.b. is

$A_f = \frac{A}{1+A\beta}$ given A = 1000 and $\beta = 2.5 \times 10^{-3}$,

$$A_f = \frac{1000}{1+1000+2.5\times10^{-3}} = \frac{1000}{1+2.5} = 285.7$$

When A is reduced by 20%, the new A, say $A_n = 1000 - 0.2 \times 10^3 = 800$

The new voltage gain with f.b. is

$$A_f = \frac{800}{1+800\times2.5\times10^{-2}} = 266.67 .$$

Q.10 A full wave rectifier is fed with a voltage, 50 sin 100 πt. Its load resistance is 400Ω. The diodes used in the rectifier have an average forward resistance of 30Ω. Compute the

(i) average and rms values of load current,
(ii) ripple factor and
(iii) efficiency of rectification. **(6)**

Ans:

The maximum value of load current

$I_{L\,max} = \frac{V_{max}}{R_L + R_F}$; given: V_{max} = 50volts; R_L = 400Ω, R_F = 30 Ω

Thus $I_{L\,max} = \frac{50}{400+30} = 0.1163$ Amp

Average current $I_{avg} = \frac{2\, I_{max}}{\pi}$ for a FWR

i.e. $I_{avg} = \frac{2 \text{ X } 0.1163}{\lambda} = 0.074$A or 74 mA = I_{dc}

The r.m.s value of load current is

$$I_{max} = \frac{I_{max}}{\sqrt{2}} = \frac{0.1163}{\sqrt{2}} = 0.0822\text{A or } 82.2\text{mA}$$

Ripple factor $\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\frac{(0.0822)^2}{(0.074)^2} - 1} = 0.483$

Efficiency of rectification in a FWR is given by

$$\eta = \frac{0.812}{1+\frac{R_F}{R_L}} \quad \text{i.e. } \eta = \frac{0.812}{1+\frac{30}{400}} = 0.755 \text{ or } 75.5\%.$$

Q.11 For the circuit shown in Fig.2, find thee maximum and minimum values of zener diode current. **(8)**

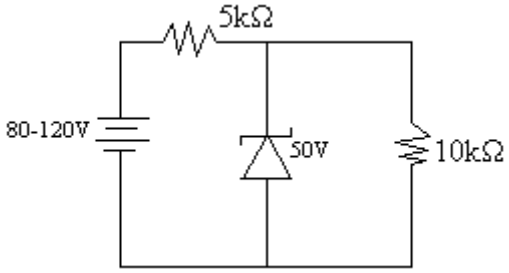


Fig.2

Ans: 9mA, 1.0mA.

Q.12 The parameters of the transistor in the circuit shown in Fig.3 are $h_{fe} = 50, h_{ie} = 1.1k\Omega, h_{re} = h_{oe} = 0$. Find
(i) midband gain
(ii) the value of C_b necessary to give a lower 3 dB frequency of 20Hz
(iii) the value of C_b necessary to ensure less than 10% tilt for a 100 Hz square wave input.
(8)

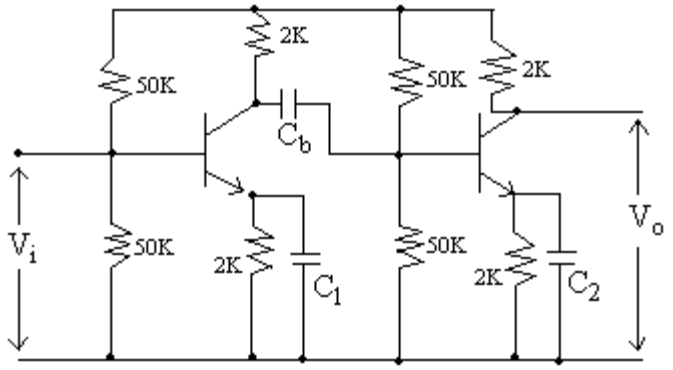


Fig.3

Ans:
(i) 32.26 (ii) 2.567 Mf (iii) 16.13 Mf

Q.13 For the circuit shown in Fig.4, determine voltage gain, input impedance, output impedance, common-mode gain and CMRR if $V_{CC} = 15v$, $V_{EE} = -15v$, $R_C = R_E = 1M\Omega$ and transistors Q_1 and Q_2 are identical with $\beta_{dc} = 100$. Determine output voltage when $V_{in} = 0$ and when $V_{in} = -1mV$. **(8)**

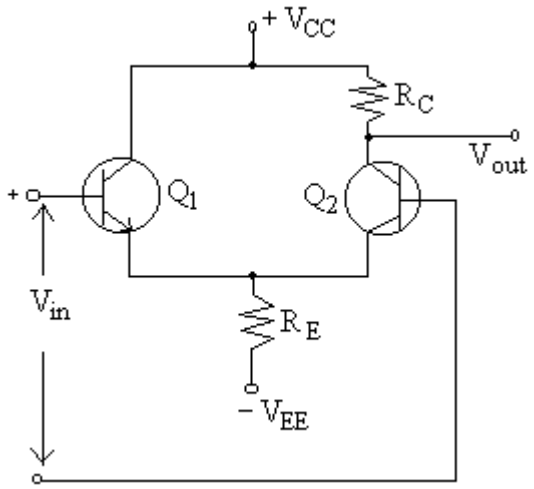


Fig.4

Ans:

A = 150, Z_{in} = 0.66MΩ, Z_{out} = 1MΩ

A_{cm} = 0.5, CMRR = 300

V_{out} = 7.5V and 0.15V

Q.14 A class B push-pull amplifier is supplied with $V_{cc} = 40V$. The minimum voltage reached by the collector due to signal swing is $V_{min} = 8V$. The dissipation in both the transistors totals 30 W. What is the conversion efficiency of the amplifier? **(7)**

Ans:

DC supply voltage, Vcc = 40v

Vmin = 8v, Pd = 30w.

As Pd = Pin(dc) – Pout(ac)

$$30 = \frac{2}{\pi} Vcc\, I_{c\max} - \frac{I_{c\max}}{2}\left(Vcc - V_{c\max}\right)$$

$$30 = I_{c\max}\left[\frac{2Vcc}{\pi} - \frac{Vcc - V_{c\min}}{2}\right]$$

$$= I_{c\max}\left[\frac{2\times 40}{\pi} - \frac{40-8}{2}\right]$$

$$= I_{c\max}\left[25.46 - 16\right] = 9.46 I_{c\max}$$

$$or \quad I_{c\max} = \frac{30}{9.46} = 3.17A$$

$$\therefore P_{in(dc)} = \frac{2}{\pi} Vcc\, I_{c\max} = \frac{2}{\pi}\times 40 \times 3.17$$

$$P_{in(dc)} = 80.712.w$$

$$P_{out(ac)} = \frac{I_{c\max}}{2}\left(Vcc - V_{\min}\right) = \frac{3.17}{2}\left(40-8\right)$$

$$P_{out(ac)} = 50.72w$$

Conversion Efficiency, $\eta = \frac{P_{out(ac)}}{P_{in(dc)}} \times 100 = \frac{50.72}{80.712} \times 100$

$\eta = 62.84\%$

Q.15 The input to an op-amp differentiator circuit is a sinusoidal voltage of peak value 10μV and frequency of 2 kHz. If the values of differentiating components are given as R = 40 kΩ and C = 3μF, determine the output voltage. **(4)**

Ans:

$V_{in} = V_{\max} \sin 2\pi ft = 10 \times 10^{-6} \sin 2\pi .2000.t$

$V_{in} = 10 \sin 4000\pi t \mu v$

Scale factor = CR = $3 \times 10^{-6} \times 40 \times 10^{3} = 0.12$

$\therefore V_{out} = -CR \frac{dV_c}{dt} = -0.12 \frac{d}{dt}(10 \sin 4000\pi t) \mu v$

$V_{out} = -0.12 \times 10 \times \frac{d}{dt}(\sin 4000\pi t) \mu v$

$V_{out} = 1.2(4000\pi .\cos 4000\pi t) \mu v$

$V_{out} = 15.0816(\cos 4000\pi t) \mu v$

Q.16 Draw the circuit of a monostable multivibrator using two transistors. Use the following data in your circuit: $V_{cc} = 10V$, $V_{CE(sat)} = 0.2V$, B $V_{BE(sat)} = 0.8V$, $\beta = 80$ for both the transistors. The resistor and capacitor connected to the base of Q_2 have values $R_B = 20\,k\Omega$ and C = 0.1 μF, respectively. Determine the monostable pulse width. **(8)**

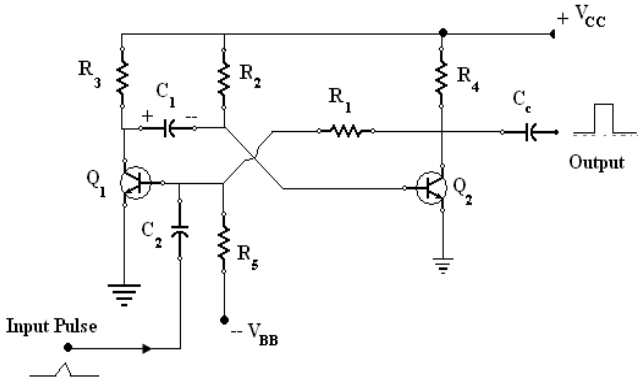
Ans:

$V_{cc} = 10v$, Input pulse width,

$T = R_B G \quad \log e \frac{2V_{cc} - V_B(on)}{V_{cc} - V_B(on)}$

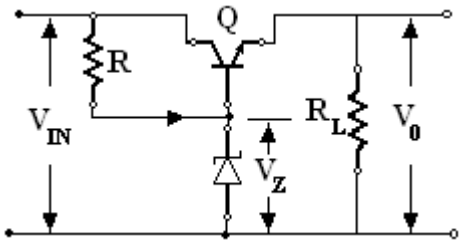
$T = 20 \times 10^{3} \times 0.1 \times 10^{-6} \log e \frac{2 \times 10 - 0.8}{10 - 0.8}$

T = 1.4 714 m sec.

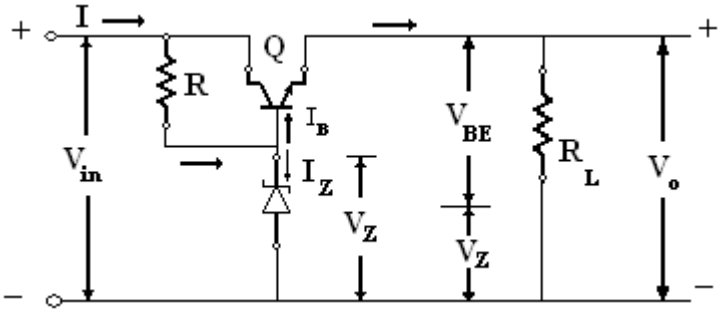


Monostable Multivibrator Circuit

Q.17 For the series regulator given below, $V_{in} = 15V$, $R = 200\Omega$, the transistor $\beta = 50$, $R_L = 1.2\ K\Omega$, $V_z = 10V$ and $V_{BE} = 0.4V$. Calculate (i) output voltage (ii) load current (iii) the base current in the transistor (iv) zener current. **(8)**



Ans:



$V_{BE} = 0.4v, B = 50, R_L = 1.2k, V_Z = 10v\ V_{in} = 15v$

$R = 200\Omega$

$V_{out} = V_Z - V_{BE} = 10 - 0.4 = 9.6v$

$V_R = V_{in} - V_Z = 15 - 10 = 5v$

$\therefore \quad I = \dfrac{V_R}{R} = \dfrac{5}{200} = 0.025A$

Q.18 Find the values of collector and emitter currents in a transistor having I_{CBO}=3μA, and α_{dc}=0.98 when its base current is 60μA. **(6)**

Ans:

$I_B = 60\mu A = 60\times10^{-6}\ A =\ I_{CBO} = 3\mu A = 3\times10^{-6}\ A$

We know that

$I_C = \alpha_{dc} I_E + I_{CBO}$

$I_C = \alpha_{dc}(I_C + I_B) + I_{CBO}$

$I_C(1-\alpha_{dc}) = \alpha_{dc} I_B + I_{CBO}$

$I_C = \dfrac{\alpha_{dc} I_B}{1-\alpha_{dc}} + \dfrac{I_{CBO}}{1-\alpha_{dc}}$

$Ic = \dfrac{60\times10^{-6}\times0.98}{1-0.98} + \dfrac{3\times10^{-6}}{1-0.98}$

$I_C = 2.94\times10^{-3} + 0.15\times10^{-3}$

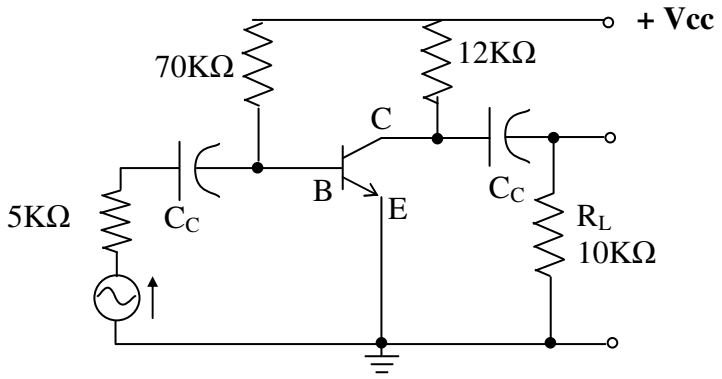
$I_C = 3.09mA$

Emitter current, $I_E = I_C + I_B$

$= 3.09\times10^{-3} + 50\times10^{-6}$

$I_E = 3.14mA$.

Q.19 The h-parameters of the transistor in the amplifier circuit shown below are: h_{ie}=2.2 KΩ , h_{fe}=52, h_{oe}= 25μmhos and h_{re} is negligible. The output load resistor dissipates a signal power of 9 mW. Determine the power gain of the amplifier using its equivalent circuit. The reactances of the capacitors may be neglected. **(8)**



Ans:

$Z_b = h_{ie} = 2.2k\Omega$

$$Z_{in} = R_B \parallel h_{ie} = 70k \parallel 2.2k = \frac{70k\times2.2k}{(70+2.2)k}$$

$$Z_{in} = \frac{154\times10^6}{72.2\times10^3} = 2.132k\Omega$$

Input impedance to E, $Z_S = R_S + Z_{in}$

$$Z_S = 5k + 2.132k = 7.132k\Omega$$

Power drawn from the source, $P_{in} = \frac{E^2}{Z_S} = \frac{E^2}{6.95}mw$.

Base current, $I_b = I_S \times \frac{R_B}{R_B + h_{ie}}$

$$= \frac{E}{6.95}m \times \frac{70}{70+2.2}$$

$I_b = 0.14E(mA)$

Output impedance,

$$Z_{out} = \frac{1}{h_{oe}} \parallel R_G = \frac{1}{25\times10^{-6}} \parallel 12\times10^3$$

$$Z_{out} = \frac{\frac{1}{25\times10^{-6}}\times12\times10^3}{\frac{1}{25\times10^{-6}} + 12\times10^3}$$

$$Z_{out} = \frac{480\times10^6}{52\times10^3}$$

$Z_{out} = 9.23k\Omega$

AC-load resistance,

$R_{ac} = Z_{out} \parallel R_L = 9.23k \parallel 10k$

$$R_{ac} = \frac{9.23\times10^3 \times 10\times10^3}{(9.23+10)10^3}$$

$R_{ac} = 4.8k\Omega$

Output voltage,

$V_{out} = -h_{fe} I_b R_{ac}$

$V_{out} = -52\times0.14E\times10^{-3}\times4.8\times10^3$

$V_{out} = 34.94E$

$$P_{out} = \frac{(V_{out})^2}{R_L} = \frac{(34.94E)^2}{10\times10^3} = 9mw$$

$1220.80\times E^2 = 90$

$$E^2 = \frac{90}{1220.80}$$

E = 0.2715

Power gain, Ap = $\dfrac{Power\ dissipated}{Power\ input}$

$$Ap = \frac{9mw}{\frac{E^2}{6.95}mw}$$

$$Ap = \frac{6.95\times9}{E^2}$$

$$Ap = \frac{6.95\times9}{(0.2715)^2}$$

$$Ap = \frac{62.55}{0.0737} = 848.71.$$

Q.20 The collector voltage of a Class B push pull amplifier with V_{CC}=40 Volts swings down to a minimum of 4 volts. The total power dissipation in both the transistors is 36 watts. Compute the total dc power input and conversion efficiency of the amplifier. **(7)**

Ans:

$V_{cc} = 40v, \quad V_{\min} = 4v \quad P_d = 36w$

$\therefore P_d = P_{in(dc)} - P_{out(ac)}$

$$36 = \frac{2}{\pi}V_{cc}I_{c_{\max}} - \frac{I_{c_{\max}}}{2}\left(V_{cc} - V_{c_{\min}}\right)$$

$$= I_{c_{\max}}\left[\frac{2V_{cc}}{\pi} - \frac{V_{cc} - V_{c_{\min}}}{2}\right]$$

$$36 = I_{c_{\max}}\left[\frac{2\times40}{\pi} - \frac{40-4}{2}\right]$$

$$36 = I_{c_{\max}}\left[25.46-18\right]$$

$$I_{c_{\max}} = \frac{36}{7.46} = 4.825A$$

$$\therefore P_{in}(dc) = \frac{2}{\pi}V_{cc}I_{c\max} = \frac{2}{\pi}\times 40\times 4.825$$

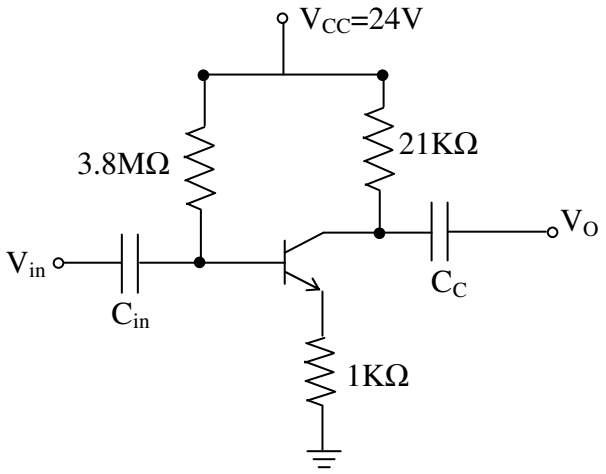
$$P_{in}(dc) = 122.85w$$

$$P_{out}(ac) = \frac{I_{c\max}}{2}\left(V_{cc} - V_{c\min}\right)$$

$$= \frac{4.825}{2}(40-4) = 86.85w$$

$$\eta = \frac{P_{out}(ac)}{P_{in}(dc)}\times 100 = \frac{86.85}{122.85}\times 100 = 70.65\%$$

Q.21 The transistor in the feedback circuit shown below has β=200. Determine (i) feedback factor, (ii) feedback ratio, (iii) voltage gain without feedback and (iv) voltage gain with feedback in the circuit. In the transistor, under the conditions of operation, V_{BE} may be assumed to be negligible. **(6)**



Ans:

$V_{cc} = 24V$, $R_B = 3.8M\Omega$, $\beta = 200$, $R_E = 1k\Omega$

$$I_E = \frac{V_{cc}}{\frac{R_B}{\beta} + R_E} = \frac{24}{\frac{3.8\times 10^6}{200} + 1\times 10^3}$$

$$I_E = 1.2mA$$

AC Emitter resistance, $r_{e'} = \frac{25mv}{I_E} = \frac{25mv}{1.2mA}$

$$r_{e'} = 20.83\Omega$$

Voltage gain without feedback,

$$A = \frac{R_G}{r_{e'}} = \frac{21\times 10^3}{20.83}$$

A = 1008.16

Feedback ratio $\beta = \frac{R_E}{R_C} = \frac{1\times10^3}{21\times10^3}$

$\beta = 0.0476$

Feedback factor = $\beta A = 0.0476\times1008.16$

Feedback factor = 48.0076

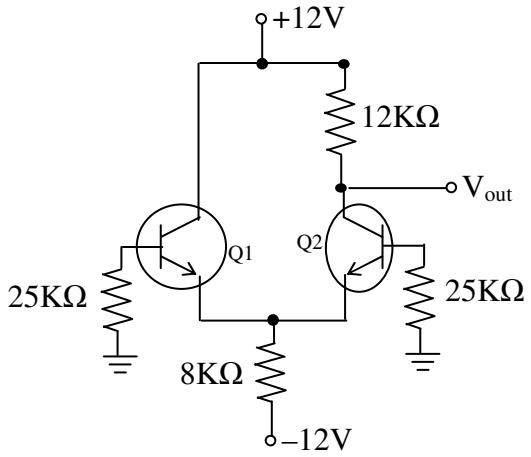
Voltage gain with feedback,

$A_f = \frac{A}{1+\beta A} = \frac{1008.16}{1+48.0076}$

$A_f = 20.57$

Q.22 In the differential amplifier circuit shown below, the transistors have identical characteristics and their β=100.Determine the (i) output voltage (ii) the base currents and (iii) the base voltages taking into account the effect of the R_B and V_{BE}. Take V_{BE}=0.7 Volts.

(8)



Ans:

Tail current, $I_T = \frac{V_{EE}}{R_E} = \frac{12v}{8k} = 1.5mA$

The collector current in transistor Q2 is half thus tail current (i.e. 0.75mA) because each transistor gets half the tail current.

$\therefore \quad V_{out} = V_{cc} - I_c. \quad Rc = 12 - (0.75)(10k)$

$V_{out} = 4.5v$

Tail current $I_T = \frac{V_{EE} - V_{BE}}{R_E} = \frac{12 - 0.7}{8k}$

$I_T = 1.41mA$

$V_{out} = V_{cc} - \frac{I_T}{2} XRc = 12 - \frac{1.41m}{2} X12k$

$V_{out} = 3.54$

And Tail current, $I_T = \dfrac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{2\beta dc}}$

$$I_T = \frac{12 - 0.7}{8k + \frac{25k}{2\times 100}}$$

$$I_T = 1.390mA$$

And output voltage,

$$V_{out} = V_{cc} - \frac{1}{2} I_T . R_c$$

$$= 12 - \frac{1}{2}\left(\frac{1.390}{2} m\right)(12k)$$

$$V_{out} = 3.66v$$

If the results obtained are compared, we find that the results obtained improve with each refinement, but the improvement is not significant.

$\therefore$ The ideal tail current is 1.41mA

$$\therefore \quad I_B = \frac{I_c}{\beta} = \frac{0.75m}{100} = 7.5\mu A$$

$$\therefore \quad V_B = -I_B . R_B = -(7.5\mu)(25k)$$

$$V_B = -0.1875v$$

Q.23 Design a series voltage regulator to supply 1A to a load at a constant voltage of 9V. The supply voltage to regulator is 15V±10%. The minimum zener current is 12mA. For the transistor to be used, assume V_{BE}=0.6V and β=50. **(7)**

Ans:

$$I_B = \frac{I_c}{\beta} = \frac{1A}{50} = 20mA$$

$$V_{out} = V_z - V_{BE}$$

$$9 = V_z - 0.6$$

$$V_z = 9.6v$$

Voltage drop in resistor $R = V_{in} - V_Z = 15 - 9.6 = 5.4v$

Current through resistor R, $I = I_B + I_Z = 20 + 12 = 32mA$

$$\therefore \quad R = \frac{Voltage\ drop\ in\ resistor\ R}{I} = \frac{5.4}{32mA}$$

$$R = 168.75\Omega .$$

Q.24 Obtain the minterms of the function

$$f(\mathrm{A,B,C}) = \mathrm{A} + \overline{\mathrm{B}}\mathrm{C}$$

and draw the K-map of the function. **(4)**

Ans:

$$f(A,B,C) = A + \overline{B}C$$

$$f(A,B,C,) = A(B + \overline{B})(C + \overline{C}) + \overline{B}C(A + \overline{A})$$

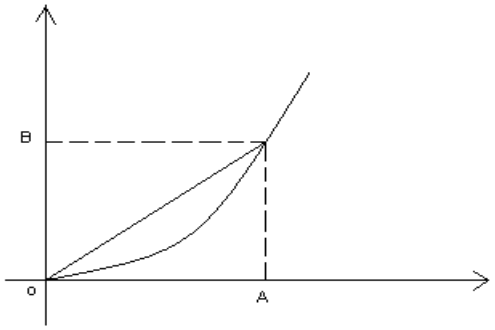
$$= AB + A\overline{B})(C + \overline{C}) + \overline{B}CA + \overline{A}\overline{B}C)$$
$$= ABC + A\overline{B}C + AB\overline{C} + A\overline{B}\overline{C} + \overline{B}CA + \overline{A}\overline{B}C$$

A \ BC	00	01	11	10
0	1	1	1	1
1		1		

Q.25 A load line intersects the forward V-I characteristic of a silicon diode at Q, where the slope of the curve is 40mA/V. Calculate the diode resistance at the point Q. **(4)**

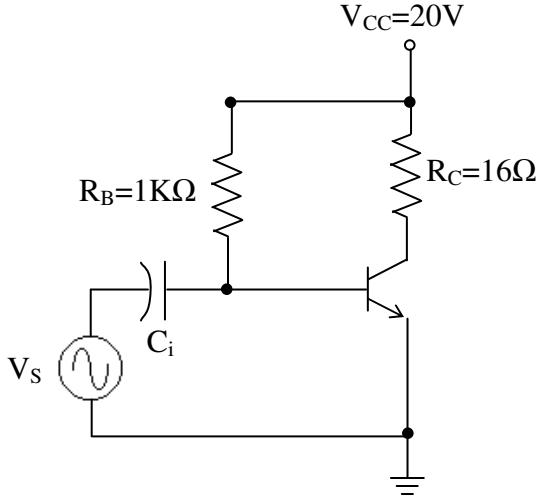
Ans:

DC or static resistance, $R = \frac{V}{I} = \frac{OA}{OB}$



$$R = \frac{V}{I} = \frac{1}{4omA/V}$$
$$R = 25\Omega .$$

Q.26 The power amplifier shown below is operated in class A, with a base current drive of 8.5mA peak. Calculate the input dc power, the power dissipated in the transistor, the signal power delivered to the load and the overall efficiency of the amplifier, if transistor β=30 and V_{BE}=0.7V. **(8)**



Ans:

$I_{c(Sat)} = \frac{V_{cc}}{R_c} = \frac{20}{16} = 1.25A$

$V_{cE} = V_{cc} = 20v$

Now dc – load line is drawn joining points (20v, 0) and (0, 1.25A)

For operating point Q,

$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{20 - 0.7}{1k} = 19.3mA$

$I_{c_Q} = \beta I_B = 30 \times 19.3m = 0.579A$

$V_{cE_Q} = V_{cc} - I_{c_Q} R_c = 20 - 0.579 \times 16 = 10.736v$

$I_{c_{peak}} = \beta . I_{b_{peak}} = 30 \times 8.5m = 0.255A$

$P_{in(dc)} = V_{cc} I_{cQ} = 20 \times 0.579 = 11.58w$.

$P_{out}(ac) = \left(\frac{I_{c_{peak}}}{\sqrt{2}} \right)^2 R_c = \left(\frac{0.255}{\sqrt{2}} \right)^2 \times 16$

= 0.5202 w.

Power delivered to the transistor,

$P_{tr(dc)} = V_{cc} I_{c_Q} - I_{cQ}^2 R_c$

= 20(0.579) – $(0.579)^2$.16

= 6.216w

Power lost in transistor = $P_{tr(dc)} - P_{out(ac)}$

= 6.216 – 0.5202

= 5.6958

Collector Efficiency, $\eta_{colleff} = \frac{P_{out(ac)}}{P_{tr(dc)}} \times 100$

$= \frac{0.5202}{6.216} \times 100$

= 8.368 %.

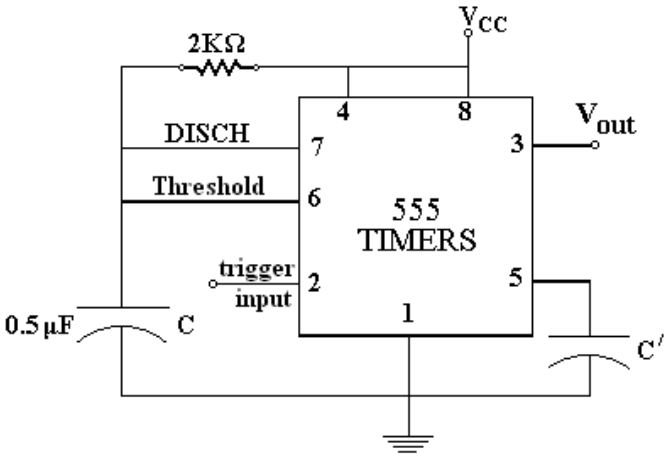
Power rating of transistor = Zero-signal power dissipation

$= V_{cE_Q} I_{c_Q}$

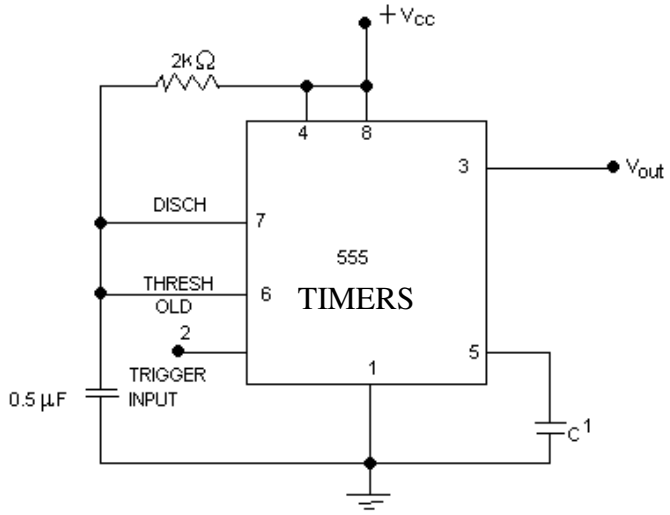
$= 10.736 \times 0.579$

= 6.216w.

Q.27 Find the period of the output pulse in the circuit shown below: **(4)**



Ans:



The pulse width = $1.1R_AC = 1.1 \times 2K \times 0.5\mu = 1.1mSec$.

Q.28 Analyze half-wave and full-wave rectifier circuits (without filter) to deduce the values of rectification efficiency assuming ideal diodes. **(8)**

Ans:

Rectification efficiency of half-wave rectifier, which is defined as the ratio of dc-output power to the ac-input power, is given as

$$\eta = \frac{DC - Power\ delivered\ to\ the\ load}{AC - input\ power\ from\ the\ transformer}$$

$$= \frac{P_{dc}}{P_{ac}}.$$

Now, $P_{dc} = I_{dc}^2 .\ R_L = \left(\frac{I_{\max}}{\pi}\right)^2 .R_L$

P_{ac} = Power dissipated in diode junction + Power dissipated in load resistance R_L

$$= I_{rms}^2 R_F + I_{rms}^2 R_L = I_{rms}^2 (R_F + R_L)$$

$$= \frac{I_{\max}^2}{4}(R_F + R_L)$$

$$\eta = \frac{Pdc}{Pac} = \frac{I_{\max}^2 \, {}^{R_L}\!/_{\pi^2}}{I_{\max}^2 (R_F + R_L)/4} = \frac{4}{\pi^2}\frac{R_L}{R_F + R_L}$$

$$\eta = \frac{0.406}{1 + {}^{R_F}\!/_{R_L}}$$ i.e. 40.6 % if R_F is neglected.

Full-wave rectifier:

$$P_{dc} = I_{dc}^2 . R_L = \left(\frac{2}{\pi} I_{\max}\right)^2 R_L = \frac{4}{\pi^2} I_{\max}^2 R_L$$

$$P_{ac} = I_{rms}^2 . (R_L + R_F) = \frac{I_{\max}^2}{2}(R_L + R_F)$$

Rectification efficiency, $\eta = \dfrac{P_{dc}}{P_{ac}} = \dfrac{\frac{4}{\pi^2} I_{\max}^2 R_L}{\frac{I_{\max}^2}{2}(R_L + R_F)}$

$$\eta = \frac{8}{\pi^2}\frac{1}{\left(1 + {}^{R_F}\!/_{R_L}\right)} = \frac{0.812}{1 + {}^{R_F}\!/_{R_L}}$$

$\eta = 81.2\ \%$ if R_F is neglected.

Q.29 An intrinsic silicon bar is 4mm long and has a rectangular cross section 60x100 $(\mu m)^2$. At 300K, find the electric field intensity in the bar and voltage across the bar when a steady state current of 1μA is measured. (Resistivity of intrinsic silicon at 300K is 2.3 x 10^3 Ω–m **(7)**

Ans:

Length=4mm
A=60 x 100 $(\mu m)^2$
Current I =1μA
Resistivity r = 2.3 x 10^3 Ωm

J = σ E
E = J / σ = (I/A) (1/σ) = (I/A) r
E = (1 x 10^{-6}/ (60 x 10^{-6} x 100 x 10^{-6}))x 2.3 x10^3
= 383.33 x 10^3 V/m
V = EL = 383.33 x 10^3 x 4mm =1.53 x 10^3 V

Q.30 The resistivity of doped silicon material is 9 x 10^{-3}ohm-m. The Hall co-efficient is 3.6 x $10^{-4}$$m^3$ $columb^{-1}$. Assuming single carrier conduction, find the mobility and density of charge carrier (e = 1.6 x 10^{-19} coulomb) **(7)**

Ans:

R_H = 3.6x10^{-4} m^3/columb, ρ = 9x10^{-3} ohm-m
Mobility = $\mu_n = \sigma R_H = (1/\rho)R_H$ = (1/9x10^{-3})x 3.6x10^{-4} = 400 cm^2/V-s

Density of charge carriers = σμ

$= (1/9x10^{-3})\ 400 = 44.44m$ coulomb

Q.31 A single tuned amplifier with capacitive coupling consists tuned circuit having R=10, L=20mH and C=0.05 F. Determine the (i) Resonant frequency (ii) Q-factor of the tank circuit (iii) Bandwidth of the amplifier. **(7)**

Ans:

(i) Reasonant frequency: $f_r = 1 / (2\pi\sqrt{LC}) = 1 / (2\pi\sqrt{20x10^{-3}x0.05x10^{-6}}) = 5032$ Hz

(ii) Q-factor of the tank circuit: $Q = X_L / R = 2\pi f_r L / R$.

$X_L = 2\pi f_r L / = (2\ \pi\ x\ 5032\ x\ 20x10^{-3})/10 = 63.23$

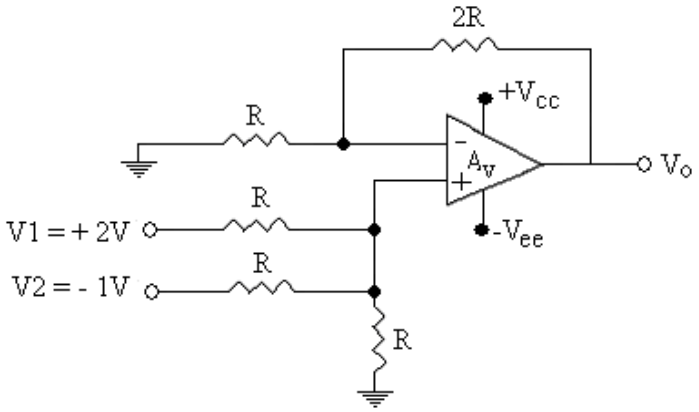
$Q = 63.23 / 10 = 6.32$

(iii) Band width of the amplifier: As $Q = f_r / BW$

$\therefore 6.32 = 5032 / BW$

$BW = 769.20$Hz

Q.32 Calculate the output voltage 'V_0' for the following non inverting op-amp summer, with V_1 =2V and V_2 = -1V **(7)**



Ans:

$V_O = ([R_2V_1 + R_1V_2] / [R_1 + R_2])^* ([R + R_f] / R)$

If in the summer circuit the value of resistance are selected as $R_1 = R_2 = R$ and $R_f = 2R$. Then

$V_O = - [(2R)\ V_1/R + (2R)\ V_2/R]$

$= - [2(V_1 + V_2)]$

$= - [2(2 -1)\ ] = -2$ V

Q.33 The current flowing through a certain P-N junction at room temperature when reverse biased is 0.15μA. Given that volt-equivalent of temperature, V_T is 26mV, and the bias voltage being very large in comparison to V_T, determine the current flowing through the diode when the applied voltage is 0.12V. **(7)**

Ans:

The diode current is given by

$I = Io\ (e^{-(V_p/\eta V_T)} - 1)$

For large reverse bias, the diode current

$I = Io = 0.15\ x\ 10^{-6}$A.

Given V=0.12V, V_T = 0.026 V, assuming Si diode, i.e.,η = 2
$I = 0.15 \times 10^{-6} (e^{(0.12/(2 \times 0.026))} - 1)$
$= 1.36\ \mu A$

Q.34 In a transistor amplifier, change of 0.025V in signal voltage causes the base current to change by 15μA and collector current by 1.2 mA. If collector and load resistances are of 6kΩ and 12kΩ, determine

i) input resistance (ii) current gain
iii) ac load (iv) voltage gain
v) power gain **(7)**

Ans:

i) Input resistance = change in input voltage / change in input current = $0.025/15 \times 10^{-6}$ = 1.67kΩ
ii) Current gain = β = change in output current / change in input current = $1.2mA/15 \times 10^{-6} = 80$
iii) AC load = Rc || R_L = 6k x 12k/(6k+12k) = 4kΩ
iv) Voltage gain: output voltage = $1.2 \times 10^{-3} \times 4 \times 10^{3} = 4.8V = Vo$
input voltage = 0.025V = Vi
Voltage Gain = Vo / Vi = 4.8 / 0.025 =192
v) Power gain = voltage gain x current gain = 192 x 80 = 15360

Q.35 What is a load line and how is it used in the calculation of current and voltage gains for a single stage amplifier? **(7)**

Ans:

In a transistor, the collector current I_C depends on base current I_B. The variation of I_C for a specific load R_C as a function of input voltage is along a straight line. This line for a fixed load is called as dc load line. The output characteristic of a CE amplifier is plotted in the Fig. 13a. Consider the following specifications of the CE amplifier.

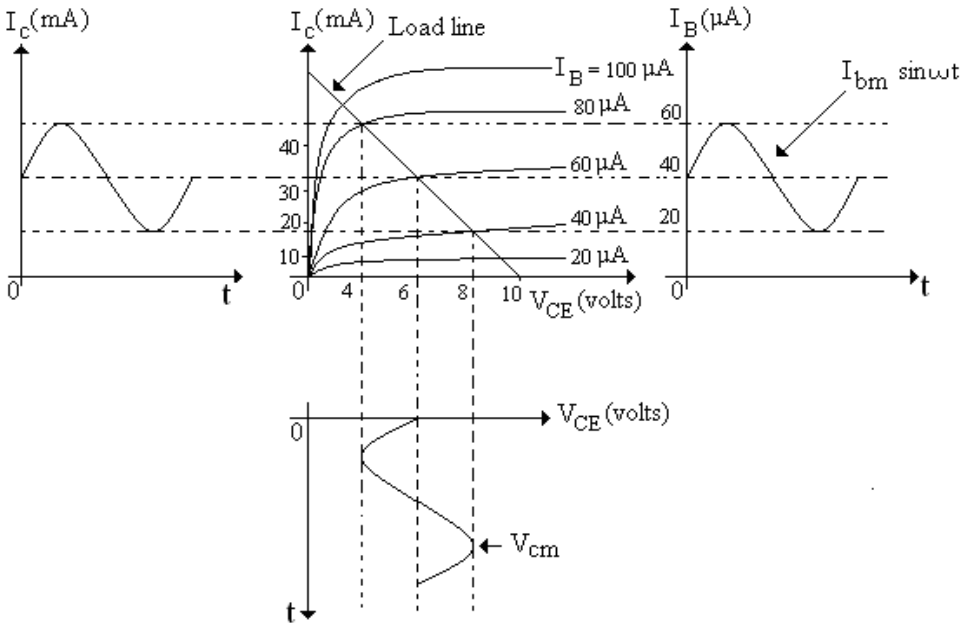


Fig. 13a

$I_{BQ} = 40\mu A$
I_{CQ}=8mA, $V_{CEQ} = 6V$
$V_S = V_m \sin\omega t$
The amplitude V_m is chosen to provide a signal component of base current
$I_b = I_{bm} \sin\omega t$
Where $I_{bm} = 20\mu A$

Total instantaneous base current i_B is the superposition of the dc level and the signal current.
Therefore $i_B = I_{BQ} + I_b = 40 + 20 \sin\omega t\ \mu A$
From the figure, we see that variation in I_B causes both I_C and V_{CE} to vary sinusoidally about their quiescent levels. These quantities are expressed as
$i_C = I_{CQ} + i_C = I_{CQ} + I_{cm} \sin\omega t$
$v_{CE} = V_{CEQ} + v_{ce} = V_{CEQ} + V_{cm} \sin\omega t$ V
From figure 3a, I_{cm} = 4mA and V_{cm}= 2V

Q.36 The transconductance of a FET used in an amplifier circuit is 4000 micro-siemens. The load resistance is 15kΩ and drain circuit resistance is 10 MΩ. Calculate the voltage gain of the amplifier circuit .

Ans:
Given: $g_m = 4000$, $R_L = 15k\Omega$, $r_d = 10M\Omega$ **(7)**
$V_o = -g_m \times V_{gs} (r_d \parallel R_L)$
$V_o / V_{in} = -(g_m \times V_{gs} (r_d \parallel R_L)) / V_{in}$
But $V_{gs} = V_{in}$
Therefore voltage gain $V_o / Vin = -(g_m (r_d \parallel R_L))$
$V_o / V_{in} = 4000x10^{-6} \times ((10^6x15x10^3) / (10^6 + 15x10^3))$
$= (60x10^6) / (10^3(10^3 + 1)$
≈ 60

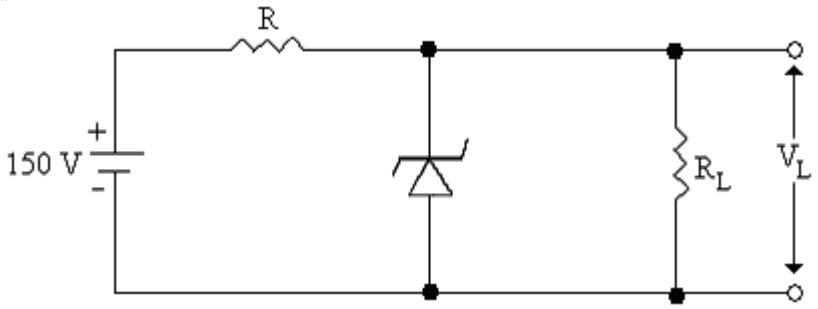
Q.37 An output waveform displayed on an oscilloscope provided the following measured values
i) V_{CE} min=1.2V, V_{CE} max=22V, V_{CEQ}=10V
ii) V_{CE} min=2V, V_{CE} max=18V, V_{CEQ}=10V
Determine the percent second harmonic distortion in each case. **(14)**

Ans:
$D_2 = (|B_2| / |B_1|) \times 100\%$
i) $B_2 = (I_{max} + I_{min} - 2I_{CQ}) / 4$
$= (V_{CE\ max} + V_{CE\ min} - 2V_{CEQ}) / 4$
$= (22+1.2-20) / 4 = 3.2 / 4 = 0.8$
$B_1 = (I_{max} - I_{min}) / 2 = (V_{CE\ max} - V_{CE\ min}) / 2 = (22-1.2) / 2 = 10.4$
$D_2 = (0.8 / 10.4)x100 = 7.69\%$
ii) $B_2 = (2+18-20) / 4 = 0$
$B_1 = (18-2) / 2 = 8$
$D_2 = 2.5/8 \times 100 = 0\%$

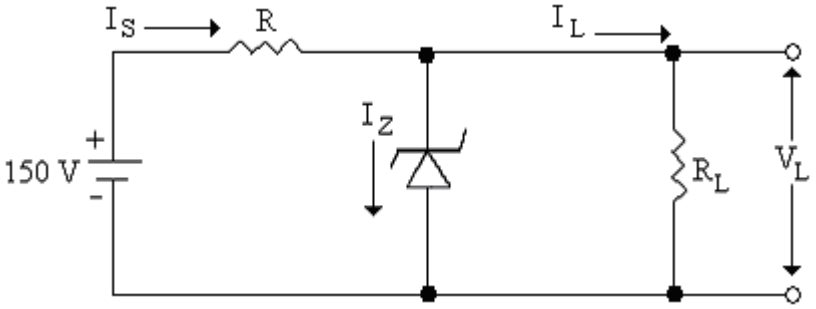
Q.38 A sample of pure silicon has electrical resistivity of 3000Ωm. The free carrier density in it is $1.1x10^{16}/m^3$. If the electron mobility is three times that of hole mobility, find electron mobility and hole mobility. The electronic charge is equal to $1.6x10^{-19}$coulomb. **(6)**
Ans:

For pure Silicon, $n_i = n = p = 1.1x10^{16}/ m^3$, and $\mu n = 3\mu p$
$\sigma = n_i (\mu_n + \mu_p) e = 1.1x10^{16} (\mu_p + 3\mu_p) 1.6x10^{-19} = 7.04 \times 10^{-3} \mu_p$
$= (3000\ \Omega m)^{-1}$
Thus $\mu_p x 7.04x10^{-3} = 1/3x10^{-3}$
i.e., $\mu_p = .047\ m^2\ V^{-1}\ S^{-1}$ and $\mu_n = 3\ \mu_p = 0.141\ m^2\ V^{-1}\ S^{-1}$

Q.39 Explain '**Zener breakdown**'. The zener diode in the circuit shown below regulates at 50V, over a range of diode currents from 5 to 40mA. The supply voltage V = 150V. Compute the value of R to allow voltage regulation from a zero load current to a maximum load current I_{max}. What is I_{max}? **(8)**



Ans:
Zener break down takes place in diodes having heavily doped p and n regions with essentially narrow depletion region. Considerable reverse bias gives rise to intense electric field in the narrow depletion region causing breakdown of covalent bonds and so creating a number of electron-hole pairs which substantially add to the reverse current which may sustain at a constant voltage across the junction. This breakdown is reversible.



Problem:
For $I_L = 0$, $V_L = 50$ volts and
$I_z = I_s = (150 - 50) / R \leq 40$ mA
Hence $R \geq 100/40\ K\Omega$, i.e $2.5\ K\Omega$
For $I_L = I_{max}$, $I_z \geq 5$mA
But for $R = 2.5\ K\Omega$, $I_s = 40$ mA.
Hence $I_{max} = 40 - 5 = 35$ mA

Q.40 Draw a figure to show the output V-I characteristic curves of a BJT in CE configuration. Indicate thereon, the saturation, active and cut off regions. Explain how, using these characteristics, one can determine the value of h_{fe} or β_F. **(6)**

Ans:

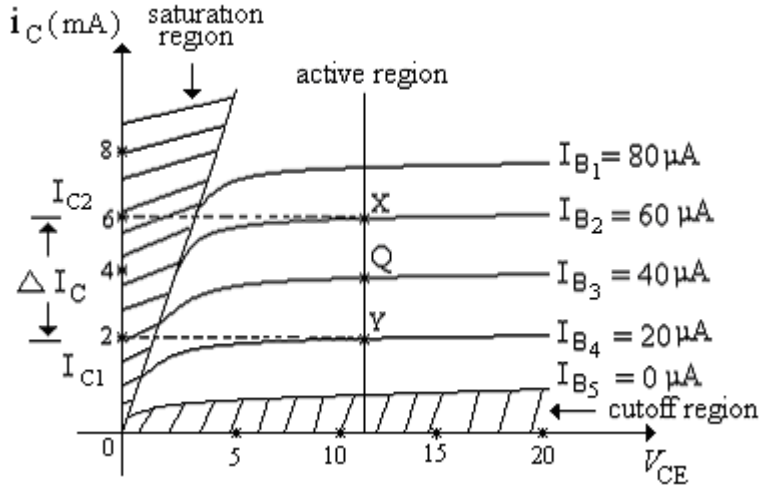


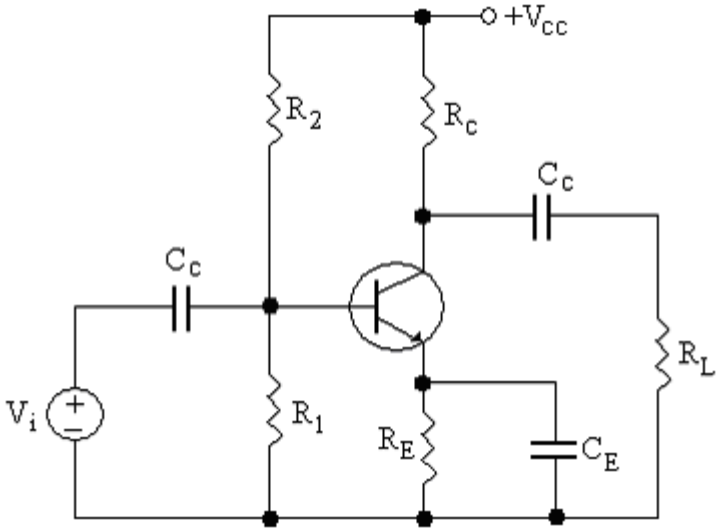
Fig. 18b

Fig. 18b. shows the characteristics of BJT in CE configuration. To find h_{fe}, draw a constant V_{CE} line (vertical) going through desired Q point. Choose constant I_B lines suitably, which cut the constant Vce line at X and Y.

$h_{fe} = \Delta I_C / \Delta I_B$. From fig $h_{fe} = (I_{C2}-I_{C1}) / (I_{B4}-I_{B2})$

$= (6\text{-}2)$ mA / $(60\text{-}20)$ µA $=100$.

Q.41 Draw a small signal h-parameter equivalent circuit for the CE amplifier shown in fig below.



Find an expression for voltage gain of the amplifier.Compute the value of voltage gain, if $R_C = R_L = 800\Omega$, $R_1 = 1.5k\Omega$, $R_2 = 3k\Omega$, $h_{re} \approx 0$, $h_{oe} = 100\mu S$, $h_{fe} = 90$ and $h_{ie} = 150\Omega$. **(9)**

Ans:

Fig. 19 shows the small signal h-parameter model for CE amplifier

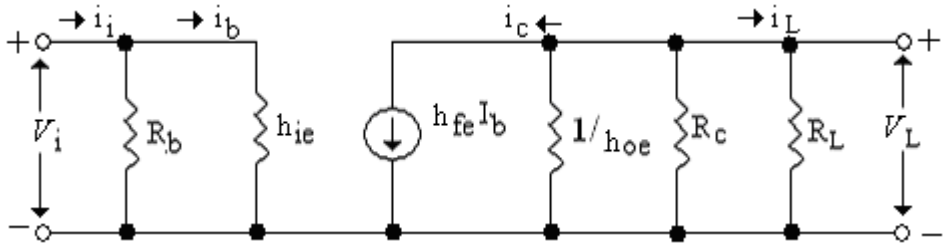


Fig.19

Voltage gain of amplifier is $A_v = V_L / V_i$

$R_b = R_1R_2 / (R_1 + R_2)$ in the equivalent circuit.

By current division in output circuit,

$$\frac{1}{h_{oe}} 11P_c = \frac{R_c \dfrac{1}{h_{oe}}}{R_e + \dfrac{1}{h_{oe}}} = \frac{R_c}{1 + R_c h_{oe}}$$

$$\frac{1}{h_{oe}} \Big\| R_c \Big\| R_c = \left(R_c \cdot \frac{1}{1 + R_c h_{oe}} \right) + R_c$$

$$= R_c R_L / [R_c + (1 + R_c\, h_{oe}) R_L] = R_c R_L / [R_c + R_L + h_{oe} R_L R_c]$$

$$V_i = i_b . h_{ie}$$

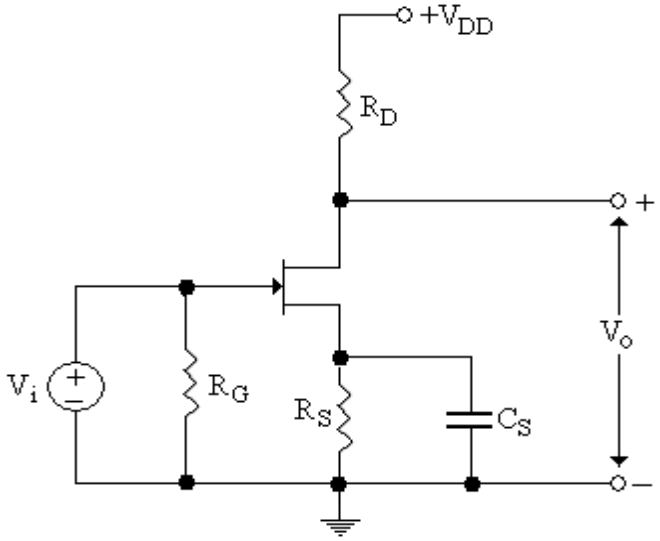
$$V_o = (-h_{ge} \cdot i_b)(R_c R_L / [R_c + R_L + h_{oe} R_L R_c])$$

$$\therefore A_v = V_0 / V_i = -(h_{fe} R_c R_L) / [h_{ie} (R_c R_L + h_{oe} R_L R_c)]$$

$R_b = (R_1R_2) / (R_1+R_2) = (1.5\text{x}10^3\text{x}3\text{x}10^3) / (1.5+3)10^3 = 1\text{k}\Omega$

$Av = (-90\text{x}800\text{x}800) / [150(800+800+100\text{x}10^{-6}\text{x}800\text{x}800) = -230.7$

Q.42 The circuit of a common source FET amplifier is shown in the figure below. Find expressions for voltage gain A_v and current gain A_i for the circuit in mid frequency region where R_s is bypassed by C_s. Find also the input resistance R_{in} for the amplifier. If $R_D = 3\text{k}\Omega$, $R_G = 500\text{k}\Omega$, $\mu = 60$, $r_{ds} = 30\text{k}\Omega$, compute the value of A_v, A_i, and R_{in}. **(8)**



Ans:

Using voltage source model of the FET, the equivalent circuit is as in Fig. 20a

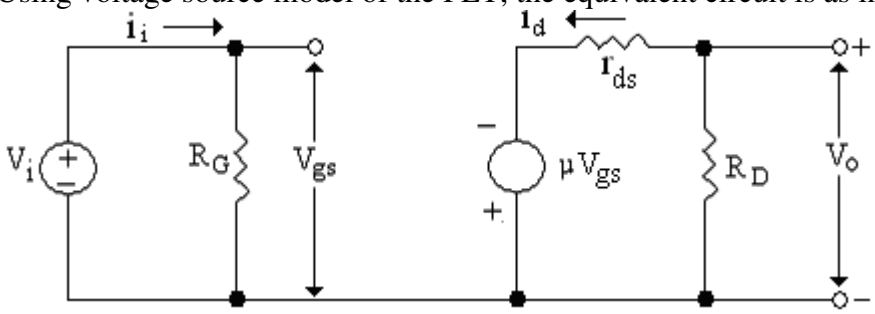


Fig. 20 a

$Vo = (-R_D \mu V_{gs}) / (R_D + r_{ds})$

$V_{gs} = V_i$

$A_v = V_o / V_i = (-\mu R_D) / (R_D + r_{ds})$

$i_d = (\mu V_{gs}) / (r_{ds} + R_D)$

$V_{gs} = i_i R_G$

$A_v = (-60 \times 3 \times 10^3) / (3 \times 10^3 + 30 \times 10^3) = -5.45$

$A_i = i_d / i_i$; i.e $Ai = \mu R_G / (R_D + r_{ds}) = [60 \times 500 \times 10^3] / [30 \times 10^3 + 3 \times 10^3] = 909$

It is obvious that $R_{in} = R_G = 500k\Omega$

Q.43 State Barkhausen criterion for sustained oscillations in a sinusoidal oscillator. The capacitance values of the two capacitors C1 and C2 of the resonant circuit of a colpitt oscillator are C1 = 20pF and C2 = 70pF.The inductor has a value of 22µH. What is the operating frequency of oscillator? **(5)**

Ans:

Consider a basic inverting amplifier with an open loop gain 'A'. With feedback network attenuation factor 'ß' less than unity. The basic amplifier produces a phase shift of 180^o between input and output. The feedback network must introduce 180^o phase shift. This ensures positive feedback.

Barkhausen criterion states that for sustained oscillation,

1. The total phase shift around the loop, as the signal proceeds from input through the amplifier, feedback network and back to input again, is precisely 0^o or 360^o.
2. The magnitude of the product of the open loop gain of the amplifier, 'A' and the feedback factor 'ß' is unity, i.e. $|A\beta| = 1$.

Operating frequency of Colpitts oscillator is given by

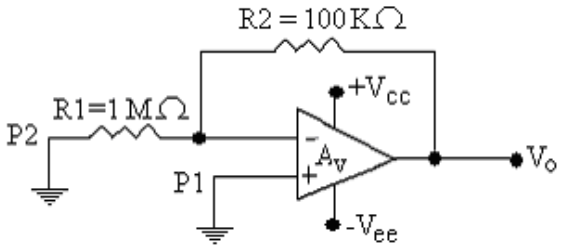
$f = 1 / (2\pi\sqrt{LC_{eq}})$

Where $C_{eq} = (C_1 C_2) / (C_1 + C_2)$

$= (20 \times 70) / (20 + 70) = 15.56pF.$

$f = 1 / \{2 \times \pi \sqrt{22 \times 10^{-6} \times 15.56 \times 10^{-9}}\} = 272.02$ KHz

Q.44 Suggest modification in the given circuit of Opamp to make it (i) inverting (ii) non inverting. **(7)**



Ans:

Fig 24 a (i) shows an inverting amplifier. For an inverting amplifier, the input is to be applied to the inverting terminal. Therefore point P_2 is connected to the signal to be amplified.

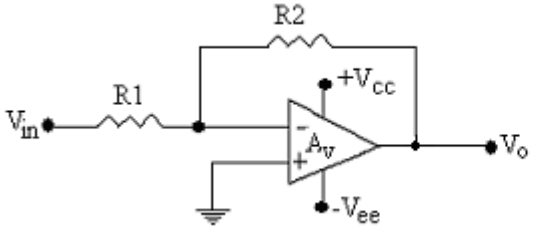


Fig 24 a (i)

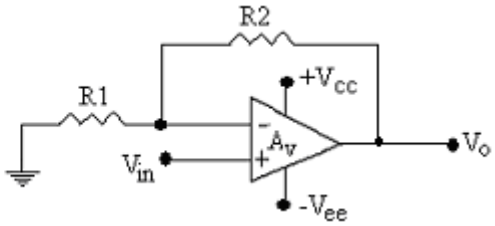


Fig 24 a (ii)

Fig 24 a (ii) shows a non-inverting amplifier. For a non-inverting amplifier, the input is to be applied to the non-inverting terminal. Therefore point P_1 is connected to the source.

Q.45 In the circuit of Q44, if input offset voltage is 0,

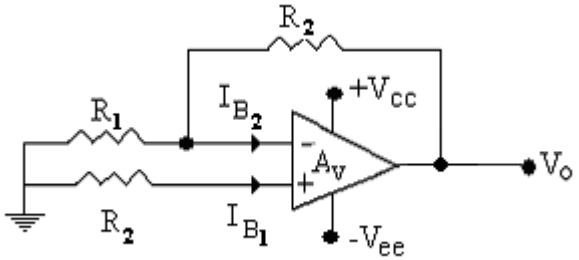
(i) Find the output voltage V_o due to input bias current, when I_B=100nA **(3)**

(ii) How can, the effect of bias current be eliminated so that output voltage is zero? **(4)**

Ans:

(i) When the voltage gain of op-amp is very large, no current flows into the op-amp. Therefore I_B flows into R_2

$Vo = I_B \times R_2 = 100 \times 10^{-9} \times 10^6 = 100$ mV



(ii) If Vo = 0, then $R_1 \parallel R_2$.

Let $Rp = R_1 \parallel R_2$

Then voltage from inverting terminal to ground is

$V_I = -I_{B2} \times Rp$

Let $R^1 = Rp = (R_1 \times R_2) / (R_1 + R_2) = 90.9k\Omega$

Add resistor R^1 between non-inverting terminal and ground

Choose the value of $R^1 = 90.9k\Omega$ to make the output voltage as zero.

Since, $V_I - V_N = 0$ or $V_I = V_N$

where V_I : Voltage at the inverting terminal w.r.t. ground

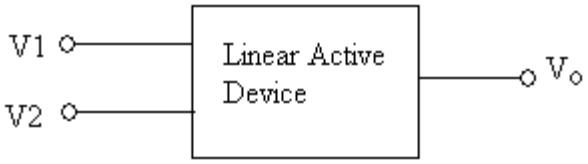
and V_N : Voltage at the non-inverting terminal w.r.t. ground

Hence, $-I_{B2} \times Rp = -I_{B1} \times R^1$
For $I_{B1} = I_{B2}$

Q.46 A differential amplifier has inputs V_{s1}=10mV, V_{s2} = 9mV. It has a differential mode gain of 60 dB and CMRR is 80 dB. Find the percentage error in the output voltage and error voltage. Derive the formulae used. **(14)**

Ans:
In an ideal differential amplifier output V_o is given by
$V_o = A_d (V_1-V_2)$
A_d = gain of differential amplifier

But in practical differential amplifiers, the output depends on difference signal V_d as well as on common mode signal V_C.
$V_d = V_1 - V_2$ ---------- 1
$V_C = (V_1 + V_2) / 2$ --------2
Therefore output of above linear active device can be given as
$V_o = A_1V_1 + A_2V_2$



Where A1(A2) is the voltage amplification factor from input 1(2) to output under the condition that input 2(1) is grounded.
Therefore from 1 and 2
$V_1 = V_c + 0.5V_d$ and $V_2=V_c-0.5V_d$
$V_o = A_dV_d + A_cV_c$
Where $A_d = 0.5(A_1-A_2)$ and $A_c = 0.5(A_1+A_2)$
the voltage gain of difference signal is A_d and voltage gain of common mode signal is A_c.
Common mode rejection ratio = $\rho = |A_d/A_c|$. The equation for output voltage can be written as
$V_o = A_dV_d (1+ (A_d/A_c) (V_c/V_d))$
$V_o = A_dV_d (1+ (1 / \rho) (V_c/V_d))$
V_{s1}=10mV = V_1 , V_{s2}=9mV = V_2
A_d=60dB, CMRR=80dB
$V_d = V_1-V_2$=10mV-9mV=1mV
A_d = 60dB = $20\log_{10} A_d$, since A_d =1000
$V_c = (V_1+V_2)/2 = (10+9) / 2 = 9.5$mV
CMRR = A_d / A_c
$10^3 = 1000 / A_c$
$A_c = 0.1$
$V_o = A_dV_d + A_cV_c = 1000 \times 10^{-3} + 0.1 \times 9.5 \times 10^{-6}$
$= 1.00095$ V

Q.47 Prove the following postulate of Boolean algebra using truth tables
$x + y + z = (x + y).(x + z)$ **(3)**

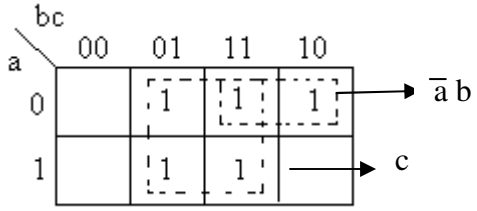
Ans:
The truth table below demonstrates the equality (x + y + z) = (x + y) (x + z)

X	y	z	(x+y)	(x+z)	(x+y)(x+z)	x+y+z
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	1	0	0	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

Q.48 Simplify the following Boolean function using K-map:

$f(a,b,c) = \bar{a}\,c + \bar{a}\,b + a\,\bar{b}\,c + b\,c$ Give the logic implementation of the simplified function in SOP form using suitable gates. **(6)**

Ans:



The simplified function by implementation of K-map is $f(a,b,c) = \bar{a}\,b + c$. Assuming the availability of complements, the logic implementation is as in Fig. 40b.

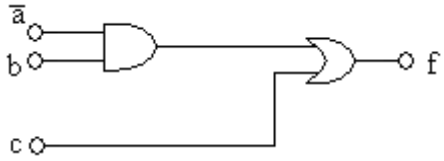
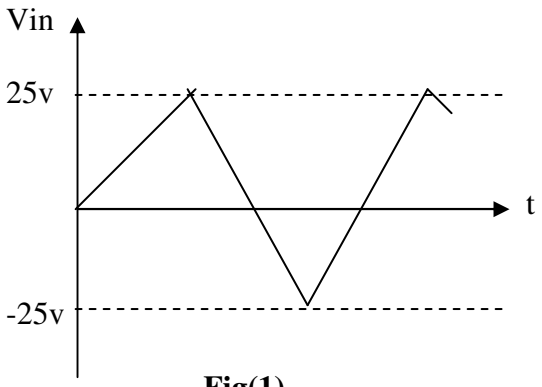


Fig. 40b

PART – III

DESCRIPTIVES

Q.1 A triangular wave shown in fig(1) is applied to the circuit in fig(2). Explain the working of the circuit. Sketch the output waveform.



Fig(1)

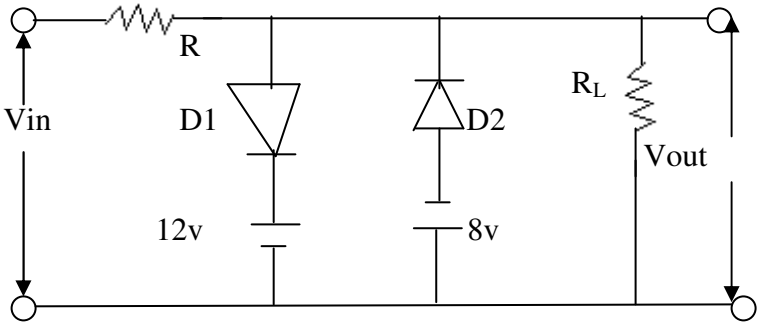
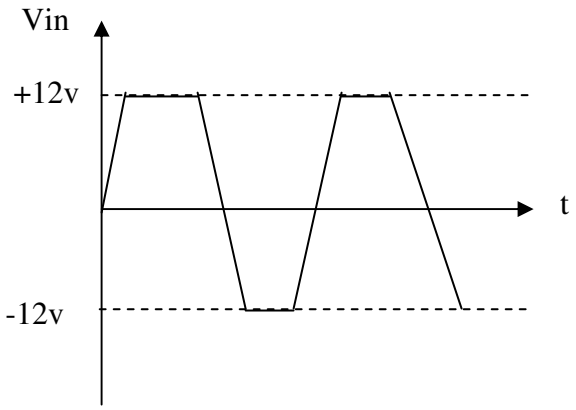


Fig (2)

Ans:



During the positive half-cycle of the input triangular voltage, the diode D_1 remain forward biased as long as input voltage exceeds battery voltage +12v and diode D_2 remains reverse biased and acts as open circuit. Thus up to +12v of the applied signal there would be output

voltage across the output terminals and the triangular signal will be clipped off above 12v level.
During negative half-cycle of the input signal voltage, diode D_1 remains reverse-biased while D_2 remains forward-biased as long as input signal voltage exceeds the battery voltage -8v in magnitude.

Q.2 Define 'diffusion capacitance' of a pn junction diode. Obtain an expression for the same. Why is the diffusion capacitance negligible for a reverse biased diode? **(9)**

Ans:
When a P-N junction is forward biased, a capacitance which is much larger than the transition capacitance, comes into play. This type of capacitance is called the diffusion capacitance, C_D.

Diffusion capacitance is given by the equation, $C_D = \frac{dQ}{dV}$ where dQ represents the change in number of minority carriers stored outside the depletion region when a change in voltage across diode, dV, is applied.

If τ is the mean life-time of charge carriers, then a flow of charge Q yields a diode current I given as

$$I = \frac{Q}{\tau} \quad or \quad Q = \tau I$$

We know that $I = I_0\left[e^{\frac{V}{\eta V_T}} - 1\right]$

So, $Q = \tau I_0\left[e^{\frac{V}{\eta V_T}} - 1\right]$

$$Q = \tau I_0 e^{\frac{V}{\eta V_T}} \quad \therefore \quad e^{\frac{V}{\eta V_T}} >> 1$$

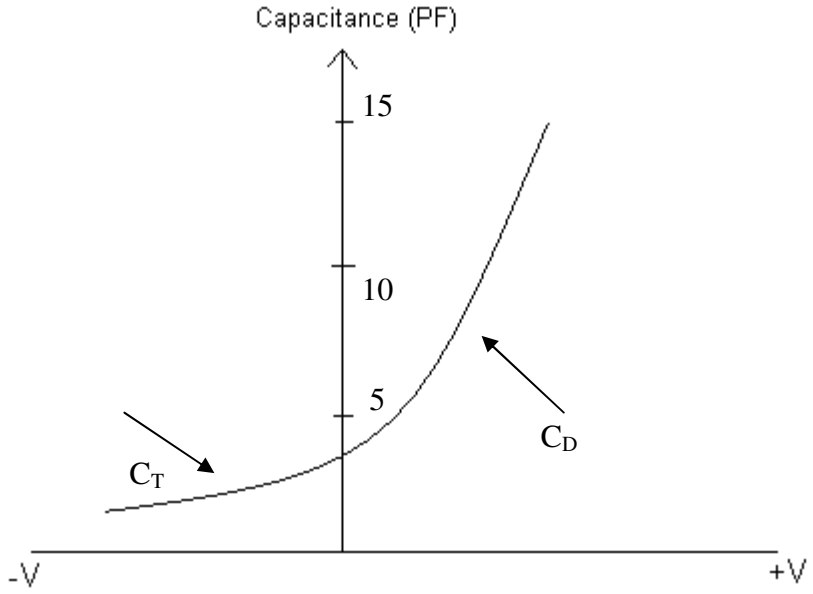
So diffusion capacitance $C_D = \frac{dQ}{dV} = \frac{d}{dV}\left(I_0 \tau e^{\frac{V}{\eta V_T}}\right)$

$$C_D = \frac{\tau I_0}{\eta V_T} . e^{\frac{V}{\eta V_T}} = \frac{\tau[I + I_0]}{\eta V_T}$$

For a forward bias, $\left[\frac{V}{\eta V_T}\right] >> 1 \; and \; I >> I_0$

$$\therefore So, C_D = \frac{\tau I}{\eta V_T}$$

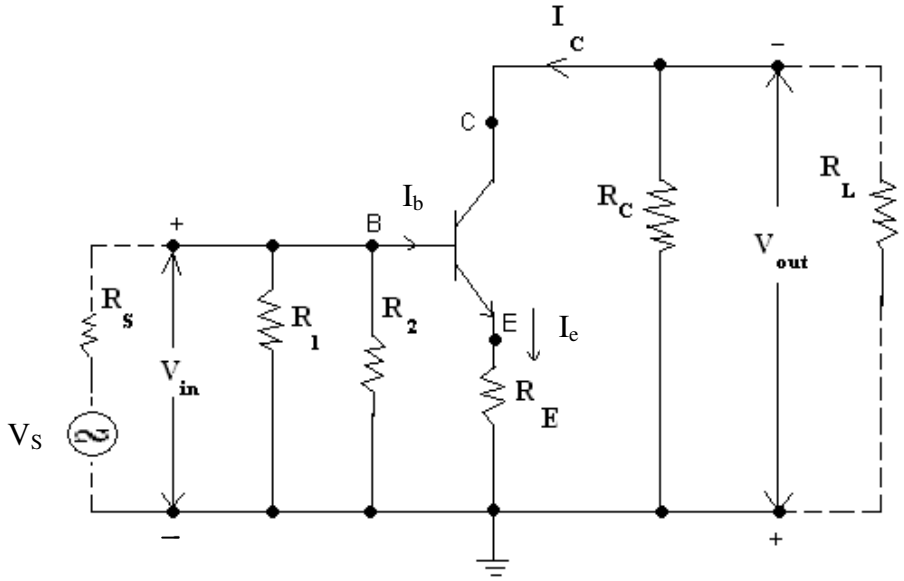
Thus the diffusion capacitance is directly proportional to the forward current through the diode.
C_D: Diffusion capacitance.
C_T: Transition capacitance.



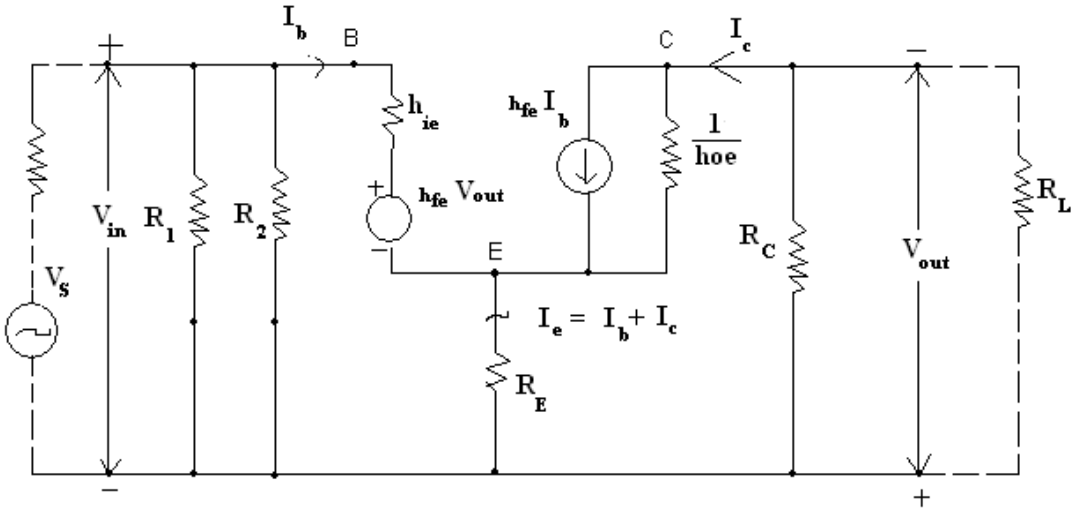
In a reverse biased diode both C_D and C_T are present but $C_T >> C_D$. Hence in a reverse biased diode C_D is neglected and only C_T is considered.

Q.3 Draw the circuit of h-parameter equivalent of a CE amplifier with un by-passed emitter resistor. Derive an expression for (i) its input impedance and (ii) voltage gain, using the equivalent circuit. **(10)**

Ans:



CE – amplifier AC – Equivalent Circuit with an un-bypassed Emitter Resistor (R_E).



CE – Amplifier n – parameter Equivalent circuit with R_E.

Input Impedance:

Zin (base) or $Z_b = h_{ie}$

With an un-bypassed emitter register R_E in the circuit,

$$V_{in} = h_{ie} I_b + I_e R_E = h_{ie} I_b + R_E (I_b + I_c)$$

$$= I_b h_{ie} + I_b R_E + I_c R_E .$$

But $I_c = h_{fe} I_b .$

$$\therefore V_{in} = I_b (h_{ie} + R_E) + h_{fe} I_b . R_E$$

$$V_{in} = I_b (h_{ie} + R_E + R_E h_{fe})$$

$$\therefore Z_b = \frac{V_{in}}{I_b} = h_{ie} + R_E (1 + h_{fe})$$

Voltage Gain:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-I_c Z_{ac}}{I_b Z_{in}} = \frac{-I_c (R_c \parallel R_L)}{I_b . h_{ie}}$$

$$A_v = \frac{-h_{fe} I_b (R_c \parallel R_L)}{I_b h_{ie}} = \frac{-h_{fe}}{hie} (R_G \parallel R_L)$$

The minus sign indicates that output voltage V_{out} is 180^0 out of phase with input voltage V_{in}.

With an un-bypassed R_E in the circuit,

$$V_{in} = I_b h_{ie} + I_e R_E = I_b h_{ie} + R_E (I_b + I_c)$$

$$V_{in} = I_b h_{ie} + I_b R_E (1 + h_{fe}) = I_b (h_{ie} + R_E (1 + h_{fe}))$$

$$\therefore A_v = \frac{-I_c (R_c \parallel R_h)}{I_b [h_{ie} + R_E (1 + h_{fe})]} = \frac{-h_{fe} (R_c \parallel R_h)}{h_{ie} + R_E (1 + h_{fe})}$$

Usually $R_E (1 + h_{fe}) >> h_{ie}$,

$$\therefore \quad A_v = \frac{-R_c \parallel R_L)}{R_E}$$

Q.4 What is a 'multistage amplifier'? Give the requirements to be fulfilled for an ideal coupling network. **(6)**

Ans:

The voltage amplification or power gain or frequency response obtained with a single stage of amplification is usually not sufficient to meet the needs of either a composite electronic circuit or load device. Hence, several amplifier stages are usually employed to achieve greater voltage or current amplification or both. A transistor circuit containing more than one stage of amplification is known as a MULTI-STAGE amplifier.

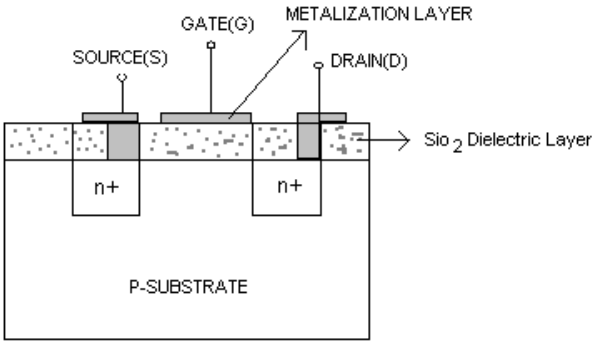
In a multistage amplifier, the output of first-stage is combined to next stage through a coupling device.

For an ideal coupling network the following requirements should be fulfilled.

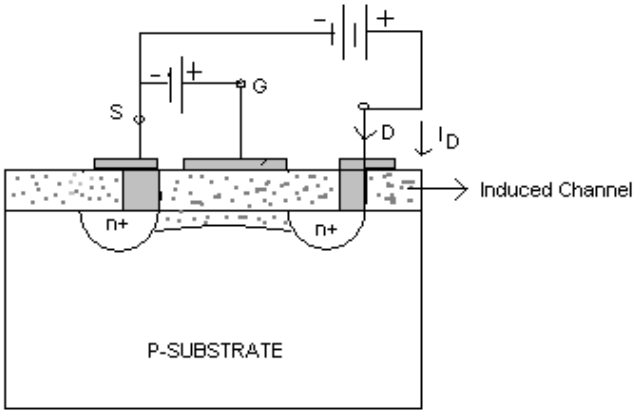
1. It should not disturb the dc-bias conditions of the amplifiers being coupled.
2. The coupling network should transfer ac signal waveform from one amplifier to the next amplifier without any distortion.
3. Although some voltage loss of signal cannot be avoided in the coupling network but this loss should be minimum, just negligible.
4. The coupling network should offer equal impedance to the various frequencies of signal wave.

Q.5 Draw a neat sketch to illustrate the structure of a N-channel E-MOSFET. Explain its operation. **(9)**

Ans:



N-Channel E-MOSFET Structure



Operation of N-Channel E-MOSFET

Operation:

It does not conduct when V_{GS} = 0. In enhancement mosfet drain (I_D) current flows only when V_{GS} exceeds gate-to-source threshold voltage.

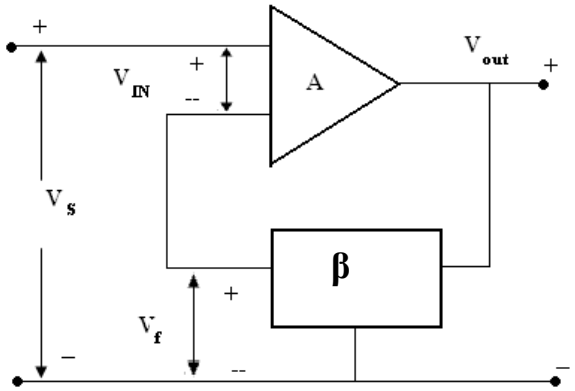
When the gate is made positive with respect to the source and the substrate, negative change carriers within the substrate are attracted to the +ve gate and accumulate close to the surface of the substrate. As the gate voltage increased, more and more electrons accumulate under the gate, these accumulated electrons i.e., minority charge carriers make N-type channel stretching from drain to source.

Now a drain current starts flowing. The strength of the drain current depends upon the channel resistance which, in turn, depends on the number of charge carriers attracted to the positive gate. Thus drain current is controlled by the gate potential.

Q.6 Show that in an amplifier, the gain reduces if negative feedback is used. **(6)**

Ans:

When the feedback voltage (or current) is applied to weaken the input signal, it is called negative feedback



For an open-loop amplifier,

Voltage again, $A = \frac{V_{out}}{V_{in}}$

Let a fraction (say β) of the output voltage V_{out}, be supplied back to the input and A be the open-loop gain. Now $V_{in} = V_S + V_f = V_S + \beta V_{out}$

For + ve feedback case

And $V_{in} = V_S - V_f = V_S - \beta V_{out}$

For negative feedback case,

Actual input voltage to amplifier, $V_{in} = V_S - \beta . V_{out}$

$\therefore V_{out} = A.V_{in} = A(V_S - \beta . V_{out})$

$$\frac{V_{out}}{V_S} = \frac{A}{1 + \beta A}$$

$$A_f = \frac{V_{out}}{V_S} = \frac{A}{1 + \beta A}$$

Q.7 In a voltage series feedback amplifier, show that

a. the input impedance increases with negative feedback.

b. the output impedance decreases due to negative feedback. **(10)**

Ans:

The input impedance can be determined as follows:

$$I_{in} = \frac{V_{in}}{Z_{in}} = \frac{V_S - V_f}{Z_{in}} = \frac{V_S - \beta V_{out}}{Z_{in}}$$

$$= \frac{V_S - \beta A.V_{in}}{Z_{in}}$$

Or $I_{in} Z_{in} = V_S - \beta.A.V_{in}$

$$V_S = I_{in}Z_{in} + \beta.A.V_{in}$$

$$= I_{in}Z_{in} + \beta A I_{in}.Z_{in}.$$

$$\frac{V_S}{I_{in}} = Z_{in} + (\beta A)Z_{in} = Z_{in}(1 + \beta A)$$

$$\therefore Z_{\text{inf}} = Z_{in}(1 + \beta A)$$

The effect of negative feedback on the output impedance of an amplifier is explained below.

$$V_{out} = I_{out}\ Z_{out} + AV_{in} = I_{out}.Z_{out} - A.V_f$$

$$\therefore \quad V_{in} = -V_f$$

$$V_{out} = I_{out}.Z_{out} - A(\beta V_{out})$$

Or $V_{out}(1 + \beta A) = I_{out}\ Z_{out}$

Or $$\frac{V_{out}}{I_{out}} = \frac{Z_{out}}{1 + \beta A}$$

$$Z_{outf} = \frac{Z_{out}}{1 + \beta A}$$

Thus, series voltage negative feedback reduces the output impedance of an amplifier by a factor (1 + βA).

Q.8 List the advantages of a crystal oscillator. **(4)**

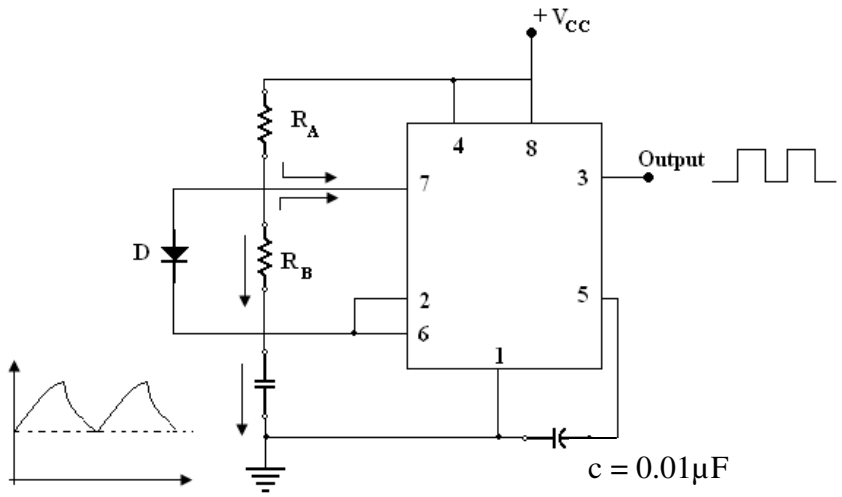
` **Ans:**

Advantages:

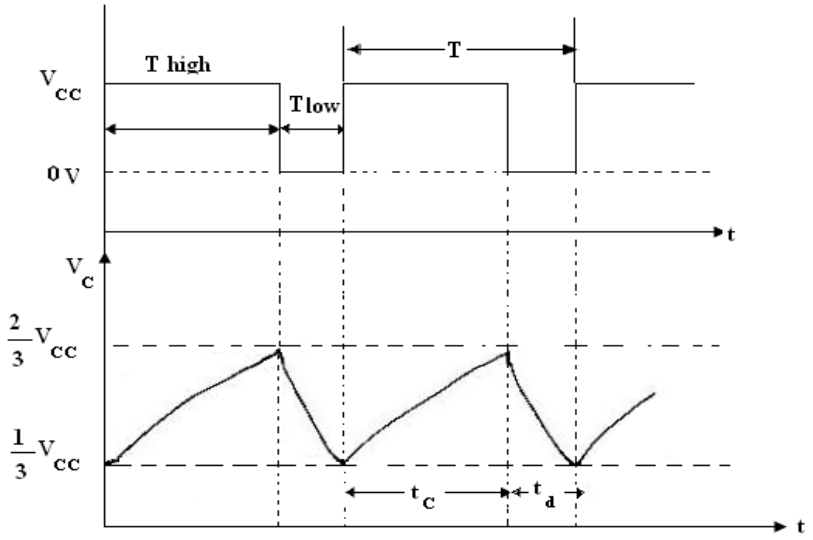
1. It is very simple circuit as it does not need any tank circuit rather than crystal itself.
2. Different oscillation frequencies can be had by simply replacing one crystal with another.
3. The Q-factor, which is a measure of the quality of resonance circuit of a crystal, is very high.
4. Most crystals will maintain frequency drift to within a few cycles at 25^0c.

Q.9 Explain how the timer IC 555 can be operated as an astable multivibrator, using timing diagrams. **(8)**

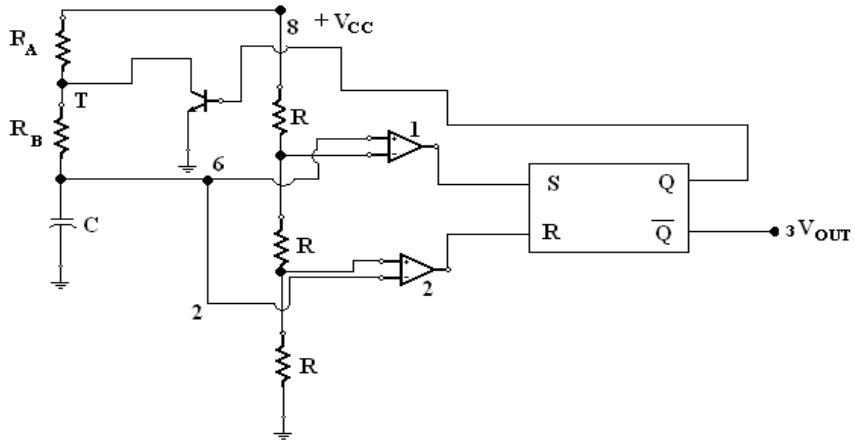
Ans:



The Timer -555 As An Astable Multivibrator



An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave generating circuit. The timing during which the output is either high or low is determined by the externally connected two resistors and a capacitor.

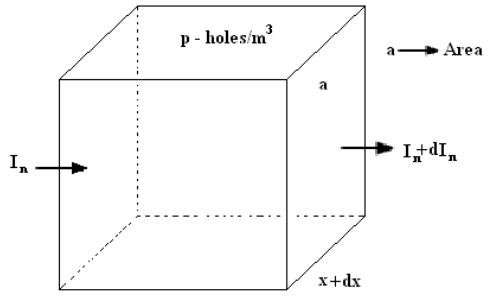


Internal Circuitary With External Connections

When Q is low, or output V_{out} is high, the discharging transistor is cut-off and capacitor C begins charging towards V_{cc} through resistances R_A and R_B. Because of this, the charging time constant is $(R_A + R_B)C$. Eventually, the threshold voltage exceeds + $\frac{2}{3}V_{cc}$, comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin-7 grounds so that the capacitor C discharges through resistance R_B, trigger voltage at inverting input of comparator-2 decreases. When it drops below $\frac{1}{3}V_{cc}$. The output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high.

Q.10 Establish from first principles, the continuity equation, valid for transport of carriers in a semi-conductor. **(10)**

Ans:



The continuity equation states a condition of a dynamic equilibrium for the concentration of mobile carriers in any elementary volume of the semiconductor.

The carrier concentration in the body of semiconductor is a function of both time and distance. The differential equation governing this functional relationship, called the continuity equation, is based upon the fact that charge can be neither created nor destroyed.

Consider an infinitesimal element of volume of area a, and length dx, as shown in fig, within which the average hole is p. If τ_n is the mean lifetime of holes then P/τ_n equals the holes per second lost by recombination per unit volume. If 'e' is the electronic charge, then, because of recombination, the number of coulombs per second decreases within the volume

and decrease within the volume = $e.adx\frac{P}{\tau_n}$ ------(1)

If 'g' is the thermal rate of generation of electron-hole pairs per unit volume, the number of coulombs per second increases within the volume and increase within the

volume = e.a.dx.g ------(2)

In general, the current varies with distance within the semiconductor. If the current entering the volume at x is I_n and leaving at x + dx is $I_n + dI_n$

Decrease within the volume = dI_n. -------(3)

Because of three effects enumerated above, the hole concentration must change with time, and the total number of coulombs per second increases within the volume.

Increase within the volume = $e.a.dx.\frac{dp}{dt}$ ------(4)

Since the charge must be conserved, so

$$eadx.\frac{dp}{dt} = -eadx\frac{p}{\tau_n} + eadxg - dI_n \qquad \text{-------(5)}$$

The hole current I_n is the sum of drift current and diffusion current so,

$$I_n = aEpe\mu_n - aeD_n\frac{dp}{dx} \qquad \text{------(6)}$$

If the semiconductor is in thermal equilibrium with its surroundings and is subjected to no applied fields, the hole density will attain a constant volume P_o.

Under these conditions $I_n = 0 \quad and \quad \frac{dp}{dt} = 0$.

So from the equation (5), we have $g = \frac{p_o}{\tau_n}$ ------(7)

Combining equations (5), (6) and (7) we have the equation of conservation of charge, called the continuity equation,

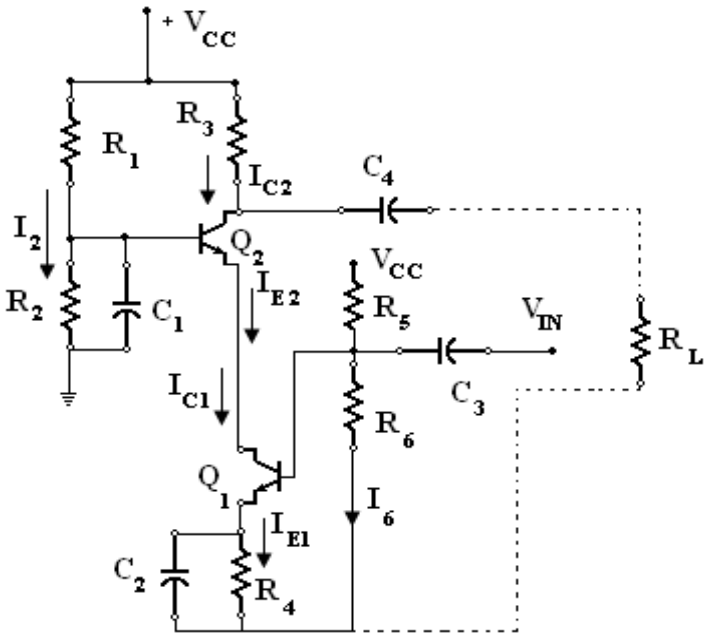
$$\frac{dp}{dt} = -\frac{p - p_o}{\tau_n} + D_n\frac{d^2p}{dx^2} - \mu_n\frac{d(PE)}{dx}$$

Q.11 What are the important characteristics of a cascade amplifier? Write the circuit of cascade amplifier and determine an expression for its voltage gain in terms of its circuit parameters. **(8)**

Ans:

Important characteristics:

1. High input impedance
2. Low voltage gain
3. Input Miller capacitance is at a minimum with the common base stage providing good high frequency operation.



$$A_{v1} = \frac{-h_{fe}}{h_{ie}} \times (Z_{in} \text{ to } Q_2)$$

$$= \frac{-h_{fe}}{h_{ie}} \left[\frac{h_{ie}}{1+h_{fe}} \right] \approx -1.$$

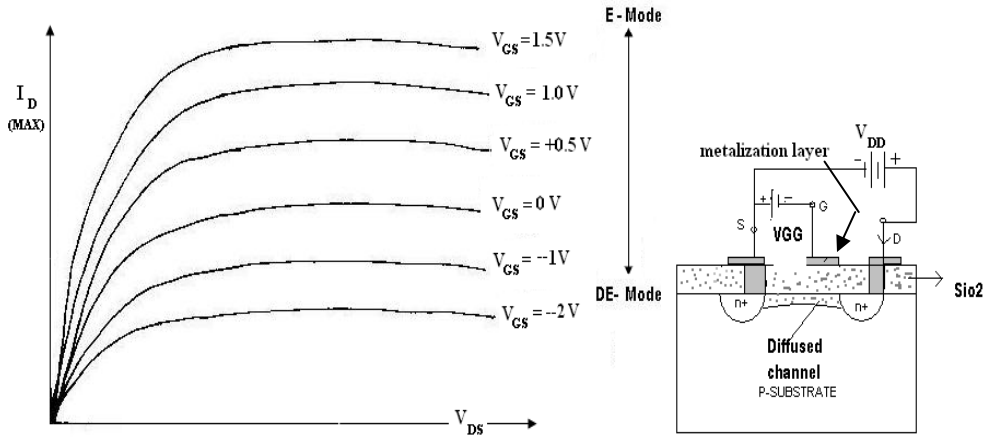
With a stage gain of only 1, no Miller effect occurs at transistor Q_1. Voltage gain of stage-2,

$$A_{v2} = \frac{h_{fb} \times (R_3 \parallel R_h)}{h_{ib}}$$

$\therefore$ Over-all voltage gain, $A_v = \dfrac{-h_{fe} \times (R_3 \parallel R_h)}{h_{ie}}$.

Q.12 Write a neat sketch to shown the construction of a depletion-enhancement MOSFET and explain its operation in both the modes. **(9)**

Ans



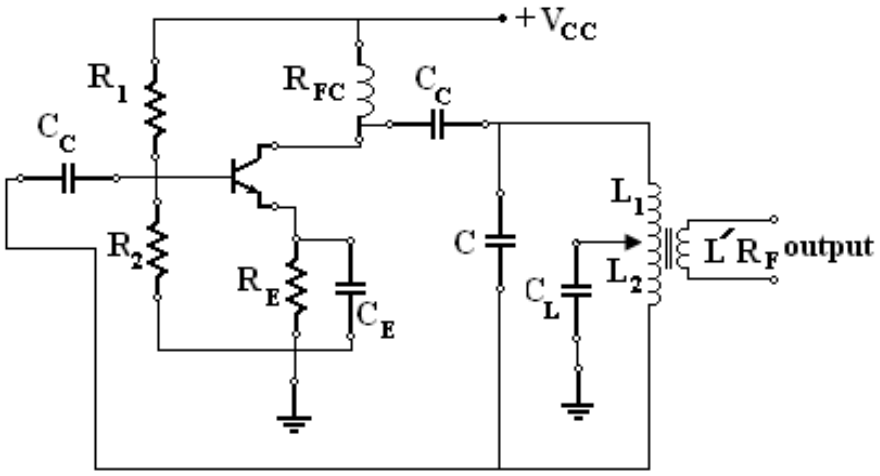
N-channel DE- MOSFET Structure

DE-MOSFET can be operated with either a positive or a negative gate. When gate is positive with respect to the source it operates in the enhancement. When the gate is negative with respect to the source, it operates in depletion-mode.

When the gate is made negative w.r.t the substrate, the gate repels some of the negative charge carriers out-of the N-channel. This creates a depletion region in the channel and therefore, increases the channel resistance and reduces the drain current. The more negative the gate, the less the drain current.

Q.13 Draw the circuit of Hartley oscillator and derive an expression for its frequency of oscillation. **(10)**

Ans:



The Hartley oscillator widely used as a local oscillator in radio receivers.

$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1Z_2(1 + h_{fe}) + Z_2Z_3 = 0$ --------(1)

Here $Z_1 = jwL_1 + jwM$, $Z_2 = jwL_2 + jwM$ and $Z_3 = \frac{1}{jwc} = -\frac{j}{wc}$

Substituting these values in equation (1), we get

$$h_{ie}\left[(jwL_1 + jwM) + (jwL_2 + jwM) - \frac{j}{wc}\right] + (jwL_1 + jwM)(jwL_2 + jwM)(1 + h_{fe}) + (jwL_2 + jwM)\left(-\frac{j}{wc}\right) = 0$$

$$jwh_{ie}\left[L_1 + L_2 + 2M - \frac{1}{w^2c}\right] - w^2(L_2 + M)\left[(L_1 + M)(1 + h_{fe}) - \frac{1}{w^2c}\right] = 0$$

Equating imaginary parts of above equation to zero we get,

While $\left[L_1 + L_2 + 2M - \frac{1}{w^2c}\right] = 0$

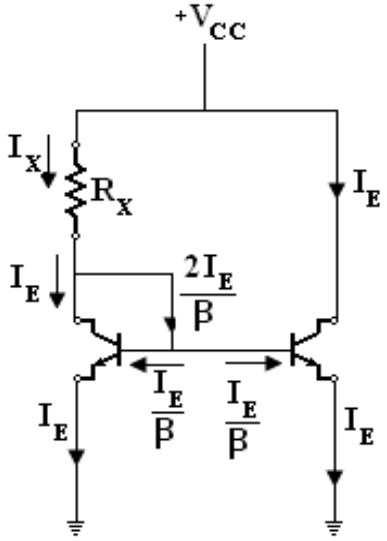
Or $L_1 + L_2 + 2M - \frac{1}{w^2c} = 0 \quad \therefore wh_{ie} \neq 0$

$$w^2c = \frac{1}{L_1 + L_2 + 2M}$$

Or $f = \frac{w}{2\pi} = \frac{1}{2\pi\sqrt{c(L_1 + L_2 + 2M)}}$

Q.14 Write the circuit of current mirror used in a op-amp design and explain its operation. **(8)**

Ans:



Current Mirror Circuit

In the design of op-amps, current strategies are used that are not practical in discrete amplifiers. The new strategies are prompted by the fact that resistors utilize a great deal of 'real-estate', and precise matching of active devices is very practical since they share same piece of silicon. One such approach is the use of the current mirrors to bias differential pairs. The current I_x, set by transistor Q_1 and resistor R_x is mirrored in the current I through the transistor Q_2.

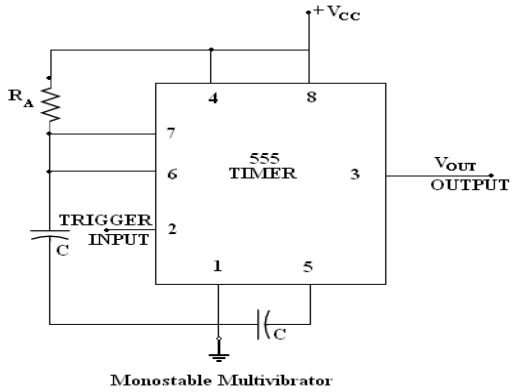
$I_B = \frac{I_E}{\beta+1} \approx \frac{I_E}{\beta}$ and $I_C \approx I_E$.

$\therefore I_X = I_E + \frac{2I_E}{\beta} = \frac{\beta I_E + 2I_E}{\beta} = \frac{(\beta+2)I_E}{\beta} \simeq I_E$

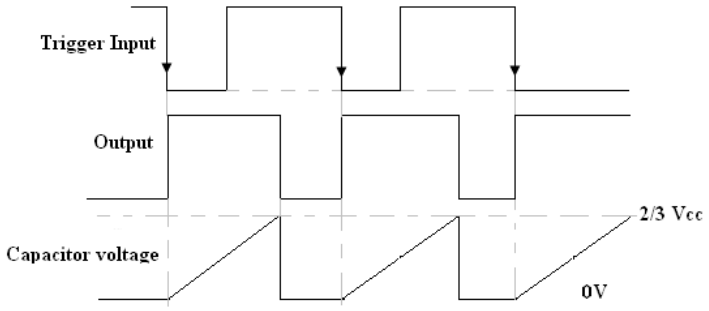
Since $I_X = \frac{V_{cc} - V_{BE}}{R_X}$

Q.15 Explain, using neat circuit diagram and waveforms, the application of timer IC555 as monostable multivibrator. **(9)**

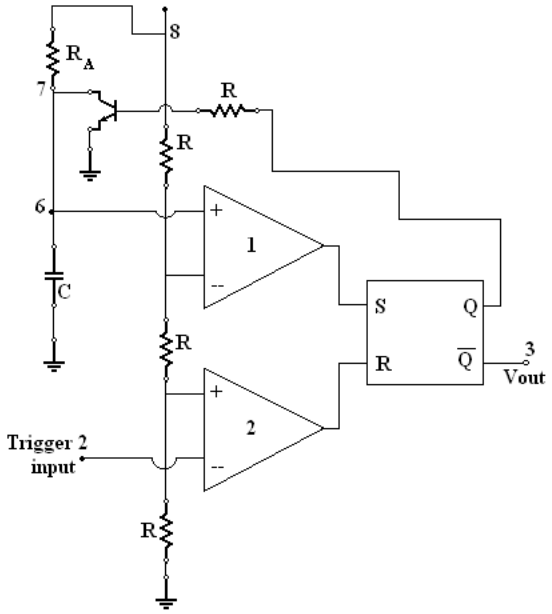
Ans:



Monostable Multivibrator



Trigger Input, Output and Capacitor Voltage Wave Forms



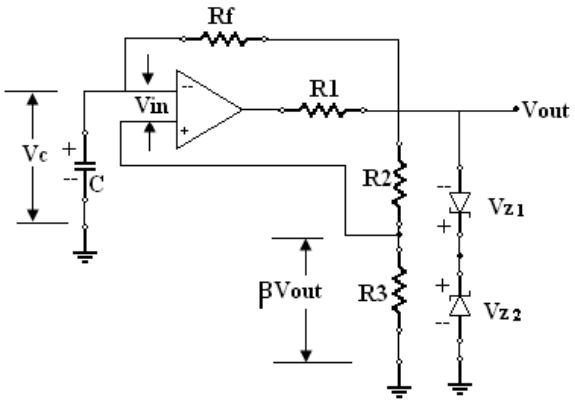
Internal Circuitry with external connections

Operation:

Initially, when the output at pin-3 is low i.e., the circuit is in a stable state, the transistor is on and capacitor C is shorted to ground, when a negative pulse is applied to pin 2, the trigger input false below $\frac{1}{3}V_{cc}$, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and output at pin-3 goes high. As the discharge transistor is cut-off, the capacitor C begins charging towards $+V_{cc}$ through resistance RA with a time constant equal to RAC. When the increasing capacitor voltage becomes slightly greater than $+\frac{2}{3}V_{cc}$, the output of comparator-1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and output of the timer goes low.

Q.16 Write the circuit diagram of a square wave generator using an opamp and explain its operation. **(7)**

Ans:



The circuit's frequency of oscillation is dependable on the charge and discharge of a capacitor C through feedback resistor R_f. The heart of the oscillator is an inverting op-amp comparator.

The comparator uses positive feedback that increases the gain of the amplifier. A fraction of the output is feedback to the non-inverting input terminal. Combination of R_f and C acting as a low-pass R-C-Circuit is used to integrate the output voltage V_{out} and the capacitor voltage V_c is applied to the inverting input terminal in place of external signal.

$V_{in} = V_c - \beta V_{out}$ where $\beta = \dfrac{R_3}{R_2 + R_3}$

When V_{in} is positive, $V_{out} = -V_{z_1}$ and

When V_{in} is negative, $V_{out} = V_{z_2}$.

Q.17 Distinguish between synchronous and asynchronous counters.
Show the logic diagram of a 3-bit UP-DOWN synchronous counter using suitable flip-flops, with parallel, carry based on NAND gates and explain its operation drawing wave diagrams. **(12)**

Ans:

Difference between synchronous and asynchronous counter :

1. In synchronous counters synchronized at the same time. But in the case of asynchronous counter the output of first flip-flop is given as the clock input of the next flip-flop.
2. In synchronous counter the output occurs after nth clock pulse if number of bits are N. But in asynchronous counter the output is derived by previous one that's why n+1 step or clock pulse will be required.

Design of 3 bit UP DOWN counter:-

For M = 0, it acts as an UP counter and for M = 1 as a DOWN counter. The number of flip-flop required is 3. The input of the flip-flops are determined in a manner similar to the following table.

Truth Tables

Direction	**Present State**			**Required FlipFlop**					
M	Q_3	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	0	1	X	0	X	0	X
0	0	0	1	X	1	1	X	0	X
0	0	1	0	1	X	X	0	0	X
0	0	1	1	X	1	X	1	1	X
0	1	0	0	1	X	0	X	X	0
0	1	0	1	X	1	1	X	X	0
0	1	1	0	1	X	X	0	X	0
0	1	1	1	X	1	X	1	X	1
1	0	0	0	1	X	0	X	1	X
1	1	1	1	X	1	1	X	X	0
1	1	1	0	1	X	X	0	X	0
1	1	0	1	X	1	X	1	X	0
1	1	0	0	1	X	0	X	X	1
1	0	1	1	X	1	1	X	0	X
1	0	1	0	1	X	X	0	0	X
1	0	0	1	X	1	X	1	0	X

From truth table

The $J_0 = K_0 = 1$

$J_1 = K_1 = Q_0\overline{M} + \overline{Q_0}M$

$J_2 = K_2 = \overline{M}Q_1Q_0 + M\overline{Q_1}\,\overline{Q_0}$

Connecting the equations of all the flip-flops into NAND realization circuit

$J_1 = K_1 = Q_0\overline{M} + \overline{Q_0}M$

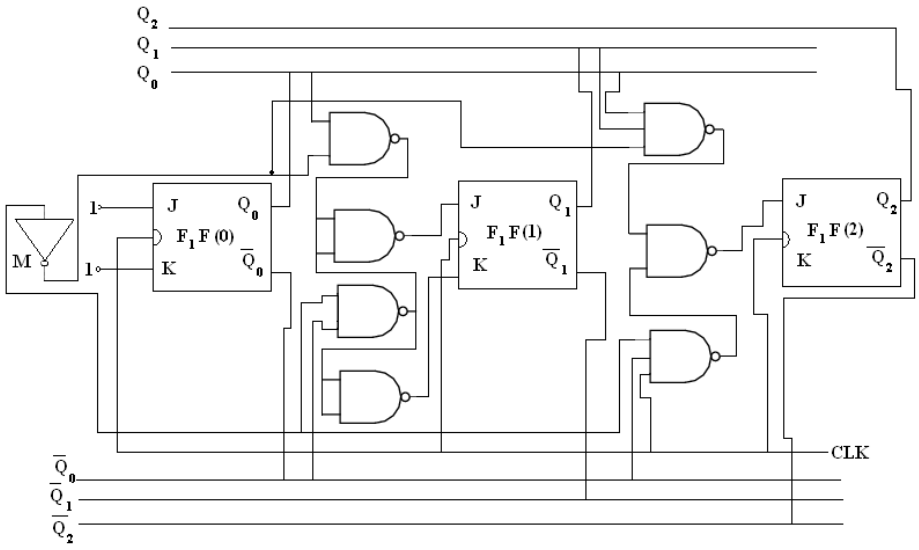
$= \overline{Q_0\overline{M} + \overline{Q_0}M}$

$= \overline{Q_0\overline{M}}.\overline{\overline{Q_0}M}$

$J_2 = K_2 = \overline{M}Q_1Q_0 + M\overline{Q_1}\,\overline{Q_0}$

$= \overline{\overline{M}Q_1Q_0 + M\overline{Q_1}\,\overline{Q_0}}$

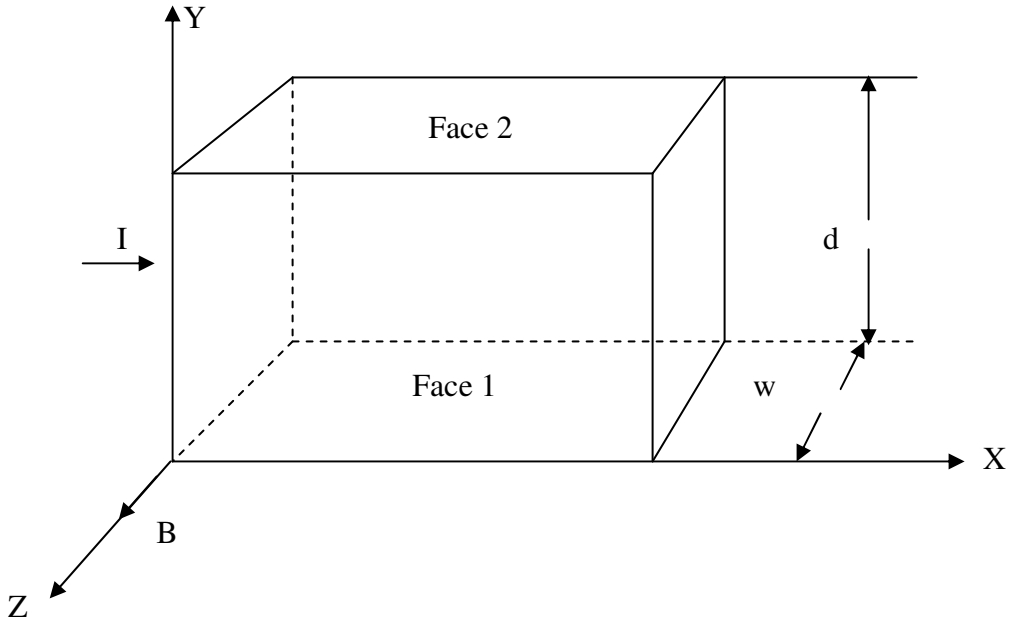
$= \overline{\overline{M}Q_1Q_0}.\overline{M\overline{Q_1}\,\overline{Q_0}}$



Logic diagram of 3 bit UP – DOWN Counter

Q.18 Describe how conductivity and carrier mobility of a sample of semiconductor can be determined by subjecting it to Hall-effect. **(8)**

Ans:



When a specimen (Metal or Semiconductor) is placed in a transverse magnetic field and a direct current is passed through it, then an electric field is induced across its edges in the perpendicular direction of current as well as magnetic field. Thus phenomenon is called the **Hall-Effect**.

A semiconductor bar carrying a current I in the positive X-direction and placed in a magnetic field B acting in the positive Z-direction.

In the equilibrium state the electric field intensity E due to Hall-effect must exert a force on the charge carriers which just balances the magnetic force.

i.e. eE = Bev

where e = Magnitude of charge on electron or hole
and v = Drift-velocity.

Now electric field, $E = \frac{V_H}{d}$ or

$V_H = E.d = B.v.d$

Where d = distance between surfaces 1 and 2.
The current density is given as

$J = \frac{I}{a} = \frac{I}{w.d} = \rho.v$

$\therefore \quad v = \frac{I}{\rho w.d}$

Where ρ is charge density, w = width of specimen.

Now, $V_H = B.d.\frac{I}{\rho wd}$

$V_H = \frac{BI}{\rho w}$

Hall-coefficient R_H is defined by,

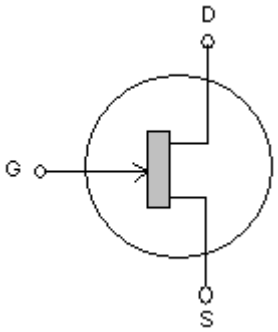
$R_H = \frac{1}{\rho} = \frac{V_H.w}{B.I}$

and conductivity, $\sigma = \rho\mu$

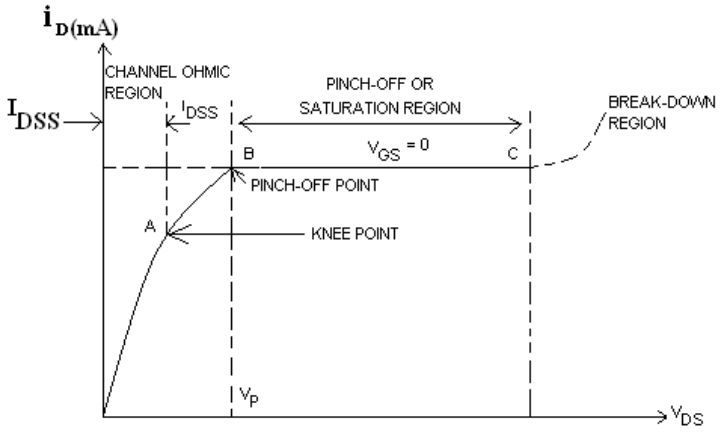
and mobility, $\mu = \sigma.R_H$

Q.19 Draw the symbol and characteristics of an N-channel JFET and mark linear region, saturation region and breakdown region. **(8)**

Ans:



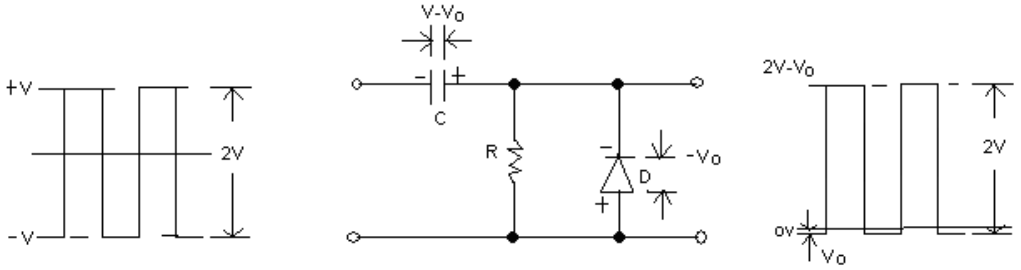
N-Channel JFET



JFET-drain characteristics

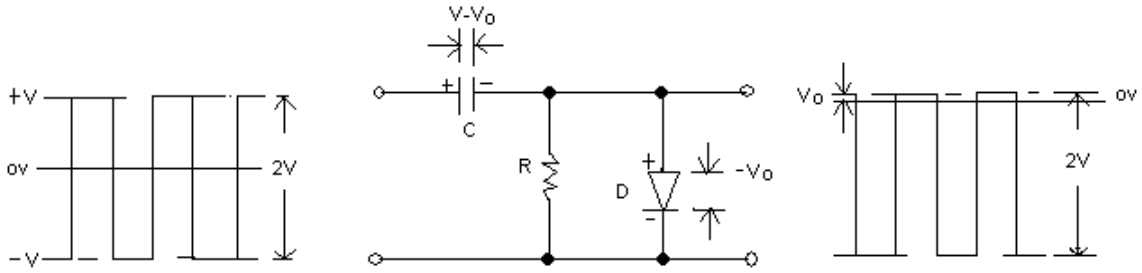
Q.20 Using necessary circuits and waveforms illustrate and explain positive and negative clamping of voltages. **(12)**

Ans:



Input waveform **Positive Clamper** **Output waveform**

The positive clamping circuit shifts the original signal in a vertical upward direction. A positive clamping circuit is shown in above figure. It contains a diode D and a capacitor C.



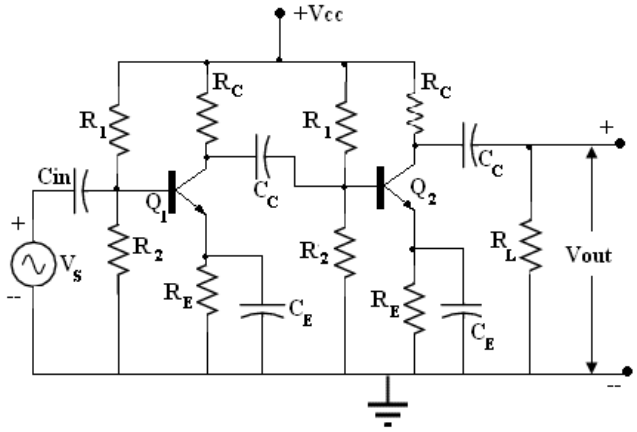
Input waveform **Negative Clamper** **Output waveform**

In negative clamping circuit, with the positive input, the diode D is forward biased and capacitor C charged with the polarity shown. During the positive half-cycle of input, the output voltage is equal to barrier potential of the diode, V_o and the capacitor is charged to $(V - V_o)$. When the input goes negative, the diode is reverse biased and acts as an open-circuit and thus has no effect on the capacitor voltage. R being of very high value cannot discharge C by very much during the –ve portion of input waveform. Thus during negative input, the output voltage being the sum of the input voltage and the capacitor voltage is

equal to $-V - (V - V_o)$ or $-(2V - V_o)$. Thus peak-to-peak output being the difference of the negative and positive peak voltage levels is equal to $V_o - [-(2V - V_o)]$ or $2V$.

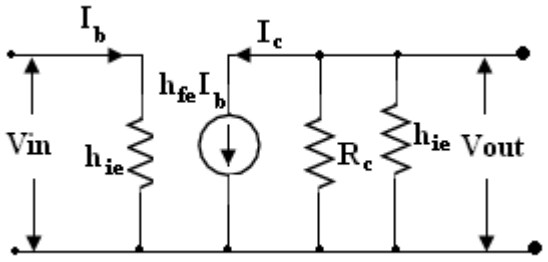
Q.21 Draw the circuit of a RC-coupled amplifier. Explain its behaviour at low, mid and high frequencies by drawing separate equivalent circuit for each frequency region. **(16)**

Ans:



Two stage RC- Coupled Transistor Amplifier

1. Mid Frequency Range

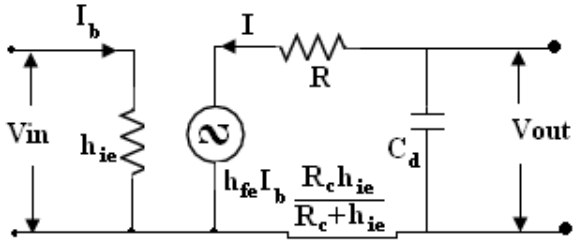


Current, $I = \dfrac{h_{fe} I_b R_c}{R_c + h_{ie}}$

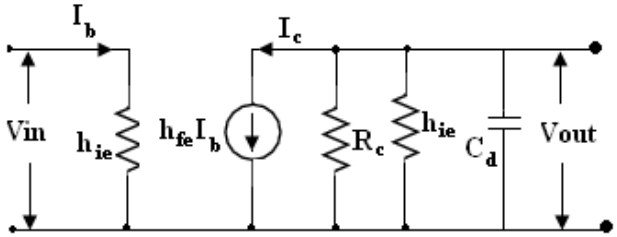
So current gain, $A_{in} = \dfrac{I}{I_b} = \dfrac{h_{fe} I_b R_c}{R_c + h_{ie}}$

$V_{out} = h_{ie}\, I = \dfrac{h_{ie}\, h_{fe} I_b R_c}{R_c + h_{ie}}$

2. High Frequency Range



Thevenin's equivalent circuit



Equivalent circuit for high frequency range

$$I = \frac{h_{fe} I_b \dfrac{R_c h_{ie}}{R_c + h_{ie}}}{\dfrac{R_c h_{ie}}{R_c + h_{ie}} + \dfrac{1}{jwc_d}} = \frac{h_{fe} I_b R_c h_{ie}}{R_c h_{ie} + \dfrac{1}{jwc_d}(R_c + h_{ie})}$$

So current gain, $A_{in} = \dfrac{I}{I_b} = \dfrac{h_{fe} h_{ie} R_c}{h_{ie} R_c + \dfrac{1}{jwc_d}(h_{ie} + R_c)}$

$$V_{out} = \frac{h_{fe} h_{ie} I_b . R_c}{h_{ie} R_c jwc_d + h_{ie} + R_c}$$

$$V_{in} = h_{ie} I_b$$

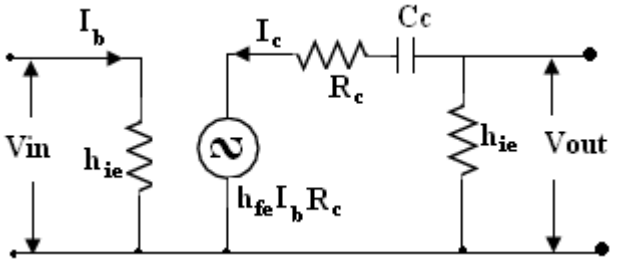
$$A_{in} = \frac{V_{out}}{V_{in}} = \frac{h_{fe} R_c}{h_{ie} R_c jwc_d + h_{ie} + R_c}$$

$$V_{in} = h_{ie} I_b$$

$$A_{v_{in}} = \frac{V_{out}}{V_{in}} = \frac{h_{ie} h_{fe} I_b R_c / (R_c + h_{ie})}{h_{ie} I_b}$$

$$A_{v_{in}} = \frac{h_{fe} R_c}{R_c + h_{ie}}$$

Low frequency range:



Thevenin's Equivalent circuit for low frequency range

$$I = \frac{h_{fe} I_b R_c}{h_{ie} + R_c + j / wC_c}$$

So current gain, $A_{i_i} = \dfrac{I}{I_b} = \dfrac{h_{fe} R_c}{h_{ie} + R_c - j / wC_c}$

Output-voltage, $V_{out} = h_{ie} I = \dfrac{h_{fe} h_{ie} I_b R_c}{h_{ie} + R_c - j/wC_c}$

Input-voltage, $V_{in} = h_{ie} I_b$

So voltage gain $A_{v_l} = \dfrac{V_{out}}{V_{in}}$

$$= \frac{\dfrac{h_{ie} h_{fe} I_b R_c}{h_{ie} + R_c - j/wC_c}}{h_{ie} I_b}$$

$$A_{v_l} = \frac{h_{fe} R_c}{h_{ie} + R_c - j/wC_c}$$

Q.22 Derive mathematical expressions to illustrate the effects of negative feedback (i) to improve gain stabilization (ii) to reduce distortion (iii) to modify input and output impedances. **(8)**

Ans:

Stability:- The variations in temperature, supply voltages, ageing of components or variations in transistor parameters with replacement are some factors that affect the gain of an amplifier and cause it to change

$$A_f = \frac{A}{1+\beta A} = \frac{A}{\beta A} \approx \frac{1}{\beta}$$

The gain is thus independent of internal gain of the amplifier and depends on the passive elements such as resistors.

$A_f = \dfrac{A}{1+\beta A}$ Diff. equation w.r.t. A,

We have $\dfrac{dA_f}{dA} = \dfrac{(1+\beta A) - A.\beta}{(1+\beta A)^2}$

$$= \frac{1}{(1+\beta A)^2} \quad \text{or}$$

$$dA_f = \frac{dA}{(1+\beta A)^2}$$

Or $\dfrac{dA_f}{A_f} = \dfrac{dA}{A} \times \dfrac{(1+\beta A)}{(1+\beta A)^2}$

$$= \frac{1}{(1+\beta A)} . dA/A$$

In negative feedback (1+βA) >> 1, the percentage change in gain with negative feedback is less than the percentage change in gain without feedback. Thus negative feedback improves the gain stability of the amplifier.

Reduction in frequency distortion:

Let the amplifier with open-loop gain A produce a distortion D in the output signal without feedback. Now when feedback is applied, output as well distortion is feedback to the input.

Let the gain with feedback be A_f and distortion in the output D_f. A part βD_f of this distortion is feedback to the input. It gets amplified by factor A and becomes βAD_f.

Net distortion, $D_f = D - \beta A D_f$

$$D_f = \frac{D}{1+\beta A}$$

Thus the distortion is reduced by a factor $(1 + \beta A)$.

Input Impedance:

$$I_{in} = \frac{V_{in}}{Z_{in}} = \frac{V_s - V_f}{Z_{in}} = \frac{V_s - \beta V_{out}}{Z_{in}}$$

$$\frac{V_{s'}}{I_{in}} = Z_{in} + \beta A Z_{in}$$

$$Z_{in_f} = \frac{V_{s'}}{I_{in}} = Z_{in(1+\beta A)}$$

Output impedance:

$$V_{out} = I_{out}.Z_{out} + A V_{in}$$

$$= I_{out} Z_{out} - A.V_f \qquad \therefore V_{in} = -V_f .$$

$$= I_{out} Z_{out} - A.\beta V_{out} \quad \therefore V_f = \beta . V_{out} .$$

Or

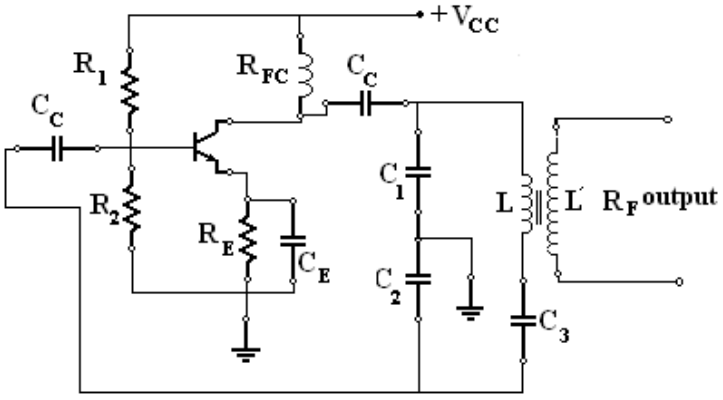
$$V_{out} + A\beta V_{out} = I_{out} Z_{out}$$

$$\therefore \frac{V_{out}}{I_{out}} = \frac{Z_{out}}{1+\beta A} = Z_{out}, f$$

Thus a series voltage negative feedback reduces the output impedance of an amplifier by a factor $(1 + \beta A)$.

Q.23 Write the circuit of **CLAPP** oscillator and explain its operation. What is its distinct advantage over other tuned oscillators? **(7)**

Ans:



As the circulating tank current flows through C1, C2, C3 in series, the equivalent capacitance is

$$C = \frac{1}{1/C_1 + 1/C_2 + 1/C_3} = \frac{C_1C_2C_3}{C_1C_2 + C_2C_3 + C_3C_1}$$

$$f = \frac{1}{2\pi}\sqrt{1/LC_1 + 1/LC_2 + 1/LC_3}$$

In a clapp oscillator C3 is much smaller than C1 and C2. As a result, the equivalent capacitance C is approximately equal to C3, and frequency of oscillation is given as

$$f = \frac{1}{2\pi\sqrt{LC_3}}$$

Advantages:

In a clap - oscillator, the transistor and stray capacitances have no effect on capacitor C3, so the oscillation frequency is more stable and accurate.

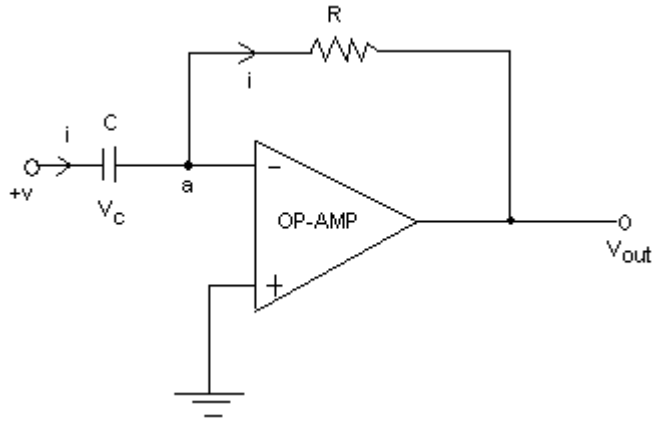
Q.24 Explain how opamp can be used as a

(i) Differentiator (ii) Integrator

(iii) Inverting amplifier (iv) Summer **(9)**

Ans:

(i) Differentiator:



Let i be the rate of change of charge i.e. dq/dt

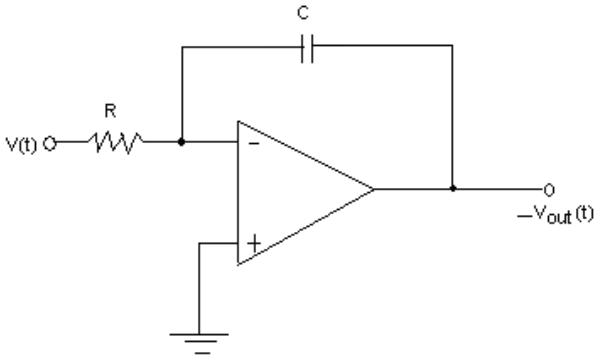
Now charge, $q = CV_c$

$$i = \frac{dq}{dt} = \frac{d}{dt}CV_c = C\frac{dV_c}{dt}$$

$$V_{out} = -iR = -\left[C.\frac{dV_c}{dt}\right]R$$

$$V_{out} = -CR\frac{dV_c}{dt}$$

(ii) Integrator:



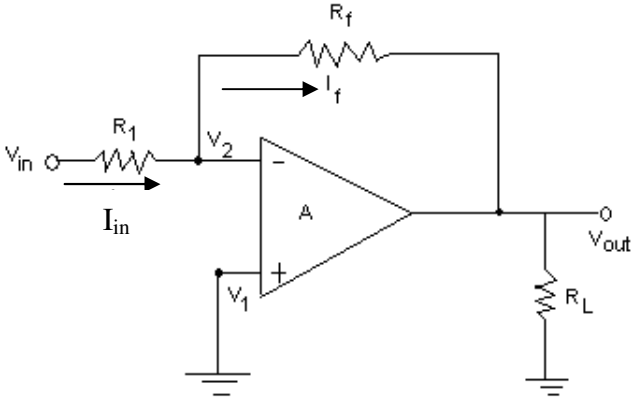
$$i(t) = \frac{V(t)}{R}$$

$$V_{out}(t) = -\frac{1}{c}\int i(t).dt$$

$$V_{out}(t) = -\frac{1}{c}\int \frac{V(t)}{R}.dt$$

$$V_{out}(t) = -\frac{1}{Rc}\int V(t).dt + A$$

(iii) Inverting Amplifier:



$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_{out}}{R_f}$$

$$V_2 = 0$$

$$\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_f}$$

$$A_f = \frac{V_{out}}{V_{in}} = -R_f / R_1$$

(iv) Summer

shows the summer circuit

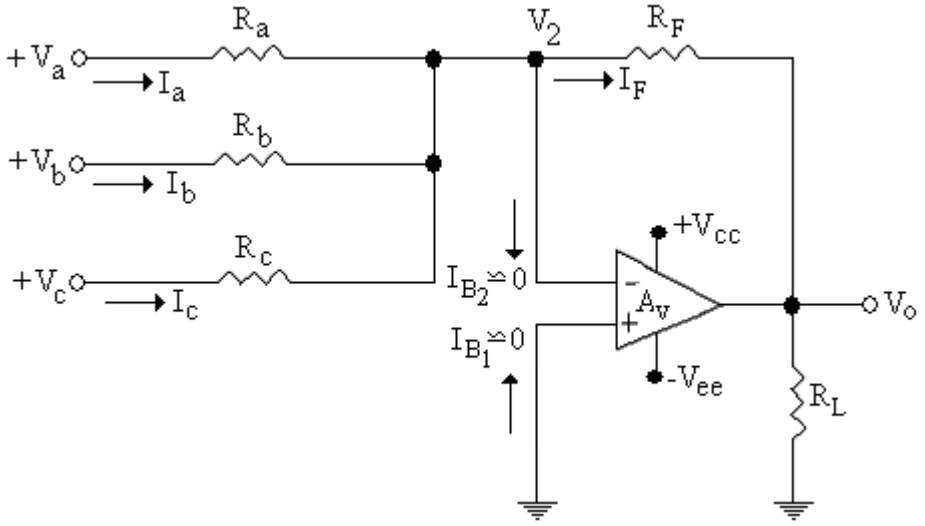
Since R_i and A_v of the opamp are ideally infinity, I_B = zeroAmps and $V_1=V_2=0V$ because of virtual ground.

Therefore, $V_a/R_a + V_b/R_b + V_c/R_c = - (V_o/R_F)$

$Vo = - [(R_F/R_a) V_a + (R_F/R_b)V_b + (R_F/R_c)V_c]$

(v) If $R_a = R_b = R_c = R$ then $V_o = (-R_F/R) [V_a+V_b+V_c]$

i.e., output voltage is equal to the negative sum of all the input times the gain of the circuit R_F/R.



Q.25 Explain the operation of a foldback current-limiting circuit connected to a series voltage regulator, by drawing a neat circuit diagram. **(8)**

Ans:

In a simple current limiting circuit, a large amount of power dissipation in series pass transistor Q_1 while the regulator remains short-circuited. The fold-back current limiting circuit is the solution to this problem.

In this circuit base of transistor Q_3 is based by a voltage divider network consisting of resistor R_6 and R_7.

$$V_{B_3} = \frac{R_7}{R_6 + R_7}\left(I_L R_5 + V_{out}\right) = K\left(I_L R_5 + V_{out}\right) \qquad \text{--------(1)}$$

Where $K = \dfrac{R_7}{R_6 + R_7}$

$$V_{out} + V_{BE_3} = V_{B_3}$$

$$V_{BE_3} = V_{B_3} - V_{out} = K\left(I_L R_5 + V_{out}\right) - V_{out}$$

$$V_{BE_3} = KI_L R_5 + (K-1)V_{out} \qquad \text{---------(2)}$$

Now if load resistance decreases, may be due to any reason, load current I_L will increase causing voltage drop $I_L R_5$ to increase. This causes V_{B_3} to increase and therefore V_{BE_3} to increase. This makes transistor Q_3 – ON in a stronger way. The increased collector current I_{C_3} of transistor Q_3 flows through the resistor R_3 thereby decreasing the base voltage of transistor Q_1. This results in reduction of the conduction level of transistor Q_1. Thus further increase in load current is prevented.

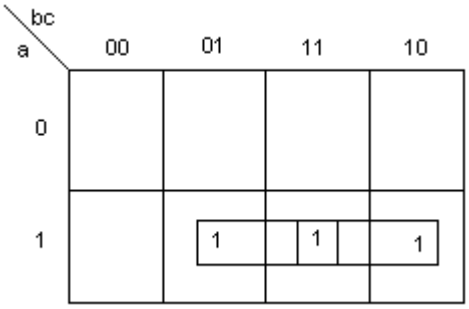
Q.26 Prepare the truth-table for the function

$$f(a, b, c) = ab\bar{c} + abc + a\bar{b}c$$

Minimize the function using K-map. Draw the logic diagram using gates of your choice to realize the minimized function. **(8)**

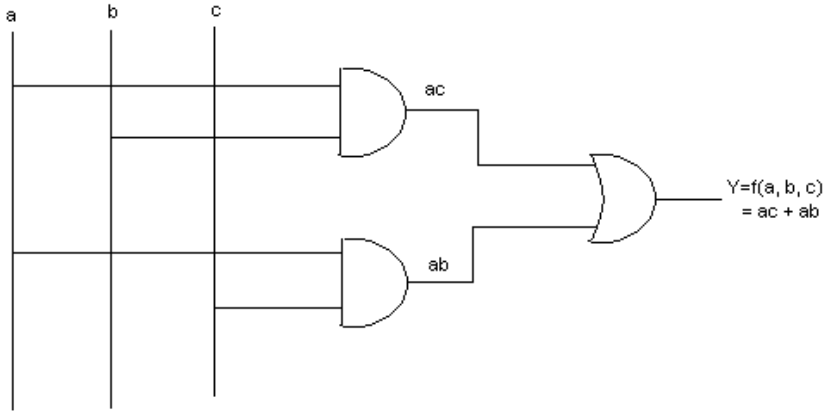
Ans:

The function is f(a, b, c) = $ab\bar{c} + abc + a\bar{b}c$



f(a, b, c) = ac + ab

Logic realization:-



Q.27 Define mobility in a semiconductor. Does it also depend on doping levels? **(3)**

Ans:

In the presence of electric field in a semiconductor, the electrons move with an average velocity called drift velocity. Mobility is the ratio of drift velocity and electric field.

The drift velocity is given by $v_d = \mu E$ where

E=Electric field

μ=constant called "mobility" of the charge carrier.

Yes, the mobility depends on the doping levels.

Q.28 What is the quantity of mobility for electrons and for holes in a silicon semiconductor? **(2)**

Ans:

The typical value of mobility of electrons in a silicon semiconductor is $0.13 m^2/V\text{-}s$ and that of holes is $0.046 m^2/V\text{-}s$.

Q.29 A semiconductor has donor and acceptor concentrations of N_D and N_A, respectively. What relationship must be used to determine the electron n and hole p concentrations in terms of intrinsic concentration n_i? **(2)**

Ans:

We know that $np = n_i^2$

For n type semiconductors: $n \approx N_D$

$\therefore \quad p = (n_i)^2 / N_D$

For p type semiconductors: $p \approx N_A$

$\therefore \quad n = (n_i)^2 / N_A$

Q.30 What do you understand by 'cut-in' voltage of a diode? **(4)**

Ans:

The cut in voltage is the voltage across the diode below which current is very small(less than 1% of rated current) in the forward biased condition only.

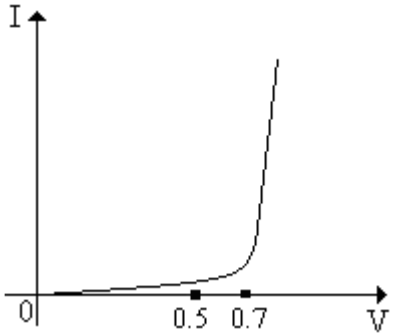


Fig. 3(i)

The above figure shows the V-I characteristics of diode in the forward biased region. The current is negligibly small for V smaller than about 0.5V. This value is usually referred to as cut in voltage.

Q.31 Sketch the volt-ampere characteristics of zener diode. Indicate the knee on the curve and explain its significance. What happens when the current in zener decreases below the knee current? **(10)**

Ans:

In the normal applications of zener diode, cathode is made positive with respect to the anode. From the characteristics shown in fig 3 (ii), we see that for currents greater than the knee current (I_{zk}), the V-I characteristic is almost a straight line. The zener voltage V_z is specified at nominal current I_{zt}. As the current through the zener deviates from I_{zt}, voltage across changes only slightly.

The current change ΔI is related to zener voltage change ΔV by

$\Delta V = r_z \Delta I$ where r_z = inverse of the slope of V-I curve at point Q.

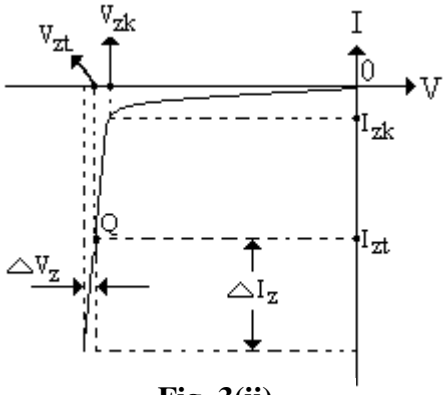
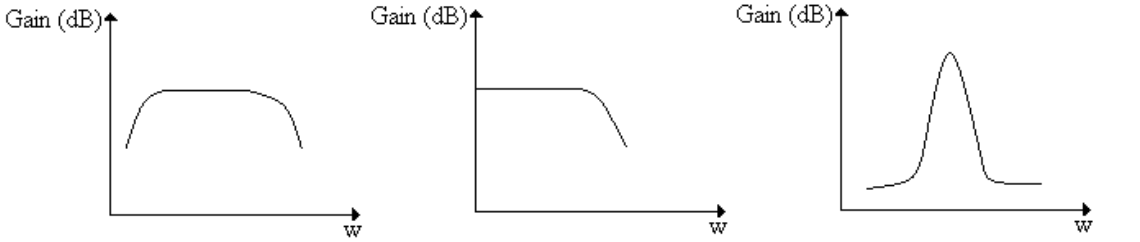


Fig. 3(ii)

Resistance r_z is called dynamic resistance or incremental resistance of the zener diode at operating point Q. Lower the value of r_z, more constant is the zener voltage as the current varies. From the V- I characteristics, it can be seen that r_z remains low and almost constant over a wide range of current. When the magnitude of 'I' decreases below I_{zk}, the zener ceases to operate as a voltage regulator. Because small variations in current gives rise to large voltage variations.

Q.32 Classify the amplifiers based on frequency response. **(6)**

Ans:



(i) Wide band **(ii) Direct coupled** **(iii) Tuned amplifier**

(i) **Wide band amplifier**: The gain remains constant over wide frequency range, but falls off at low and high frequencies as shown in the above Fig **(i) .**These are also called R-C coupled or capacitively coupled amplifiers.

(ii) **Direct coupled amplifier**: It is also called as dc amplifier. The amplifier maintains its gain at low frequencies as well as for dc signal as shown in Fig **(ii).**

(iii)**Tuned amplifier**: The gain peaks around certain frequency say ω_0 and falls off drastically on both sides of this frequency. This is shown in Fig **(iii).**

Q.33 The low frequency response of an amplifier is characterized by the transfer Function $F_L(s) = s(s+10) / [(s+100)(s+25)]$. Represent its 3dB frequency graphically. **(8)**

Ans:

$F_L(s) = ((s+\omega_{z1})(s+\omega_{z2})\ldots\ldots) / ((s+\omega_{p1})(s+\omega_{p2})\ldots\ldots)$

ω_{p1} and $\omega_{p2}\ldots..$ represent poles.

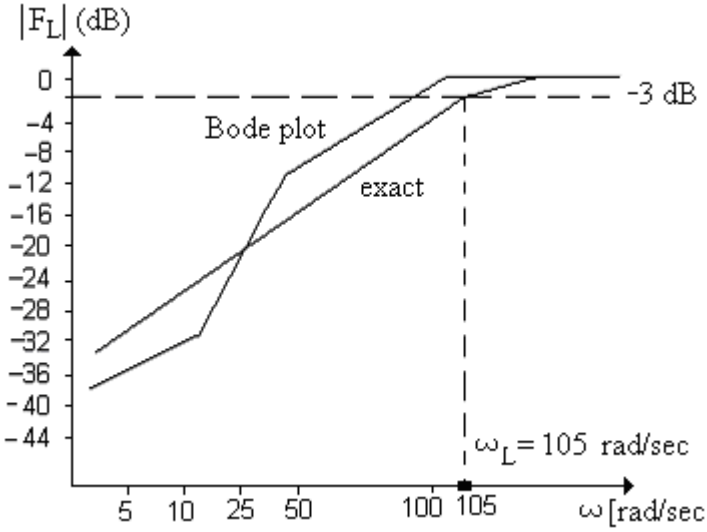
ω_{z1} and $\omega_{z2}\ldots..$ represent zeros.

In many cases zeros have lower frequency much smaller than ω_L. Also one of the poles will have much higher frequency than all the other poles.

Therefore $F_L(s) \cong s / (s+\omega_{p1})$, where ω_{p1} = the largest value pole.

In this case, low frequency response of amplifier is dominated by the pole at $s = -\omega_{p1}$ and lower 3dB frequency is approximately = ω_{p1}

i.e., $\omega_L \approx \omega_{p1}$



This is called as dominant pole approximation. This approximation can be made if highest frequency pole is separated from the nearest pole or zero by at least 2 octaves (i.e., factor of 4). If dominant low frequency pole does not exist, then

$$\omega_L = \sqrt{(\omega_{p1}^2+\omega_{p2}^2-2\omega_{z1}^2-\omega_{z2}^2)}$$

If $F_L(s) = (s\,(s+10)) / ((s+100)\,(s+25))$

ω_{p1}=100rad/sec is 2 octaves higher than 2nd pole and a decade higher than 0.

Hence, $\omega_L = \omega_{p1} = 100$ rad/sec

Or $\omega_L = \left(\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{p1}\right)^{1/2}$

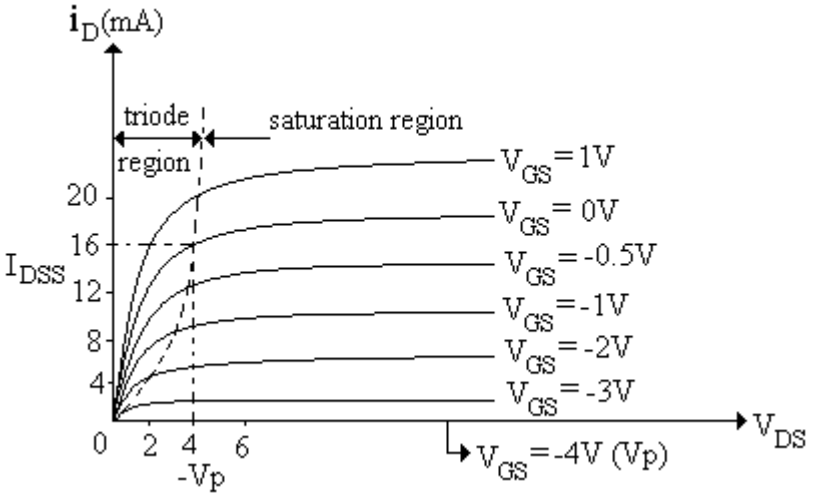
$$\omega_L = \sqrt{\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{p1}}$$

$$= \sqrt{(100^2 + 25^2 - 2\times 10^2} = 102 \text{ rad/sec}$$

Q.34 Draw the characteristics of an n channel JFET. Enunciate the linear relationship that represents the i_p- V_s characteristics near the origin. **(8)**

Ans:

The figure below shows a family of I_D v/s V_{DS} characteristics of an n channel JFET for various values of V_{GS}. For small values of V_{DS} (below pinch-off), the depletion region of the gate would not be affected much by the flow of drain current I_D from one end of the gate to the other end of the gate. This is true for a given value of $V_{GS.}$ As such, a linear relationship exists between I_D and V_{DS} and the JFET behaves like a voltage-controlled resistor.



Q.35 Why are the characteristics of an n channel JFET, called static? **(2)**

Ans:
The characteristics shown in answer to Q 34 are valid for dc conditions. Hence they are called static characteristics.

Q.36 Write the equation, which represents the boundary between the triode region and pinch off region? **(4)**

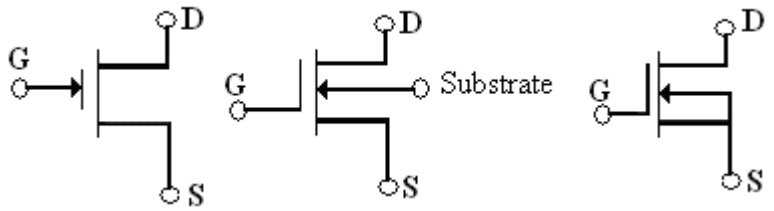
Ans:
The JFET operates in the triode region for

$$V_{ds} > V_{gs} - V_p$$

Where V_{ds} = drain to source voltage
V_{gs} = gate to source voltage
V_p = pinch off voltage

Q.37 Give the simplified circuit symbol for the depletion type n-channel MOSFET. **(2)**

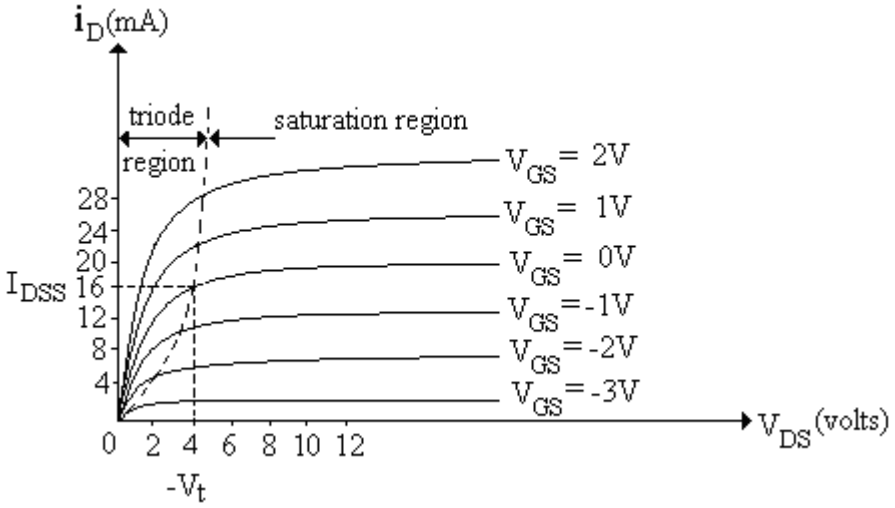
Ans:



Q.38 With the help of i_D-V_{DS} characteristic curve for small values of V_{DS} explain the physical operation of depletion type MOSFET (assume I_{DSS}=16mA, V_P=-4V for the device) **(12)**

Ans:
The depletion type n-channel MOSFET has originally n-type channel region. If a voltage V_{DS} is applied between drain and source, a current i_D flows even for V_{GS}=0. Applying positive

V_{GS} enhances the conductivity of the channel by attracting more electrons into it (Enhancement mode). Applying negative V_{GS} causes electrons to be repelled from the channel resulting in lower conductivity and therefore is called depletion mode operation.
The depletion MOSFET can be operated in 3 distinct regions: Cut off, triode and saturation region. FET used as an amplifier should be operated in saturation region. For operation as a switch, cut off and triode regions are used.



For a depletion type n channel MOSFET, threshold voltage V_t is negative. The MOSFET will operate in triode region as long as drain voltage does not exceed the gate voltage by more than $|V_t|$. For it to operate in saturation, the drain voltage must be greater than the gate voltage by at least $|V_t|$ volts. The device is cut off when $|V_{GS}| < |V_t|$. In saturation region the MOSFET provides a drain current whose value is independent of drain voltage V_{DS} and is determined by gate voltage only. When V_{GS}=0, application of positive V_{DS} produces an appreciable drain current I_{DSS}. As V_{GS} decreases towards threshold, the drain current decreases. At fixed V_{GS}, increasing values of V_{DS} cause the drain current to saturate as the channel becomes pinched off.

Q.39 What is Hall effect in a semiconductor? How the Hall Effect can be used to determine some of the properties of a semiconductor? **(7)**

Ans:
If a specimen of semiconductor carrying a current(I) is placed in a transverse magnetic field (B) then an electric field is induced in a direction perpendicular to both I and B. This phenomenon is known as Hall Effect.
Hall effect is used to measure carrier concentration and mobility. Consider an N type semiconductor carrying current (I) placed in a transverse magnetic field (B) in the direction as shown in the Fig.
Due to forces exerted on the electron by electric and magnetic field, a Hall voltage (V_H) is induced as shown. In order to obtain equilibrium state,

$$F(\text{electric}) + F(\text{magnetic}) = 0$$
$$n.q.E + B.J = 0$$

i.e $E = -BJ/n.q$

where J = current density
n = electron concentration
q = electronic charge

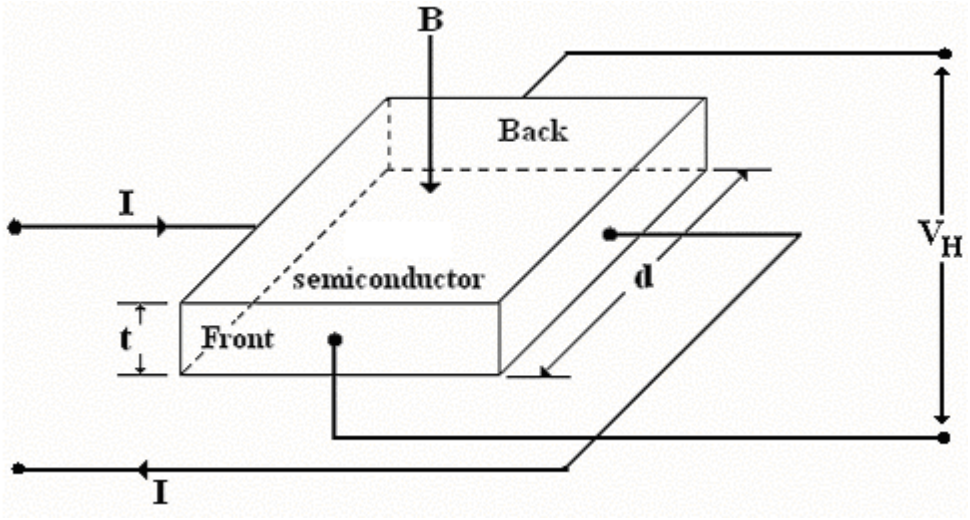


Fig.

The Hall co-efficient R_H is given by $R_H = 1/n.q$

$E = + B.J. R_H$

But $E = V_H / d$

where V_H = Hall voltage

d = distance between front and back surface

Also $J = I/A = I/d.t$

where t = thickness of the semiconductor.

$V_H /d = B (I / d t)^* (1 / n q)$

$V_H = BI / n.q.t$ or $n = BI / q tV_H$

n = density of electrons.

Conductivity of an extrinsic semiconductor is given by

$\sigma = n.q.\mu_n$ Where μ_n = electron mobility &

Or $\sigma = p.q.\mu_p$ μ_p = Hole mobility

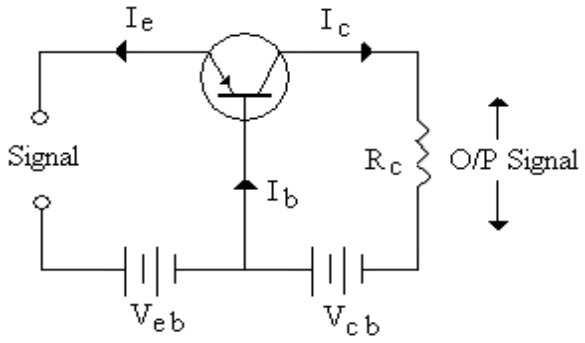
Therefore $\mu_n = \sigma/nq = \sigma R_H$

Q.40 Draw the circuits of the various transistor configurations. Why common emitter configuration is mostly used? Give its typical uses. **(7)**

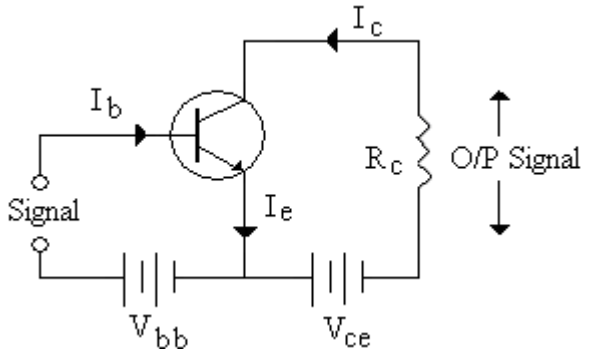
Ans:

A transistor can be connected in a circuit in the following three configurations.

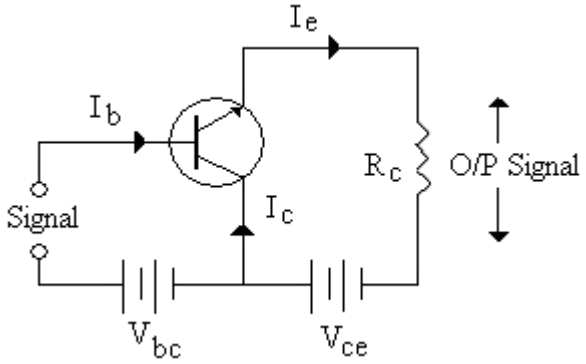
1. Common base configuration



2. Common emitter configuration



3. Common collector configuration



The reasons for wide use of CE configuration are

(i) **High current gain**: In CE configuration I_C is output current and I_B is the input current. Collector current is given by $I_C = ß\ I_B$. As the value of ß is very large output current I_C is much more than the input current I_B. The value of ß is ordinarily high and ranges from 10 to 500.

(ii) **High voltage and power gain**: Due to high current gain the CE configuration has the highest voltage and power gain of the three transistor configurations.

(iii) **Moderate output to input impedance ratio**: In the CE configuration the ratio of output impedance to input impedance is small. Therefore this configuration is ideal for coupling between various transistor stages. CE configuration is used for small signal and power amplifier applications.

Q.41 What is transistor biasing? What are the basic conditions which are to be necessarily fulfilled for achieving faithful amplification of input signal in transistor amplifiers? **(7)**

Ans:

Fixing the d.c values of current and voltages of transistor under quiescent or no signal condition is biasing. The quiescent point should lie in the central area of an active, linear region of the transistor.

The basic purpose of transistor biasing is to keep the base emitter junction properly forward biased and collector base junction properly reverse biased.

The basic conditions required for achieving faithful amplification of input signal in transistor amplifiers are:

1) Proper zero signal collector current: The value of zero signal current should be at least equal to the maximum collector current when the signal is present.

2) Proper minimum base emitter voltage: To achieve faithful amplification the base emitter voltage (V_{BE}) should not fall below 0.5V for germanium and 0.7V for silicon transistors at any instant.

Q.42 What are the advantages of the FET over a conventional bipolar junction transistor? Define pinch off voltage, transconductance, amplification factor and drain resistance of a FET. Explain with the help of circuit diagram how an FET is used as a voltage amplifier and as voltage dependent resistor (VDR). **(14)**

Ans:

FET is a majority carrier device. FET is a voltage controlled current source. An important advantage of the FET is that it is simpler to fabricate and occupies less space on a chip than does a BJT. FET has a negative temperature co-efficient at high current levels, which prevents FET from thermal break down. FET has high switching speed and cut off frequency.

Pinch off Voltage:

It is the voltage at which the drain current reaches the maximum value and beyond which drain current becomes constant.

Transconductance (g_m):

It is the ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain to source voltage V_{DS}. i.e.,

$g_m = \Delta I_D / \Delta V_{GS} \big| V_{DS}$ constant.

Amplification factor (μ):

It is the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a small constant drain current I_D. i.e.,

$\mu = \Delta V_{DS} / \Delta V_{GS}$ at constant I_D.

Drain resistance:

This may be DC or AC. DC or static drain resistance is the ratio of V_{DS} to I_D.

i.e $R_{DS} = V_{DS} / I_D$

A.C or dynamic drain resistance is the resistance between the drain and source when FET is operating in pinch off or saturation region.

$r_d = \Delta V_{DS} / \Delta I_D$

FET as an amplifier is shown in Fig.9 i.

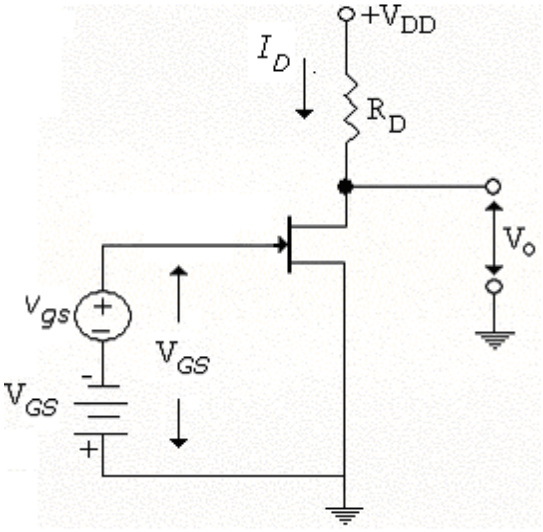


Fig:9 (i)

An enhancement n-channel MOSFET is biased with a battery V_{GS}. A time varying signal v_{gs} which is to be amplified is superimposed on gate to source dc bias V_{GS}. Thus the total instantaneous gate voltage is

$$v_{GS} = V_{GS} + v_{gs}$$

The operating point can be got by intersection of load line and I_D versus V_{DS} curve corresponding to instantaneous values of v_{GS}.

When a sinusoidal signal v_{GS} is applied the instantaneous operating point will move along the load line in correspondence with total instantaneous voltage v_{GS}. The output signal is an amplified replica of the input signal. Linear amplification can be obtained by properly choosing the dc bias point Q and by keeping the input signal amplified.

FET as voltage dependent resistor:

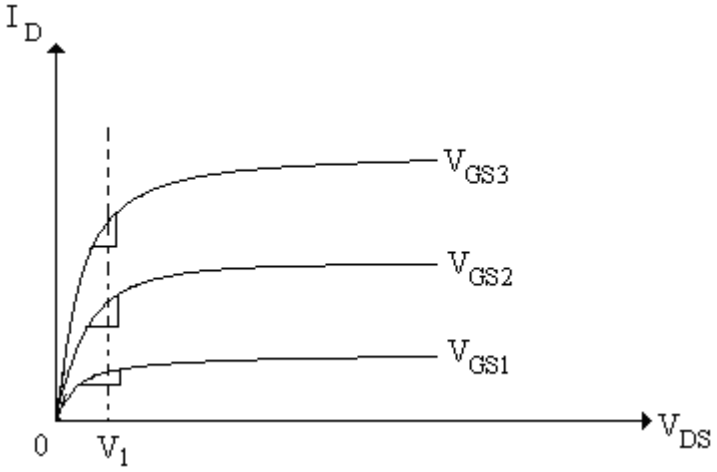


FIG: 9 (ii)

Figure 9 (ii) shows the output characteristics of an FET. It shows the variations of I_D with V_{DS} for constant V_{GS}.

If we consider the slope of the curve for low values of V_{DS}, we see that the slope varies with variations in V_{GS}. As the slope is related to the resistance, we can say that the resistance would be different for different values of V_{GS}.

Hence for a given $V_{DS} = V_1$, the resistance depends on gate voltage and thus it is seen that FET acts as voltage dependent resistor.

Q.43 What is a tuned amplifier? What is the fundamental difference between audio amplifiers and tuned amplifiers? How is bandwidth related to resonant frequency (f_r) and the quality factor (Q). **(7)**

Ans:

Tuned amplifiers are the ones, which amplify a specific frequency or a narrow band of frequencies. Audio amplifiers provide the constant gain over a wide band of frequencies. Tuned amplifiers are designed to have specific, usually narrow bandwidth. This is shown in **Fig. 10 (a)**. BW_A is the bandwidth of response of a typical audio amplifier, while BW_T is the bandwidth of tuned amplifier and f_r is called the center frequency of tuned amplifier.

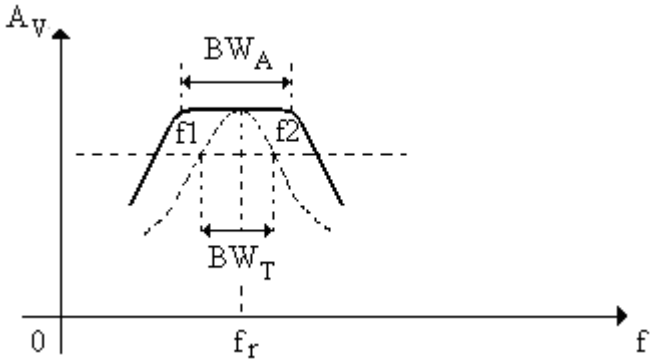


Fig. 10(a)

The quality factor Q of a tuned amplifier is equal to the ratio of center frequency (f_r) to bandwidth (BW_T) i.e

$Q = f_r/BW_T$

Q is determined by the circuit component values. For a parallel resonance circuit is given by $f_r = 1/ (2\pi\sqrt{LC})$ and $Q = X_L / R$ where X_L is the reactance of the inductor having resistance R.

Q.44 Discuss the terminal properties of an ideal operational amplifier. **(7)**

Ans:

The **Fig. 11(a)** shows the schematic of an ideal op-amp. The following are the important properties of an ideal op-amp.

i) The input impedance of an ideal op-amp is infinite. Hence it draws no current at both the input terminals.

ii)The gain of an ideal op-amp is infinite (∞), hence the differential input $V_d = V_1 - V_2$ is zero for the finite output voltage V_0.

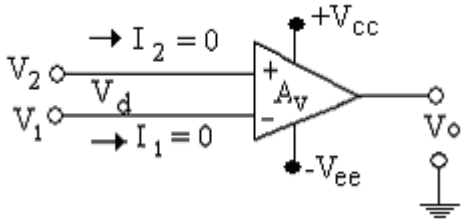


Fig. 11(a)

iii) The output voltage V_0 is independent of the current drawn from the output terminal. Thus its output impedance is zero.

This results in the following Characteristic of an ideal op-amp.

a) Infinite Voltage gain: It is denoted as A_{OL}. It is the differential open loop gain.
b) Infinite input impedance: It is denoted as R_{in} and ensures that no current flows into an ideal op-amp.
c) Zero output impedance: It is denoted as R_o and ensures that the output voltage of the op-amp remains the same, irrespective of the load.
d) Zero offset voltage: This ensures zero output for zero input signal voltage in an ideal op-amp.
e) Infinite bandwidth: This ensures that the gain of the op-amp will be constant over the frequency range from d.c to infinite.

f) Infinite CMRR: This ensures zero common mode gain for an ideal op-amp. Due to this common mode noise output voltage is zero.
g) Infinite slew rate: This ensures that the changes in the o/p voltage occur simultaneously with the changes in the input voltage.

Q.45 What is an ideal diode? Sketch the characteristics of an ideal diode. **(7)**

Ans:
An ideal diode may be defined as a two terminal device which
a. Conducts with $R_f = 0$, when forward biased
b. $R_r = \infty$, when reverse biased
In other words, an ideal diode acts as a short circuit in the forward direction and as an open circuit in the reverse direction. An ideal diode behaves like a switch which is closed in the forward direction and open in the reverse direction.
VI characteristics of an ideal diode:
The **VI** characteristics of an ideal diode are shown in Fig. 12a. The part of the characteristics in forward biased condition coincides with the i_D axis, and the part for reverse condition coincides with the V_D axis as shown by the dark lines.

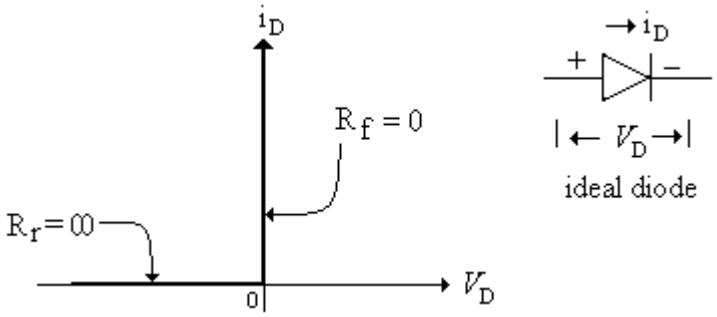


Fig.12a

Q.46 Describe the construction and operation of JFET. How does it differ from a MOSFET? Draw the equivalent circuit of a JFET and explain how do we bias for operation as an amplifier. **(7)**

Ans:
The basic structure of an n-channel JFET is as shown in Fig.14a(i). The drain and source terminals are made by ohmic contacts at the ends of n-type semiconductor bar. Gate is formed by electrically connecting two shallow p+ regions. The n-type region between two p+ gates is called the channel through which majority carriers flow between the source and the drain.
Operation:
Gate regions and channel constitute pn junction. In normal operating mode, this pn junction is maintained in reverse biased state. Gate to source voltage is negative and drain to source voltage is positive. This reverse biases the junction, and hence the depletion region exists. The depletion region contains immobile charges.

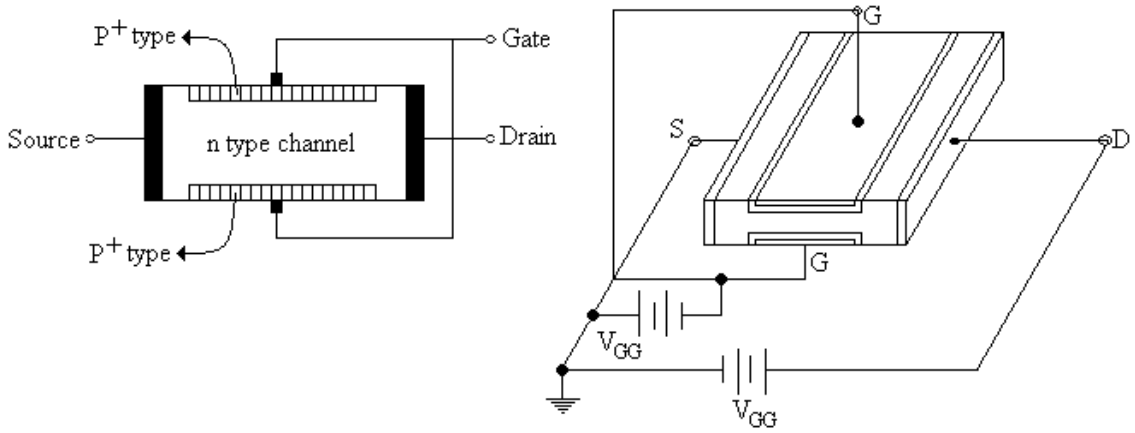


Fig.14a(i)

Also, depletion region extends more into region of lower doping. Since gate region is heavily doped than the channel region, depletion region penetrates more deeply into the channel. The conductivity of this region is nominally zero because of unavailability of charge carriers. Therefore, as reverse bias increases, the effective width of the channel decreases. At specific value of gate to source voltage (V_{GS}) the channel width becomes zero because all the free charges have been removed from the channel. This voltage is called pinch off voltage (V_p). Therefore, for a fixed drain to source voltage, the drain current will be a function of reverse bias voltage across the gate junction.

In a MOSFET metal gate electrode is separated by an oxide layer from the semiconductor channel.

FET as an amplifier: Fig.14a(ii) shows a Common Source (CS) configuration. The signal to be amplified is V_1. V_{GG} provides the necessary reverse bias between gate and source of JFET. This is the biasing arrangement for the operation of JFET as an amplifier.

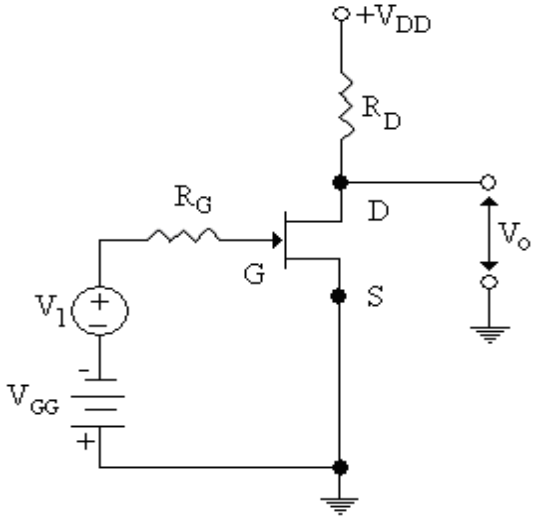


Fig.14a(ii)

Low frequency small signal equivalent circuit of JFET

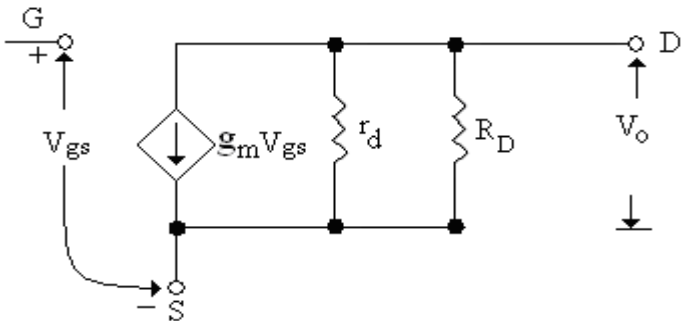


Fig.14a(iii)

Q.47 Draw the circuit diagram of a collector tuned amplifier and derive the expression for the voltage gain at the tuned frequency. **(7)**

Ans:

The collector tuned circuit is shown in Fig.16a (i)

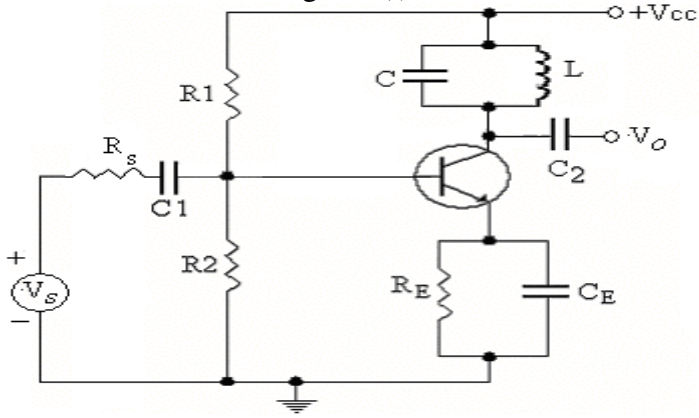


Fig.16a(i)

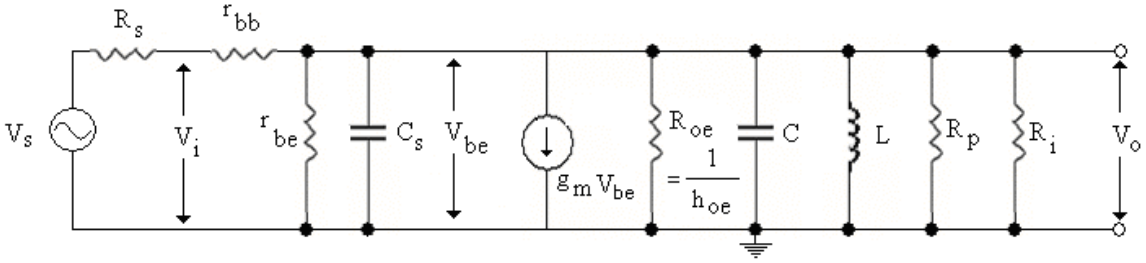


Fig.16a(ii)

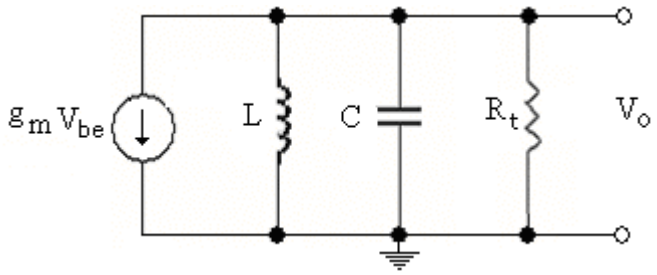


Fig.16a(iii)

The equivalent circuit of the amplifier is shown in Fig.16a(ii),
$R_t = R_o \parallel R_p \parallel R_i$
where R_0 = output resistance of current generator $g_m V_{be}$ and is equal to $(1/h_{oe})$
R_i = input resistance of next stage
R_p = equivalent internal resistance of L calculated when series L circuit is represented by its equivalent parallel circuit.
Voltage Gain $A_V = V_o/V_i$
From Fig.16a(iii) output voltage can be given as
$Vo = -g_m V_{be} Z$
where Z = impedance of C, L and R_t in parallel or,
$Z = R_t/(1+2jQ_{eff}\delta)$
$Q_{eff} = R_t/\omega_r L$
and ω_r = resonant frequency
and δ = fractional variation in resonant frequency = $(\omega-\omega_r) / \omega_r$
At resonant frequency $\omega = \omega_r$ and $\delta = 0$.
Z (at resonance) = R_t
Fig.16a(iii)shows the final equivalent circuit of Fig.16a(ii).
Hence $V_o = -g_m V_{be} R_t$ at resonance
Also $V_{be} = V_i(r_{be}/(r_{bb}+r_{be}))$ (from Fig.16a(ii) neglecting C_s)
$V_o = -g_m V_i(r_{be}Z / (r_{bb}+r_{be}))$
$A_V = V_o/V_i = -g_m V_i(r_{be}Z/(r_{bb}+r_{be}))$
$= -g_m(r_{be}/(r_{bb}+r_{be})) \times (R_t/(1+2jQ_{eff}\delta))$
At resonance, voltage gain is
$A_V = -g_m(r_{be}/(r_{bb}+r_{be})) \times R_t$

Q.48 Explain the reasons for potential instability in tuned amplifiers. **(7)**

Ans:
A tuned amplifier is required to be highly selective. Instability is because of positive feedback in tuned amplifiers.

Q.49 What are 'intrinsic' and 'extrinsic' semiconductors? Comment on the conductivity of extrinsic semiconductor. **(4)**

Ans:
A pure semiconductor which is not doped is said to be intrinsic semiconductor. They have very low conductivity. When pure semiconductors are mixed (doped) using trivalent or pentavalent elements, we get extrinsic ones, which are p type in the former case and n type in the latter.
The crystalline nature of the original semiconductor is unaltered by doping as the doping element atoms replace the original semiconductor atoms without disturbing the crystal structure as such. This happens by participation of electrons of doping element with those of semiconductor in forming bonds. However, either an extra electron as in the case of pentavalent dopant or a free hole as in the case of trivalent dopant greatly enhances the conductivity.

Q.50 Explain the classification of power amplifiers according to operational modes. **(6)**

Ans:

Classification according to operation mode:

The duration of device conduction with respect to input signal cycle period determines the class of operation.

Class A: Device current flows for the full period of input (Q point in the active region of the device).

Class B: Device conducts only during one half cycle of input. (Q point just at the cut off region of the device)

Class AB: Device conducts for greater than half cycle but less than full cycle of input.

Class C: Device conducts for less than half cycle of input. (Q point beyond cut off).

These different operations are achieved by appropriate biasing of the device by setting up the desired quiescent current and voltage (or Q-point). **Fig. 20 b.** illustrates the conditions for class A and class B.

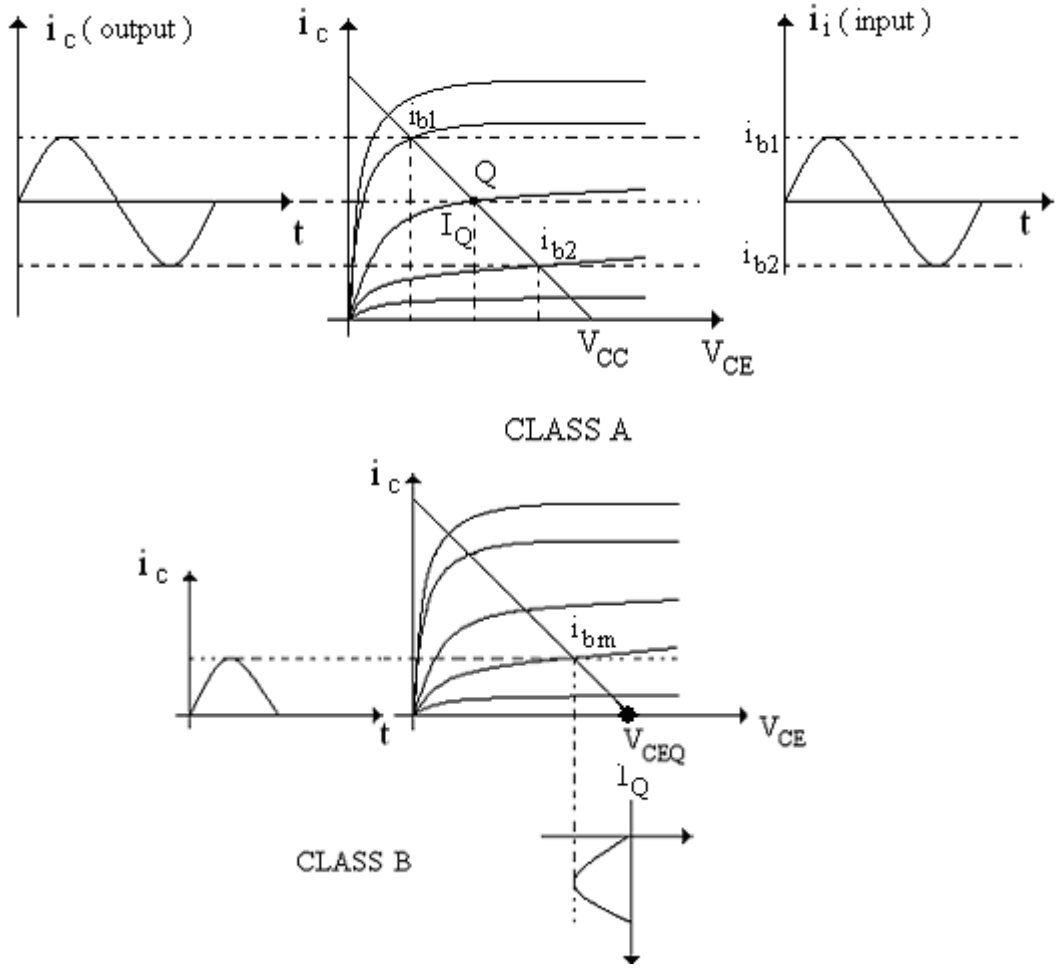


Fig. 20 b

Q.51 Draw a block diagram of a single loop feedback amplifier, and explain the function of each block. What are the characteristics of an amplifier that are modified by negative feedback? For the four topologies of negative feedback, indicate whether the input impedance and out impedance increase or decrease as a result of feedback. **(9)**

Ans:

The block diagram of a single loop feedback amplifier is as shown in Fig. 21a

Signal source: The signal source is either a voltage source or a current source providing input X_s.

Comparator or mixer: This block combines the source signal with the feedback signal. Depending upon the nature of signal and feedback this may be series or shunt mixing.

Basic amplifier: The ratio of output signal to the input signal of a basic amplifier is represented by 'A' and depends on the type of amplifier.

Sampling network: It is used to sample the output signal of the basic amplifier. When voltage has to be sampled, feedback network is connected in parallel to the output terminals and in series when current is to be sampled.

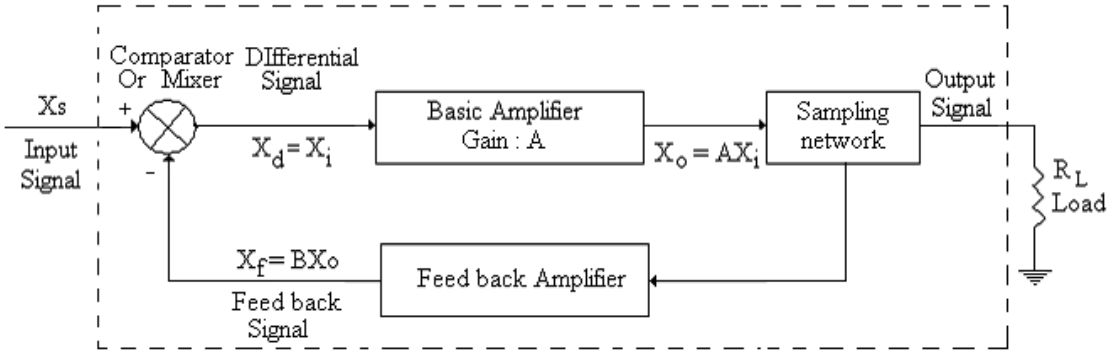


Fig. 21a

Feedback network: This is a passive two port network providing a known fraction of the input to the mixer at input.

The characteristics of an amplifier that are modified by negative feedback are:

1. Sensitivity of transfer characteristics.
2. Non linear distortion.
3. Noise.
4. Frequency distortion.
5. Bandwidth.
6. Input and output impedances of the amplifier.

Table below shows how the input impedance and output impedance in the four topologies of negative feedback are affected.

	Voltage Series	Current Series	Current Shunt	Voltage Shunt
I/P impedance	Increases	Increases	Decreases	Decreases
O/P impedance	Decreases	Increases	Increases	Decreases

Q.52 Write short notes on any two. **(2x7)**

i) Nyquist criterion.
ii) BIFET and BIMOS circuits.
iii) Schmitt trigger.
iv) The digital comparator.

Ans:

i) Nyquist criterion:

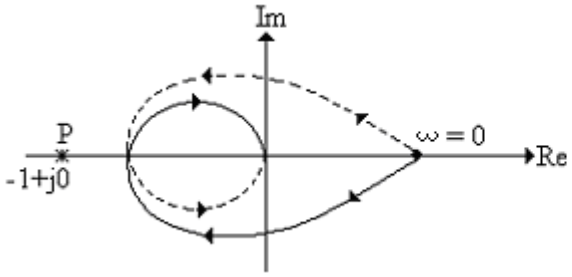


Fig.22 (i)-Stable system

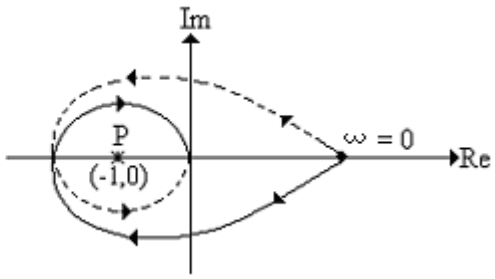


Fig.22(ii) unstable system

The diagrams above shows Nyquist plot for 2 types of systems (stable and unstable). Solid line is for positive frequencies. The Nyquist plot intersects the negative real axis at a frequency ω_{180}. If intersection occurs to the left of point (-1, 0), then the magnitude of loop gain at this frequency is greater than unity and amplifier will be unstable. If intersection occurs to the right of point (-1, 0) the amplifier will be stable. In other words, if Nyquist plot encircles the point (-1, 0) then amplifier will be unstable.

Nyquist plot is used to determine whether there are any poles on the right half of s-plane for a feedback amplifier.

Nyquist criterion states that the number of clockwise encirclements of the point –1+j0 is equal to the difference between the number of poles and zeros of F(s)=1+T(s) in the right half of s plane. (T(s) is the return ratio).

Closed loop gain of feedback amplifier = $A_F(s) = A_{OL}(s) / F(s)$

$A_{OL}(s)$ = loop gain of the amplifier without feedback.

Therefore for a stable feedback amplifier, the Nyquist plot of function $A_F(s)$ should not encircle the point –1+j0. The clockwise encirclements of –1+j0 are determined by drawing a radius vector from –1+j0 to Nyquist diagram and tracing the locus of points from $-\infty < \omega < \infty$.

In **Fig.22 (i)** there is no encirclement, therefore $A_F(s)$ has no right half poles and hence the amplifier is stable.

In **Fig.22 (ii)**there are two encirclements, therefore $A_F(s)$ has two right half poles and hence the amplifier is unstable.

ii) BIFET and BIMOS circuits:

Ion implantation permits the fabrication of JFETs / MOSFETs and BJTs on the same chip. The ICs fabricated by this process are called as BIFET/BIMOS. (BIFET=BJT+FET, BIMOS=BJT+MOSFET). All BIFET (BIMOS) op-amps use FET input stages. The remaining stages use BJTs. FET input stages have the following advantages over BJT input stages:

1) Higher differential mode input resistance.

2) Lower input current and hence decreased input offset currents and higher slew rates.

The input resistances of FET differential stages are 4 times higher in magnitude than that of BJTs. Input bias current of JFET is the reverse saturation current I_{GSS} of reverse biased gate to channel junction. The gate current of FET is usually much smaller than the base current of BJT for similar values of drain/collector currents. Since the input current I_G is very small, the offset current due to device mismatch is also much smaller than that with BJT circuits. For a given drain current I_D, value of g_m in FET is smaller than the g_m of BJT biased at $I_C = I_D$. Therefore, the reduction of g_m results in increased slew rate. This lower value usually results in lower differential mode gain in FET stage compared to that with BJT circuits. To overcome this limitation, BIFET and BIMOS Op-amps employ three-stage architecture.

iii) Schmitt trigger:

It is also called as regenerative comparator. It converts any given waveform into a rectangular output. The Schmitt trigger circuit is shown in Fig 7 (iii a). Input is applied to inverting terminal (2) and feedback voltage to non-inverting terminal (1).

Assuming that the output resistance of the comparator is negligible compared with R_1+R_2, we get $V_i = [R_2 / (R_1+R_2)] V_o$.

Let $v_o = Vz+V_D$

Vz = drop across reverse biased zener.

V_D = drop across forward biased zener.

And if $v_2<v_1$ so that $v_o= +V_o$

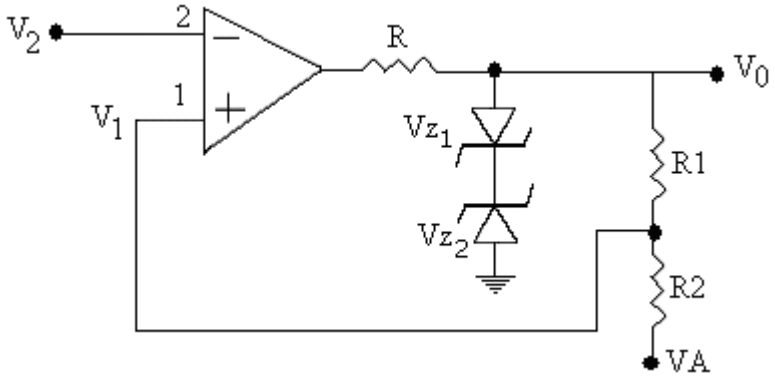


Fig 22 (iiia) Schmitt Trigger

The voltage at non-inverting terminal is given by

$$V_A + \frac{R_2 (V_0-V_A)}{R_1+R_2} = V_1 \quad (v_2<V_1)$$

If v_2 is now increased, then v_o remains constant and $v_o = + V_0$ constant until $v_2=V_1$, when v_2 exceeds V_1, v_0 changes.

At this threshold voltage, the output regeneratively switches to $-V_0$ and remains at this value as long as $V_2>V_1$. This is shown in **Fig 22 (iiib).**

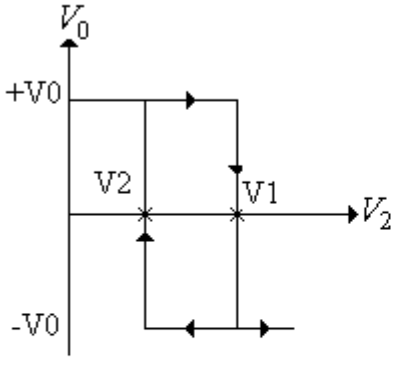


Fig 22 (iii c): Hysteresis curve

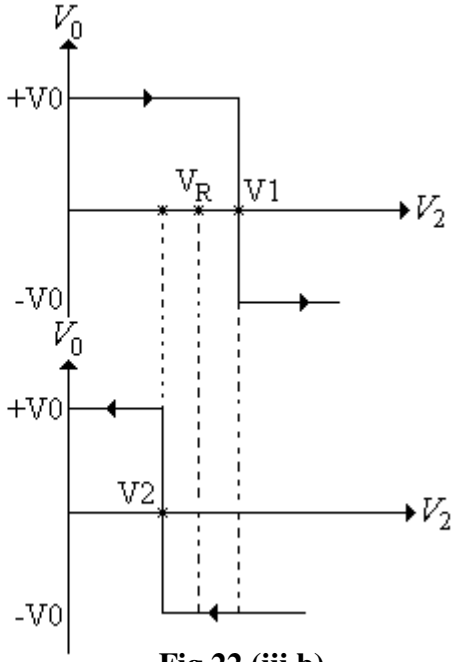


Fig 22 (iii b)

The voltage at non-inverting terminal for $V_2>V_1$ is given by

$$V_1 = V_A - \frac{R_2(Vo+V_A)}{R_1+R_2} = V_2 \quad (V_2<V_1)$$

Note that and difference between these 2 values is called as hysteresis V_H.

$V_H=V_1-V_2$

If we now decrease V_2, output remains at $-V_o$ until $V_2 = V_2$. At this voltage a regenerative transition takes place as indicated in fig 22(iii c) and output returns to $+V_o$ almost instantaneously.

This circuit can be used as a squaring circuit. The output is asymmetric square wave, the amplitude of which is independent of peak-to-peak value of input signal. The input and output waveforms are as shown in the following figure below.

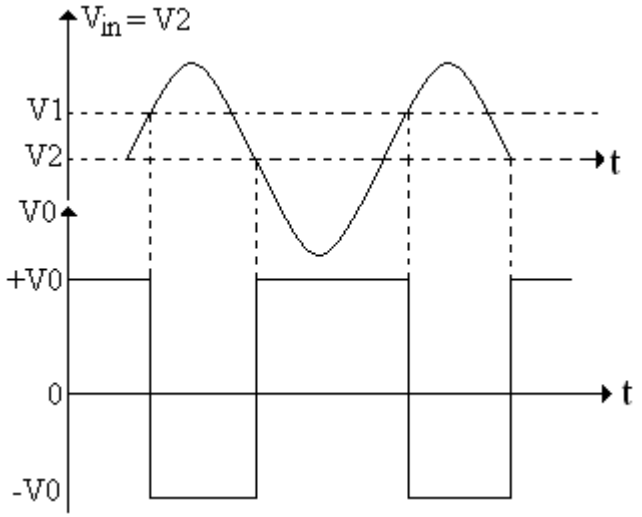


Fig 22 (iiid)

(a) Alternative Solutions I

Schmitt trigger:

Consider the circuit shown in figure 22 (i). This circuit converts an irregular shaped waveform to a square wave or pulse. The circuit is known as the Schmitt trigger or squaring circuit.

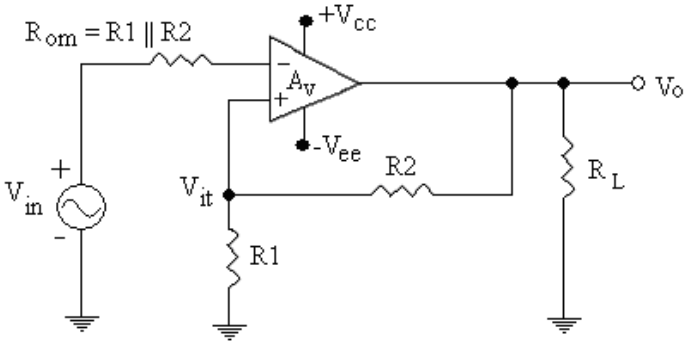


Fig.1

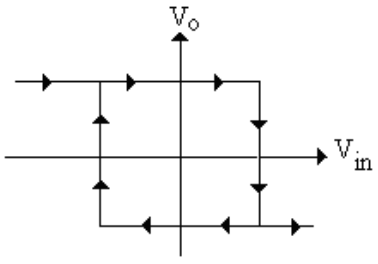
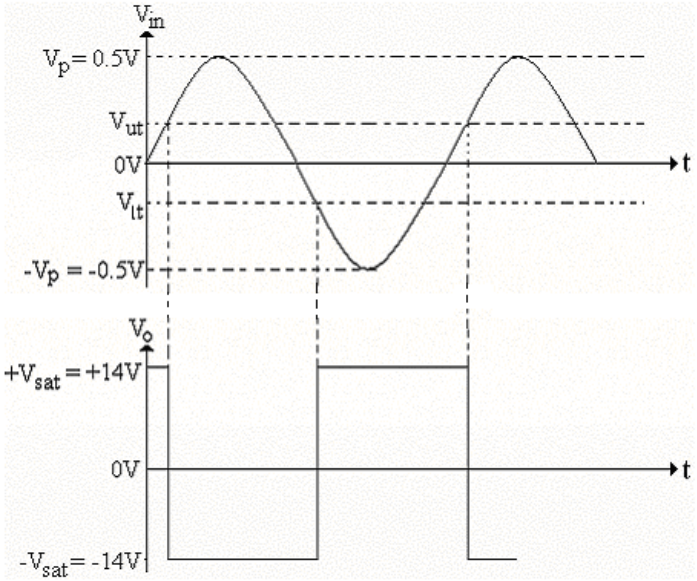


Fig. 2

The input voltage V_{in} triggers the output V_o every time it exceeds certain voltage level called the upper threshold voltage V_{ut} or becomes smaller than the lower threshold voltage V_{lt} as in Fig below. These threshold voltages are maintained in the circuit by using the voltage divider R_1, R_2 where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is dependent upon the value and polarity of V_o. When $V_o = +V_{sat}$ voltage across R_1 is called

upper threshold voltage V_{ut}, Where $V_{ut} = (R_1/(R_1 + R_2)) * V_{sat}$. When $V_0 = -V_{sat}$ voltage across R1 is referred to as the lower threshold voltage V_{lt} and is given by
$V_{lt} = (R_1/ (R_1 + R_2))* (-V_{sat})$.
If V_{ut} & V_{lt} are larger than the input noise voltages, +ve feedback will eliminate the false output transitions & due to regenerative action V_o switches faster between $+V_{sat}$ and $-V_{sat}$. $R_{OM} \approx R_1 \parallel R_2$ is used to minimize the offset problems.



A comparator with a positive feedback exhibits hysteresis. When input of the comparator exceeds V_{ut}, its output switches from $+V_{sat}$ to $-V_{sat}$ & reverts to its original state. Hysteresis voltage $V_{hy} = V_{ut} - V_{lt}$.

(b) Alternative Solution II

Schmitt trigger is used to change a slowly varying input voltage into an output waveform of an abrupt discontinuous change that occurs at a precise value of the input voltage. It is used as a squaring circuit.

Schmitt trigger is also called as regenerative comparator. Input is applied to inverting terminal and feedback voltage to non-inverting terminal .The Schmitt trigger circuit is as shown in the Fig.(i). It consists of two similar transistors Q_1 and Q_2 coupled through R_E and resistors R_1, R_3, R_4 from a voltage divider across V_{CC} to $-V_{BB}$ which places a small positive voltage on the base of Q_2.

Circuit operation:

When positive half cycles of input A.C voltage is applied to the input and suppose this positive voltage is sufficient to overcome the reverse bias on the base of Q_1, The sequence of events that follows is as follows.

1. Q1 comes out of cut off and starts to conduct.
2. Its collector voltage drops. (swings negative).
3. This negative swinging is coupled to the base of Q_2 via R_3 reducing its forward bias and hence its I_E .
4 With reduced I_E voltage drop across R_E is reduced.
5. Consequently, the reverse bias of Q_1 is further lowered and it conducts more heavily.
6. As a result, collector voltage of Q_1 falls further there by driving Q_2 still closer to cut off.

This process ends up with

1. Q_1 conducting at saturation with its collector voltage almost zero.

2. Q_2 becoming cut off with its collector voltage nearly V_{CC}.

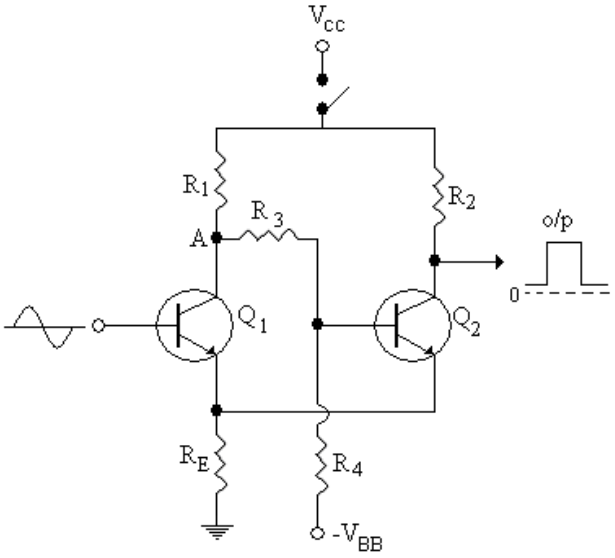


Fig.(i)-Schmitt Trigger

This circuit can be used as a squaring circuit. The output is asymmetric square wave, the amplitude of which is independent of peak-to-peak value of input signal. The input and output waveforms are as shown in the Fig.(ii).

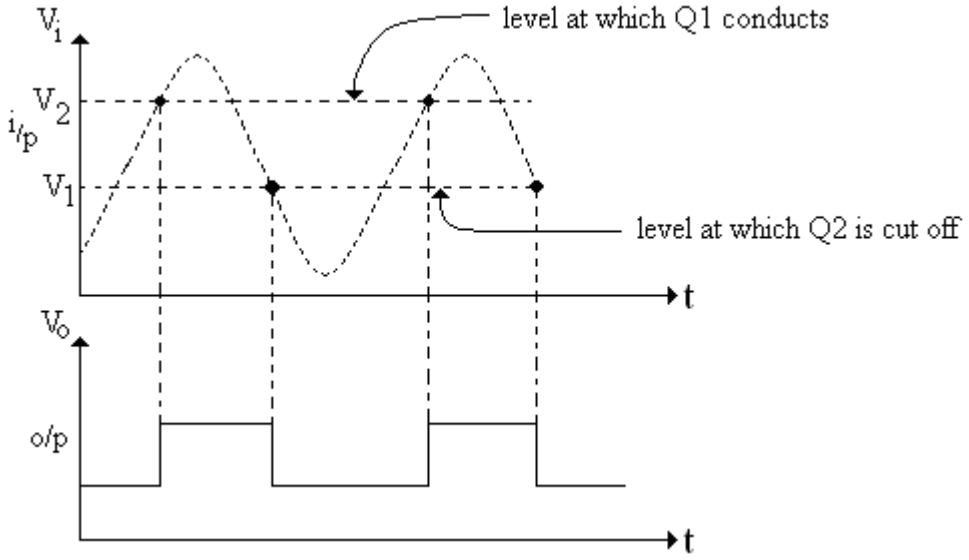


Fig.(ii)

Hysteresis:

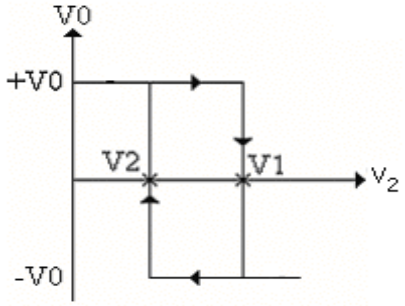


Fig.(iii)

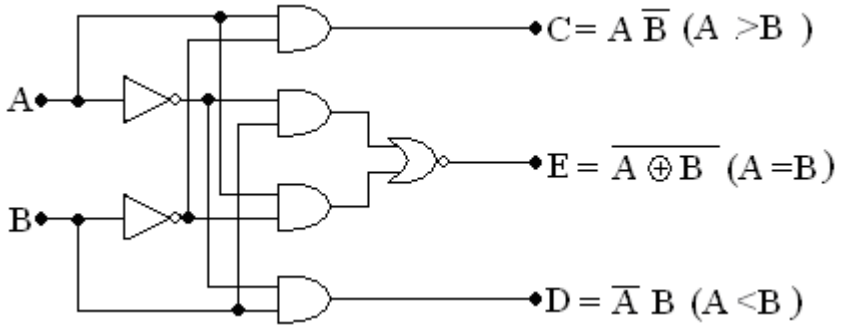
The transfer characteristics i.e., Vin v/s Vo is shown in Fig.(iii).

Due to the positive feedback the comparator is said to exhibit hysteresis. The portion without arrows may be traversed in either direction, but other segments can be obtained only if V_2 is increased or decreased in given direction.

Because of hysteresis, circuit triggers at a higher voltage for increasing than for decreasing signals.

iv) The digital comparator:

A comparator is used to detect whether a binary number is greater than, equal to or less than another binary number. Consider two single bit numbers A and B,



One bit comparator

Where C=1 for A>B
E=1 for A=B
D=1 for A<B

a) Let A=B

EX - NOR gate is an equality detector. The output E of EX-NOR is given by

$$E = \overline{\overline{A}B + A\overline{B}} = \begin{cases} 1 & A = B \\ 0 & A \neq B \end{cases}$$

b) Condition A>B is given by C=A$\overline{B}$=1 because if A>B then A=1 and B=0 therefore C=1 here

if A=B or A<B (A=0, B=1) then C=0.

c) Condition A<B is determined from D=AB=1

Consider a 4-bit comparator. ($\overline{A}$ & B are 4 bit numbers).

a) For A = B, $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, $A_0 = B_0$

Therefore $E=E_3E_2E_1E_0$

If A = B then E = 1

If A ≠ B then E = 0

b) For A>B: $A_3 > B_3$ (MSB)

Or $A_3=B_3$ and $A_2>B_2$

Or $A_3=B_3$ and $A_2=B_2$ and $A_1>B_1$

Or $A_3=B_3$ and $A_2=B_2$ and $A_1=B_1$ and $A_0>B_0$

This is given by

$C = \overline{B}_3A_3 + \overline{B}_2E_3A_2 + \overline{B}_1 E_3E_2A_1 + \overline{B}_0 E_3E_2E_1A_0$

If A>B then C = 1

d) For A<B: in the above equation interchange A and B, to get the output D.

Digital comparators are useful in comparing binary words and the result of comparison is used to initiate various actions in a digital system.

Q.53 With the help of a circuit diagram, explain the working of a half wave rectifier with capacitor filter. **(8)**

Ans:

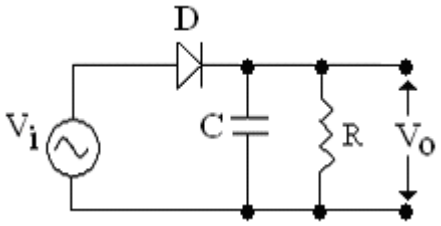


Fig 23 (i)

The circuit of a half wave rectifier is shown in the Fig 23 (i). For a sinusoidal input, the capacitor charges to the peak (Vp) of input. Then the diode cuts off and the capacitor discharges through the load resistor R. As the capacitor is discharging, the voltage at the cathode of the diode decreases. At some instant of time input voltage exceeds the capacitor voltage and the diode turns on. The capacitor now starts charging and the process repeats, and is shown in the figure 8 (ii b).To keep the output voltage from decreasing too much, during capacitor discharge, value of C is selected so that the time constant RC is much greater than the discharge interval.

Q.54 Draw the load voltage waveform for a half wave and full wave rectifier with a capacitor filter (no explanation required). **(6)**

Ans:

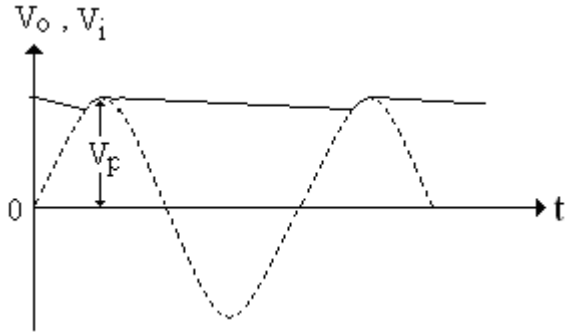


Fig 23 (ii a): for Half wave rectifier

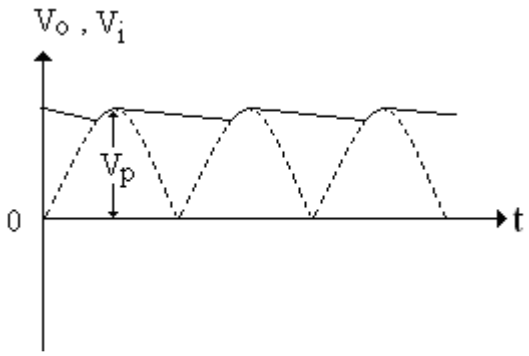


Fig 23 (ii b): for Full wave rectifier

Q.55 Explain the terms fan in and fan out in logic gates. **(4)**

Ans:

Fan in: Fan in of a gate is the number of inputs it can accept without affecting the input characteristics of the gate. If fan in is exceeded, a logic gate will produce either an undefined or incorrect output state. Also, the input signals may be deteriorated because of excessive loading.

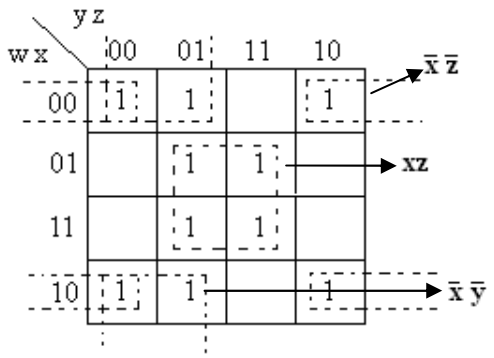
Fan out: A logic gate may be capable of providing input to several similar gates. Fan out is the number of similar circuits a gate can drive without any effect on its output characteristics.

Q.56 Using 4 variable K map, find all the prime implicants of the following switching function.

$f(w,x,y,z)=\Sigma(0,1,2,5,7,8,9,10,13,15)$

And from the set of prime implicants thus obtained, find out minimal sum of product expression of the function. **(10)**

Ans:



The K map is shown above for the given function. The prime implicants are

(i) xz (ii) $\bar{x}\,\bar{y}$ (iii) $\bar{x}\,\bar{z}$

The minimum SOP representation is:

$f(w,x,y,z) = xz + \bar{x}\,\bar{y} + \bar{x}\,\bar{z}$

Q.57 What is the function of A/D converter? **(4)**

Ans:

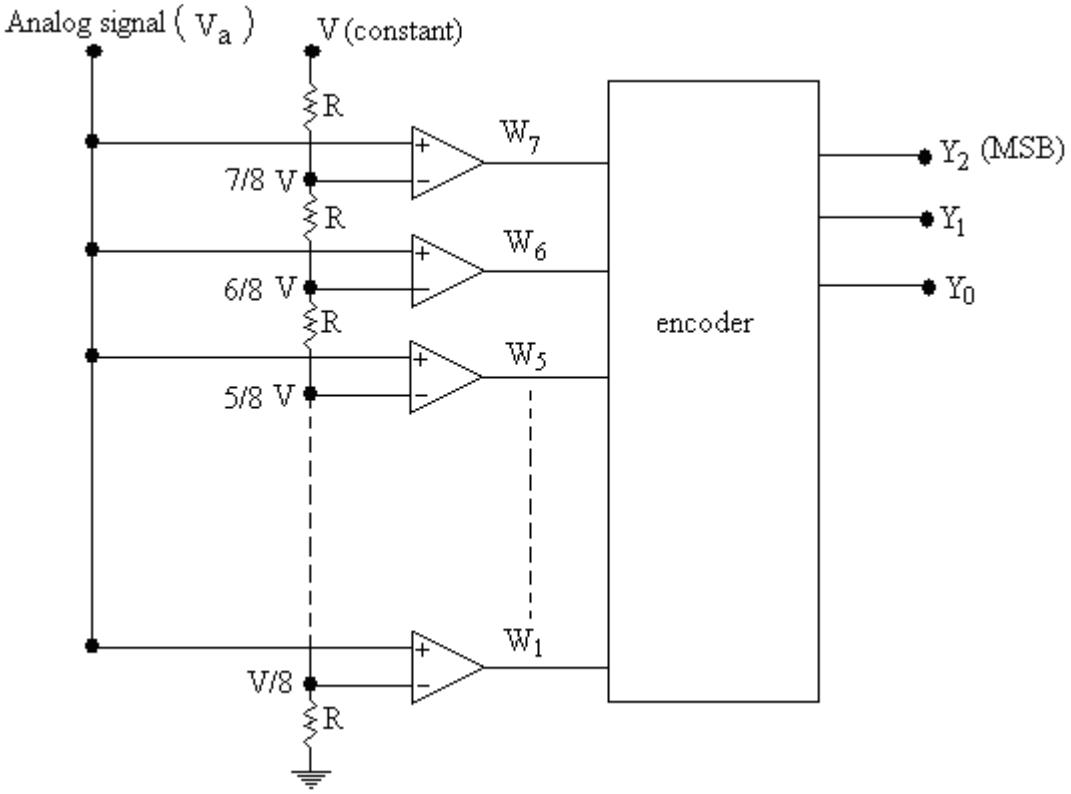
Data obtained from the physical system will be analog in nature. For processing these signals several methods are employed and all these systems require the inputs in the digital form. So if the analog signals are to be processed and analyzed, they should be converted into digital form. Therefore A/D converters are used to convert the signals in analog form into digital form.

Q.58 Explain 3 bit parallel comparator ADC with the help of a diagram and give its truth table. **(10)**

Ans:

Parallel comparator ADC is the fastest type. In this method, analog voltage V_a is applied to all the comparators. The reference voltage to first comparator is (7/8) V, to second comparator is (6/8) V and so on. The reference voltage to last comparator is V/8. Above diagram shows a 3 bit ADC. It requires 7 comparators.

Working: When input voltage is below the reference voltage of the comparator, the output of the comparator is low (logic 0). When input voltage is above the reference voltage, the output of that comparator is high (logic 1).



For example:if input voltage V_a is between (2/8) V and (3/8) V then W_1=1, W_2=1 and all other W values are 0. For this, the digital output of the encoder should be 2 (Y_2=0, Y_1=1, Y_0=0) which is interpreted as an analog voltage between (2/8) V and (3/8) V.

When V_a < (1/8) V, then W_1 to W_7 are all 0 and output is zero. (Y_2=Y_1=Y_0=0).

The truth table is as follows:

INPUTS							OUTPUTS		
W_7	W_6	W_5	W_4	W_3	W_2	W_1	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

Q.59 What is an oscillator? How does it differ from an amplifier? What are the essential parts of an oscillator circuit? **(7)**

Ans:

The oscillator is a circuit which generates signals of constant amplitude and frequency. The circuits which generate sine waves using resonance phenomena are known as linear oscillators. The circuits which generate square, pulse or rectangular waveforms are called as nonlinear oscillators.

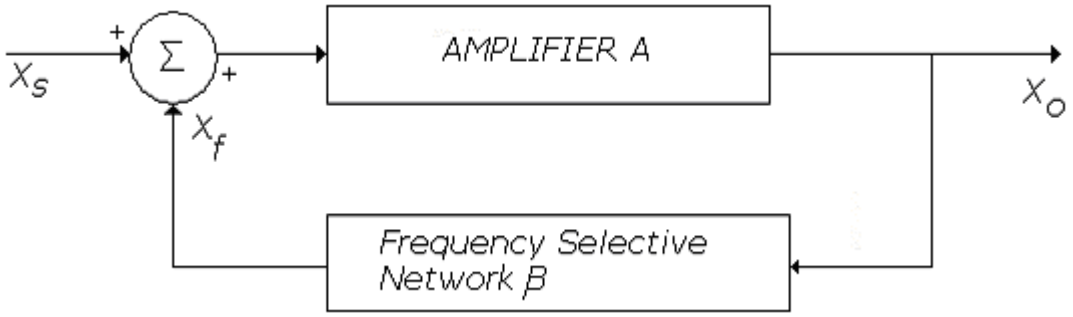


Fig 27a: Basic structure of a sinusoidal oscillator

Amplifier is a device which produces an enlarged version of the output signals same as that of input. Amplifier is an energy conversion device, which gets energy from the dc source and converts into an a.c source. Conversion is controlled by the input signal. Oscillator produces an output signal without any input signal of any frequency. It produces output signal, as long as the dc power is supplied.

An amplifier usually employs negative feedback whereas the oscillator will have positive feedback.

The essential parts of an oscillator circuit are

i) Transistor amplifier

ii) Frequency selective network: The Frequency selective network is connected in positive feedback loop. A part of the output signal is fed to the amplifier in phase to aid the oscillations, as shown in Fig 27a, where $X_s = 0$ for an oscillator.

Q 60 Draw the circuit diagram of Colpitts oscillator and explain its working. **(7)**

Ans:

The circuit diagram of a Colpitts oscillator is as shown Fig 27b.It uses two capacitors C1 and C2 placed across a common inductor L and the center of the two capacitors is tapped. This forms the frequency selective feedback network. The transistor circuit is the amplifier.

Operation:

When the circuit is turned on, the capacitors C_1 and C_2 are charged. The capacitors discharge through L, which sets up oscillations of frequency

$$f_o = 1 / 2\pi\sqrt{LC}$$

Where $C = C_1 C_2 / (C_1 + C_2)$. The output voltage of the amplifier appears across C_1 and feedback voltage is across C_2. The voltage across C_2 is 180^o out of phase with the voltage across C_1. The voltage across C_2 is fedback to the transistor providing a positive feedback.

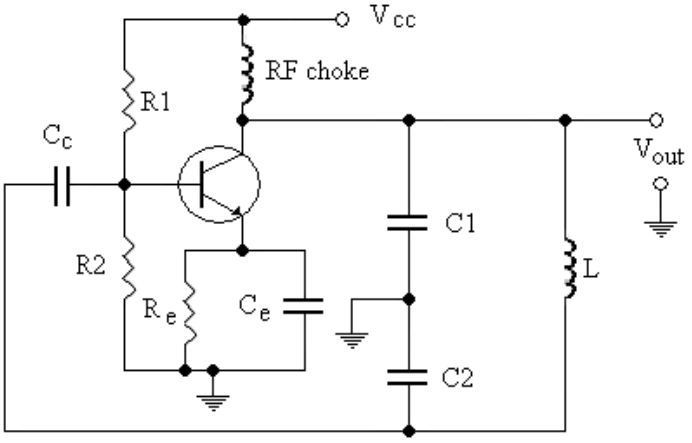


Fig 27b

A phase shift of 180^o is produced by the transistor and a further phase shift of 180^0 is produced by C_1-C_2 voltage divider. Therefore, the feedback is properly used to produce continuous undamped oscillation.

Q.61 What is an integrator? Derive the formula for its output voltage. Explain its working with neat and clean waveform i) In case of square wave input ii) In case of sine wave input. **(8)**

Ans:

A circuit in which the output voltage is directly proportional to the integral of the input voltage is called an integrator. Integrators can be passive integrator or active integrator. **Fig** 28a(i) shows an active integrator using op-amp.

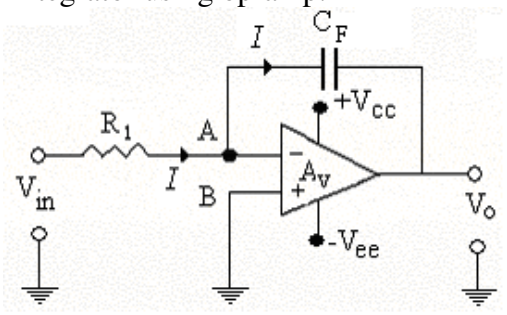


Fig 28a(i)

Expression for output voltage:

Since node B is grounded, node A is also at ground potential. Hence $V_A=V_B=0$. As the input current of op- amp is zero, the current through C_F is the current through R_1. From input side

$I = V_{in}/R_1$

From output side

$I = C_F\, d(V_A-V_O)/dt = - C_F(dV_O/dt)$

Therefore

$V_{in}/R_1 = - C_F\,(dV_O/dt)$

Integrating

$$\int_0^t (V_{in}/R_1)\, dt = - C_F \int dV_o / dt = - C_F\, V_O$$

$$V_o = -(1/R_1\, C_F) \int_0^t V_{in}\, dt$$

Working of an integrator for square wave input:

Let the input waveform be a square wave as shown in Fig 28a(ii). It can be observed that the square wave is made up of steps i.e., step of 'A' between time period of '0' to T/2 while a step of '-A' between T/2 and T.

Mathematically it can be expressed as

$V_{in}(t) = A, \quad 0<t<T/2$

$= -A, \quad T/2<t<T$

The output for step input is a straight line with a slope of '–A'. So in the period '0' to 'T/2', the slope is '–A'. From 'T/2' to 'T' slope becomes – (-A) i.e. +A.

Therefore output $V_O(t) = -At \quad 0<t<T/2$

$= +At \quad T/2<t<T.$

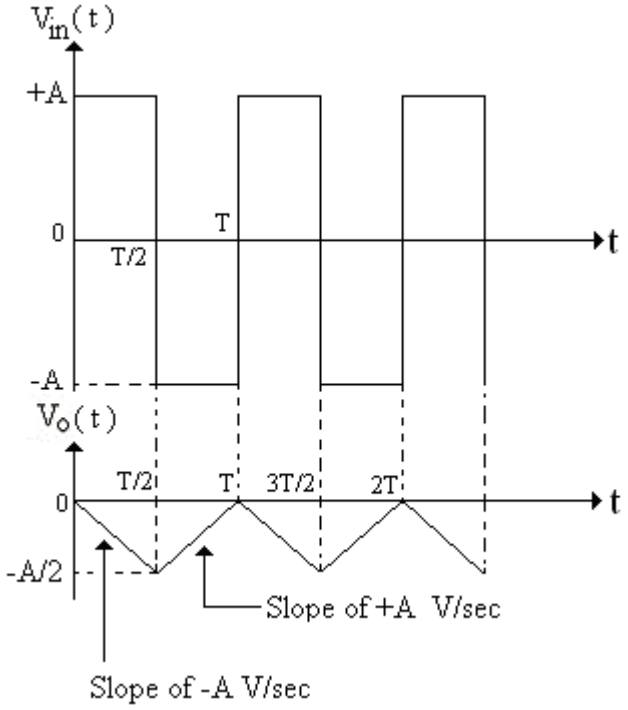


Fig 28a(ii)

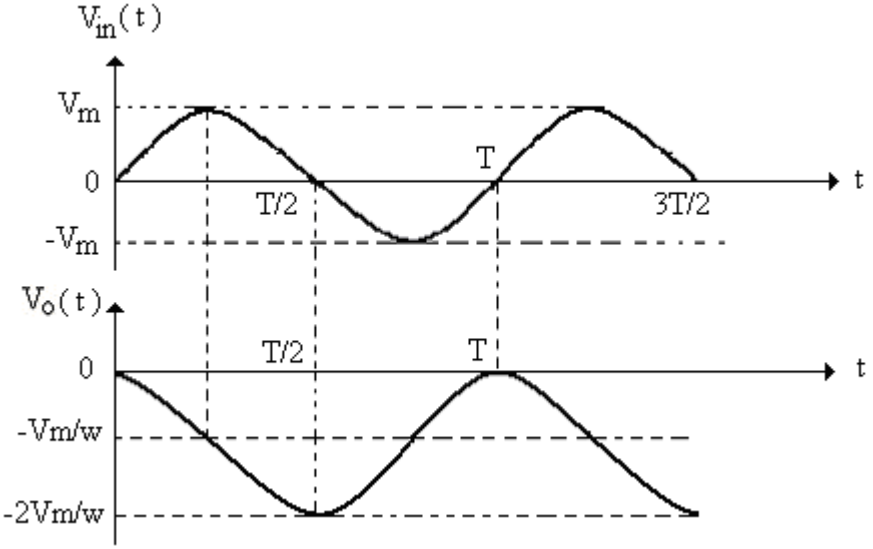


Fig 28a(iii)

Working of an integrator for sine wave input signal:

Let the input waveform is purely sinusoidal with a frequency of ω rad/sec.

i.e., V_{in} (t) = V_m Sin ωt, where V_m is the amplitude of sine wave and T is the period of the waveform. To find the output waveform, let $R_1C_1 = 1$ and V_O (0) = 0V.

$V_O(t) = -\int V_{in}\, dt = -\int V_m \sin \omega t\, dt$

$= -V_m [1/\omega (-\cos \omega t)] = -V_m /\omega (-\cos \omega t)$

Thus the output of an integrator is a cosine waveform for a sine wave input. The waveforms are as shown in Fig 28a(iii).

Q.62 Derive the formula for summing amplifier and on averaging amplifier in non Inverting configuration. **(6)**

Ans:

A summer that gives non inverted sum of the input signals is called as non-inverting summing amplifier. The circuit is shown in Fig 28b(i).

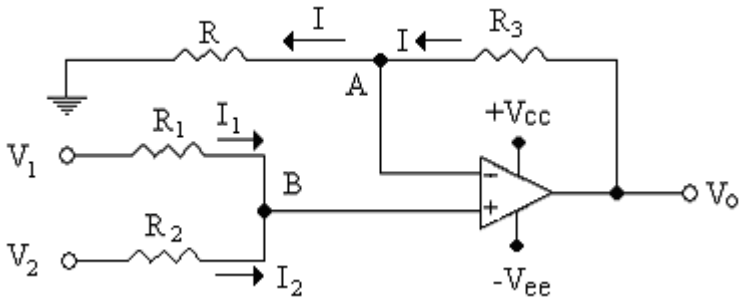


Fig 28b(i)

Let the voltage at node B be V_B. Node 'A' is at the same potential.

Therefore $V_A = V_B$

From input side $I_1 = (V_1 - V_B)/R_1$ and $I_2 = (V_2 - V_B)/R_2$

As input current of op-amp is zero, $I_1 + I_2 = 0$

Therefore $(V_1 - V_B)/R_1 + (V_2 - V_B)/R_2 = 0$

$V_1/R_1 + V_2/R_2 = V_B (1/R_1 + 1/R_2)$

This gives, $V_B = (R_2V_1 + R_1V_2)/(R_1 + R_2)$

At node A, $I = V_A/R = V_B/R$ and $I = (V_O - V_A) / R_3 = (V_O - V_B) /R_3$

Therefore, $V_B/R = (V_O - V_B) /R_3$

i.e., $V_O/R_3 = V_B (1/R_3 + 1/R)$

Therefore, $V_O = V_B [(R + R_3) / R]$

i.e., $V_O = ([R_2V_1 + R_1V_2] / [R_1 + R_2])^* ([R + R_3] / R)$

Therefore $V_O = R_2(R + R_3) V_1 / R (R_1 + R_2) + R_1(R + R_3) V_2 / R (R_1 + R_2)$

If $R_1 = R_2 = R = R_3$ we get $V_O = V_1 + V_2$

If in the summer circuit the value of resistance are selected as $R_1 = R_2 = R$ and $R_3 = R / 2$. Then

$V_O = [(R/2) V_1/R + (R/2) V_2/R]$

$= [(V_1 + V_2)/2]$

Thus the magnitude of the output voltage is the average of the input voltages. In that case the input becomes a averaging amplifier.

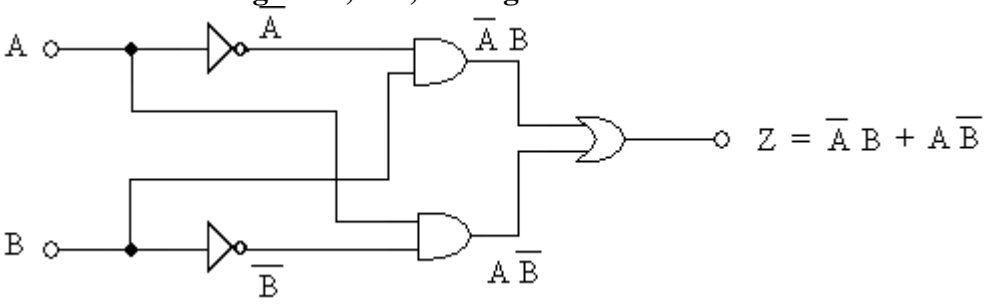
Q.63 For the logic expression $Z = \bar{A}B + A\bar{B}$

i) Obtain the truth table. **(2)**
ii) Name the operation performed **(1)**
iii) Realize this operation using *AND, OR, NOT gates * only NAND gates (**4**)

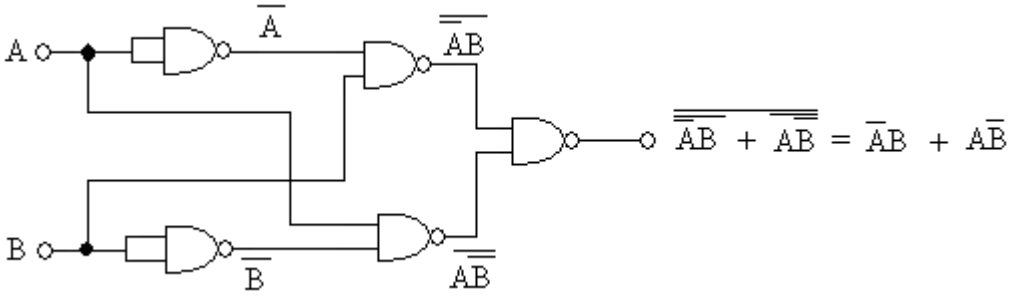
Ans:
(i) Truth Table

A	B	$\bar{A}$	$\bar{B}$	$\bar{A}B$	$A\bar{B}$	$\bar{A}B + A\bar{B} = Z$
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

(ii) The operation performed is Exclusive OR operation.
(iii)Circuit realization using AND, OR, NOT gates.



(iv)Circuit realization using NAND gates only.



Q.64 State and prove De Morgan's theorem using truth table. **(7)**

Ans:
The De Morgan's theorem can be stated as follows
Theorem 1: The complement of a product of variables is equal to the sum of the complements of the individual variables. Symbolically,
$\overline{(A.B.C.D.\ldots\ldots)} = \bar{A} + \bar{B} + \bar{C} + \bar{D} + \ldots\ldots\ldots$
Theorem 2: The complement of the sum of variables is equal to the product of individual complements of variables. Symbolically,

$\overline{(A + B + C + \ldots..)} = \bar{A}.\bar{B}.\bar{C} \ldots\ldots\ldots\ldots$

The theorems can be verified by using truth table.
The truth table shown in table 1 for two variables A and B gives justification for theorem 1, and table 2 for theorem 2.

A	B	A+B	$\overline{A+B}$	$\bar{A}$	$\bar{B}$	$\bar{A}.\bar{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Table 1

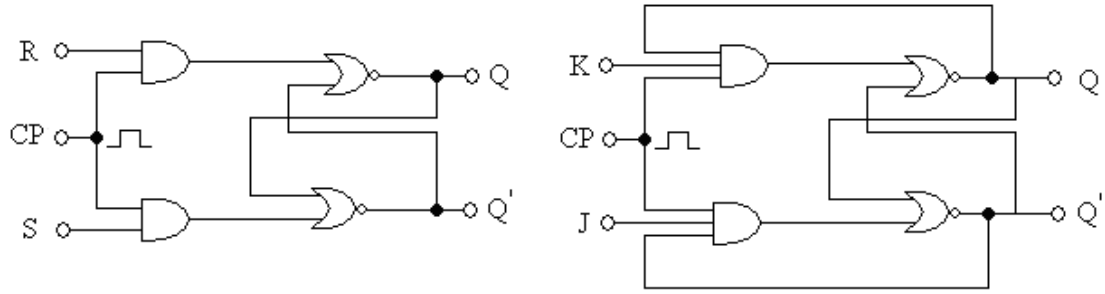
A	B	AB	$\overline{AB}$	$\bar{A}$	$\bar{B}$	$\bar{A} + \bar{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Table 2

Q.65 What is a JK flip flop? How does it differ from the SR flip flop in construction and operation? **(7)**

Ans:

A JK flip flop is a refinement of the RS flips flop, in that the indeterminate state of the RS type is well defined in the JK type. When input to RS flip flop are R=S=1, both outputs of flip-flop are at logic '0'. When J = K =1 JK is flip flop, it complements the outputs. That is if Q =1, it switches to Q =0 and vice versa. Fig 30 (a) shows the logic diagrams of SR flip flop and JK flip flop. In the logic circuit of JK flip-flop output Q is ANDed with K and CP inputs so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Q' is ANDed with J and CP inputs so that the flip-flop is set with a clock pulse only if Q' was previously 1.



RS flip flop **Fig 30 (a)** **JK flip flop**

Thus JK flip-flop behaves like an RS flip flop, except when both J & K are equal to 1. When both J & K are 1, the clock pulse is transmitted through one AND gate only, the one whose input is connected to the output which is presently equal to 1. Thus if Q = 1, the output of the upper AND gate becomes 1 upon application of a clock pulse and the flip-flop is cleared. If Q' = 1, the output of the lower AND gate becomes a 1 d the flip flop is set. In either case the output state of the flip-flop is complemented.

Q.66 What is a sequential logic circuit? How does it differ from the combinational type? **(4)**

Ans:

A sequential circuit is one whose output depends on the present inputs as well as on the past outputs In a combinational circuit, output at any instant of time depends only on the present inputs. Such systems are called memory less systems.

A block diagram of a sequential circuit is shown in Fig 30 (B). A combinational circuit and storage elements are interconnected to form the sequential circuit. Storage elements store binary information.

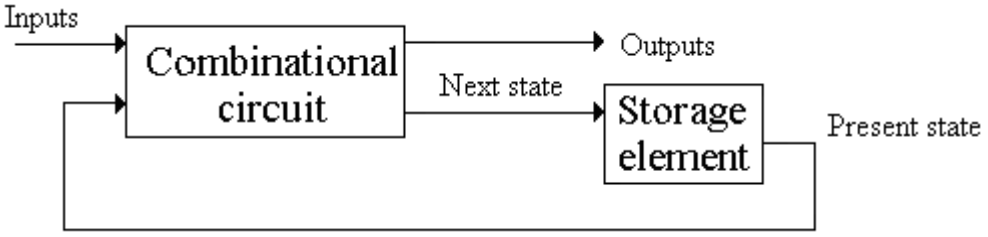


Fig 30 (B)

The sequential circuits receive binary information from its environment via inputs. These inputs together with the present state of the storage elements, determine the output. They also determine the values used to specify the next state of the storage elements.

Q.67 Show how a full adder may be implemented by using two half adders. **(3)**

Ans:

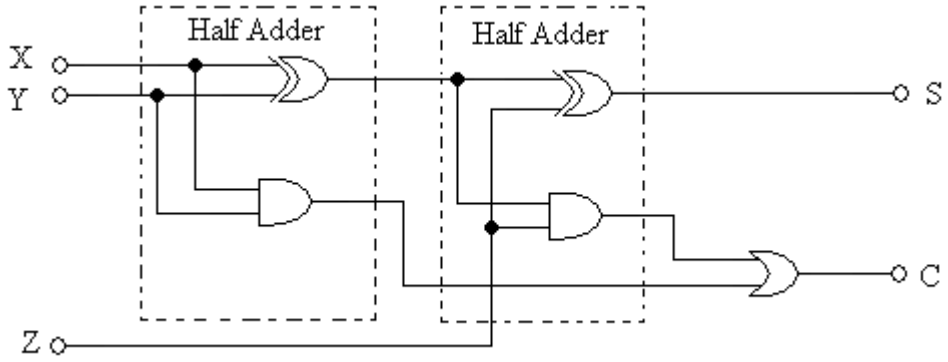


Fig 30 (c)

Q.68 Write short notes on
(i) Voltage Regulator
(ii) Multivibrator
(iii) Shift Register (2x7)

Ans:

(i) Voltage Regulator:

Voltage regulation may be defined as the ability of the power supply or source to maintain a constant output voltage in spite of a.c voltage fluctuations and changes in the load resistance. Mathematically, it is given by the relation,

((Vmax –Vmin) /Vmax)x 100

Vmax = maximum d.c. output voltage.

Vmin = minimum d.c. output voltage.

In general, the voltage regulation may also be expressed as

$((V_{NL} - V_{FL}) / V_{FL}) \times 100$

V_{FL} = full load voltage of the supply.

V_{NL} = no load or open circuit voltage of the supply.

It is a known fact, that all the electronic devices and circuits require a constant d.c voltage for their operation, and a fluctuating d.c voltage result in erratic operation of the electronic devices. The d.c voltage can be supplied from dry cells or batteries. But these are expensive compared to the conventional regulated d.c power supplies. The regulated d.c power supply is made by converting the domestic a.c supply to d.c supply. The essential elements, which constitute a regulated d.c power supply, are given below:

1)Rectifier ,
2)Filter, and
3)Voltage regulator.

The rectifier is the front or the first element of a regulated d.c power supply, the filter is the second or the intermediate element and the voltage regulator is the last element.

Working: As an example let us consider a combination of full wave rectifier and a filter circuit connected to an a.c. input voltage source. When the a.c input voltage, of the rectifier input, changes above or below its normal value, it will cause a change in d.c voltage produced at the filter output. A similar change in d.c voltage may also occur, when the load resistance connected at the filter output changes above or below its normal value. It means that the d.c. output voltage fluctuates whenever the a.c input voltage or the load resistance varies above or below the normal values.

Although there are many types of voltage regulators, yet the following ones are some of the important types of voltage regulators,

1. zener diode shunt regulator.
2. Transistor shunt regulator.
3. Transistor series regulator.
4. Controlled transistor series regulator.
5. Monolithic regulator.

(ii) **Multivibrator:** An electronic circuit that generates square wave is known as a multivibrator. A multivibrator is a switching circuit which depends, for operation, on positive feedback. It is basically a two stage amplifier with output of one given as the input to the other as shown in Fig: 31(iii).

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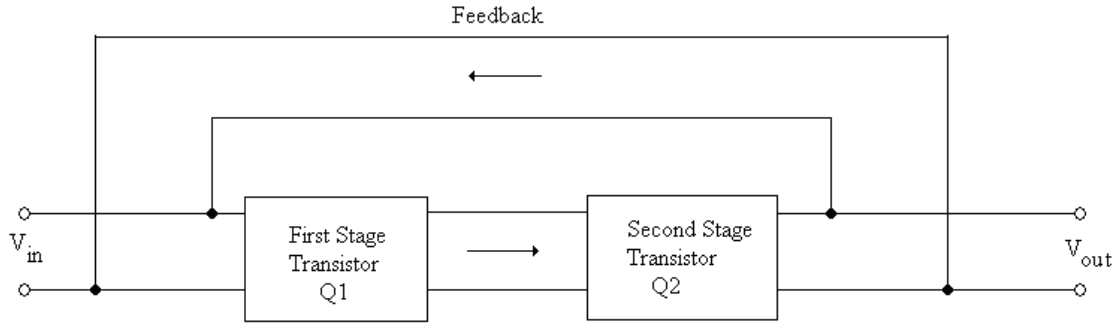


Fig: 31(iii)

The circuit operates in two stages controlled by the circuit conditions. Each amplifier stage supplies feedback to the other in such a manner that will drive the transistor of one stage to saturation and the other to cut off. After a certain time, controlled by circuit conditions, the action is reversed i.e., saturation stage is driven to cut off and cut off stage is driven to saturation. The output may be taken across any of the stages and may be rectangular or square wave depending upon the circuit conditions.

Types of multivibrators:
Multivibrators are classified into three categories.
a) Astable multivibrator or free running multivibrator
b) Monostable multivibrator or one-shot multivibrator
c) Bi-stable multivibrator or flip-flop multivibrator

a) Astable multivibrator or free running multivibrator alternates automatically between the two states and remains in each state for a time dependent upon the circuit constants. Thus, it is just an oscillator since it requires no external pulse for its operation. Because it continuously produces the square-wave output, it is often referred to as a free running multivibrator.

b) Monostable multivibrator or one-shot multivibrator has one stable state and one quasi-stable state. The application of input pulse triggers the circuit into its quasi-stable state, in which it remains for a period determined by circuit constants. After that period of time the circuit returns to its initial state, the process is repeated upon application of each trigger pulse.

c) Bi-stable multivibrator or flip-flop multivibrator has two stable states. It requires the application of an external triggering pulse to change the operation from one state to the other. Thus one pulse is used to generate half-cycle of square wave and another pulse is to generate the next half-cycle of square wave. It is also known as flip-flop multivibrator because of its two possible states it can assume.

d) **Shift registers:** A register capable of shifting its stored bits laterally in one or both directions is called a shift register. The logical configuration of a shift register consists of a chain of flip flops in cascade with the out put of one flip flop connected to the input of the next flip flop. All the flip flops receive a common clock pulse, which activates the shift from each stage to the next.

The simplest possible one is that which uses only D flip flops as shown in figure 18.

The output of a given flip flop is connected to the D input of the flip flop at its right. Clock is common to all flip flops. Serial input SI is the input to the leftmost flip flop during the shift. The serial output SI is taken from the output of the right most flip flop.

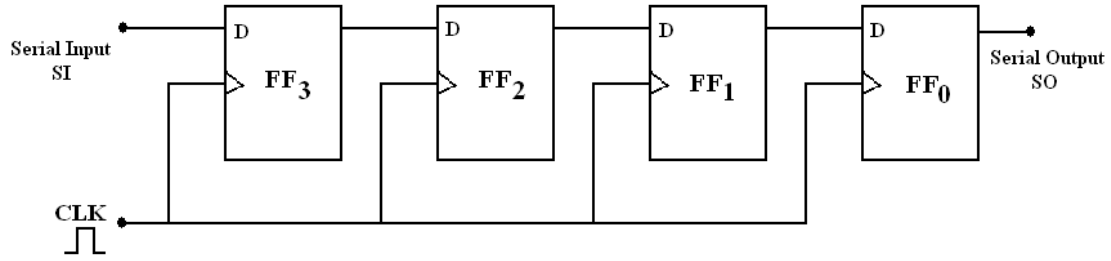


Fig 18 A 4 bit shift register

Shift registers can be used for converting serial data to parallel data and vice versa. If we have access to all the flip flop outputs of a shift register, then information entered serially by shifting can be taken out in parallel from the outputs of the flip flops or vice versa.

Q.69 Discuss the basic concept behind the operation of a Wien-bridge oscillator with the help of suitable circuitry and derive expression for relevant oscillation frequency. **(7)**

Ans:

Wein-bridege oscillator is used in audio frequency range. It uses two transistors, each producing a phase shift of 180^0 and thus producing a total phase shift of 360^0 or 0^0.

The Fig. 32a. shows the circuit diagram of an Wien-bridge oscillator. It is a two stage amplifier with an RC bridge circuit. RC bridge circuit is a lead lag network. The phase shift

across the network lags with increasing frequency and leads with decreasing frequency. By adding a feedback network, the oscillator becomes sensitive to a signal of only one particular frequency. This frequency is that at which Wien bridge is balanced and for which phase shift is 0^0.

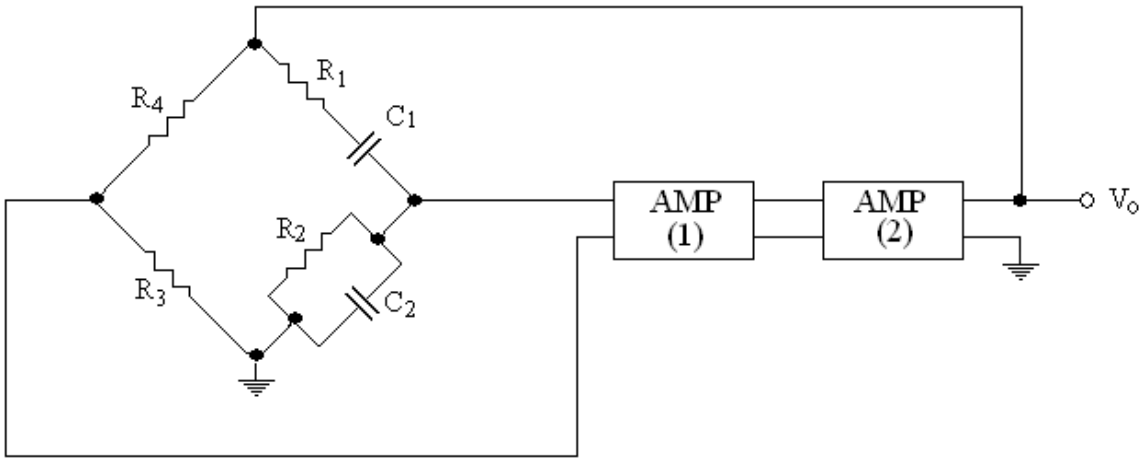


Fig. 32a.

The bridge is balanced only when

$R_4 (R_2 / (1+j\omega C_2R_2)) = R_3 (R_1 - j / \omega C_1)$

$R_2 R_4 = R_3 (1 + j\omega C_2R_2) (R_1 - j / \omega C_1)$

or

$R_2R_4 - R_3R_1 - (C_2 / C_1) R_2R_3 + (jR_3 / \omega C_1) - j \omega C_2R_2R_1R_3=0$

Separating real and imaginary parts, we have

$R_2R_4 - R_3R_1 - (C_2 / C_1) R_2R_3=0$

or

$(C_2 / C_1) = (R_4/ R_3) - (R_1 / R_2)$

and $(R_3 / \omega C_1) - \omega C_2R_2R_1R_3=0$

$\omega^2= (1 / C_2C_1R_2R_1)$ or $\omega=\sqrt{(1 / C_2C_1R_2R_1)}$

$f_o= 1/ (2 \pi \sqrt{(R_1R_2C_1C_2)})$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then

$f_o = 1/(2\pi \text{ x R x C})$ and $R_4=2R_3$

Q.70 What are the main considerations which are to be kept in view while selecting an oscillator for a particular application? **(7)**

Ans:

The main considerations which are kept in view while selecting an oscillator for a particular application are

1.Frequency range:

The oscillator selected for a particular application should be capable of supplying an output signal whose upper and lower frequency limits exceeds those required by the application. The frequency of operation of the oscillator has been selected, it should not drift from the related frequency.

2.Accuracy and dial resolution:

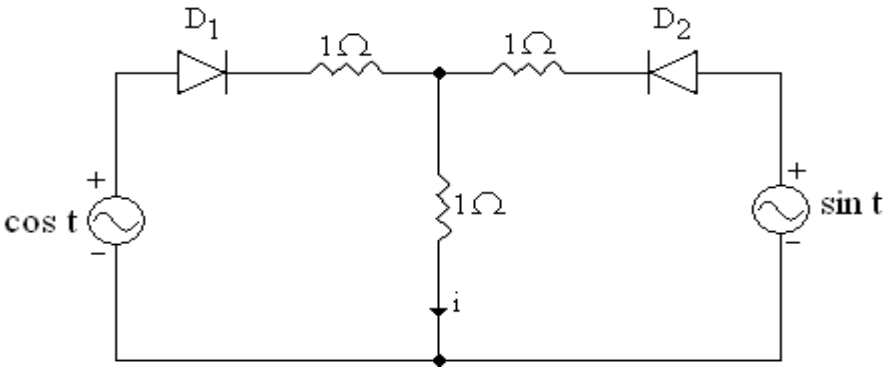
The accuracy of an oscillator specifies how closely the output frequency corresponds to the frequency indicated on the dial of the output frequency value the dial setting can be read.

3.Amplitude and frequency stability:
The amplitude stability is a measure of an oscillator's ability of maintaining a constant voltage amplitude with variations in the output signal frequency. Frequency stability determines how closely the oscillator maintains a constant frequency over a given time period.

4.Waveform distortion:
This quantity is the measure of how closely the output waveform of the oscillator resembles a pure sinusoidal signal. The distortion should be kept minimum.

5.Output impedance:
This is the impedance value of load which must be connected to it for maximum power transfer. The output impedance of the oscillator be equal to the characteristic impedance of the system to which it is to be connected.

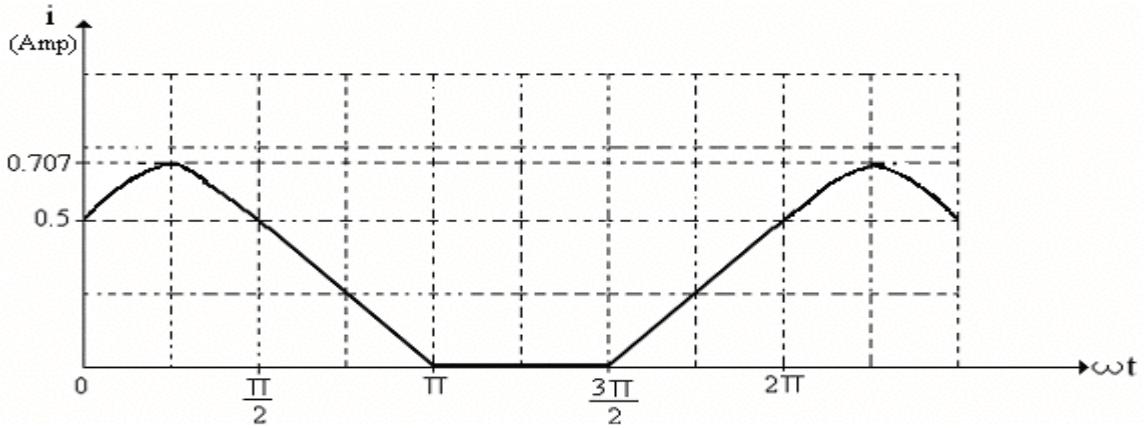
Q.71 In a circuit shown in figure below, calculate and sketch the waveforms of current i over one period of input voltage. Assume the diodes to be ideal. **(14)**



Ans:

Between the duration 0 and $\pi/2$ both diodes are ON.
Between the duration $\pi/2$ and π diode D_2 is ON.
Between the duration π and $3\pi/2$ both diodes are OFF.
Between the duration $3\pi/2$ and 2π diode D_1 is ON.

$i = 1/2 (\sin t + \cos t)$ for $0 \le t \le \pi/2$
$i = 1/2 (\sin t)$ for $\pi/2 \le t \le \pi$
$i = 0$ for $\pi \le t \le 3\pi/2$
$i = 1/2 (\cos t)$ for $3\pi/2 \le t \le 2\pi$



Q.72 State the principle of operation of a bistable multivibrator with the help of a circuit diagram. **(7)**

Ans:

Bistable multivibrator (BVM)

It has two absolutely stable states. It can stay in one of its two states indefinitely, and changes to other state only when it receives a trigger pulse from outside.

Since one trigger pulse causes the multivibrator to flip from one state to another and the next pulse causes it to flip back to its original state, the multivibrator is also known as "flip-flop" circuit.

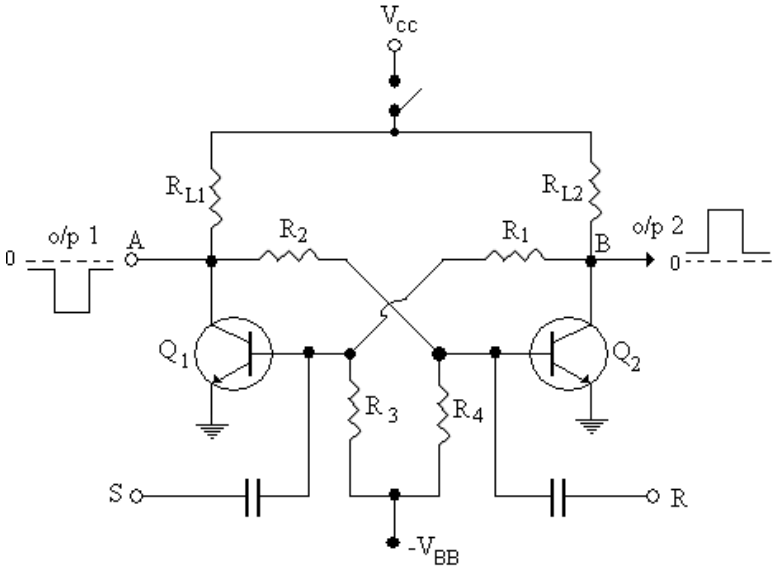


Fig.34a

Circuit operation:

In the circuit shown in Fig.34a**,** when Q_1 is conducting, then the fact that point A is at nearly 0V makes the base of Q_2 negative (by the potential divider R_2-R_4) and holds Q_2 OFF. Similarly, when Q_2 is OFF, the potential divider from V_{CC} to $-V_{BB}$ (R_{L2}, R_1, and R_3) is designed to keep the base of Q_1, at about 0.7V, ensuring that Q_1 conducts. Now suppose a positive pulse is applied to R, it will cause Q_2 to conduct. As collector of Q_2 falls to '0', it cuts Q_1 OFF and bistable multivibrator switches to its other state.

Q.73 What is flip-flop? Explain the principle of operation of S-R flip-flop with truth table. **(7)**

Ans:

For a sequential system, we must know what has happened in the past. Therefore we must have storage device to retain this information until we are ready to use it. The basic unit of this storage is flip-flop. It is a device with two stages i.e., the output is either '0' (logic 0) or +5V dc (logic 1).

A flip-flop maintains its output state until directed by an input signal to change its state. This means that it can store 1-bit information.

S-R flip-flop:

It uses a pair of cross coupled transistors as shown in Fig. 36a. When, transistor T1 is in saturation then its collector voltage is the base drive for transistor T2, i.e., no base drive for T2. Hence T2 is cutoff and its collector voltage is approximately + V_{CC} (logic 1). This drives the base of T1 and thus T1 operates in saturation region.

R	S	Q
0	0	No change
0	1	1
1	0	0
1	1	Invalid

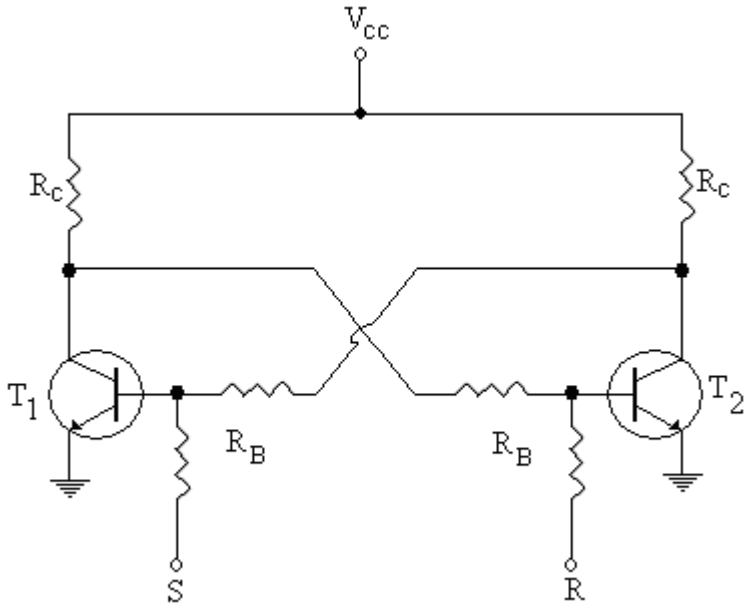


Fig. 36a

In effect T2 is OFF and T1 is ON making Q=1(+Vcc). Similarly if T2 is in saturation T1 is OFF resulting Q=0. By introducing one input at the base of each transistor we can control the state of operation of the transistor.

Q.74 Explain with a neat diagram the working of a BCD counter **(7)**

Ans:

BCD decade counter goes through a straight binary sequence from 0000 to 1001 state. Then recycles back to 0000 state. The circuit of a BCD counter is given in fig.

States of BCD decade counter:

FlipFlop-A toggles on each clock pulse so that logic equation for its J and K inputs is

$$J_A = K_A = 1$$

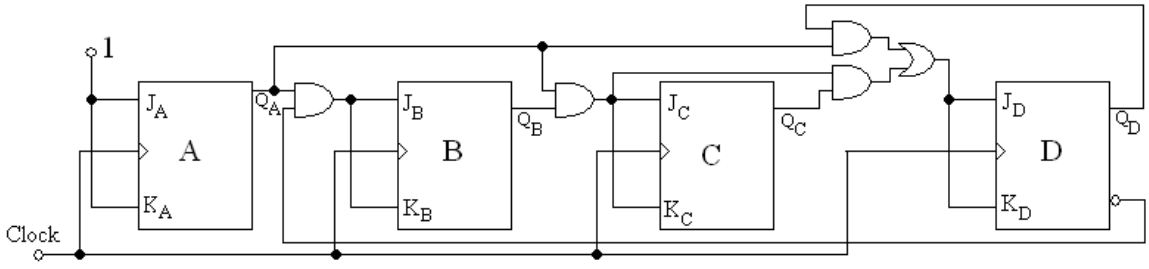


Fig. – A BCD counter

This is implemented by connecting these inputs to a constant high level.

FlipFlop-B changes state on next clock pulse each time $Q_A = 1$ and $Q_D = \overline{1}$ so that

$J_B = \overline{K_B} = Q_A Q_D$.

This is implemented by ANDing Q_A and $\overline{Q_D}$ and connecting the gate output to JK inputs of FlipFlop -B.

Clock	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

FlipFlop-C changes on next clock pulse each time both $Q_A = 1$ and $Q_B = 1$

$J_C = K_C = Q_A Q_B$

This is implemented by ANDing Q_A and Q_B and connecting gate output to JK inputs of FlipFlop F-C.

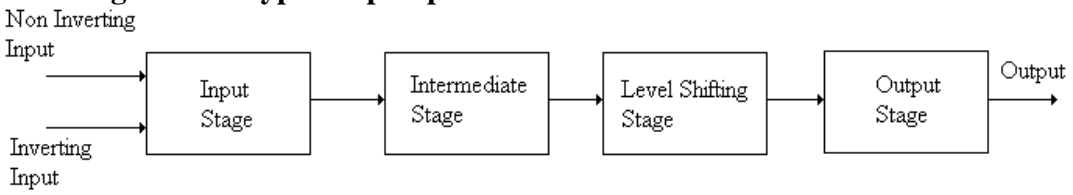
FlipFlop -D changes on next clock pulse each time $Q_A = 1$ and $Q_B = 1$, $Q_C = 1$ or when $Q_A = 1$ and $Q_D = 1$

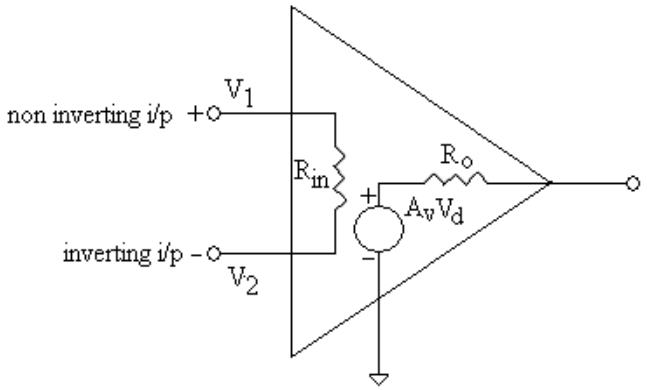
$J_D = K_D = Q_A Q_B Q_C + Q_A Q_D$

Q.75 Draw the block schematic of a typical operational amplifier and briefly explain the function of each block. Also give the equivalent circuit of the opamp. **(9)**

Ans:

The block diagram of a typical opamp





Equivalent circuit of the opamp

The first –stage is double-ended high-gain differential amplifier. In this stage high-gain is desirable so that there would be a negligible effect on the output of any shortcoming in the following stages. Also this stage determines the input resistance of the op-amp.
The second stage is usually another differential amplifier, which is driven by the output of first stage. In most amplifiers the intermediate stage is dual input, unbalanced output differential amplifier in order to increase the gain. In this amplifier output is measured at the collector of only one of the two transistors with respect to ground. In the quiescent condition some dc- voltage exists at the output terminal and there is no other collector voltage at output to balance or nullify this output dc voltage.
The third stage, known as level shifting stage, is usually an Emitter-follower circuit in order to shift dc-level at the output of the intermediate stage downward to zero volts with respect to ground. Here error signals is developed in the intermediate stage due to direct coupling and gets amplified in the succeeding stages. This increase in dc-level tends to shift the operating point of the succeeding stages which also limits the output voltage swing or may distort the output signal.
The final stage is usually a push-pull complementary amplifier. This stage increases the output voltage swing and current supplying capability of the amplifier. A well designed output stage also provides low output resistance.

Q.76 Draw the circuit of a monostable multivibrator using op-amp. Describe its operation and derive an expression for its pulse period. **(10)**

Ans:
Monostable multivibrator circuit using op-amp can be drawn as in the Fig. 38a(i). The circuit remains in its stable state until a triggering signal causes a transition to the quasi stable state.

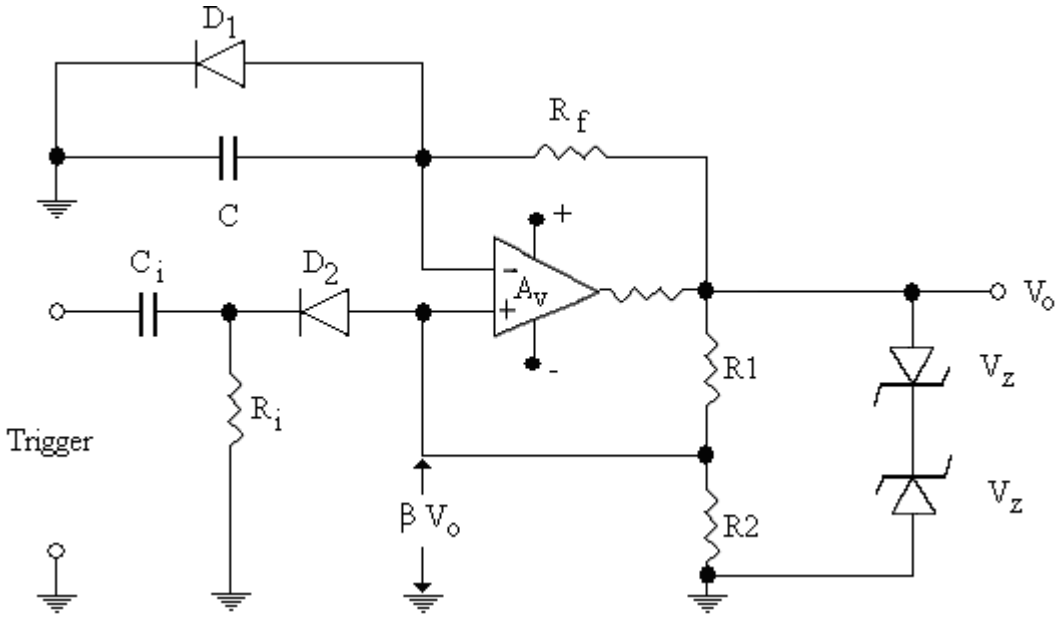


Fig. 38a(i)

At stable state $V_o = +V_z$ and C is clamped at $V_c = V_d = 0.7V$.
By trigger of suitable duration and amplitude, output will switch to $V_o = -V_D$. The capacitor will charge through R_f towards $+V_z$ as D_1 becomes reverse biased.

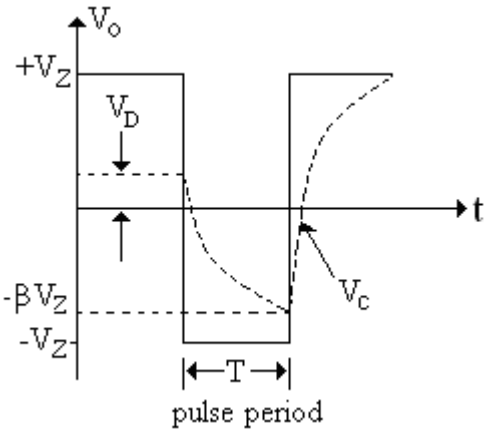


Fig. 38a(ii)

When $V_c < -\beta V_z$, the comparator again swings back to $+V_z$ and capacitor C will charge towards $+V_z$ until $V_o = V_D$ where 'C' will be clamped again at V_D

Derivation:

Charging from V_D to $-V_z$: $V_c = -V_z + (V_D + V_z)\, e^{-t/\tau}$

Where $\tau = R_f C$.

At t = T, $V_c = -\beta V_z$. Hence $-\beta V_z = -V_z + (V_D + V_z)\, e^{-T/\tau}$

Solving for T, we get $T = R_f C \ln [(V_D+V_z)/ (V_z- \beta V_z)] = R_f C \ln [(1 + V_D/ V_z)/ 1-\beta]$

Q.77 Show how the monostable multivibrator circuit you have drawn can be converted to astable type by simple changes in the monostable circuit. **(4)**

Ans:

Removing triggering circuit, D_2 and D_1 from the circuit shown in Q.76, we can convert monostable multivibrator to astable multivibrator as shown in Fig. 38b**.**

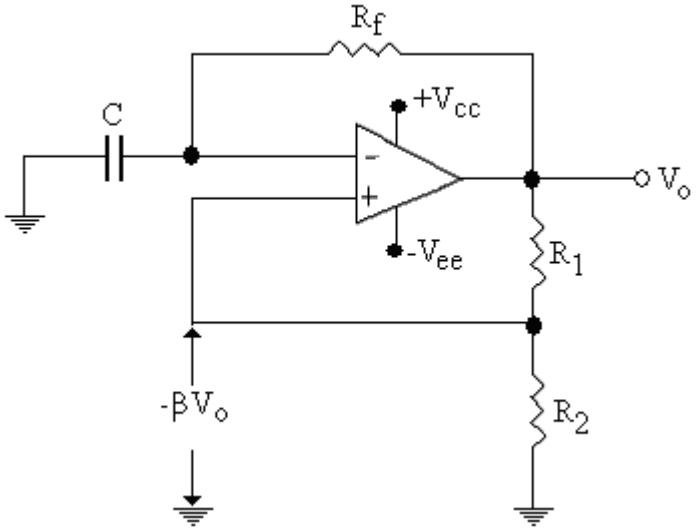


Fig. 38b.

Q.78 Sketch the circuit of a bridge rectifier and describe its operation. Derive expressions for rectification efficiency and ripple factor of the circuit. If a capacitor is added to the circuit, show the output voltage waveform of the rectifier. **(8)**

Ans:
The bridge rectifier circuit is as shown in Fig. 39a(i).

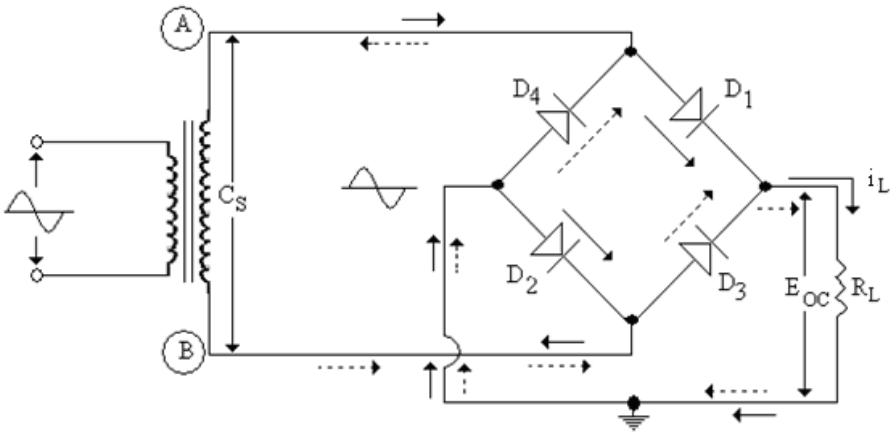


Fig. 39a(i)

Operation: During positive half cycle of the input voltage point A becomes positive. Diodes D_1 and D_2 will be forward biased and D_3 and D_4 reverse biased. D_1 and D_2 conduct in series with the load and the current flows in the direction as shown in figure1 by solid arrows.
In the next half cycle, when the polarity of the ac voltage reverses, 'B' becomes positive D_3 and D_4 are forward biased, while D_1 and D_2 are reverse biased. D_3 and D_4 conduct in series with the load and the current flows as shown by dotted arrows.
During both the half cycles of input signal, the current through R_L is in same direction and is as shown in Fig. 39a(ii).

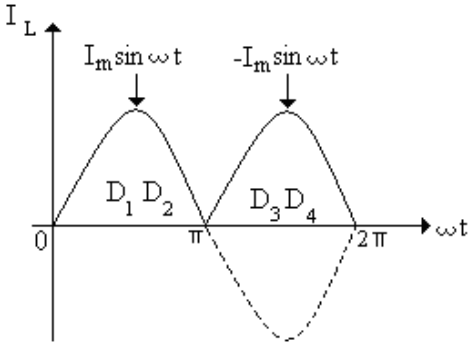


Fig. 39a(ii)

Expression for efficiency and ripple factor:

$i_L = I_m \sin \omega t \quad 0 \le \omega t \le \pi$

$i_L = -I_m \sin \omega t \quad \pi \le \omega t \le 2\pi$

$$I_{dc} = (1/\pi) \int_0^{\pi} I_m \sin \omega t \, d(\omega t)$$

$I_{dc} = 2I_m / \pi$ and $E_{dc} = 2E_m / \pi$

$$I_{RMS} = \sqrt{\left(\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d\omega t\right)} = \sqrt{\left(\frac{2}{2\pi}\int_0^{\pi} (I_m \sin\omega t)\right)^2 d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi}\int_0^{\pi} [(1-\cos 2\omega t)/2]\, d(\omega t)} = I_m/\sqrt{2}$$

In bridge rectifier, in each half cycle two diodes conduct simultaneously. Hence maximum value of load current is

$I_m = E_m / (R_s+2R_f+R_L)$, where R_s = transformer secondary winding resistance.

$P_{DC} = I_{DC}^2 R_L = (2I_m/\pi)^2 R_L$

$P_{AC} = I_{rms}^2 (2R_f+R_s+R_L) = (I_m/\sqrt{2})^2 (2R_f+R_s+R_L)$

Therefore, rectification efficiency $= P_{DC}/P_{AC} = \dfrac{[(4I_m^2/\pi^2) R_L]}{I_m^2/2\,(2R_f+R_s+R_L)} \approx \dfrac{8R_L}{\pi^2 R_L}$ (since $2R_f+R_s << R_L$)

$= 8/\pi^2 = 81.05\%$

Ripple factor $= \sqrt{(I_{rms}/I_{DC})^2 - 1}$

$= \sqrt{[(I_m/\sqrt{2})/(2I_m/\pi)]^2 - 1} = \sqrt{(\pi^2/8) - 1} = 0.48.$

The Fig. 39a(iii) shows how a capacitor filter is connected to the rectifier output and the output voltage waveform of the rectifier across the load, with capacitor filter.

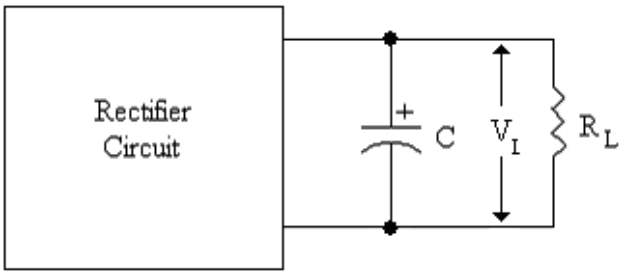


Fig. 39a(iii)

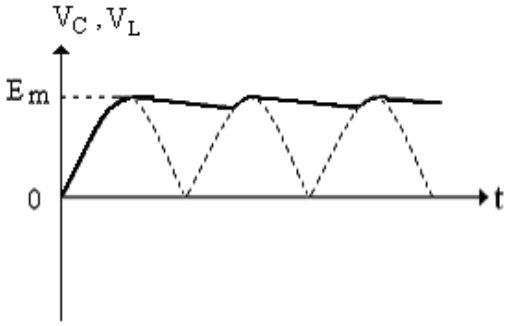


Fig. 39a(iv)

The dotted line in Fig. 39a(iv) shows the rectifier output without filter and solid line shows the output across the capacitor filter.

Q.79 Describe using a neat circuit diagram, the operation of a transistor series voltage regulator. **(6)**

Ans:

Fig. 39b shows the circuit of a transistor series voltage regulator.

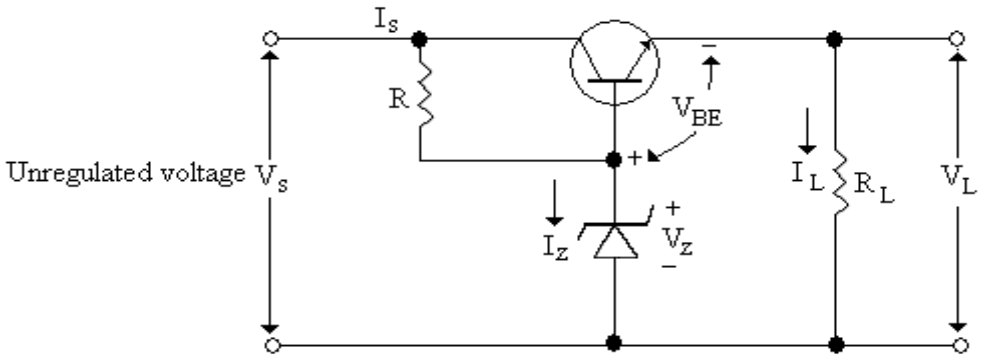


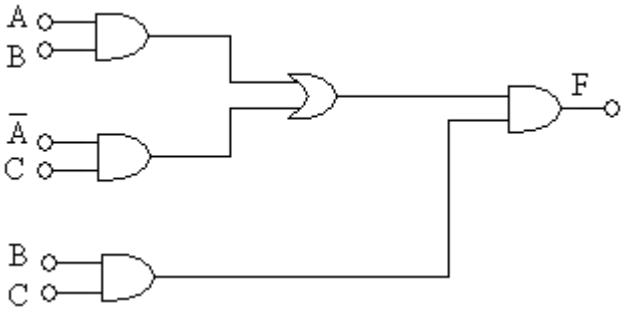
Fig. 39b

In the above circuit, transistor behaves as an emitter follower. i.e it behaves as a variable resistor whose value is determined by the base current. The load voltage V_L is equal to the difference of zener voltage (V_z) and the base to emitter voltage V_{BE}.

i.e $V_L = V_z - V_{BE}$ or $V_{BE} = V_z - V_L$

Any increase in V_L decreases V_{BE} as V_z is fixed. Therefore the forward bias of the transistor is reduced, which reduces the level of conductance. Due to this V_{CE} of transistor increases which in turn slightly decreases the input current to compensate for the increase in the value of load resistance, so load voltage may remain at a constant value.

Q.80 Prepare the truth table for the output 'F' of the logic circuit shown in figure below. Write also the canonical SOP expression for F.



Ans:

The truth table for the above expression is as shown below.

A	B	C	AB	$\bar{A}C$	$AB+\bar{A}C$	BC	$(AB+\bar{A}C)BC$
0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	0
0	1	0	0	0	0	0	0
0	1	1	0	1	1	1	1
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	1	1

The canonical SOP expression for F is found from 1's in the 4^{th} and 8^{th} rows.

i.e. F (A,B,C) = $\bar{A}BC + ABC$

Q.81 Write the logic diagram and truth table of clocked S-R flip flop and explain its operation. What are the drawbacks of S-R flip flop? **(6)**

Ans:

Fig. 41a(i) shows clocked RS flip flop. It consists of a basic NOR gate and two AND gates. The outputs of the two AND gates remain at '0', regardless of the R and S inputs as long as Cp=0.When the clock pulse goes to '1', information from the R and S inputs are allowed to reach the basic flip flop.

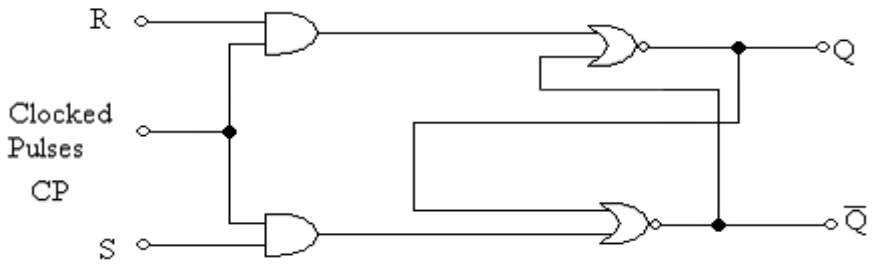


Fig.41a(i)

Fig. 41a(ii) shows truth table for clocked RS flip flop. The waveforms in Fig. 41a(iii) illustrate the operation of clocked RS flip flop.

Cp	S	R	Q	$\bar{Q}$	State
0	0	0	NC	NC	No Change
0	0	1	NC	NC	No Change
0	1	0	NC	NC	No Change
0	1	1	NC	NC	No Change
1	0	0	NC	NC	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1/0	1/0	Indeterminate

Fig. 41a(ii)

Drawbacks of SR flip-flop:

i) A 11 input (R =S =1) is not allowed as it will make both Q and $\bar{Q}$ = 1 while the clock pulse is 1. The state of output will be unpredictable when C_p goes to '0'.

ii) While clock pulse is 1, change in inputs changes the output.

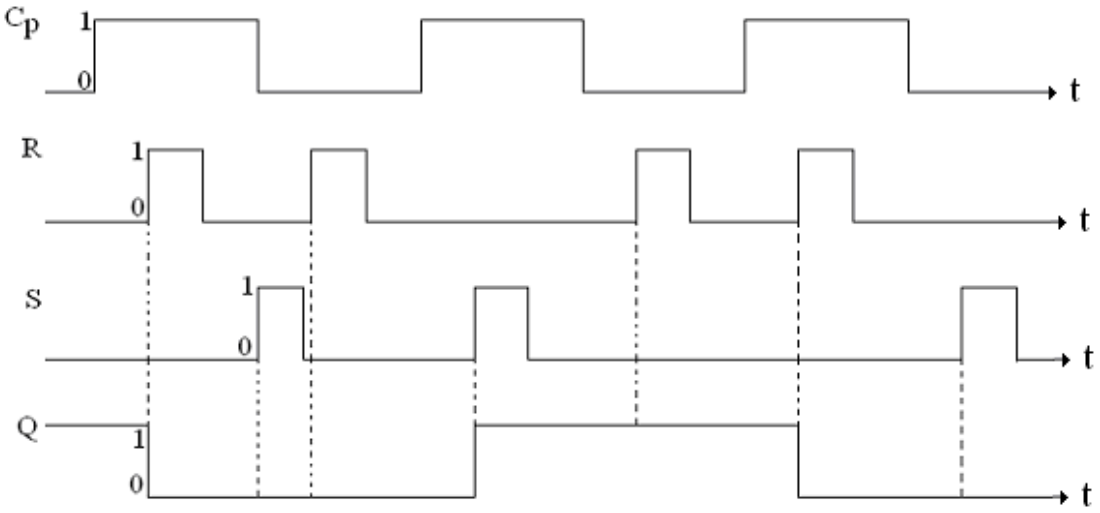


Fig. 41a(iii)

Q.82 Construct a 4-bit binary ripple counter using suitable flip-flop and describe its working? **(6)**

Ans:

Fig. 41b shows the circuits of a 4-bit ripple counter consisting of edge-triggered flip-flop (JK).

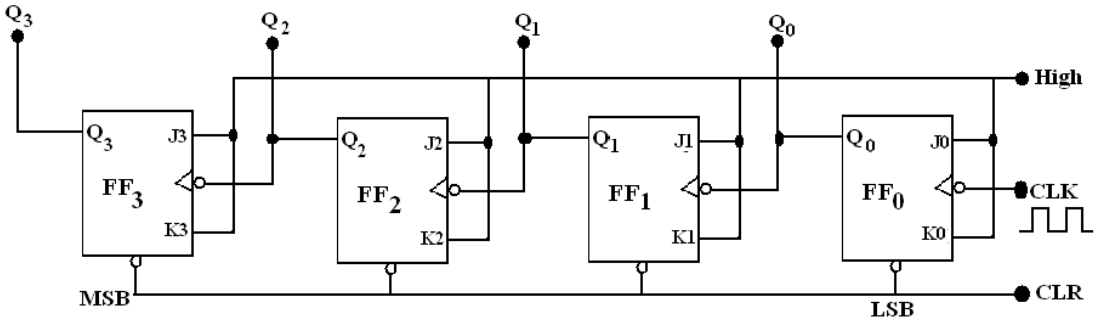


Fig. 41b

In this ripple or asynchronous counter, the clocking for all flip-flops except the one at the LSB is obtained by the transition of the flip-flop at the previous stage. By keeping J=K= 1 all flip flop's are ready to change state at the arrival of clock pulse which is effective only when a transition from 1 to 0 takes place. Flip-flops as shown are sensitive to negative edge of clock signal. The output of one stage acts as a clock to the next stage. For each negative transition of a clock, Q_0 changes its state. Q_1 changes its state for every 1 to 0 transition of Q_0. Q_2 changes its state for every 1 to 0 transition of Q_1. Similarly Q_3 changes its state for every 1 to 0 transition of Q_2. The truth table is as follows:

Clk	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0

Clk	Q_3	Q_2	Q_1	Q_0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Q.83 What is 'doping' of a semiconductor? Explain how p- and n-type semiconductors are formed. Also write their energy band diagrams, clearly showing the different energy levels. **(8)**

Ans: pp 102 - 104

Q.84 What is Early effect? Explain how it affects the characteristics of BJT in CB configuration. **(8)**

Ans: p. 238 - 39

Q.85 Draw a neat circuit of a differential amplifier and explain its operation. **(8)**

Ans: p. 450 – 52

Q.86 Explain the effect of temperature on a JFET. **(8)**

Ans: p. 276.

Q.87 Describe how oscillations are developed in a tank circuit.

Ans: p. 655

Q.88 Define the following terms as applied to characterisation of opamps.
(i) CMRR (ii) slew rate

Ans: p. 800, p. 826

Q.89 Draw a neat diagram to show the functional blocks of a complete regulated power supply. Explain the role of each block. **(9)**

Ans: p. 908 – 09.

Q.90 Draw the circuit of 4-bit ring counter using suitable flip-flop. Explain its operation using timing diagrams and truth table. **(8)**

Ans: p. 1021

Q.91 Show how a T-flop-flop can be constructed using J-K flip-flop. Write the truth table of T flip-flop. **(2)**

Ans: p. 1016

Q.92 Distinguish between avalanche and zener breakdown in p-n junction diode. **(7)**

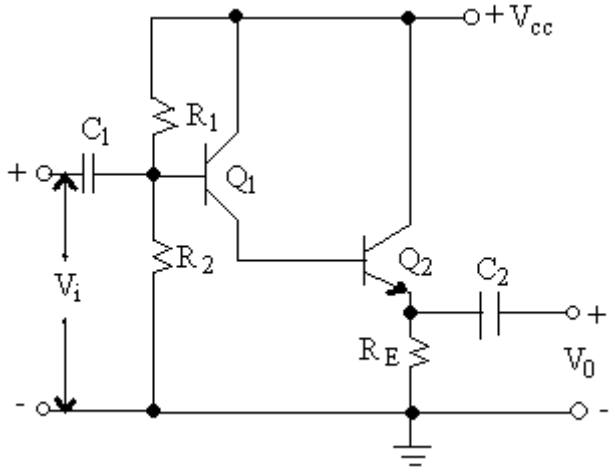
Ans:

Both avalanche breakdown and zener breakdown occur under reverse biased condition of p-n junction and the common cause is the electric field accelerating a carrier which collides with an ion and breaks the covalent bond releasing one or more extra carriers. In the case of avalanche breakdown, the carriers are thermally generated ones accelerating under externally applied large electric field in reverse bias and the process is cumulative giving rise to more and more pairs of carriers by multiple collision of ions. The result is destructive.

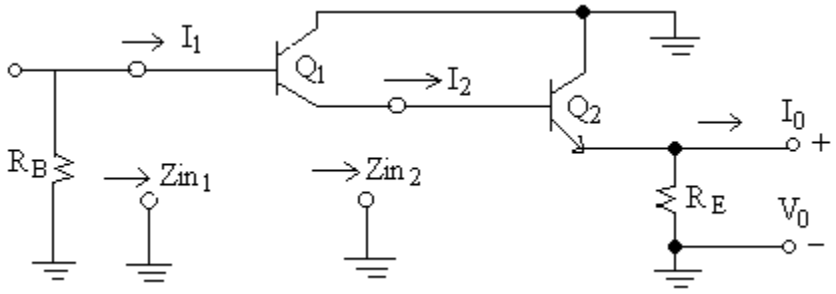
On the other hand, in a zener diode, the breaking of ionic bond and generation of extra carriers is by the intense electric field across a very narrow depletion region at the junction, due mainly to rather heavy doping of both p and n regions of the diode. The resulting process gives rise to large reverse current and is reversible. This phenomenon is called 'Zener breakdown'.

Q.93 Draw the circuit of Darlington amplifier and analyse it to obtain expressions for its current gain and input impedance. Also mention its merits and application. **(10)**

Ans: The circuit for Darlington amplifier is shown below



The equivalent circuit for small signal is as shown below



Considering Q_2, $Zin_2 = hfe_2\ R_E$ ……(1)

Current Gain: $A_{i2} = I_0e2 / I_2 = I_{e2} / I_{b2} \simeq hfe_2$ …..(2)

For transistor Q_1, $1/h_{oel}$ is comparable with becomes the load impedance for Q_1. Hence without neglecting $1/h_{oel,}$ the current gain for Q_1 is

$$A_{i1} = \frac{I_2}{I_1} = \frac{h_{fe1}}{1+h_{Oe1}Z_{in2}} = \frac{h_{fe1}}{1+h_{Oe1}(h_{fe2}R_E)} \quad \ldots\ldots(3)$$

If $h_{fe1} = h_{fe2}$ and $h_{oe1} = h_{oe2} = h_{oe}$, equation (3) can be written as

$$A_{i1} = \frac{h_{fe}}{1+h_{oe}\left(h_{fe}R_E\right)} \text{ and } Ai_2 = h_{fe}$$

The overall gain of the amplifier is $A_i = A_{i1}Ai_2$

$$\text{i.e., } A_i = \frac{h_{fe}{}^2}{1+h_{oe}h_{fe}R_E} \quad \ldots\ldots(4)$$

For $h_{oe}h_{fe}R_E \le 0.1$, a good approximation would be ignored w.r.t Zin_2, …..(5)

Input impedance

$$Zin_1 = h_{fe1}\left(Zin_2 \parallel \frac{1}{h_{oe1}}\right) = h_{fe1}\left(h_{fe2}R_E \parallel \frac{1}{h_{oe1}}\right)$$

$$= \frac{h_{fe1}h_{fe2}R_E}{h_{Oe1}h_{fe2}R_E + 1}$$

If $h_{fe1} = h_{fe2} = h_{fe}$ and $h_{oe1} = h_{oe2} = h_{oe}$ then

$$Zin_1 = \frac{h_{fe}{}^2R_E}{h_{Oe}h_{fe}R_E}$$

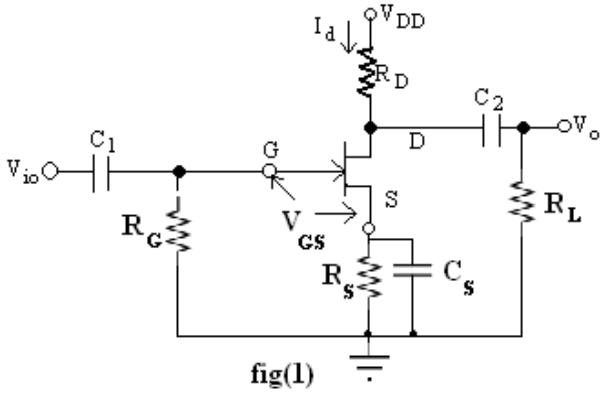
if $h_{oe}h_{fe}R_E \le 0.1$, then $Zin_1 \cong h_{fe}{}^2R_E = \beta^2R_E$

The advantage of darlington amplifier is its very high current gain and very high Zin. It is used to isolate high impedance source from low impedance load.

Q.94 Draw the circuit of common source amplifier using JFET and show its equivalent circuit. Analyse the equivalent circuit to find an expression for voltage gain and output resistance. **(6)**

Ans:

The circuit of n-channel, JFET common source amplifier is shown below in fig(1) and its ac equivalent circuit is shown in fig(2).



fig(1)

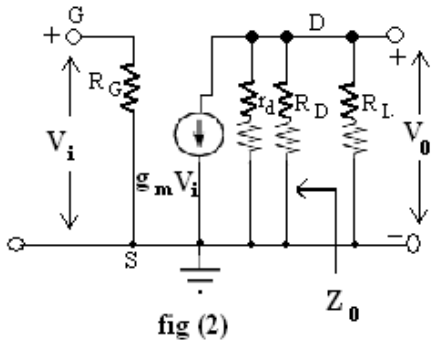


fig (2)

Fig(2) shows current source equivalent circuit where gm Vi represents controlled source and rd represents the incremental drain resistance. The output impedance Zout of the amplifier is given by the parallel combination of rd RD

i.e. $Z_O = R_D \parallel r_d = \dfrac{R_D r_d}{R_D + r_d}$

The voltage gain is found as follows:

$$V_o = g_m V_i (r_d \parallel R_D \parallel R_L)$$

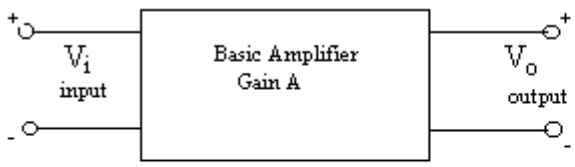
The voltage gain, $A_v = \dfrac{V_o}{V_i} = -g_m (r_d \parallel R_D \parallel R_L)$

Or $A_v = -g_m \dfrac{Z_o R_L}{Z_o + R_L}$.

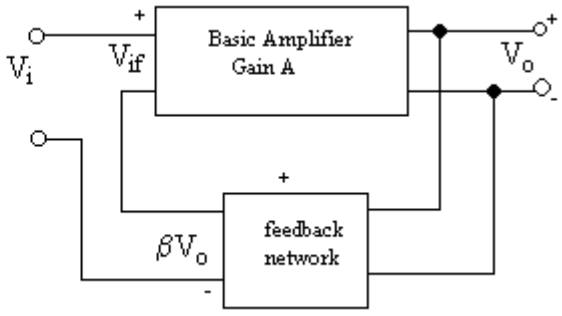
Q.95 For an amplifier having open loop gain A, find an expression for gain with negative feedback of feedback ratio β. Show how stabilization of gain of an amplifier is achieved with negative feedback. **(6)**

Ans:

An amplifier block without any feedback is shown in fig(1). If to this amplifier negative(voltage) feedback is provided, the situation is shown in fig(2).



Fig(1)



Fig(2)

In the basic amplifier, the gain is A i.e. $A = V_o / V_i$ which is now called the open loop gain. In fig(2), it is shown that a fraction of the output voltage (i.e. βV_o) is added negatively (i.e.

negative feedback) to the signal input V_i so that the actual input to the basic amplifier is $V_i - V_f = V_i - \beta V_o$. Thus by the basic amplifier characteristic

$A(V_i - \beta V_o) = V_o$,i.e. $AV_i - A\beta V_o = V_o$

i.e. $AV_i = V_o(1+A\beta)$ or $\frac{V_0}{V_i} = \frac{A}{1+A\beta} = V_i$

where Af is the gain with negative feedback

i.e. $A_f = \frac{\text{Basic amplifier gain}}{1+(\text{Basic amplifier gain})\beta}$

Gain stability with negative feedback consider the expression for A_f

i.e. $A_f = \frac{A}{1+A\beta}$ .....(1)

Differentiating this expression w.r.t. A

$$\frac{dA_f}{dA} = \frac{(1+A\beta)-A\beta}{(1+A\beta)^2} = \frac{1}{(1+A\beta)^2}$$

$dA_f = \frac{dA}{(1+A\beta)^2}$ Now divide this expression by (1)

Then $A_f = \frac{A}{1+A\beta}$

This shows that though the per unit change in the gain of the basic amplifier is $\frac{dA}{A}$, the change in the gain of the overall amplifier with negative feedback is $\frac{1}{1+A\beta}$ times the same.

Generally $(1+A\beta) >> 1$ Hence considerable improvement in gain stability is effected by negative feedback.

Q.96 Show an FET source follower circuit. What type of negative feedback takes place in the circuit? Analyse the circuit to derive an expression for voltage gain with feedback. **(6)**

Ans:

An FET source – follower circuit is shown below. Its equivalent circuit for analysis is also shown.

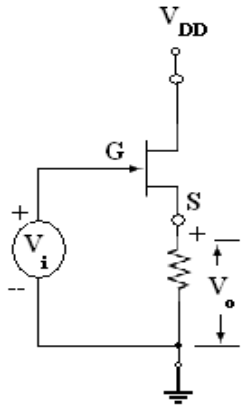
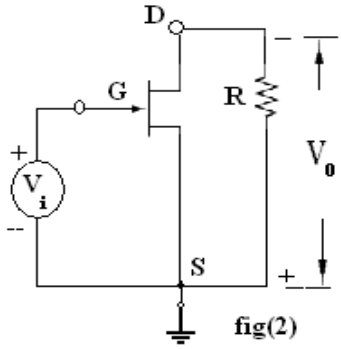


fig (1) Source follower



fig(2)

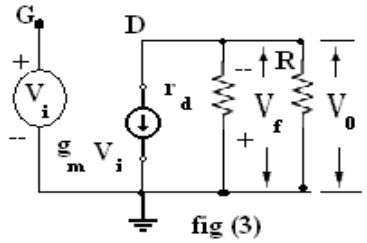


fig (3)

The sampled signal is the voltage across R which is fully fed back. Hence this is a case of voltage series feedback.

To identify the basic amplifier without feedback, let $V_o = 0$. Then V_i appears across G and S. The output circuit is found by setting $I_i = 0$. Then R is present only in the output circuit. Thus the basic amplifier is shown in fig (2).

The equivalent circuit, by replacing the FET by its low frequency model, is shown in fig(3).

It is seen that V_f and V_o are equal. Hence $\beta = \frac{V_f}{V_o} = 1$

The gain of the basic amplifier is (as $V_i = V_{GS}$)

$$A_f = \frac{V_o}{V_i} = \frac{g_m r_d V_i}{(r_d + R)V_i} = \frac{\mu R}{r_d + R} \quad \text{.....(1)}$$

where $\mu = g_m r_d$

using the general relation in a –ve f.b. amplifier

i.e. $A_f = \frac{A}{1+\beta A}$ the gain with f.b. in the source follower is

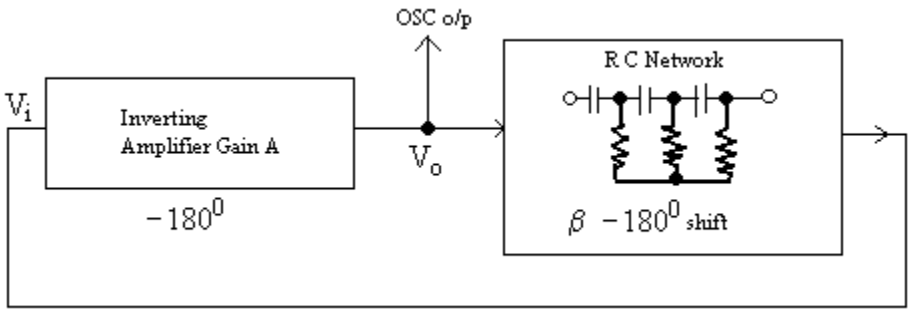
$$A_f = \frac{A}{1+\beta A} = 1 + \frac{\frac{\mu R}{r_d + R}}{1 + \frac{\mu R}{r_d + R}} = \frac{\mu R}{r_d + (1+\mu)R}$$

i.e. $A_f = \frac{\mu R}{r_d + (1+\mu)R}$ .....(2) the expression for gain of the source follower.

Q.97 Explain the principle underlying the working of R-C oscillators. Mention the applications of R-C oscillators. **(7)**

Ans:

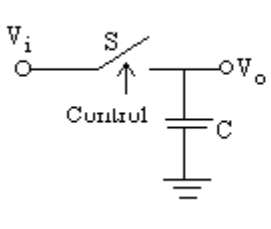
The general requirement for producing oscillations in an amplifier is to provide positive feedback so that feedback voltage is in phase with the input to the amplifier. This means there should be 2π shift in phase from input through the output and back at input. As an inverting amplifier provides π (180^0) phase shift, it can be used along with a phase shifting network that provides further π (180^0) shift at the desired frequencies as shown in the block schematic below.

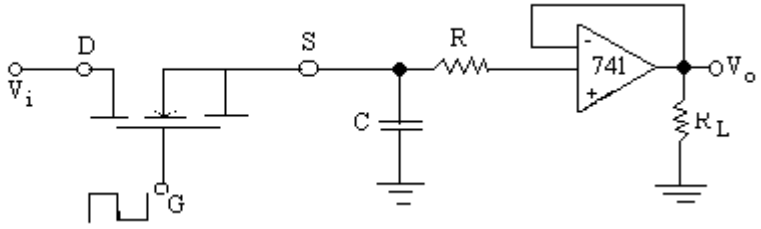


Typically, for phase shift, RC networks may be used as shown in figure. The R's and C's must be so chosen as to produce 180^0 shift at the frequency of oscillation required.
It is also necessary that the output impedance of the phase shift network must be much smaller than the input impedance of the amplifier. All these, essentially mean that Barkhausen criterion of unity loop gain i.e. $-A\beta = 1$, is network, which also means that there should be positive feedback to the basic amplifier.
Application: RC oscillators are commonly used as audio oscillators.

Q.98 Draw the circuit of sample and hold using op-amp and explain its operation. **(9)**

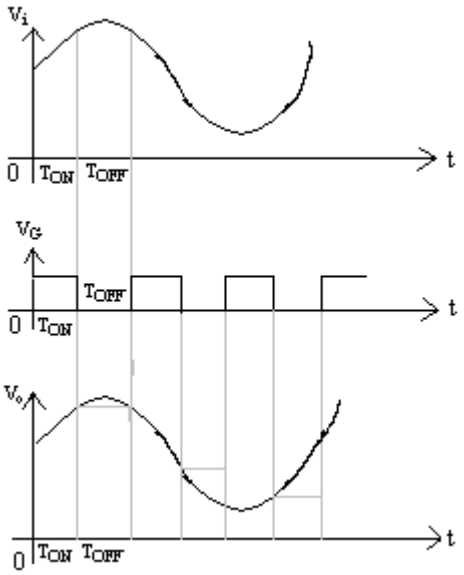
Ans:
A sample – and – hold circuit is essentially a switch in series with a capacitor, as in fig(1)





fig(1) **S/H Control voltage** **Fig(2)**

The voltage across the capacitor C tracks the input signal V_i during the time T_{ON}, when a logic control closes the switch S. The capacitor holds the instantaneous value developed on C at the end of T_{on}, when the control opens S. The switch may be a relay, a diode bridge gate, a BJT or a MOSFET controlled by a gating signal.
A S/H circuit using op – amp and an n-channel enhancement MOSFET is shown in fig(2). The analog signal V_i to be sampled is to be applied at the drain terminal of the E-MOSFET and a pulse train is applied at the gate, the MOSFET connects the drain to the source so that V_{in} is applied across the capacitor during the time the pulse is present. The action of the switch and the capacitor are illustrated in the timing diagram in fig(3).



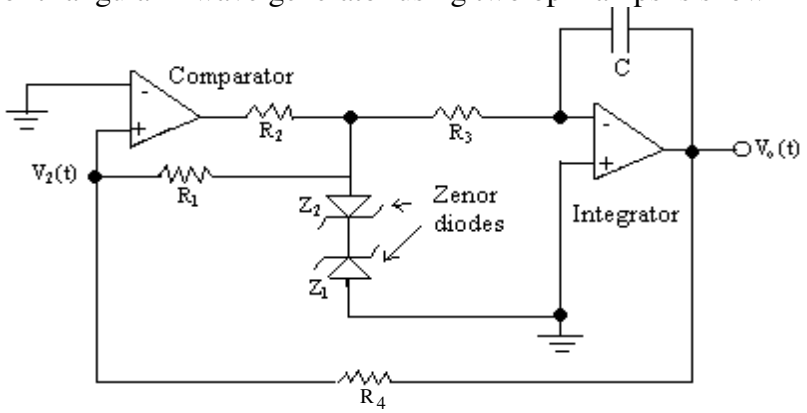
fig(3)

During the time the MOSFET is ON, the V_i appears across the capacitor and so at the output of the non-inverting amplifier as V_o. When MOSFET is off during T_{OFF}, the input is isolated from C and thee op-amp circuit. During this time, the voltage on C will be held constant at a value of V_i, which prevailed at the end of T_{ON}. The T_{ON} is often called the 'sample period' and the T_{OFF} the 'hold period'. To obtain an output that closely approximates the input, the frequency of the control voltage at the gate should be as large as possible. To retain the sampled voltage without loss, the capacitor should be of very good quality with the least charge leakage.

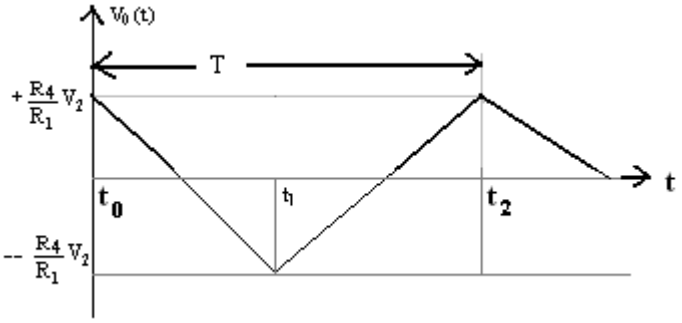
Q.99 Write a neat circuit diagram of saw-tooth wave generator using op-amps and describe its operation. Derive an expression for the frequency of the wave. **(10)**

Ans:

The circuit of triangular – wave generator using two op – amps is shown in the figure below



The operation of the circuit is explained with reference to the wave diagram shown below.



The Zener diodes will clamp the voltage V_i at either + V_z or – V_z depending on the polarity of the saturation voltage at the output of the comparator.
To begin with say $V_1 = + V_z$ at $t = t_o$
The integrator causes charging of capacitor C and $V_o(t)$ will be a ramp with negative slope.
The current into C is $I = \frac{V_z}{R_3}$ and $V_o(t)$ is given by

$$V_o(t) = V_o(t_o) - \frac{1}{C}\int_{t_o}^{t} Idt = V_o(t_o) - \frac{1}{C}(t - t_o) \qquad \text{……(1)}$$

Now the voltage $V_z(t)$ is found by using superposition

$$V_z(t) = \frac{R_4 V_z}{R_1 + R_4} + \frac{R_1 V_o(t)}{R_1 + R_4}$$

When $V_z(t)$ reaches zero at $t = t_1$, the comparator output changes to $V_1 = -V_z$. Using equation(2) to find $Vo(t_1)$,

$$V_z(t_1) = 0 = \frac{R_4 V_z}{R_1 + R_4} + \frac{R_1 V_0(t)}{R_1 + R_4}$$

i.e. $V_z(t_1) = -\frac{R_4}{R_1}V_z$ ……(3)

The direction of current into the integrator will reverse from t_1 until t_2 and is given by

$$I = \frac{-V_z}{R_3} = -I$$

During $t_2 > t > t_1$ the $V_o(t)$ will be a positive going ramp. At t_2 the output is

$$V_o(t_2) = \frac{R_4}{R_1}V_z \qquad \text{……..(4)}$$

as this value is limited by +Vz
At t2, the comparator switches its output again and the cycle repeats.
Derivation of expression for the frequency:
As seen by the analysis above and as shown in the wave diagram,

$$V(t_o) = V_o(t_2) = \frac{R_4}{R_1}V_z$$

and at $t = t_0 + t_1$, $V_0(t_0 + t_1) = \frac{R_4}{R_1}V_z$ as at equation (3)

Now using equation(1), $V_0(t_0 + t_1) - V_0(t_0) = -\frac{I}{C} t_1$

Hence $t_1 = \frac{2R_4}{R_1} V_Z \frac{C}{I} = \frac{2R_4 R_3 C}{R_1}$ by equation $I = \frac{V_z}{R_3}$

Assuming matched zener diodes i.e. $V_{z1} = V_{z2} = V_z$

We get equal magnitudes of +ve and –ve ramps

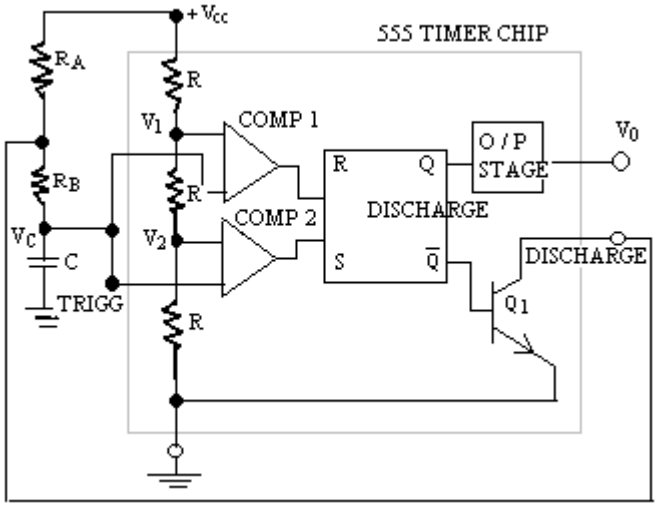
Hence the period $T = 2t_1 = \frac{4R_4R_3C}{R_1}$

The frequency of triangular waveform is therefore, $f = \frac{R_1}{4R_4R_3C}$

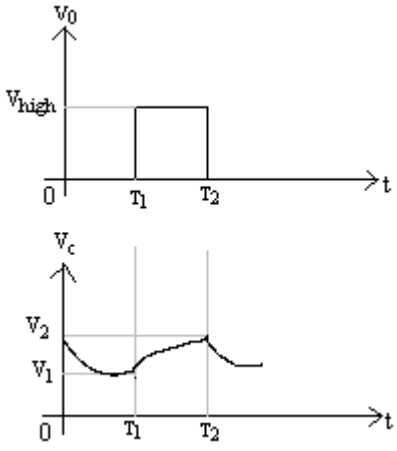
Q.100 Explain how an astable multivibrator can be implemented using 555 timer IC. **(6)**

Ans:

The connections to be made to the 555 timer IC chip and the relevant internal details are shown in the figure(1) below.



fig(1)



fig(2)

At the non-inverting inputs of comparators, the potential division of V_{cc} across the R's causes $V_1 = \frac{2}{3} V_{cc}$ and $V_2 = \frac{1}{3} V_{cc}$. The V_{cc} also charges C through R_A and R_B.

Assume that at t = 0, $V_c = V_2$, which causes comp 1 output to be high and Q output of the latch is in reset condition, which in turn makes $V_0 \simeq 0$ volts, as shown in fig 2. At the same time, as $\overline{Q} = 1$, the transistor Q_1 is 'on' causing gradual discharge of C through R_B. At t = T_1, let the value of V_c which is also 'threshold voltage' of the timer, be V_1. This will cause the output of comparator 2 to be high and thus setting the latch. The transistor Q_1 is now cut off $\overline{Q} = 0$. This leads to charging of C again and gradual rise in V_0 as shown in figure 2. At $t = T_2$, $V_c = V_2$ again which causes repetition of cycle of events described above. The duration of T1 and T2 are given by $T_1 = R_B C \ln 2$ and $T_2 - T_1 = (R_A + R_B) \ln 2$.

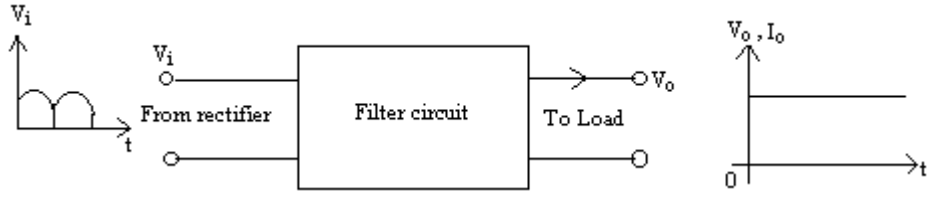
The frequency of oscillation is $f = \frac{1}{T_2}$.

Q.101 Why filters are used along with rectifiers in the construction of a power supply? List the filter types used in power supplies. Explain their effect on rectifier output waveforms. **(10)**

Ans:

Necessity of filters for rectifiers:

The output from any basic rectifiers is not a pure d.c. There would be considerable a.c. component in their output, called 'ripple', in addition to the desired d.c. component. Most sophisticated electronic systems need pure d.c. supply to drive, or power them. To construct a good power supply which gives pure d.c. output, we need to remove or filter out the a.c. component from the output of rectifiers. The output from basic rectifiers which contain a.c. component or ripple, is fed to filter circuits so that the output from the filter is pure d.c. This situation is illustrated in the figure below.



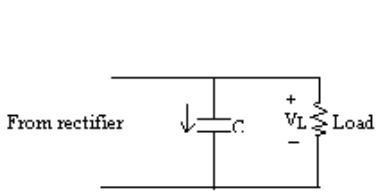
fig(1)

Following are the commonly used filter types are:

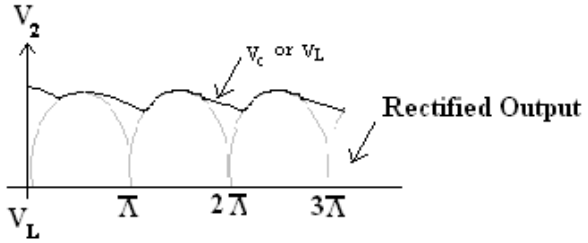
(i) Capacitor filter (ii) Series inductor filter (iii) Choke input filter (iv) π-filter (v) RC filter. Their effect on rectifier output waveforms are explained below.

(i) Capacitor filter:

It is connected in shunt or parallel with the load as shown in the fig (1)



fig(2)

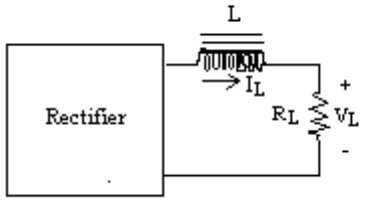


fig(3)

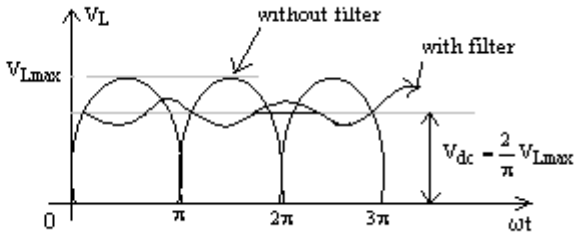
This is the simplest and the least expensive filter. A large value capacitor offers high impedance to d.c. Fig(3) shows how the capacitor helps in maintaining the load voltage as constant as possible. In the case of a full-wave rectifier without filter, the load voltage would also be the rectified waveform shown by the dotted line. But with C filter, the voltage across the load has much less ripple as shown by the full line trace.

(ii) Series Inductor filter:

Property of an inductor is to oppose any change in the current through it. An inductor can be connected to act as a filter between the load and a basic rectifier as shown in fig(4).



fig(4)

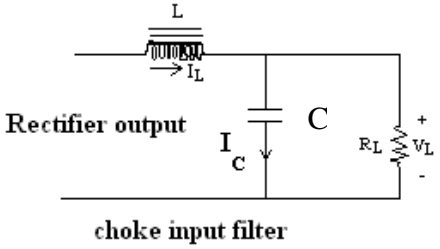


fig(5)

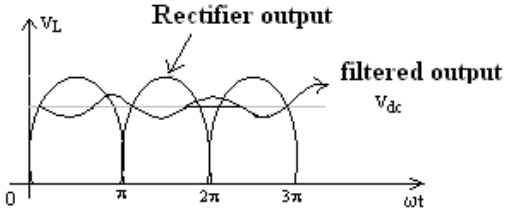
The inductor or choke stores energy in its magnetic field when the current is above an average value. The stored energy is released when the load current falls below the average value. The effect of the inductor filter is illustrated in fig 5 above.

(iii) Choke Input filter (L–Section filter):

As explained above in connection with inductor filter and capacitor filter, while capacitor acts to keep the voltage across itself constant and inductor acts to keep the current through it constant, the advantages of the properties of both an inductor and a capacitor are combined into an L-Section filter shown in fig 6.



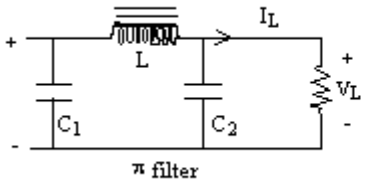
fig(6)



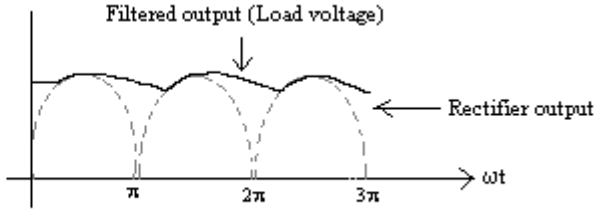
fig(7)

The effect of the L-Section filter is illustrated in fig 7. This provides d.c. output more ripple free than either C-filter alone or choke filter alone.

(iv) π-filter: The circuit of π-filter is shown in fig 8.



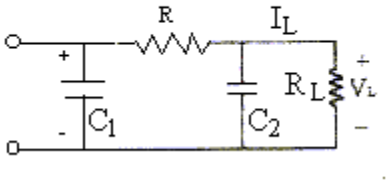
fig(8)



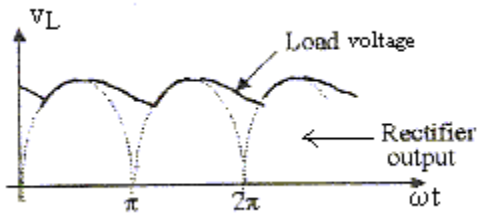
fig(9)

Because of the additional capacitor at the input of the filter, the d.c. output is of a higher value and more ripple-free than is possible by any of the filters discussed earlier. The effect of the filter on a full-wave rectifier output is illustrated in fig 9.

(v) RC-Filter: The RC filter circuit is shown in fig 10.



fig(10)



fig(11)

The disadvantages of the π-filter are its bulk, weight and higher cost. In place of L, if resistor R is used, the effect is almost similar to that obtained from π-filter. However, the R being dissipative of energy, the overall efficiency of the power supply will be less than possible with π-section filter. Also the ripple factor in this case would be poorer than in a π-section filter where an inductor is used.

Q.102 Delineate the concept of 'duality' in Boolean algebra. **(3)**

Ans:

It is the property of Boolean algebra that for a given Boolean expression there always exists a dual. Stated succinctly

Two Boolean { Functions / Expressions / tables / maps } will be called "duals" if they differ only by the simultaneous interchange of AND for OR and "0" for "1"

All postulates, theorems and axioms of Boolean algebra are to be stated in pairs, one statement being the dual of the other statement.

e.g.: The expression x + xy = x which is law of absorption has a dual x(x + y) = x.

Dual logic tables:

Table for 'OR"

x	y	x+y
0	0	0
0	1	1
1	0	1
1	1	1

If the 'I' are replaced by '0' we get the table for AND as shown on right side

Table for 'AND'

x	y	x.y
1	1	1
0	0	0
1	0	0
0	0	0

Dual K maps

Consider a function f = AC + $\overline{B}$C + BD. The K-map for this function is

CD \ AB	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	1	1	1
10	1	0	1	1

fig (1)

CD \ AB	00	01	11	10
00	1	1	1	1
01	1	0	0	1
11	0	0	0	0
10	0	1	0	0

fig (2)

If a dual map is drawn by replacing '1' by '0' and '0' by '1' as shown in, and if we simplify the function represented by the map, we get the expression

$f^d = (A + C)(\overline{B} + C)(B + D)$

$= CD + CB + A\overline{B}D$

which is the dual function f = AC + $\overline{B}$C + BD

Q.103 For the function, F(A,B,C) = Σ (1,5,7), write the canonical POS and SOP expressions. **(2)**

Ans:

Canonical SOP form is directly obtained for

$F(A,B,C) = \sum(1,5,7)\ as\ \sum(M_1 + M_5 + M_7)$

i.e. $F(A,B,C) = \overline{A}\,\overline{B}C + A\overline{B}C + ABC$ --------- canonical SOP expression.

POS expression is obtained as product of maxterms

i.e. F(A,B,C) = π (0,2,3,4,6)

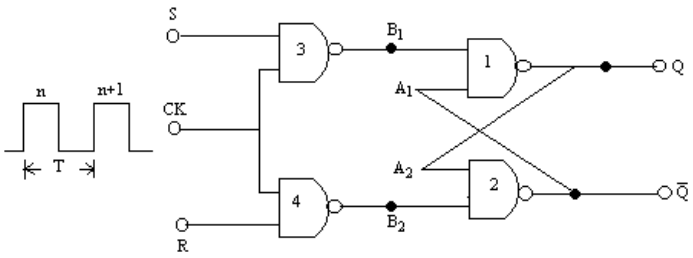
i.e. $F(A,B,C) = (A + B + C)(A + \overline{B} + C)(A + \overline{B} + \overline{C})(\overline{A} + B + C)(\overline{A} + \overline{B} + C)$

which is canonical POS expression.

Q.104 Write the logic diagram of a clocked R-S flip-flop using only NAND gates. Explain its operation with reference to truth table. **(6)**

Ans:

The logic diagram of a clocked S-R flip-flop based on NAND gates only is shown in the figure below



S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	indeterminate or undefined

Clocked S-R flip-flop

The gates 1 and 2 form the latch and the fates 3 and 4 are control or steering fates. When the clock is low of CK = 0, the outputs of both the gates are '1' irrespective of the values of S and R. The outputs Q and $\overline{Q}$ remain as they were, i.e. the flip-flop does not change state during CK = 0. Now let the CK = 1. We examine the operation for the four different combinations of S and R. For S = 0, R = 0, the outputs of 3 and 4 are 1. If Q were to be '0' (and $\overline{Q}$ = 1) there will not be change in the value of Q or the state of the flip-flop. This is indicated in the truth-table, at the first row.

For S = 1, R = 1, the inputs to 1 and 2 will be $A_1 = B_1 = 0$, and $A_2 = B_2 = 1$. For these inputs the Q is 1. That is, even if Q were to be 0 before clock is active, it will be forced to be 1. This action is called 'setting' the flip-flop and is indicated at the second row of the truth-table.

Next for S = 0, R = 1, the condition is seen to be the opposite of the one that prevailed when S = 1; R = 0.

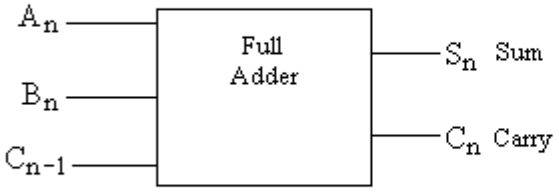
Thus Q will be forced to be at logical zero and $\overline{Q}$ = 1. This is indicated at the third row of the truth-table.

For S = 1, R = 1, the outputs from both 3 and 4 are zero and therefore the outputs of the both the gates 1 and 2 are '1'. This condition is logically inconsistent. Hence the state of the flip-flop is unidentified or indeterminate. Therefore, S = R = 1 input combination is forbidden, which is indicated in the fourth row of the truth-table.

Q.105 Write the truth table for full adder and show its implementation using gates. **(5)**

Ans:

The requirement of a full adder is indicated in the block shown below.



Truth-table

Inputs			Outputs	
A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A full adder is required to perform addition of added and augend bits at the same digit position of two binary numbers, taking into account any carry resulting from the lower digit position. Thus considering all the possible combinations for the augend(A_n), addend (B_n) and carry(C_{n-1}) inputs, the truth-table is drawn to obtain the required 'sum' and 'carry' outputs, as shown above.

From the truth-table, the Boolean expressions for S_n and C_n are given by

$S_n = \overline{A}_n\overline{B}_nC_{n-1} + \overline{A}_nB_nC_{n+1} + A_n\overline{B}_n\overline{C_{n-1}} + A_nB_nC_{n-1}$

This cannot be simplified any further.

For finding simplified expression for C_n, a k-map is drawn as below

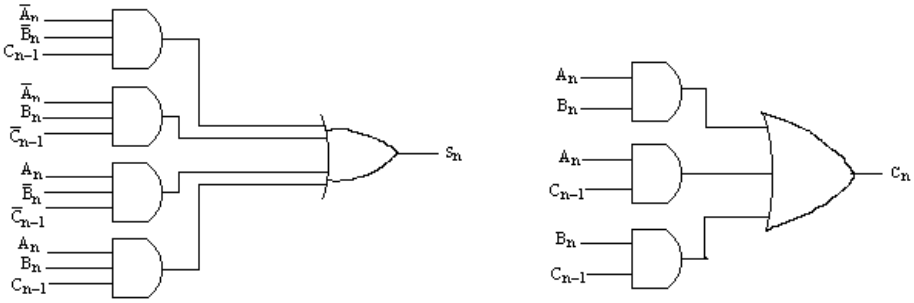
A_n \ B_nC_{n-1}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

k-map for C_n

from the map

$C_n = A_nB_n + A_nC_{n-1} + B_nC_{n-1}$

The implementations of Sn and Cn are shown by the AND – OR logic below



Q.106 In an astable multivibrator, the base registers are of 12.5 K ohm and the capacitors are of 0.01 μ ohm. Determine the PRR (pulse repetition rate).

Ans: 5772 pulses per second.

Q.107 A single-phase full-wave rectifier uses two diodes, the internal resistance of each being 20Ω. The transformer rms secondary voltage from centre tap to each end of secondary is 50V and load resistance is 980Ω. Find
(i) the mean load current. (ii) rms load current and output efficiency. **(8)**

Ans: (i) 45 mA (ii) 50 mA (iii) 79.58 %

Q.108 Simplify the following expression using Boolean algebra technique
$Z = AB + A(B + C) + B(B + C)$ **(8)**

Ans: B + AC

$Z = AB + A(B + C) + B(B + C)$
$= AB + AB + AC + BB + BC$
$= AB + AC + B(1+C)$ (∵A + A = A and B + B = B)
$= AB + AC + B(1+C)$
$= AB + AC + B$ (∵1+A = 1 AND B +1 = B)
$= B + AB + AC$
$= B(1+A) + AC$ (∵1 + A = 1 and B + 1 = B)
$= B + AC$