

Lecture 8 - PN Junction and MOS Electrostatics (V)

ELECTROSTATICS OF METAL-OXIDE-SEMICONDUCTOR STRUCTURE (*cont.*)

March 4, 2003

Contents:

1. Overview of MOS electrostatics under bias
2. Depletion regime
3. Flatband
4. Accumulation regime
5. Threshold
6. Inversion regime

Reading assignment:

Howe and Sodini, Ch. 3, §§3.8-3.9

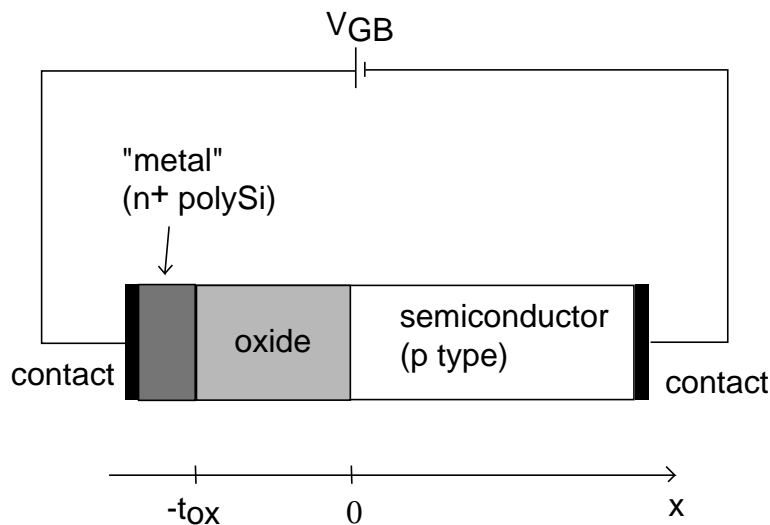
Announcements:

Quiz 1: 3/12, 7:30-9:30 PM, Walker (lectures #1-9)

Key questions

- Is there more than one regime of operation of the MOS structure under bias?
- What does "carrier inversion" mean and what is the big deal about it?
- How does the carrier inversion charge depend on the gate voltage?

1. Overview of MOS electrostatics under bias



Application of bias:

- built-in potential across MOS structure increases from ϕ_B to $\phi_B + V_{GB}$
- oxide forbids current flow \Rightarrow
 - $J = 0$ everywhere in semiconductor
 - need *drift=-diffusion* in SCR
- must maintain boundary condition at Si/SiO₂ interface: $E_{ox}/E_s \simeq 3$

How can this be accommodated simultaneously? \Rightarrow
quasi-equilibrium situation with potential build up across MOS equal to $\phi_B + V_{GB}$

Important consequence of quasi-equilibrium:

\Rightarrow Boltzmann relations apply in semiconductor

[they were derived starting from $J_e = J_h = 0$]

$$n(x) = n_i e^{q\phi(x)/kT}$$

$$p(x) = n_i e^{-q\phi(x)/kT}$$

and

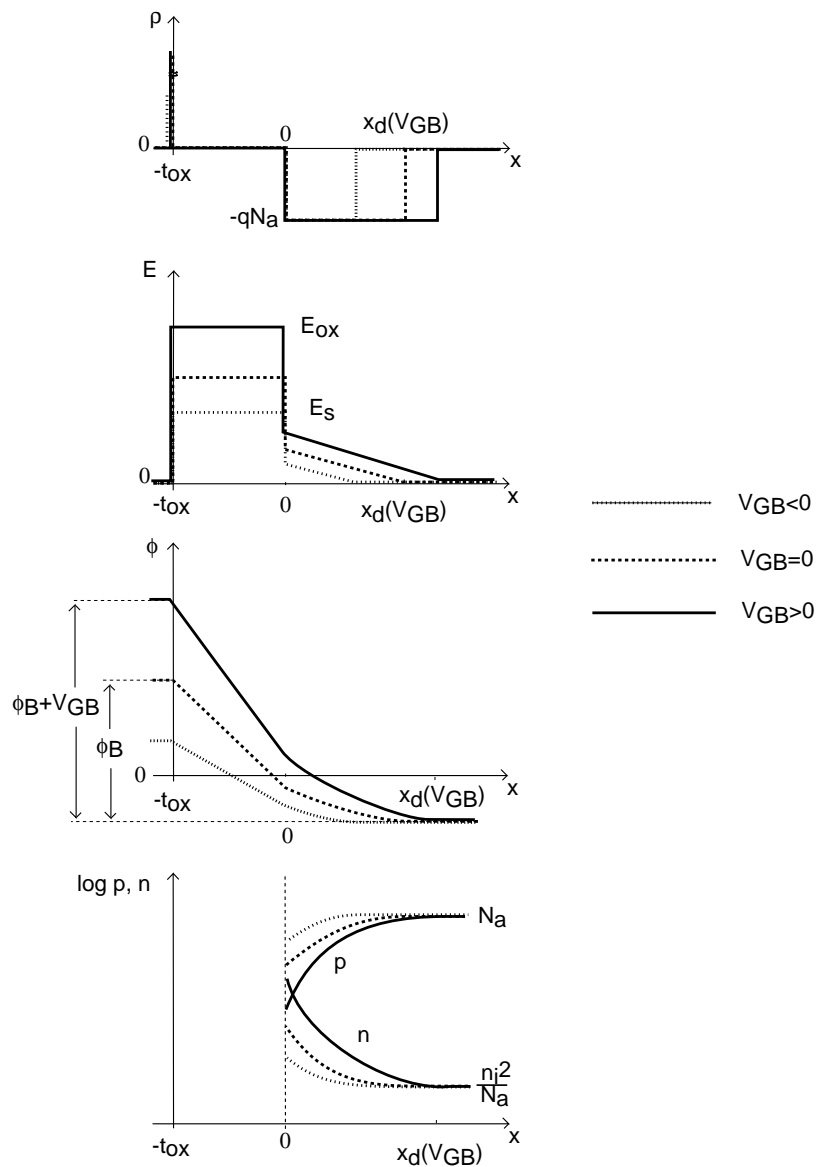
$$np = n_i^2 \quad \text{at every } x$$

[not the case in p-n junction or BJT under bias]

2. Depletion regime

For $V_{GB} > 0$ metal attracts electrons, repels holes
 \Rightarrow depletion region widens

For $V_{GB} < 0$ metal repels electrons, attracts holes
 \Rightarrow depletion region shrinks



In depletion regime, all results obtained for zero bias apply if $\phi_B \rightarrow \phi_B + V_{GB}$.

For example:

- depletion region thickness:

$$x_d(V_{GB}) = \frac{\epsilon_s}{C_{ox}} \left[\sqrt{1 + \frac{4(\phi_B + V_{GB})}{\gamma^2}} - 1 \right]$$

- potential drop across semiconductor SCR:

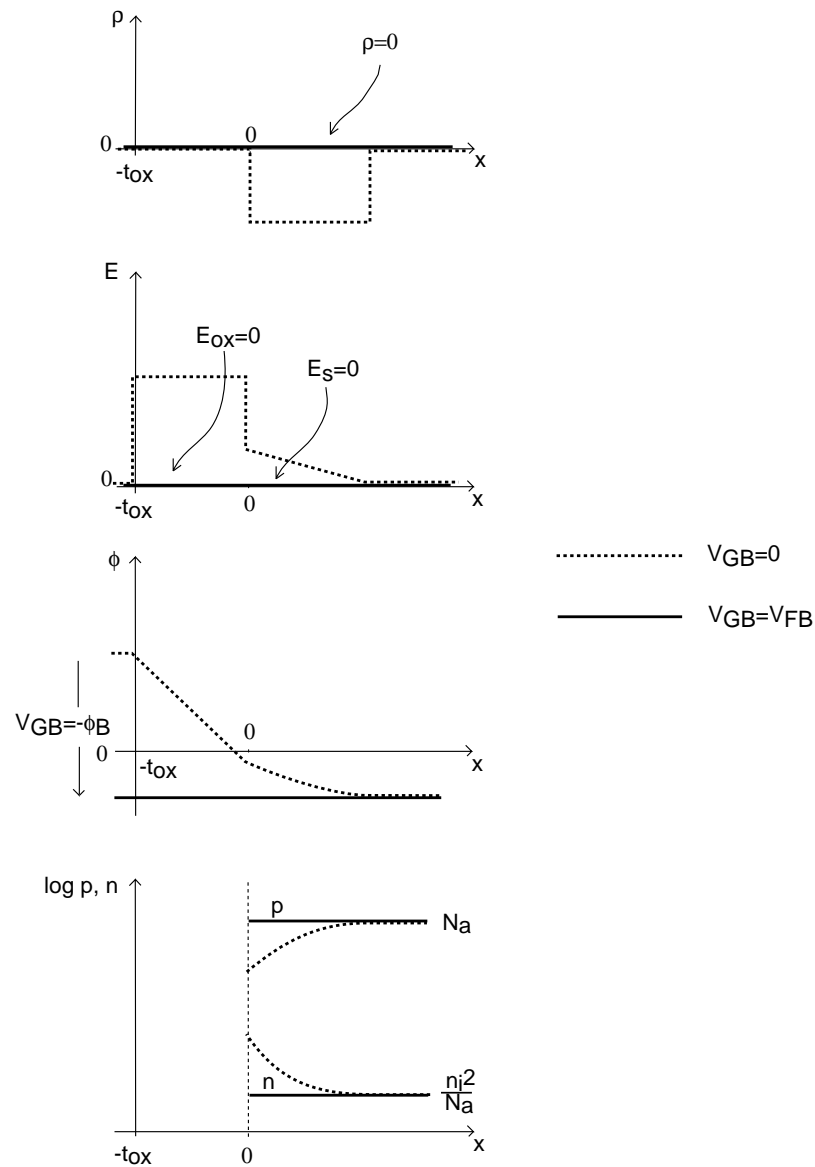
$$V_B(V_{GB}) = \frac{qN_a x_d^2(V_{GB})}{2\epsilon_s}$$

- potential drop across oxide:

$$V_{ox}(V_{GB}) = \frac{qN_a x_d(V_{GB}) t_{ox}}{\epsilon_{ox}}$$

3. Flatband

At a certain negative V_{GB} , depletion region is wiped out
 \Rightarrow *Flatband*

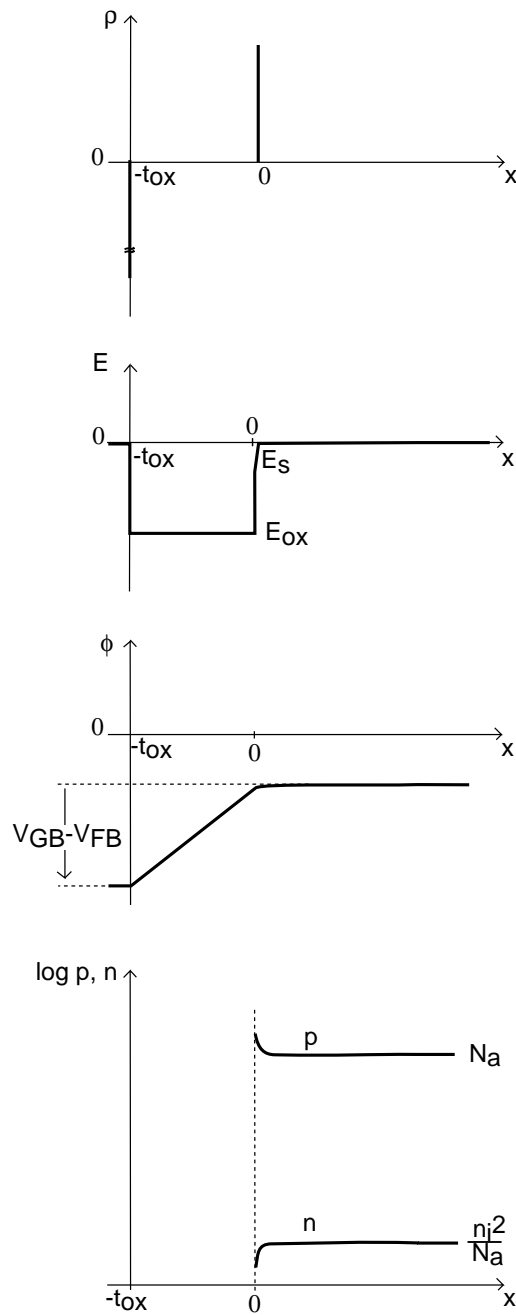


Flatband voltage:

$$V_{FB} = -\phi_B$$

4. Accumulation regime

If $V_{GB} < V_{FB}$ *accumulation* of holes at Si/SiO₂ interface

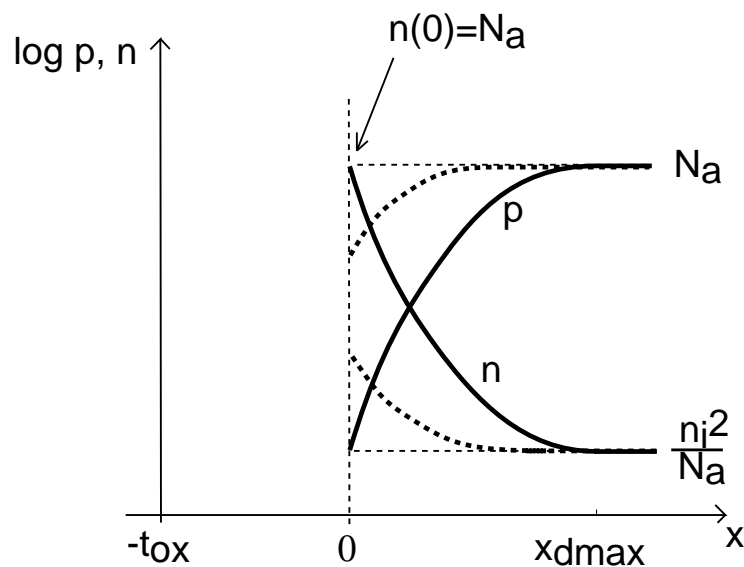


5. Threshold

Back to $V_{GB} > 0$.

For sufficiently large $V_{GB} > 0$, electrostatics change when $n(0) = N_a \Rightarrow \text{threshold}$.

Beyond *threshold*, cannot neglect contributions of electrons towards electrostatics.



Let's compute the voltage (*threshold voltage*) that leads to $n(0) = N_a$.

Key assumption: use electrostatics of depletion (neglect electron concentration at threshold).

□ Computation of threshold voltage.

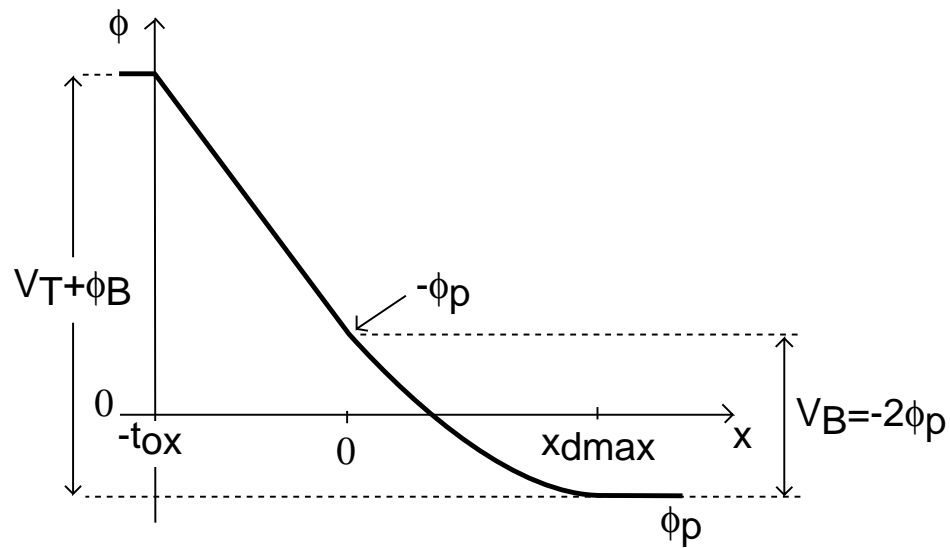
Three-step process:

• First, compute potential drop in semiconductor at threshold. Start from:

$$n(0) = n_i e^{q\phi(0)/kT}$$

Solve for $\phi(0)$ at $V_{GB} = V_T$:

$$\phi(0)|_{V_T} = \frac{kT}{q} \ln \frac{n(0)}{n_i}|_{V_T} = \frac{kT}{q} \ln \frac{N_a}{n_i} = -\phi_p$$



Hence:

$$V_B(V_T) = -2\phi_p$$

- Second, compute potential drop in oxide at threshold.

Obtain $x_d(V_T)$ using relationship between V_B and x_d in depletion:

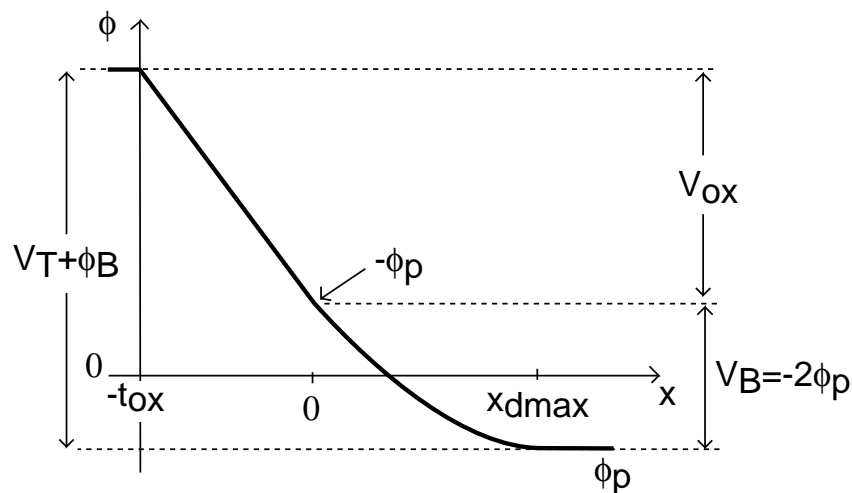
$$V_B(V_T) = \frac{qN_a x_d^2(V_T)}{2\epsilon_s} = -2\phi_p$$

Solve for $x_d(V_T)$:

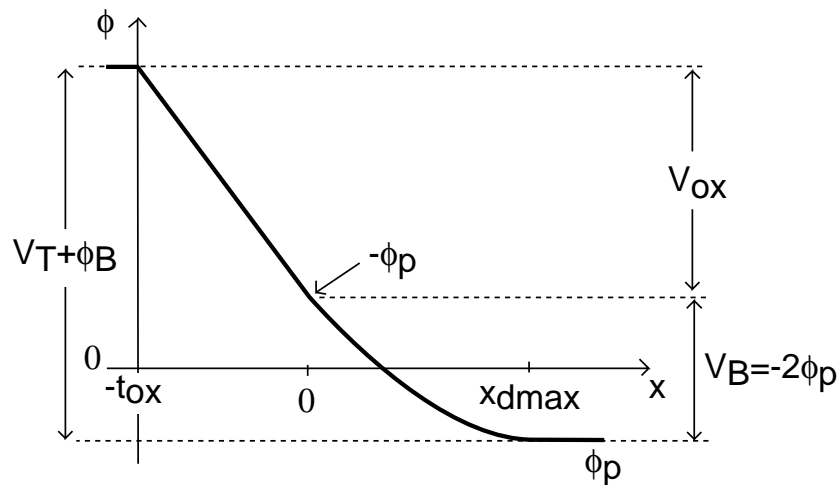
$$x_d(V_T) = x_{dmax} = \sqrt{\frac{2\epsilon_s(-2\phi_p)}{qN_a}}$$

Then:

$$V_{ox}(V_T) = E_{ox}(V_T)t_{ox} = \frac{qN_a x_d(V_T)}{\epsilon_{ox}}t_{ox} = \gamma\sqrt{-2\phi_p}$$



- Finally, sum potential drops across structure.



$$V_T + \phi_B = V_B(V_T) + V_{ox}(V_T) = -2\phi_p + \gamma\sqrt{-2\phi_p}$$

Solve for V_T :

$$V_T = V_{FB} - 2\phi_p + \gamma\sqrt{-2\phi_p}$$

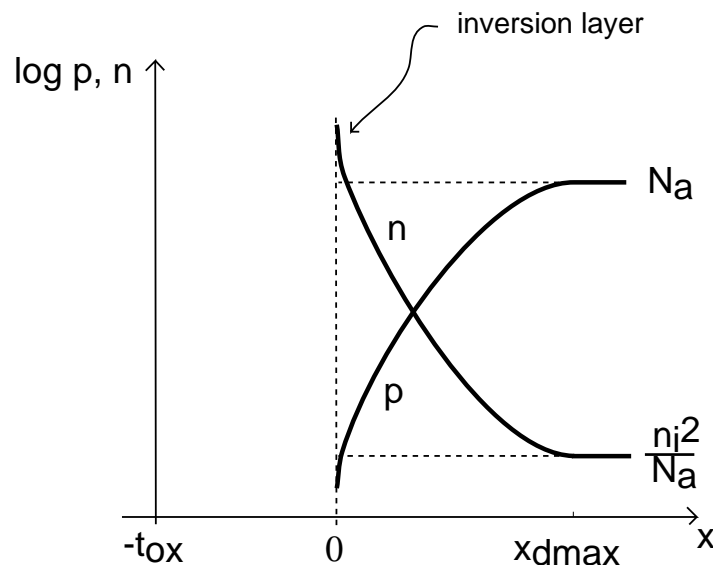
Key dependencies:

- If $N_a \uparrow \rightarrow V_T \uparrow$. The higher the doping level, the more voltage required to produce $n(0) = N_a$.
- If $C_{ox} \uparrow$ ($t_{ox} \downarrow$) $\rightarrow V_T \downarrow$. The thinner the oxide, the less voltage dropped across it.

6. Inversion

What happens for $V_{GB} > V_T$?

More electrons at Si/SiO₂ interface than acceptors
 \Rightarrow *inversion*.



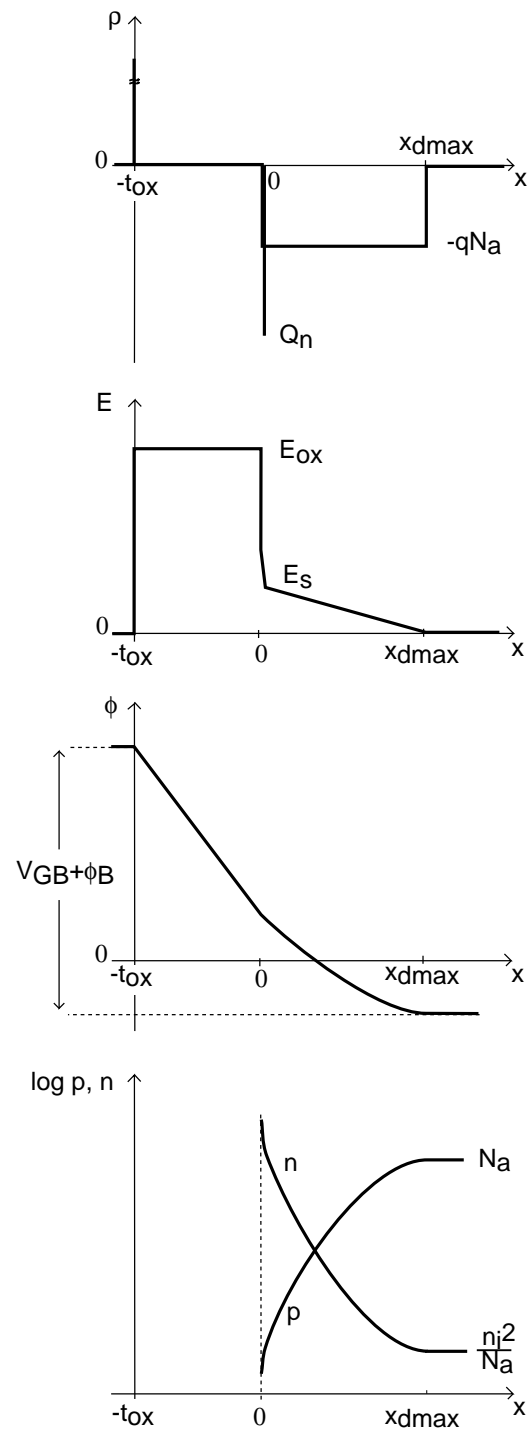
Electron concentration at Si/SiO₂ interface modulated by $V_{GB} \Rightarrow V_{GB} \uparrow \rightarrow n(0) \uparrow \rightarrow |Q_n| \uparrow$
field-effect control of mobile charge!
 [essence of MOSFET]

Want to compute Q_n vs. V_{GB} [*charge-control relation*]

Make *sheet charge approximation*: electron layer at semiconductor surface is much thinner than any other dimension in problem (t_{ox} , x_d).

□ Charge-control relation

Let us look at overall electrostatics:



Key realization:

$$|Q_n| \propto n(0) \propto e^{q\phi(0)/kT}$$

$$|Q_B| \propto \sqrt{\phi(0)}$$

Hence, as $V_{GB} \uparrow$ and $\phi(0) \uparrow$, $|Q_n|$ will change a lot, but $|Q_B|$ will change very little.

Several consequences:

- x_d does not increase much beyond threshold:

$$x_d(inv.) \simeq x_d(V_T) = \sqrt{\frac{2\epsilon_s(-2\phi_p)}{qN_a}} = x_{dmax}$$

- V_B does not increase much beyond $V_B(V_T) = -2\phi_p$ (*a thin sheet of electrons does not contribute much to V_B*):

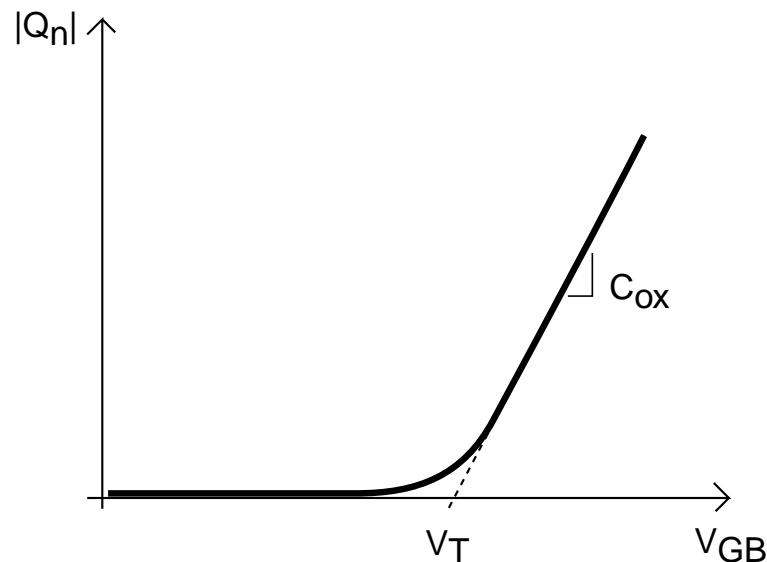
$$V_B(inv.) \simeq V_B(V_T) = -2\phi_p$$

- All extra voltage beyond V_T used to increase inversion charge Q_n . Think of it as capacitor:
 - top plate: metal gate
 - bottom plate: inversion layer

$$Q = CV$$

$$\Rightarrow Q_n = -C_{ox}(V_{GB} - V_T) \quad \text{for } V_{GB} > V_T$$

Existence of Q_n and control over Q_n by $V_{GB} \Rightarrow$ key to MOS electronics



Key conclusions

	M	O	S (p-type)	
$V_{GB} < V_{FB}$				accumulation
$V_{GB} = V_{FB}$				flatband
$V_{FB} < V_{GB} < 0$				depletion
$V_{GB} = 0$				equilibrium
$0 < V_{GB} < V_T$				depletion
$V_{GB} = V_T$				threshold
$V_{GB} > V_T$				inversion

In inversion:

$$|Q_n| = C_{ox}(V_{GB} - V_T) \quad \text{for } V_{GB} > V_T$$