

# **Lecture 12 - Digital Circuits (I)**

## **THE INVERTER**

March 18, 2003

### **Contents:**

1. Introduction to digital electronics: the inverter
2. NMOS inverter with resistor pull up

### **Reading assignment:**

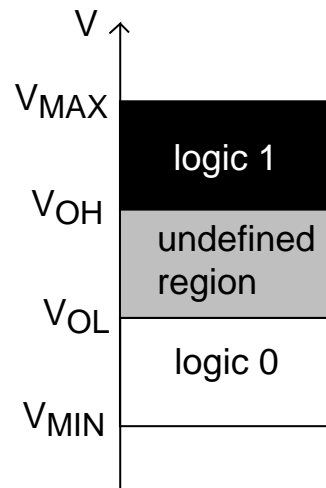
Howe and Sodini, Ch. 5, §§5.1-5.3.2

## Key questions

- What are the key figures of merit of logic circuits?
- How can one make a simple inverter using a single MOSFET?

# 1. Introduction to digital electronics: the inverter

In digital electronics, digitally-encoded information is represented by means of two distinct voltage ranges:

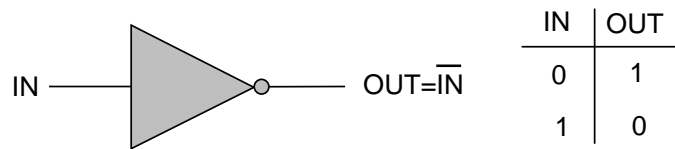


- *logic 0*:  $V_{MIN} \leq V \leq V_{OL}$
- *logic 1*:  $V_{OH} \leq V \leq V_{MAX}$
- *undefined logic value*:  $V_{OL} \leq V \leq V_{OH}$ .

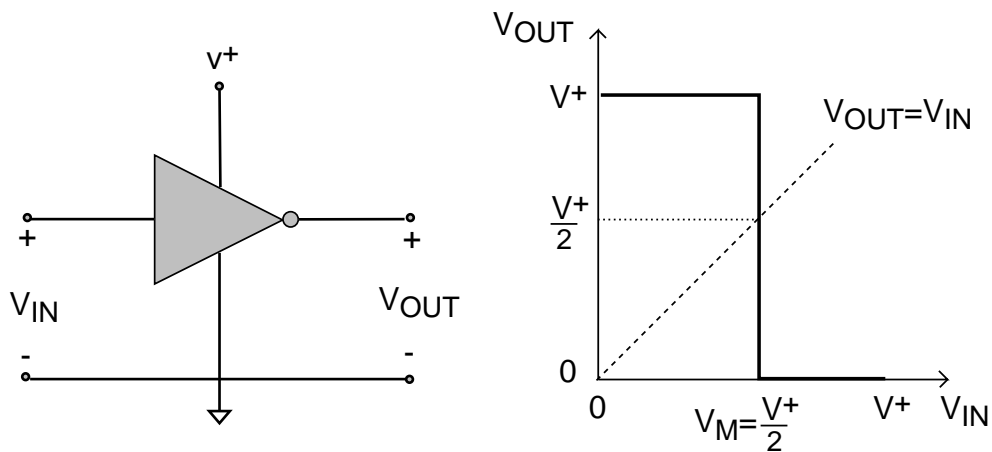
Logic operations are performed using *logic gates*.

Simplest logic operation of all: *inversion*  $\Rightarrow$  inverter

## □ Ideal inverter:



Circuit representation and ideal transfer function:



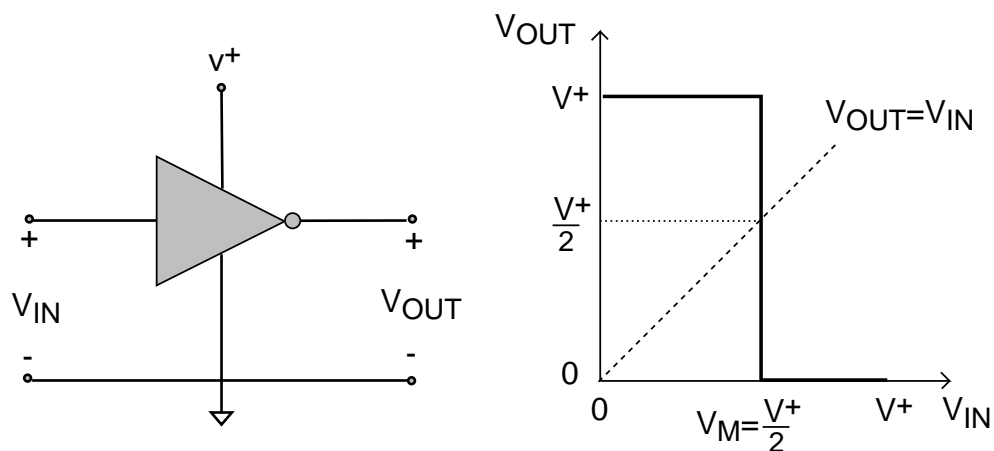
Define *switching point* or *logic threshold*:

$V_M \equiv$  input voltage for which  $V_{OUT} = V_{IN}$

-for  $0 \leq V_{IN} \leq V_M \Rightarrow V_{OUT} = V^+$

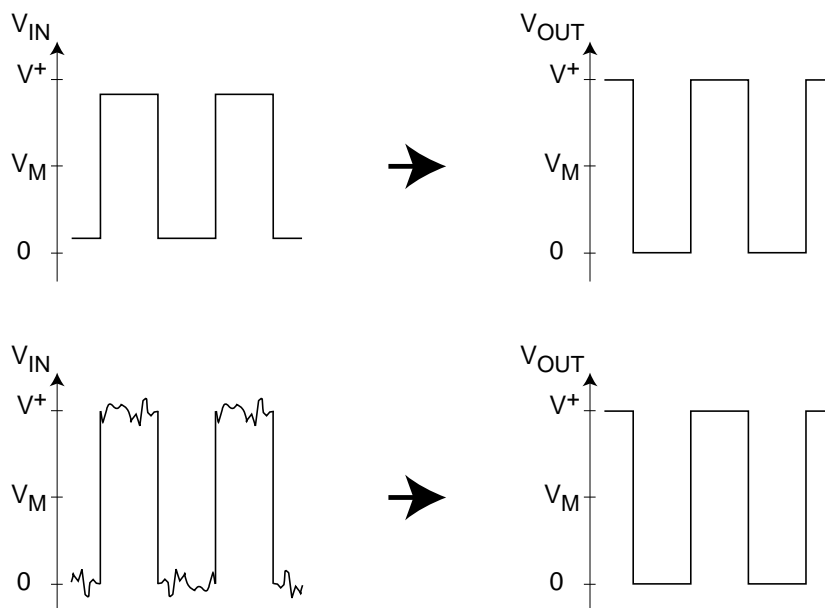
-for  $V_M \leq V_{IN} \leq V^+ \Rightarrow V_{OUT} = 0$

Key property of ideal inverter: *signal regeneration*

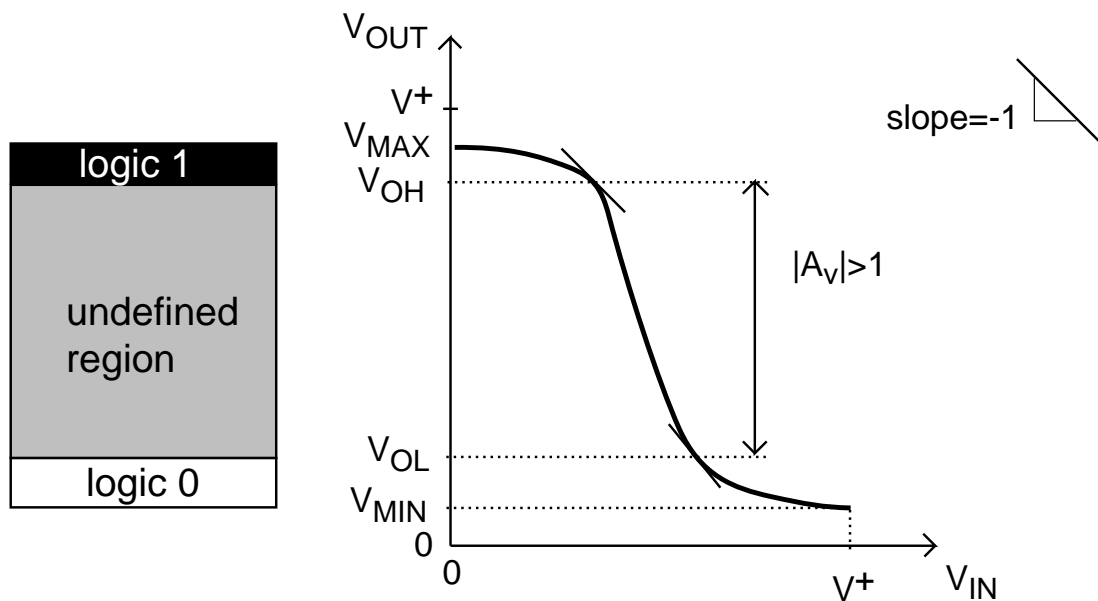


Ideal inverter returns well defined logical outputs ( $0$  or  $V^+$ ) even in the presence of considerable noise in  $V_{IN}$  (from voltage spikes, crosstalk, etc.)

$\Rightarrow$  signal is *regenerated*!



# □ "Real" inverter:



In a real inverter, valid logic levels defined as follows:

## ● *logic 0:*

$V_{MIN} \equiv$  output voltage when  $V_{IN} = V^+$

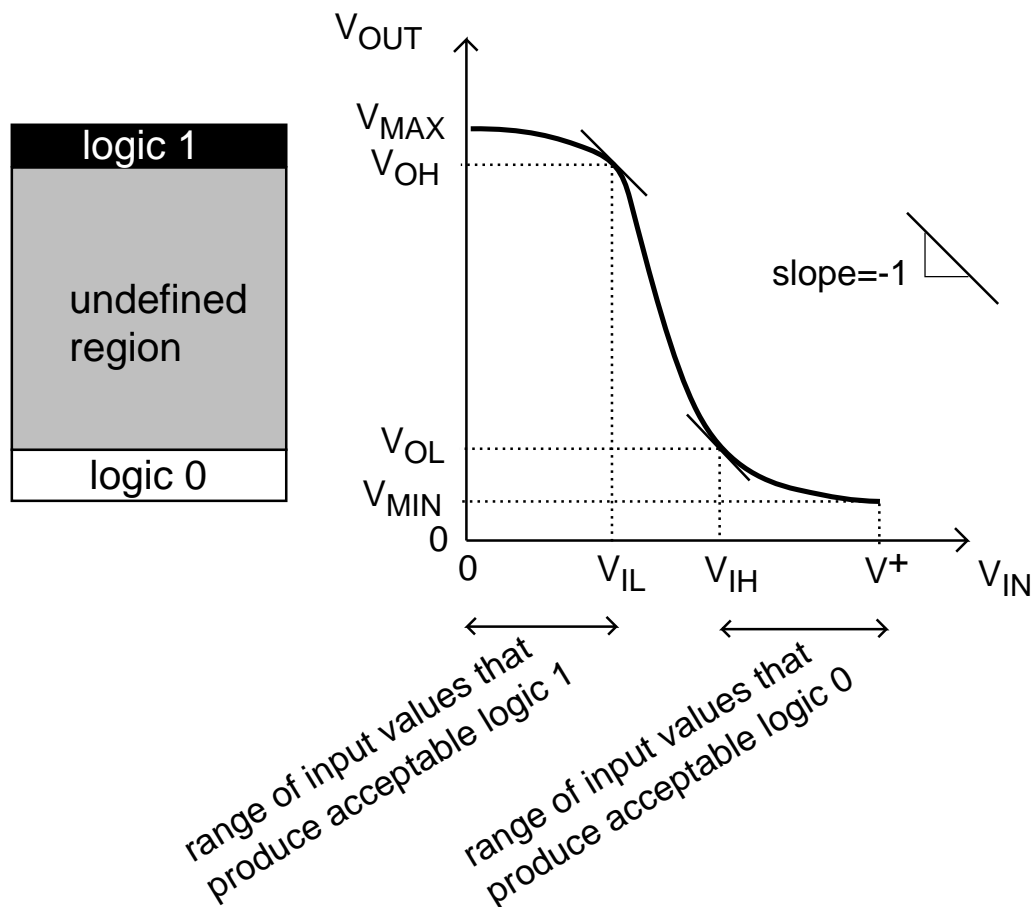
$V_{OL} \equiv$  smallest output voltage where slope=-1

## ● *logic 1:*

$V_{OH} \equiv$  largest output voltage where slope=-1

$V_{MAX} \equiv$  output voltage when  $V_{IN} = 0$

Two other important voltages:



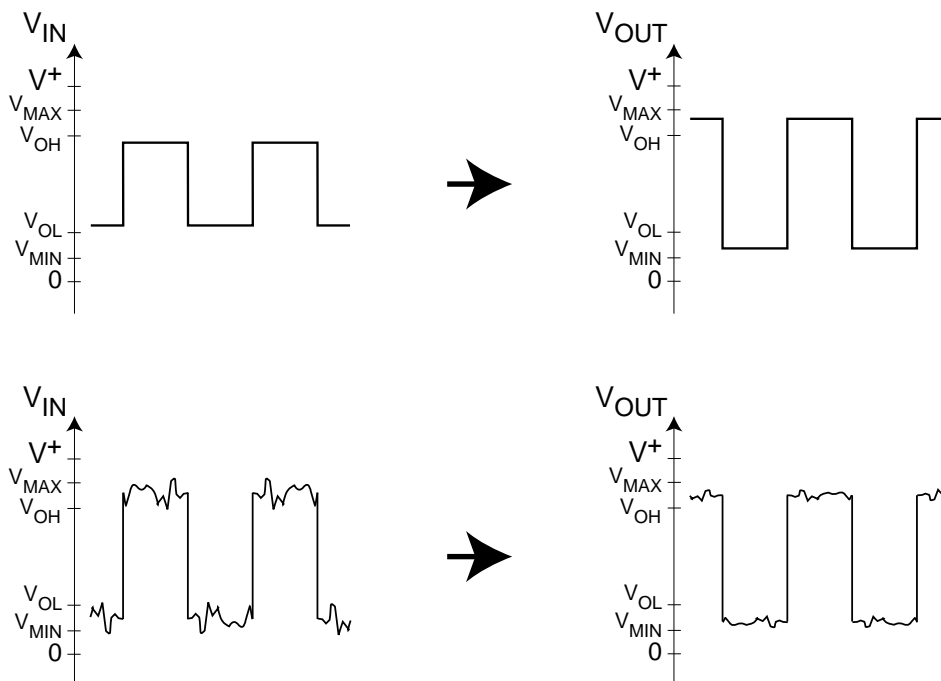
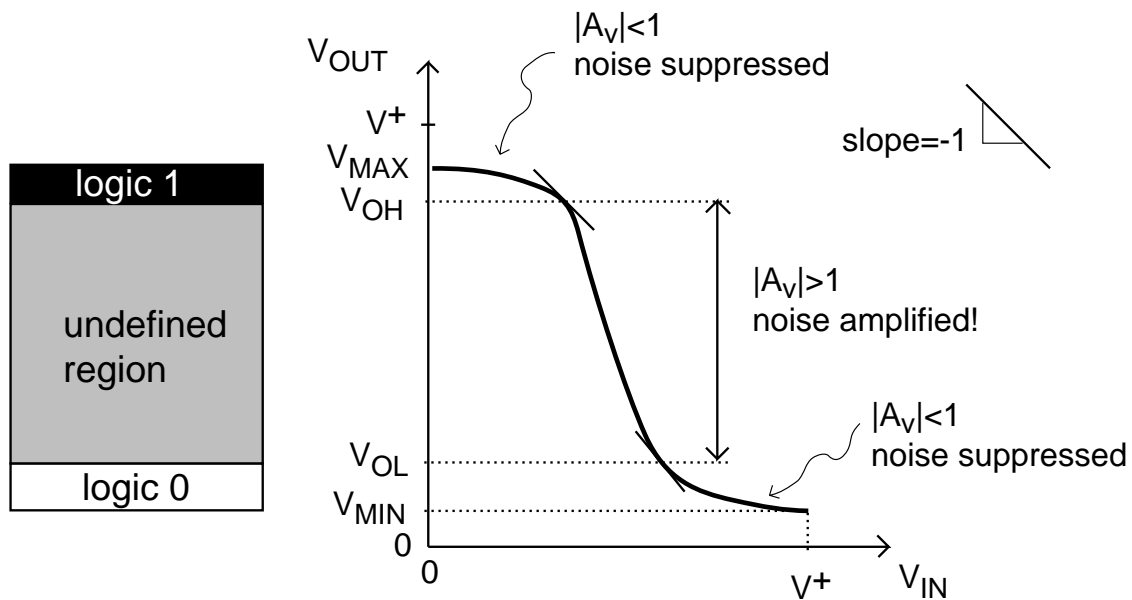
$V_{IL} \equiv$  smallest input voltage where slope=-1

$V_{IH} \equiv$  highest input voltage where slope=-1

To have *signal regeneration*:

range of input values that produce acceptable logic output  
 $>$  range of valid logic values

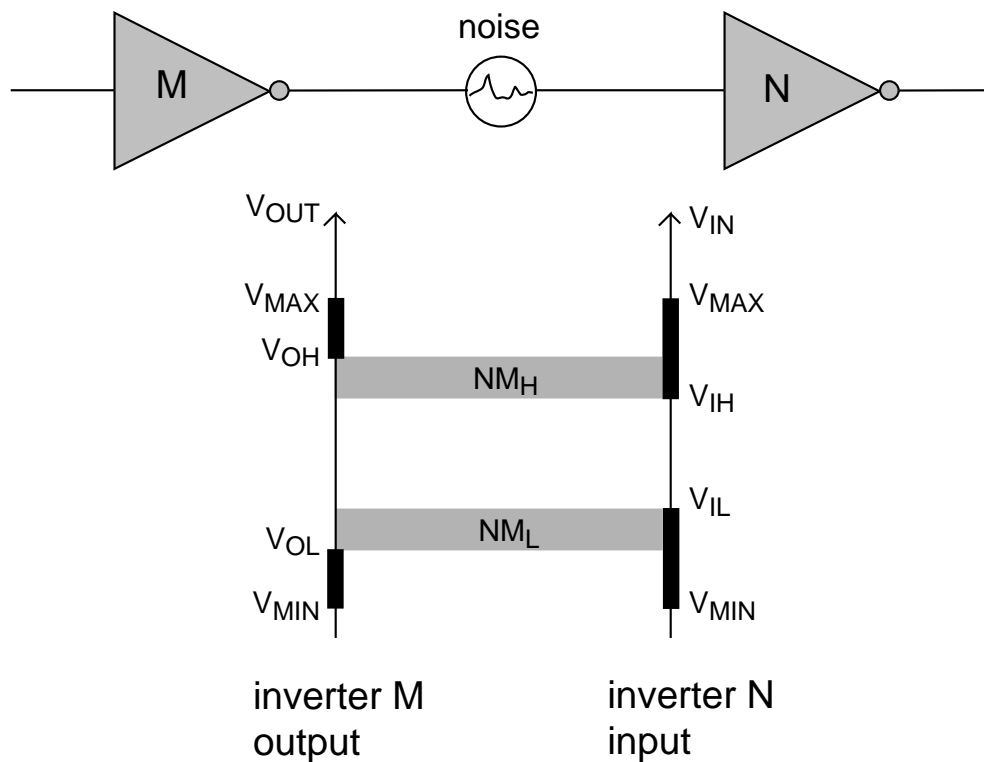
Key to signal regeneration in inverter: *noise suppression*  
 $\Rightarrow$  high voltage gain



Quantify noise immunity through *noise margins*.



Chain of two inverters:



Define *noise margins*:

$$NM_H = V_{OH} - V_{IH} \quad \text{noise margin high}$$

$$NM_L = V_{IL} - V_{OL} \quad \text{noise margin low}$$

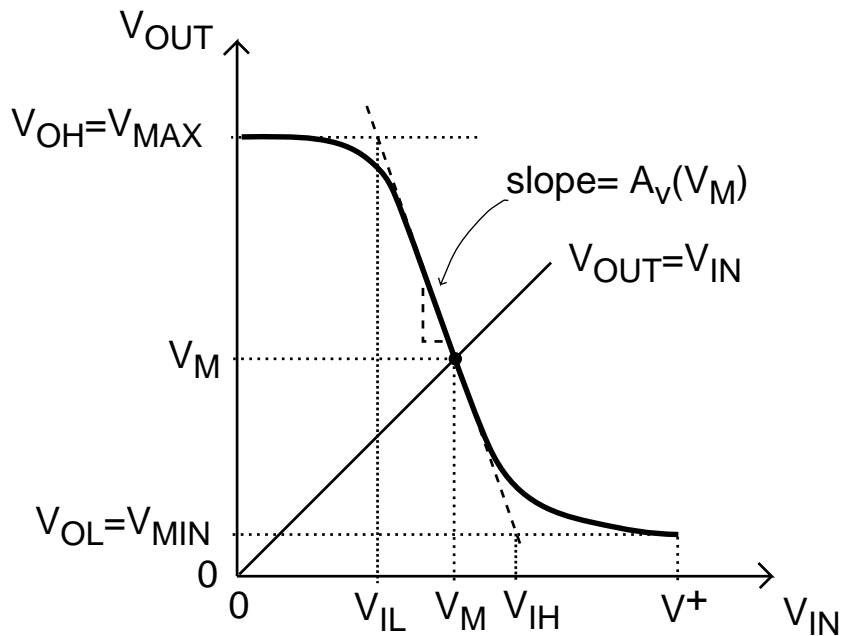
When signal is within noise margins:

- logic 1 output from first inverter interpreted as logic 1 input by second inverter
- logic 0 output from first inverter interpreted as logic 0 input by second inverter

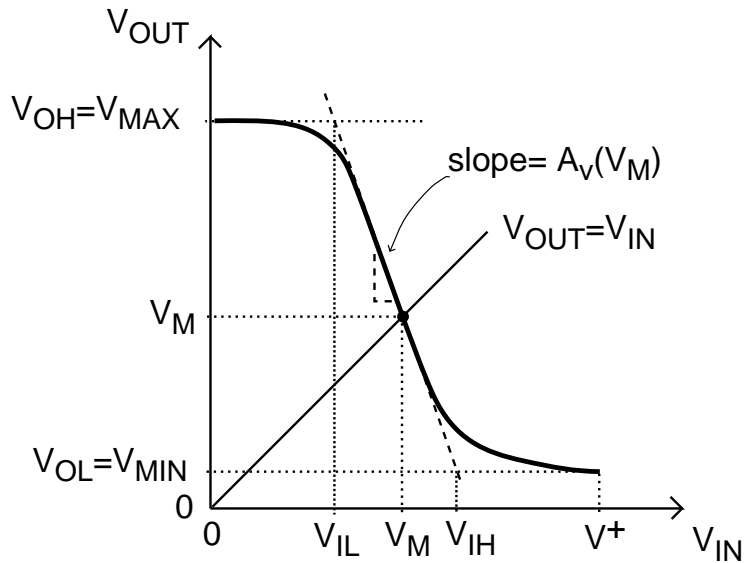
## Simplifications for hand calculations

Hard to compute  $A_v = -1$  points in transfer function.

Approximate calculation:



- Assume  $V_{OL} \simeq V_{MIN}$  and  $V_{OH} \simeq V_{MAX}$
- Trace tangent of transfer function at  $V_M$  (slope=small signal voltage gain at  $V_M$ )
- $V_{IL} \simeq$  intersection of tangent with  $V_{OUT} = V_{MAX}$
- $V_{IH} \simeq$  intersection of tangent with  $V_{OUT} = V_{MIN}$
- to enhance noise margin:  $|A_v(V_M)| \uparrow$



$$|A_v| \simeq \frac{V_{MAX} - V_M}{V_M - V_{IL}} \Rightarrow V_{IL} \simeq V_M - \frac{V_{MAX} - V_M}{|A_v|}$$

$$|A_v| \simeq \frac{V_M - V_{MIN}}{V_{IH} - V_M} \Rightarrow V_{IH} \simeq V_M \left(1 + \frac{1}{|A_v|}\right) - \frac{V_{MIN}}{|A_v|}$$

Then:

$$NM_L = V_{IL} - V_{OL} \simeq (V_{MAX} - V_{MIN}) - (V_{MAX} - V_M) \left(1 + \frac{1}{|A_v|}\right)$$

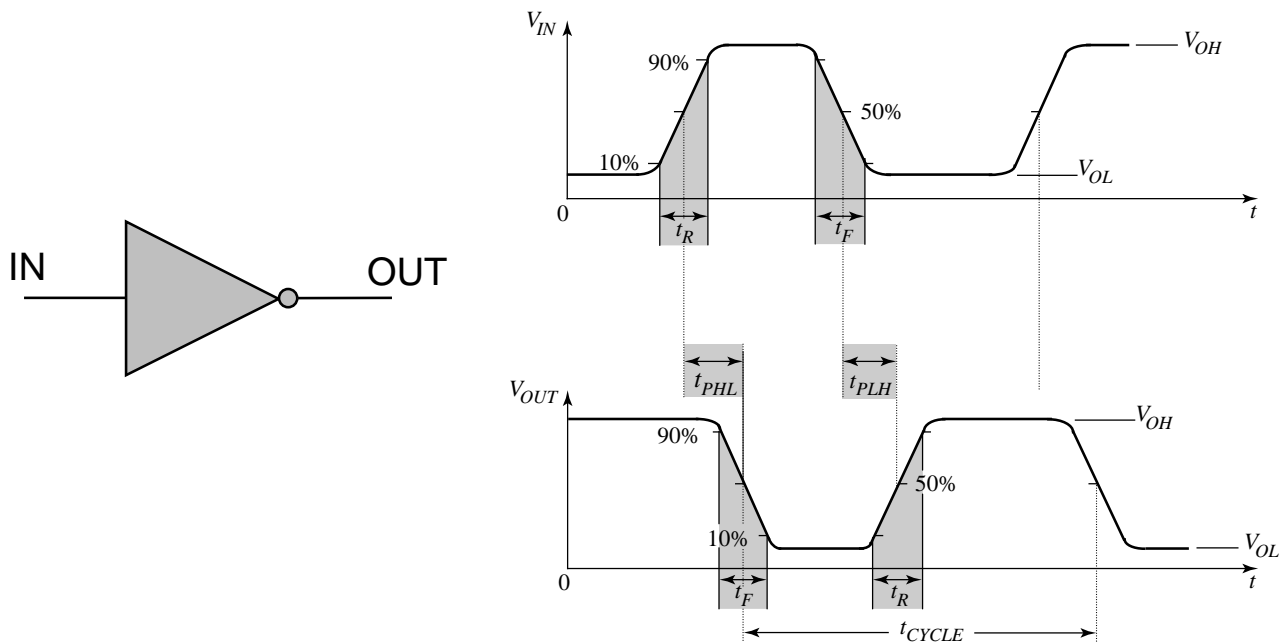
$$NM_H = V_{OH} - V_{IH} \simeq (V_{MAX} - V_{MIN}) - (V_M - V_{MIN}) \left(1 + \frac{1}{|A_v|}\right)$$

If  $|A_v| \rightarrow \infty$ :

$$NM_L \rightarrow V_M - V_{MIN} \quad NM_H \rightarrow V_{MAX} - V_M$$

## □ Transient characteristics

Look at inverter switching in the time domain:



$t_R \equiv$  *rise time* between 10% and 90% of total swing

$t_F \equiv$  *fall time* between 90% and 10% of total swing

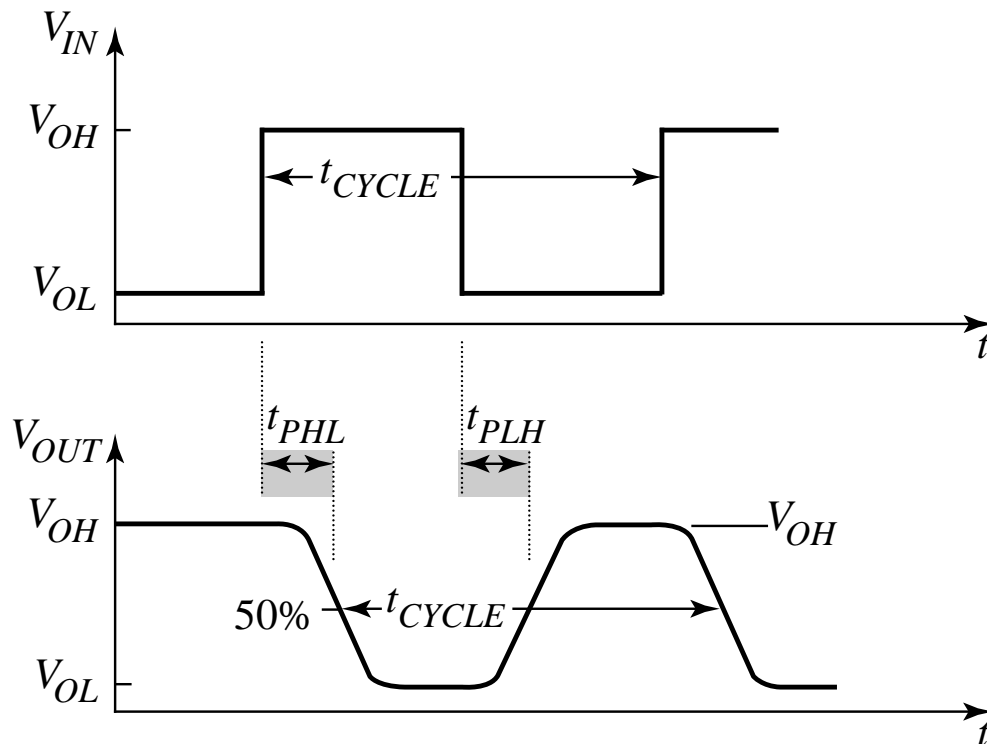
$t_{PHL} \equiv$  *propagation delay from high-to-low* between 50% points

$t_{PLH} \equiv$  *propagation delay from low-to-high* between 50% points

*Propagation delay:*  $t_P = \frac{1}{2}(t_{PHL} + t_{PLH})$

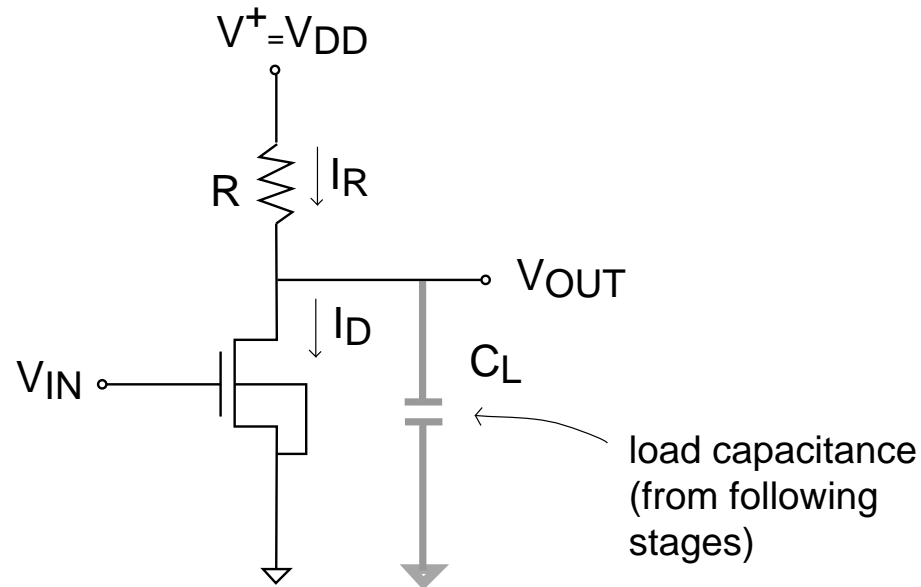
## Propagation delay: simplification for hand calculations

- Input wavefunction = ideal square wave
- Propagation delay times = delay times to 50% point



- Hand calculations only approximate
- SPICE essential for accurate delay analysis

## 2. NMOS inverter with resistor pull up

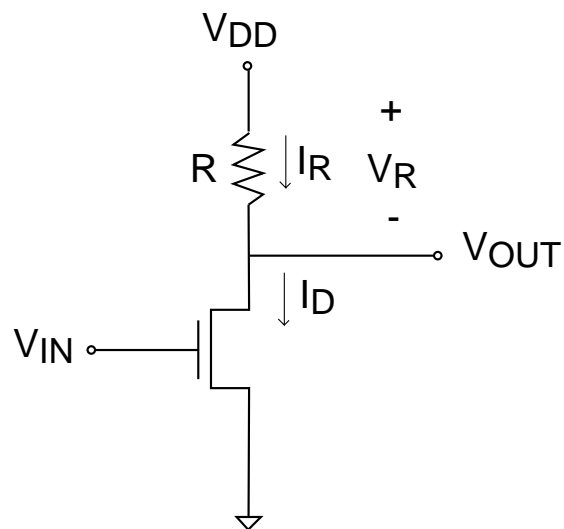


Features:

- $V_{BS} = 0$  (typically not shown)
- $C_L$  summarizes capacitive loading of following stages (other logic gates, interconnect lines)

Basic operation:

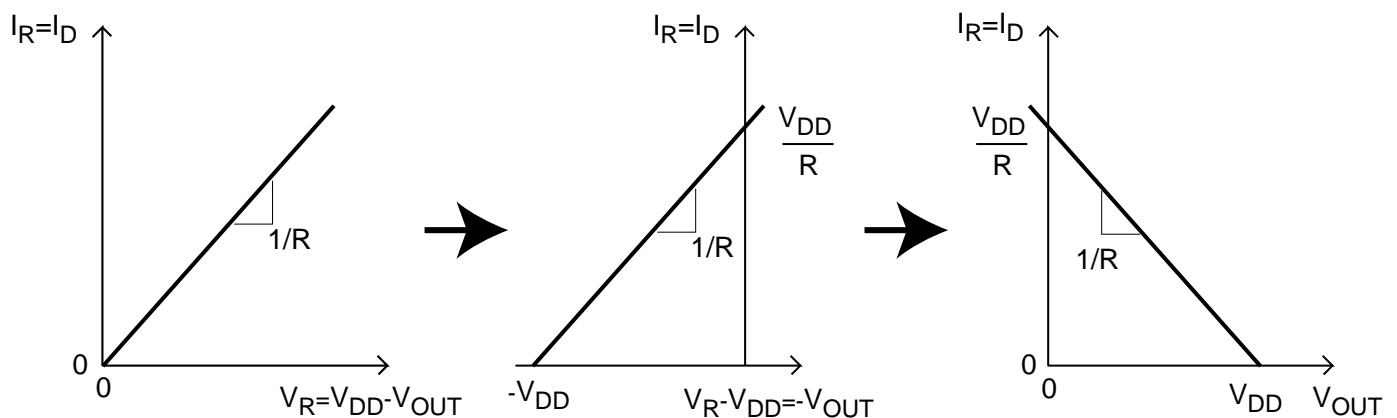
- if  $V_{IN} < V_T$ , MOSFET OFF  $\Rightarrow V_{OUT} = V_{DD}$
- if  $V_{IN} > V_T$ , MOSFET ON  $\Rightarrow V_{OUT}$  small (value set by resistor/nMOS divider)



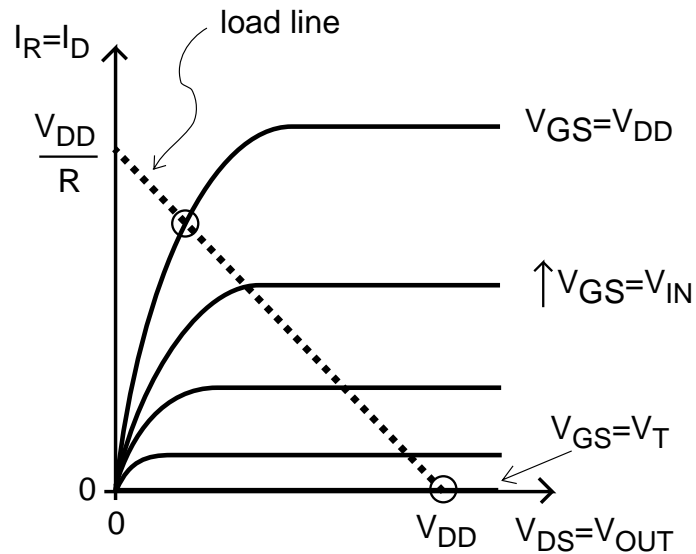
Transfer function obtained by solving:

$$I_R = I_D$$

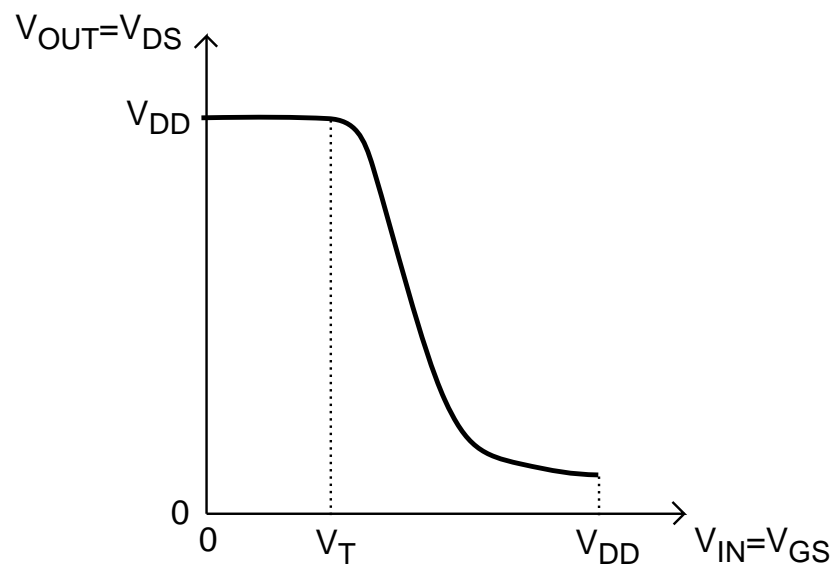
Can solve graphically: I-V characteristics of pull-up resistor on  $I_D$  vs.  $V_{OUT}$  transistor characteristics:



Overlap I-V characteristics of resistor pull-up on I-V characteristics of transistor:

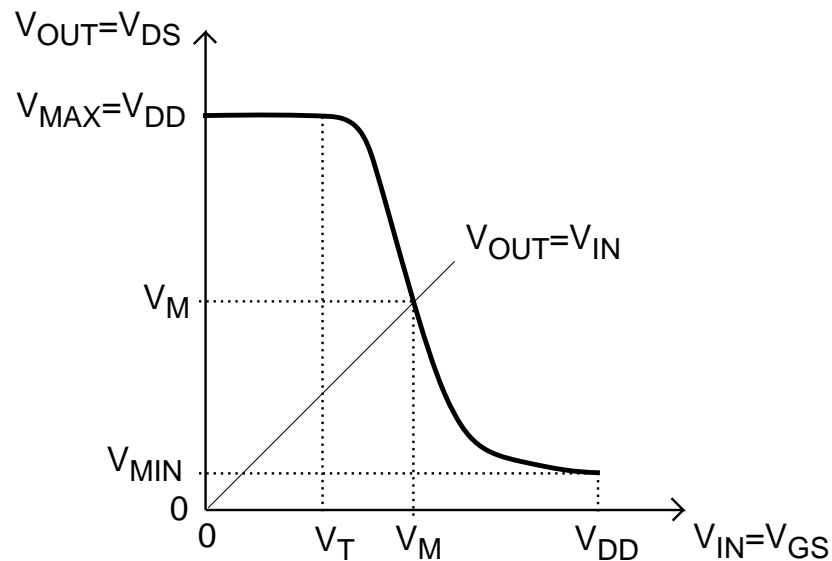


Transfer function:





Logic levels:



For  $V_{MAX}$ , transistor is cut-off,  $I_D = 0$ :

$$V_{MAX} = V_{DD}$$

For  $V_{MIN}$ , transistor is in linear regime; solve:

$$I_D = \frac{W}{L} \mu_n C_{ox} \left( V_{DD} - \frac{V_{MIN}}{2} - V_T \right) V_{MIN} = I_R = \frac{V_{DD} - V_{MIN}}{R}$$

For  $V_M$ , transistor is in saturation; solve:

$$I_D = \frac{W}{2L} \mu_n C_{ox} (V_M - V_T)^2 = I_R = \frac{V_{DD} - V_M}{R}$$

Will continue next lecture with analysis of noise margin and dynamics...

## Key conclusions

- Logic circuits must exhibit *noise margins* in which they are immune to noise in input signal.
- Logic circuits must be *regenerative*: able to restore clean logic values even if input is noisy.
- *Propagation delay*: time for logic gate to perform its function.
- Concept of *load line*: graphical technique to visualize transfer characteristics of inverter.
- First-order solution (by hand) of inverter figures of merit easy if regimes of operation of transistor are correctly identified.
- For more accurate solutions, use SPICE (or other circuit CAD tool).