# ρ-VEX

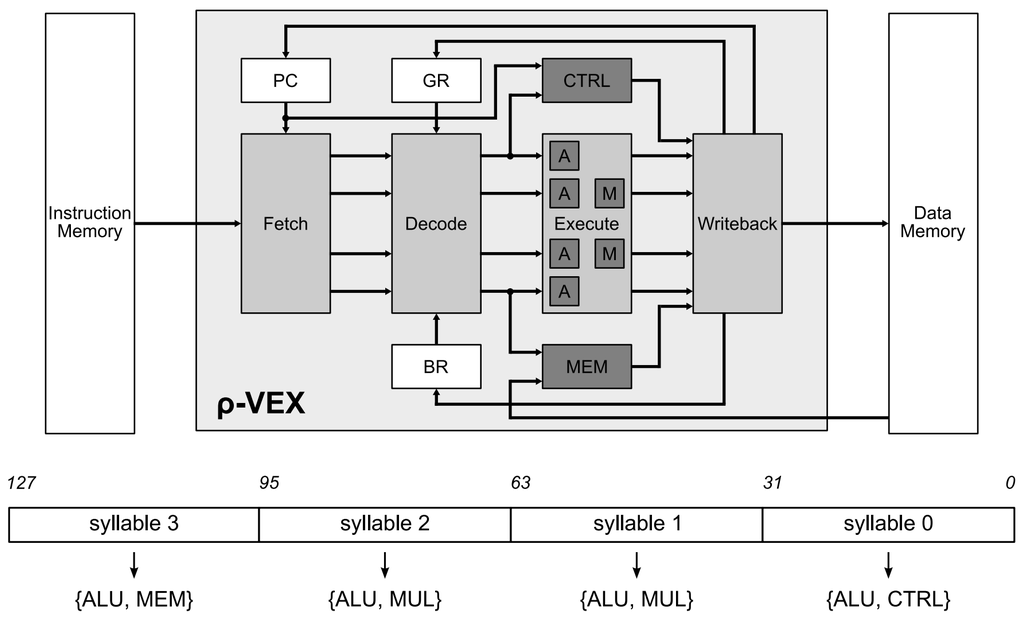
## A Reconfigurable and Extensible VLIW Processor

*Stephan Wong, Thijs van As and Geoffrey Brown*
Computer Engineering Laboratory, Delft University of Technology
***http://r-vex.googlecode.com/***

**GOAL** An open source reconfigurable and extensible processor framework to exploit Instruction Level Parallelism (ILP)

**MEANS** *VEX Very Long Instruction Word (VLIW) ISA*
- Scalable platform for embedded VLIW processors
- Software toolchain (compiler + simulator) freely available by HP
- Custom operations supported

## ORGANIZATION



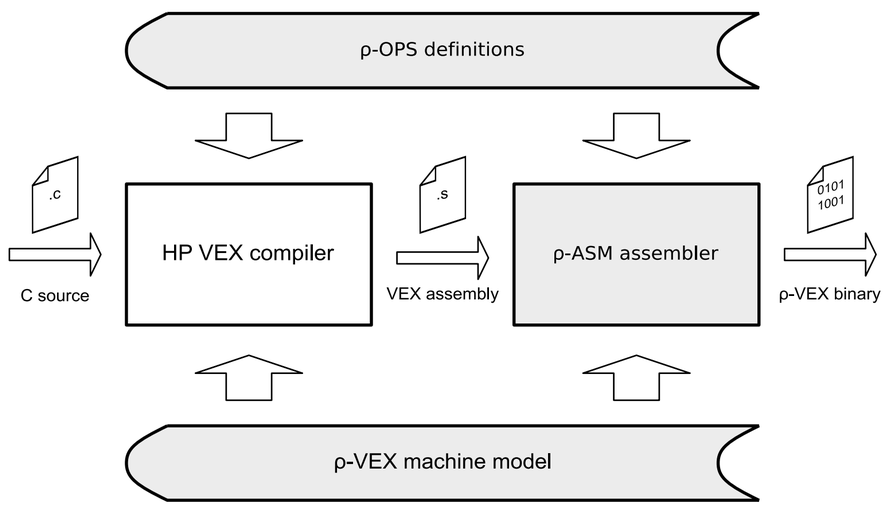

## EXTENSIBILITY

**1.) ρ-OPS**
- Reconfigurable custom operations

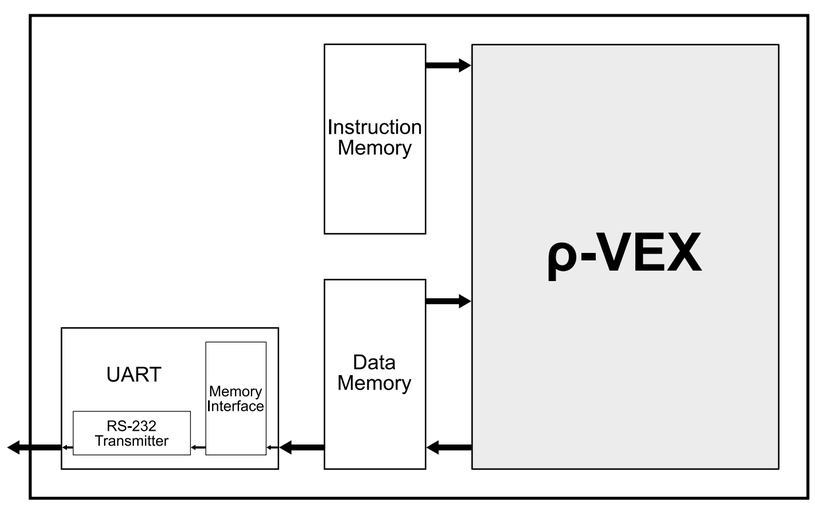
**2.) VEX Machine Models**
- Issue-width
- Number of ALU units
- Number of MUL units
- Number of GR registers
- Number of BR registers
- Types of accessible FUs per syllable
- Width of memory busses

## DEVELOPMENT FRAMEWORK

### *Software development*




### *Hardware development*




## RESULTS

*Fibonacci's Sequence benchmark*
(Performed on a Xilinx XC2VP30 FPGA)

| *ρ*-VEX | Cycles | Max. freq. | Slices | Slices GR |
|---|---|---|---|---|
| 1-issue | 1906 | 89.44 MHz | 1895 (13%) | 1 (0%) |
| 2-issue | 1080 | 89.44 MHz | 5105 (37%) | 3370 (24%) |
| 4-issue | 537 (141) | 89.44 MHz | 10433 (76%) | 3927 (28%) |

**With ρ-OPS**

## CONCLUSIONS / CONTRIBUTIONS

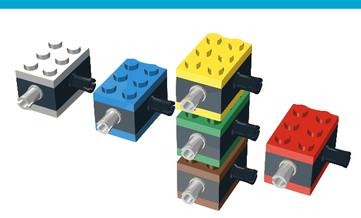
- ρ-VEX open source VLIW processor
- ρ-ASM custom assembler/instruction ROM generator
- Application development framework
- Code + documentation available at *http://r-vex.googlecode.com/*

**Faculty of Electrical Engineering, Mathematics and Computer Science**

TU Delft
Delft University of Technology

**Computer Engineering**
Mekelweg 4 (15th/16th floor)
2628 CD Delft
The Netherlands
*http://ce.et.tudelft.nl/*

**Contact:**
Thijs van As
t.vanas@gmail.com
*http://r-vex.googlecode.com/*



**ρ-VEX**

**MOLEN**