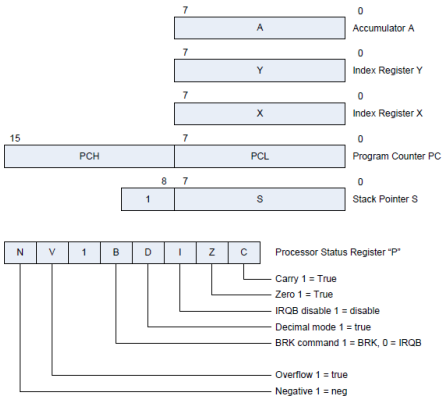


Figure 2-2 W65C02S Microprocessor Programming Model

Table 2-1 W65C816S Microprocessor Programming Model

8 Bits	8 Bits	8 Bits
Data Bank Register (DBR)	X Register (XH)	X Register (XL)
Data Bank Register (DBR)	Y Register (YH)	Y Register (YL)
00	Stack Register (SH)	Stack Register (SL)
	Accumulator (B)	Accumulator (A)
Program Bank Register (PBR)	Program (PCH)	Counter (PCL)
00	Direct Register (DH)	Direct Register (DL)

Shaded Blocks = 6502 registers

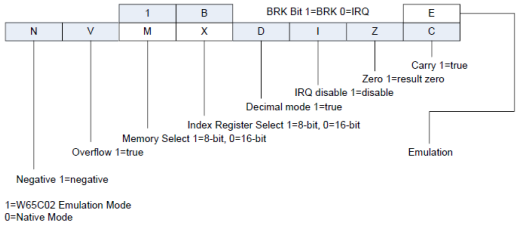
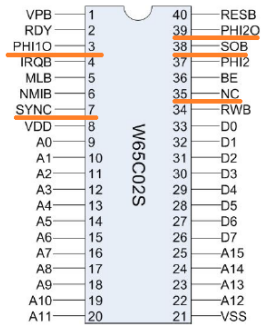


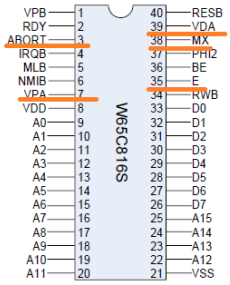
Table 3-2 Pin Function Table

Pin	Description
A0-A15	Address Bus
BE	Bus Enable
D0-D7	Data Bus
IRQB	Interrupt Request
MLB	Memory Lock
NC	No Connection
NMIB	Non-Maskable Interrupt
PHI1O	Phase 1 Out Clock
PHI2	Phase 2 In Clock
PHI2O	Phase 2 Out Clock
RDY	Ready
RESB	Reset
RWB	Read/Write
SOB	Set Overflow
SYNC	Synchronize
VDD	Positive Power Supply
VPB	Vector Pull
VSS	Internal Logic Ground

Table 2-2 Pin Function Table

Pin	Description
A0-A15	Address Bus
ABORTB	Abort Input
BE	Bus Enable
PHI2	Phase 2 In Clock
D0-D7	Data Bus/Bank Address Bus
E	Emulation OR Native Mode Select
IRQB	Interrupt Request
MLB	Memory Lock
MX	Memory and Index Register Mode Select
NC	No Connect
NMIB	Non-Maskable Interrupt
RDY	Ready
RESB	Reset
RWB	Read/Write
VDA	Valid Data Address
VPB	Vector Pull
VPA	Valid Program Address
VDD	Positive Power Supply
VSS	Internal Logic Ground





ピンの違い		
PIN No.	W65C02	W65C816S
3	PH1O (output)	/ABORT (INPUT)
7	SYNC (OUTPUT)	VPA (OUTPUT)
35	(NC)	E (OUTPUT)
38	/SOB (INPUT)	MX (OUTPUT)
39	PH2O (OUTPUT)	VDA (OUTPUT)

Table 3-1 Vector Locations

FFFE, F	BRK/IRQB	Software/Hardware
FFFC, D	RESB	Hardware
FFFA, B	NMIB	Hardware

Table 5-2 Emulation Mode Vector Locations (8-bit Mode)

Address	Label	Function
00FFFE,F	IRQB/BRK	Hardware/Software
00FFFC,D	RESETB	Hardware
00FFFA,B	NMIB	Hardware
00FFF8,9	ABORTB	Hardware
00FFF6,7	(Reserved)	Hardware
00FFF4,5	COP	Software
00FFF2,3	(Reserved)	
00FFF0,1	(Reserved)	

Table 5-3 Native Mode Vector Locations (16-bit Mode)

Address	Label	Function
00FFEE,F	IRQB	Hardware
00FFEC,D	(Reserved)	
00FFEA,B	NMIB	Hardware
00FFE8,9	ABORTB	
00FFE6,7	BRK	Software
00FFE4,5	COP	Software
00FFE2,3	(Reserved)	
00FFE0,1	(Reserved)	

The VP output is low during the two cycles used for vector location access. When an interrupt is executed, D=0 and I=1 in Status Register P.