On-chip Clock Multiplier (PLL)

Fclkin – 5MHz to 12Mhz, Fclkout – 40MHz to 100MHz at 1.8v@osu180nm

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***Abstract*—This report gives a description about the basic components involved in the design of Clock multipliers (frequency synthesizer) using Phase locked loops.**

I. Introduction

On-chip clock Multipliers are used for the multiplying the base clock frequency to higher frequencies.It is designed by using phase locked loops, delay locked loops or a combination of both in recent times.

II. Phase Locked Loops

Phase locked loop can be modeled as a negative feedback control system with major blocks such as Phase detector/Phase frequency detector(PFD), Charge Pump, Low pass Filter, Voltage controlled oscillator(VCO) and Frequency dividers [1] [2]. The reference frequency is fed as an input to the Phase locked loop along with the select lines which decide the multiplication factor m/n of the reference frequency

A. Phase detectors/phase frequency detector:

Phase detectors are used to convert the phase difference between the reference signal and the feedback signal as an error signal which changes continuously till the lock condition is reached.This error voltage signal determines whether the frequency must be increased or decreased by the VCO [5]. Dual D type phase detector is commonly used [4] .

B. Charge Pumps

The dual D type phase detector produces two outputs which need to be combined into a single output by the Charge Pumps [1] [4].It acts as a current source that can provide both positive and negative pulses of current to the Low pass Filter.

C. Low pass filters

The output signal obtained from the PFD and Charge pumps contains unwanted high frequency components which are removed by the low pass filters and the output of this filter acts as the control voltage for the VCO. [5].

D. Voltage Controlled Oscillators

Voltage controlled oscillators use a control voltage as input and produce and output signal whose frequency varies with the control voltage.It increases or decreases the frequency based on the error in the phase difference and ring type oscillators are commonly used [5].

III. Phase Locking

In the normal operation of a PLL without the frequency divider blocks, the output from the VCO which initially has an arbitrary frequency is fed back as input to the phase frequency detector. since the reference clock frequency and the feedback signal frequencies are different, a continuously varying phase error is present and this is converted as an error signal by the PFD. this error signal which has high frequency components is converted into an average dc voltage by the low pass filters and the charge pumps and fed as tuning voltage to the VCO . this process continues until the feedback signal frequency matches the reference clock frequency [2]. once the frequencies are same the tuning Voltage becomes constant and this stage of the PLL is known as phase lock.

IV. Multiplication Factor

The phase detector compares the input signals and produces a continuously varying error signal and this process continues till both the input signals to the phase detector have the same frequency. Consider an input signal with frequency fr. The VCO initially produces an arbitrary output frequency fo which changes with time as the error changes. this signal undergoes frequency division by m and introduced as input to the FPD Block. the purpose of the entire PLL block is to match this output frequency with the reference signal (fo=m*fr). Thus the frequency is multiplied by m. introducing a frequency divider in the Input path has the effect of dividing the output frequency by n and together both the divider block produce a multiplication factor of m/n and they can be changed by the use of multiplexers [3] [4].

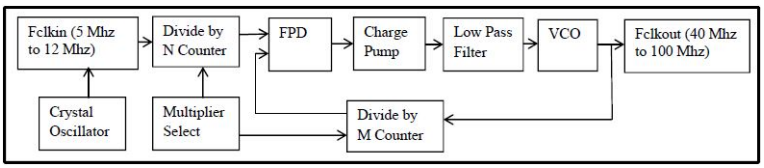

Fig. 1. Block Diagram of the Clock Multiplier

V. Applications of Clock Multipliers

On-chip clock Multipliers are essential to generate higher frequencies in a wide variety of applications which include telecommunication line cards, Optical fibre Communication, Data Converters (ADCs and DACs), WAN/LAN hardware,

Video Broadcasting applications and for Power Management in modern VLSI Chips.

A. Communication Systems

IEEE has defined standard frequencies for different communication networks and Clock Multipliers are used in most communication channels to maintain stable high frequency clock

1) Optical Networks: Synchronous optical Networking and Synchronous digital hierarchy are standardized Protocols for synchronous data transmission over optical Fibres using lasers or highly coherent LEDs. This data transmission takes place using predefined frequencies and these optical carriers are classified based on their frequencies.The general classification is of the form OC-x (ex:OC-1,OC-3 etc) where x determines the multiplication factor of the Transmission rate of 51.84 Mbit/s. Each of these Transmission lines terminate on a line card, where Clock multipliers are used to meet the required frequency standard. [6] [7].

2) Synchronous Ethernet, WAN and LANs: Ethernet cables also contain line cards on which these cables terminate on the consumer end and these line cards require jitter free clock multipliers for synchronisation and successful operation. These clock multipliers determines the rate at which the data is transmitted across the ethernet cables(GbE/10/40/100G Synchronous Ethernet) used in Wide Area Networks and Local Area Networks. [7]

3) Radio Frequency Communication: Clock multipliers are also deployed in wireless base station controllers(BSC) which are responsible for controlling multiple base transceiver stations(BTS). They are used for encrypting, decrypting and transmitting radio signals and with improving mobile technologies 2G/3G/4G etc., Jitterless clock multipliers are essential for their satisfactory working. [9]

B. Signal Processing

Digital and Analog signal processors are specialized microprocessor blocks for signal processing applications. In SOC processors, the PLL-based clock multipliers provide the necessary clock frequency which acts as the sampling clock frequency for such blocks.According to Nyquist's sampling theorem the sampling frequency must be atleast twice the frequency of the sampled continous time signal for effective reconstruction and Clock Multipliers play an important role in adapting to different frequencies. Analog to digital (ADC) and Digital to Analog(DAC) are commonly refer to as data converters.Clock jitter introduces some noise into the sampled signal which is undesirable.Thus, Pll based clock multipliers are used in these converters to reduce the signal-to-noise ratio (SNR). [10] [11]

C. DVS Controllers

Some systems usually have time varying performance. Such systems can save large amounts of energy by reducing the clock frequency to the minimum sufficient to complete the task on schedule, then reducing the supply voltage to the minimum necessary to operate at that frequency . This reduces the power consumption rapidly. The DVS controller after assessing the workload, decides on the minimum frequency required and sends control signals to the Clock Multiplier to vary the clock frequency . [12].

D. Multiple Frequency Domains

A chip may use multiple frequency domains so that certain portions can run more slowly than others. For example, a microprocessor bus interface usually runs much slower than the core. [12]

E. SERDES (serializer/deserializer)

Most communication-based ASICs contain SERDES (serializer/deserializer) macrocells designed to provide compliance to a set of standard specifications.A Clock Multiplier unit is used to provide multiples of the reference crystal oscillator to the SERDES blocks. [8]

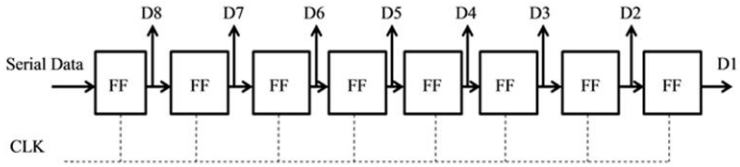

Fig. 2. Block Diagram of the Clock Multiplier

VI. Simulation

A. Steps to run

Download the Fullswing.asc file and open it in LTspice to view the circuit diagram.CLK1 and CLK2 are the respective input and output clock frequencies.

Simulation of the clock multiplier is done with the help of LTSpice Tool. TSMC180nm library is used as reference for the transistors. Frequency divider is not used , both the output and the input frequencies are same and phase locking was achievable only for certain frequencies.

B. Phase Frequency Detector

Two D flip flops are used along with a NAND gate which is connected to the reset terminals of both the flip-flops.The Block generates two output signals up and down, which acts as inputs to the charge pump.

C. Charge Pump and Low Pass Filter

The charge pump which is controlled by the Up and Down signals inject positive and negative pulses of current into the low pass filter. The Low pass filter removes the high frequency unwanted components from the input signal and an active low pass filter is used to maintain a voltage level between the operating points of the ring oscillator.

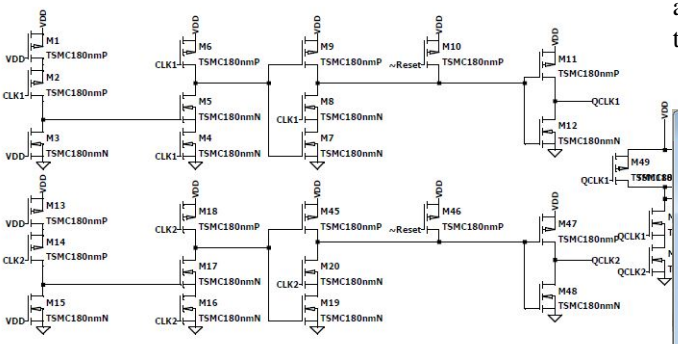

Fig. 3. Phase Frequency Detector

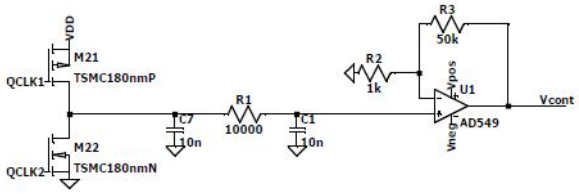

Fig. 4. Charge Pump

D. Ring Oscillator

Ring Oscillator designed in this simulation is a current starved 5-stage ring oscillator which basically contains 5 inverters back to back , to generate the required frequency. The voltage control is achieved by applying the control voltage to the Current mirror , whose output current varies with frequency and hence the output frequency changes with the control voltage since injected current determines the delay across each stage. The output and the input frequencies obtained are as shown in the waveform below.

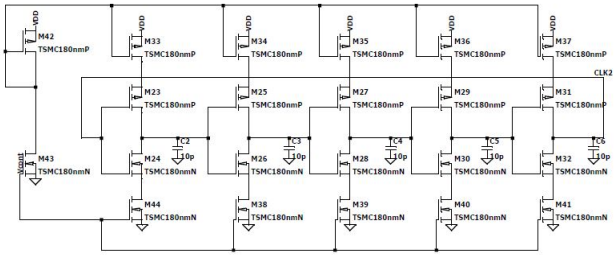

Fig. 5. Ring Oscillator

E. Waveforms

No frequency divider was used.The initial attempt was to achieve phase lock between the input and the output frequencies which are the same since no frequency divider is used in the feedback path. the output and the input voltages are shown in figure 6. the variation of the control voltage with time before settling to a stable value is show in figure 7.

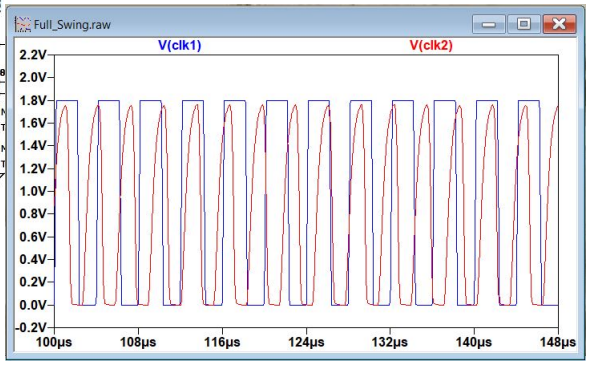

Fig. 6. Input and output Frequencies

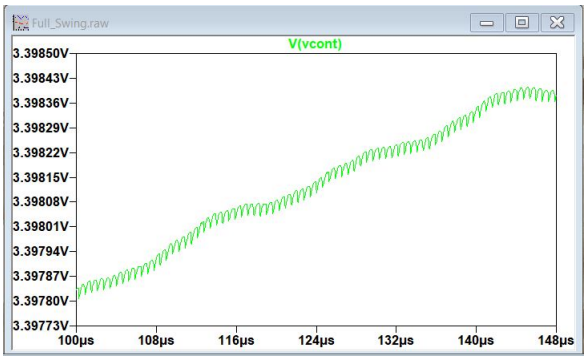

Fig. 7. VCO Control Voltage

F. Shortcomings

When specifying the widths and lengths of the transistors, the output of the ring oscillator does not show full swing.TSMC180nm library was used instead of osu180nm library since i was not able to find it. the design of low pass filter was almost impossible, the output voltage did not raise above a certain limit no matter how much change is done in resistance and capacitance. Frequency dividers must be added in the feedback path for clock multiplication.Overall, I was not able to complete the simulation since no phase lock was achieved beyond a short range of frequencies. Need to look more into transistor sizing and low pass filter design.

REFERENCES

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