T.R.
MANISA CELAL BAYAR UNIVERSITY
FACULTY OF ENGINEERING
DEPARTMENT OF COMPUTER ENGINEERING

CSE 2134 - LOGIC DESIGN

[Project-1 Report]

Team Members

170316064 / Fatma Kurtuluş (Team Leader)
170316022 / Çağatay Kılınç
170315063 /Kemal Erdem Sarıdaş
170315036/ Melih Çakmak

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Project-1: 2-bit Calculator Using Two Numbers

[Part.1] Summary of the Project

- This project aims to design a 2-bit calculator using 4 modules. The modules are Addition, subtraction, multiplication, comparison.
- These modules are combined with decoder in order to select specific module.
- All units use ... as input and give ... as output.
- Inputs are applied to this calculator utilizing manually (we will give 1 and 0) and outputs are interpreted via leds.

[Part.2] Material List

1. Addition Module: 74HC08 AND-Gate (1 pcs), Total count:3 AND-Gates
   74HC32 OR-Gate (1 pcs), Total count:1 OR-Gates
   74HC86 XOR-Gate (1 pcs), Total count:3 XOR-Gates
2. Multiplication Module: 74HC08 AND-Gate (2 pcs), Total count: 6 AND-Gates
   74HC86 XOR-Gate (1 pcs), Total count:2 XOR-Gates
3. Subtraction Module: 74HC08 AND-Gate (1 pcs), Total count:4 AND-Gates
   74HC32 OR-Gate (1 pcs), Total count:2 OR-Gates
   74HC86 XOR-Gate (1 pcs), Total count:4 XOR-Gates
   74HC04 NOT-Gate(1pcs),Total count:2 NOT-Gates
4. Comparison: 74HC08 AND-Gate (1 pcs), Total count: 2 AND-Gates
   74HC32 OR-Gate (1 pcs), Total count:3 OR-Gates
   74HC86 XOR-Gate (1 pcs), Total count:3 XOR-Gates
5. Decoder : 74HC08 AND-Gate (1 pcs), Total count:4 AND-Gates
   74HC04 NOT-Gate(1pcs),Total count:2 NOT-Gates

[Part.3] Design Details of the Modules

This part gives DETAILED "Theoretical" information about the calculator design.

2-bit calculator includes 4 basic mathematical operations and 1 selection module.

First, the user selects what action to take. Then the user enters the first number (A0-A1) and the second number (B0-B1) with a 2-bit number. Finally, the user wants the numbers and operations are performed with leds.

As addition operation performs the addition of two 2-bit numbers and outputs a 3-bit sum. It consists of two standard full-adders.

As multiplication takes two 2-bit inputs and outputs a 4-bit product.

As subtractor takes in 2-bit numbers as an input, then output 1 bit to represent the sign and 2 bits to represent the difference.

As comparison takes two 2-bit inputs and has 3 outputs; one for each result:Less than, greater than and equals. The proper output will be high depending on the inputs.The selection module is used to select one of the operations mentioned above.This is done by using the decoder's truth table to perform the operation. For example, the first process runs when the decoder is sent to 0 and 0.

[Part.4] Theoretical & Experimental Results of the Modules

Addition Module										
Inputs					Outputs					
Number1		Number2		C_{in}	Theoretical			Experimental		
A_1	A_0	B_1	B_0		S_1	S_0	C_{out2}	S_1	S_0	C_{out2}
0	0	0	0		0	0	0			
0	0	0	1		0	1	0			
0	0	1	0		1	0	0			
0	0	1	1		1	1	0			
0	1	0	0		0	1	0			
0	1	0	1		1	0	0			
0	1	1	0		1	1	0			
0	1	1	1		0	0	1			
1	0	0	0		1	0	0			
1	0	0	1		1	1	0			
1	0	1	0		0	0	1			
1	0	1	1		0	1	1			
1	1	0	0		1	1	0			
1	1	0	1		0	0	1			
1	1	1	0		0	1	1			
1	1	1	1		1	0	1			

Subtraction Module										
Inputs					Outputs					
Number1		Number2		B_{in}	Theoretical			Experimental		
A_1	A_0	B_1	B_0		D_1	D_0	B_{out2}	D_1	D_0	B_{out2}
0	0	0	0		0	0	0			
0	0	0	1		0	1	1			
0	0	1	0		1	0	1			
0	0	1	1		1	1	1			
0	1	0	0		0	1	0			
0	1	0	1		0	0	0			
0	1	1	0		0	1	1			
0	1	1	1		1	0	1			
1	0	0	0		1	0	0			
1	0	0	1		0	1	0			
1	0	1	0		0	0	0			
1	0	1	1		0	1	1			
1	1	0	0		1	1	0			
1	1	0	1		1	0	0			
1	1	1	0		0	1	0			
1	1	1	1		0	0	0			

Multiplication Module											
Inputs				Outputs							
Number1		Number2		Theoretical				Experimental			
A_1	A_0	B_1	B_0	P_3	P_2	P_1	P_0	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0	0				
0	0	0	1	0	0	0	0				
0	0	1	0	0	0	0	0				
0	0	1	1	0	0	0	0				
0	1	0	0	0	0	0	0				
0	1	0	1	0	0	0	1				
0	1	1	0	0	0	1	0				
0	1	1	1	0	0	1	1				
1	0	0	0	0	0	0	0				
1	0	0	1	0	0	1	0				
1	0	1	0	0	1	0	0				
1	0	1	1	0	1	1	0				
1	1	0	0	0	0	0	0				
1	1	0	1	0	0	1	1				
1	1	1	0	0	1	1	0				
1	1	1	1	1	0	0	1				

Comparison Module									
Inputs				Outputs					
Number1		Number2		Theoretical			Experimental		
A_1	A_0	B_1	B_0	A<B	A=B	A>B	A<B	A=B	A>B
0	0	0	0	0	1	0			
0	0	0	1	1	0	0			
0	0	1	0	1	0	0			
0	0	1	1	1	0	0			
0	1	0	0	0	0	1			
0	1	0	1	0	1	0			
0	1	1	0	1	0	0			
0	1	1	1	1	0	0			
1	0	0	0	0	0	1			
1	0	0	1	0	0	1			
1	0	1	0	0	1	0			
1	0	1	1	1	0	0			
1	1	0	0	0	0	1			
1	1	0	1	0	0	1			
1	1	1	0	0	0	1			
1	1	1	1	0	1	0			

[Part.5] Simulation printouts of the modules.

DECODER: https://simulator.io/board/q6xIgt6gwr/1
MULTIPLICATION: https://simulator.io/board/OAtfrtT4iU/1
ADDITION: https://simulator.io/board/7Gccs1CnRf/1
COMPARISON: https://simulator.io/board/qSMwWlA207/1
SUBTRACTION: https://simulator.io/board/GhhBBQLoUQ/1