CS2842 Computer Systems – Lecture VII

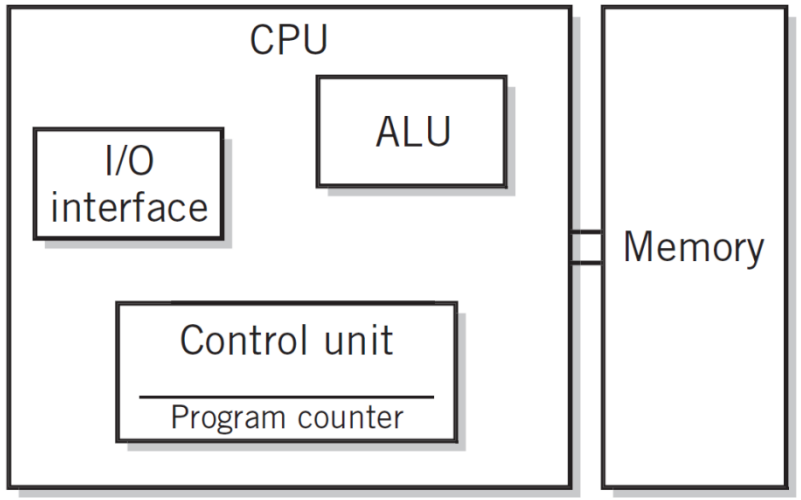
# The CPU and Memory

Dr. Sapumal Ahangama
Department of Computer Science and Engineering

# COMPONENTS OF THE CPU

- The CPU comprises of the following components
  - ALU
  - Control Unit (CU)
- Key components of the CU
  - Program Counter
  - Memory Management Unit
  - I/O Interface

System Block Diagram



# REGISTERS

- A storage location within the CPU for a specific purpose
  - Holds a binary value temporarily for storage
  - Usually each register has a defined task
  - Can be 1 bit or wide as several bytes
- Memory vs. Registers?
- A register may hold,
  - Data being processed
  - An instruction being executed
  - A memory or I/O address to be accessed
  - Special binary codes (status of the computer)
  - Conditions of calculations

# REGISTERS

- Accumulator
  - A general purpose register
  - Hold the data that are used for arithmetic operations
  - Used for moving data in memory
  - Modern computer come with multiple accumulators

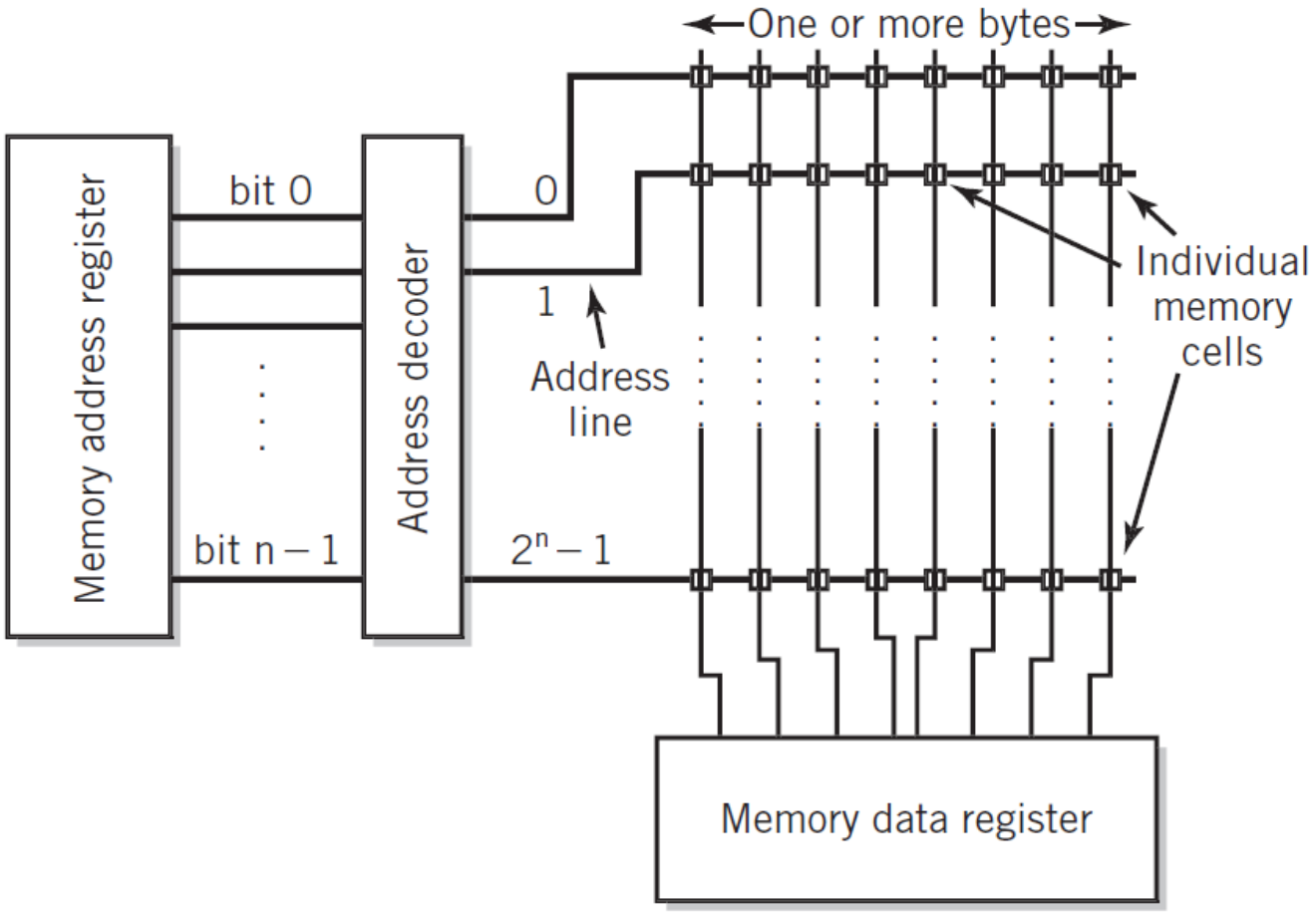
# REGISTERS

- Registers on Control Unit
  - **Program Counter (PC) register** holds the address of the current instruction being executed
  - **Instruction Register (IR)** holds the actual instruction being executed
  - **Memory Address Register (MAR)** holds the address of a memory location
  - **Memory Data Register (MDR)** holds a data value that is being stored to or retrieved from the memory
  - **Status Registers**

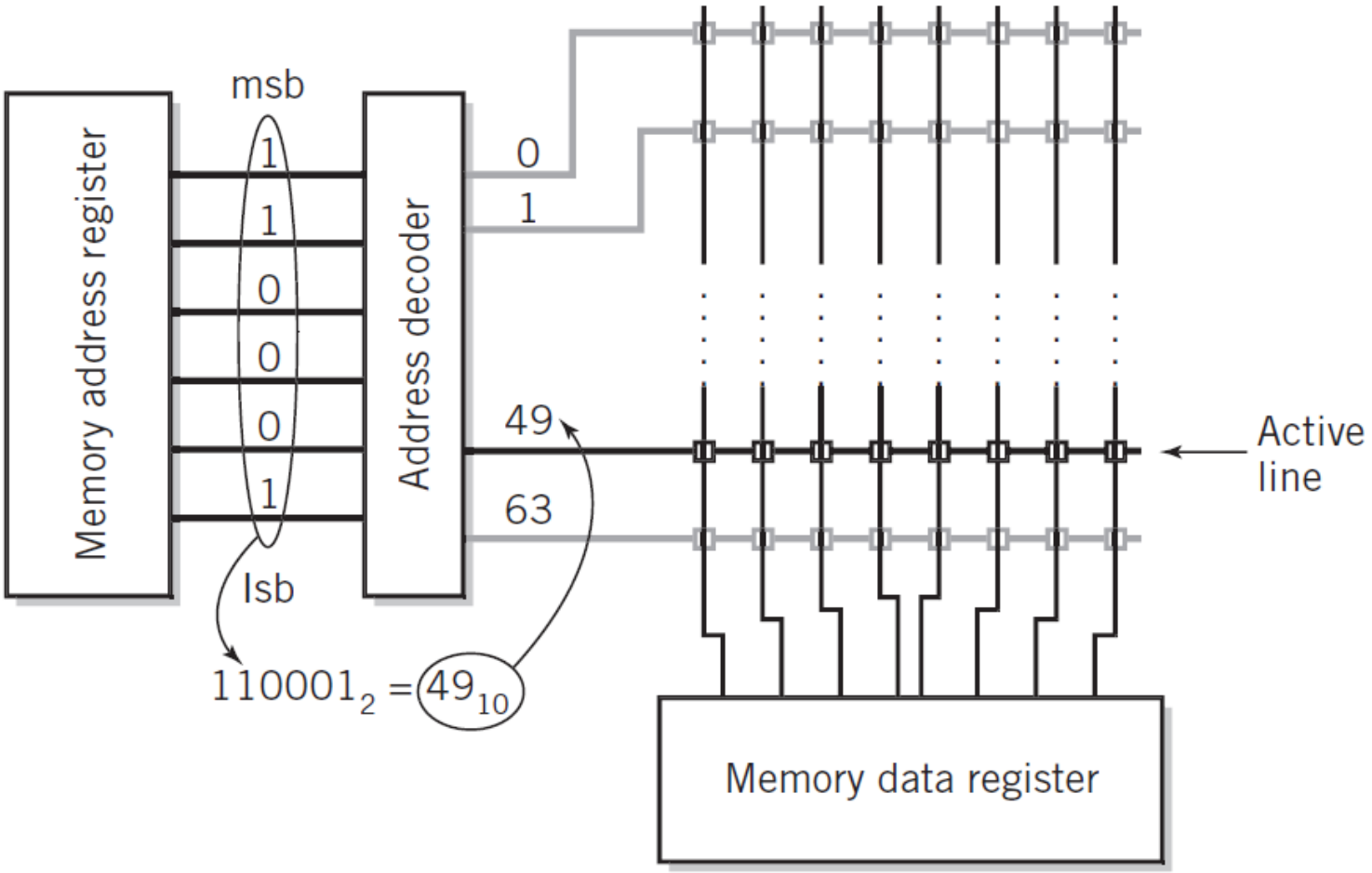
# THE MEMORY UNIT

- Each memory location has a unique address
- Address from an instruction is copied to the MAR which finds the location in memory
- CPU determines if it is a store or retrieval
- Transfer takes place between the MDR and memory

# THE MEMORY UNIT



# THE MEMORY UNIT



# MEMORY CAPACITY

- The number of bits in the MAR determines how many different address locations can be decoded

$$M = 2^k$$

- 32 bits allows 4,294,967,296 or 4 GB
- The size of MDR decides how much data can be loaded in a single operation
  - Modern computer memories are designed to allow the retrieval or storage of at least 4 and, more commonly, 8 or even 16, successive bytes

# MEMORY CHARACTERISTICS

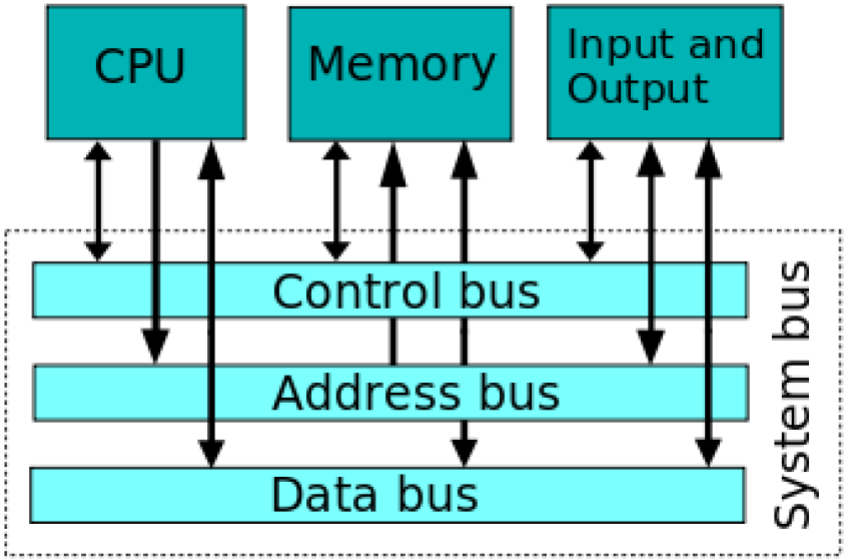
- Read-Write capable or Read-only
- Volatile or Nonvolatile
  - Nonvolatile memory retains its values when power is removed
- Dynamic and Static RAM
  - Static RAM does not require refreshing, used in cache memory

# ROM

- Read Only Memory
  - Software is built semi-permanently into the computer, and is not expected to change over the life of the computer
- Bootstrap programs and basic I/O system drivers
- Flash Memory?

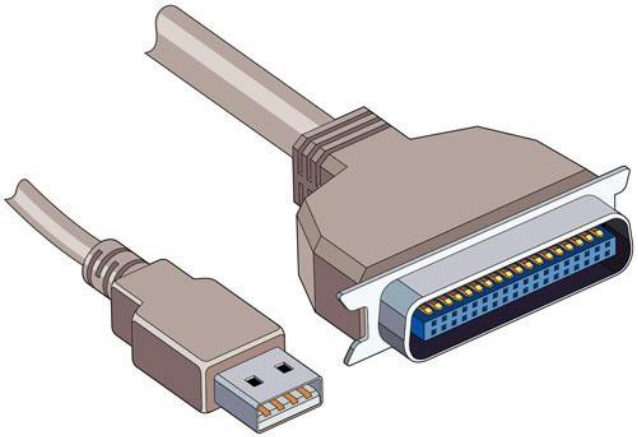
# BUSES

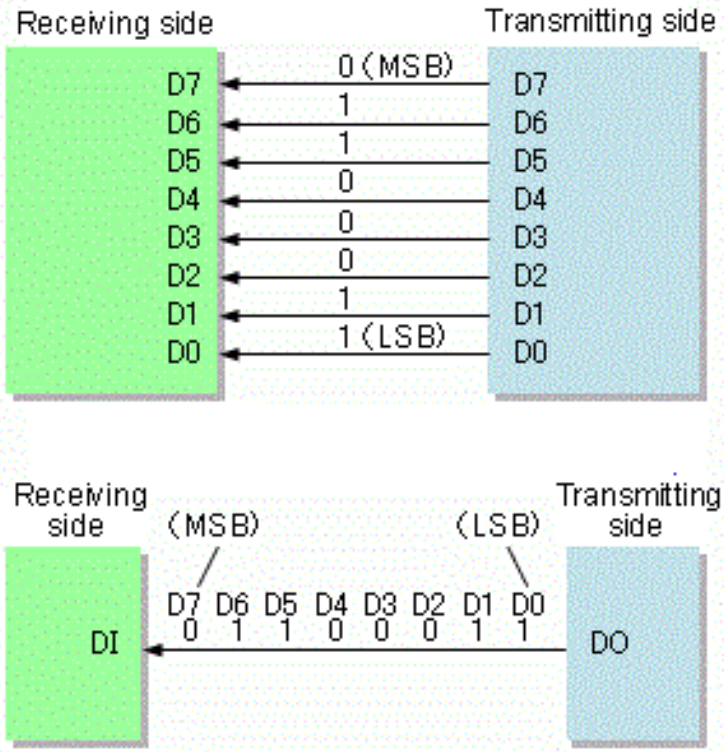
- The physical connection that makes it possible to transfer data from one location to another
  - Computer peripherals and CPU
  - CPU and memory
  - Different point of a CPU
- Four general categories
  - Data
  - Addressing
  - Control
  - Power



# BUSES

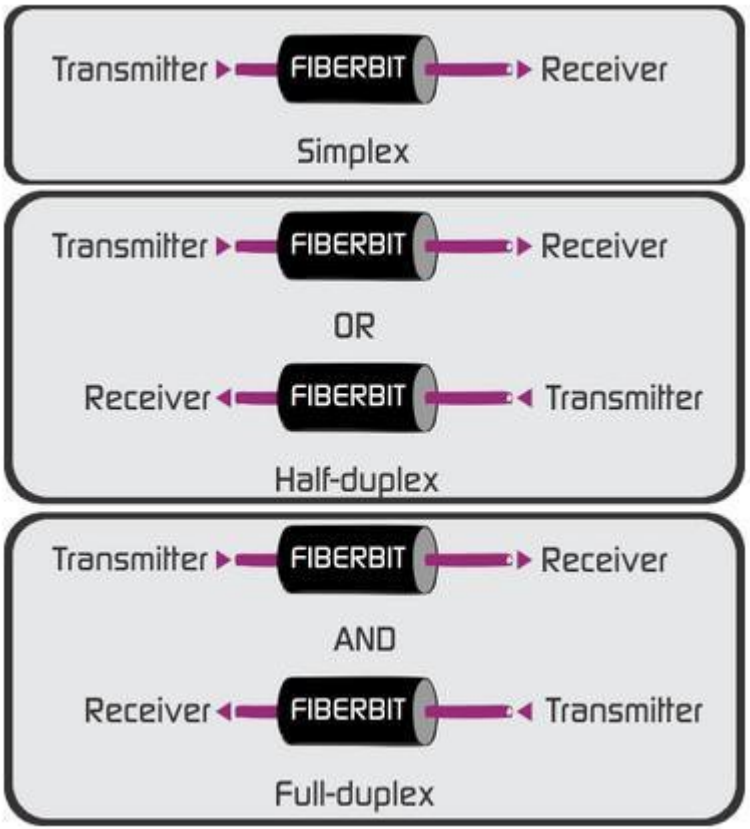
- Parallel Vs. Serial Buses
  - Parallel bus: an individual line for each bit of data
  - Serial bus: data is transferred sequentially, one bit at a time, using a single data line
  - Multiplexed data & address
  - Bus protocol





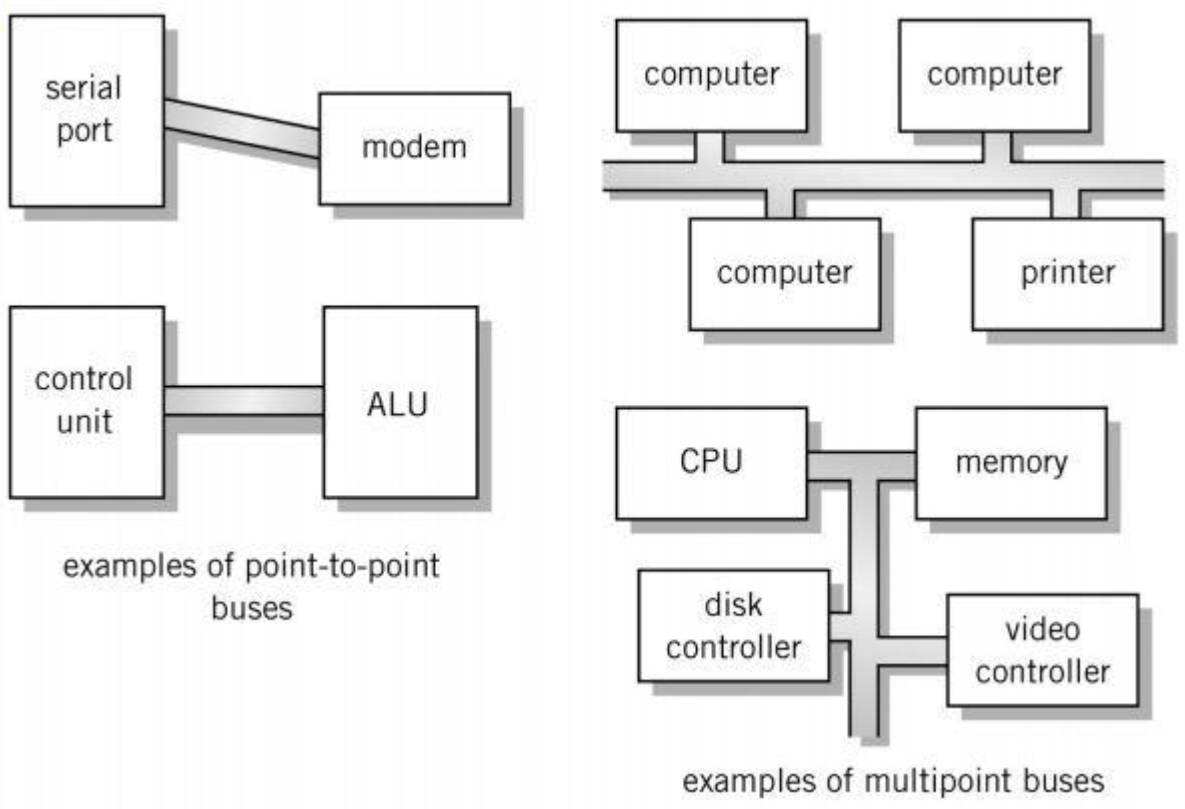
# BUSES

- Direction of transmission



# BUSES

- Method of Interconnection



# INSTRUCTIONS

- Different categories of instructions

- Data Move Instructions
  - Includes instructions to move data from memory to general registers, from general registers to memory, between different general registers
  - LOAD and STORE of LMC
  - Variations, LOAD BYTE, LOAD HALD-WORD, LOAD WORD

# INSTRUCTIONS

- Arithmetic Instructions
  - Every CPU instruction set includes integer addition and subtraction
  - Multiplication, Division, Floating Point Arithmetic, BCD
  - Most operations can be achieved using addition

# INSTRUCTIONS

- Boolean Instructions
  - Instructions for performing Boolean algebra
  - NOT
  - AND, OR, EXCLUSIVE OR

# INSTRUCTIONS

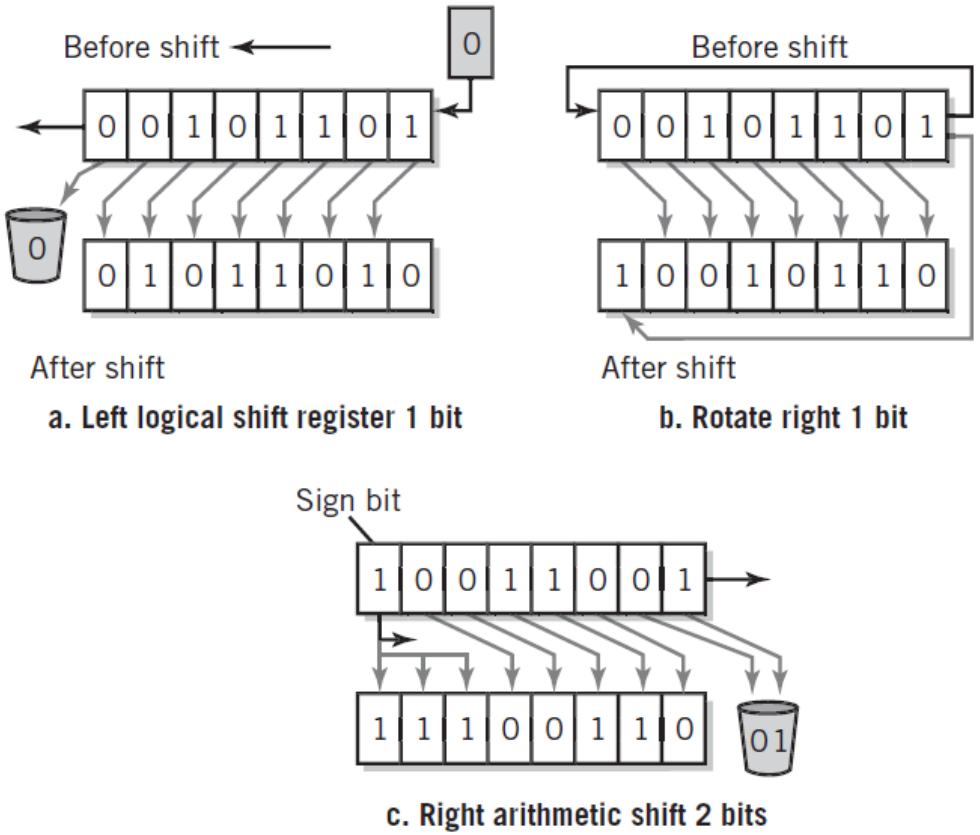
- Single Operand Instructions
  - Provide other convenient single operand instructions similar to NOT
  - Mostly operate on values in registers
  - NEGATING, INCREMENTING, DECREMENTING

# INSTRUCTIONS

- Bit Manipulation Instructions
  - For setting and resetting individual bits
  - Change, Clear, Set bits

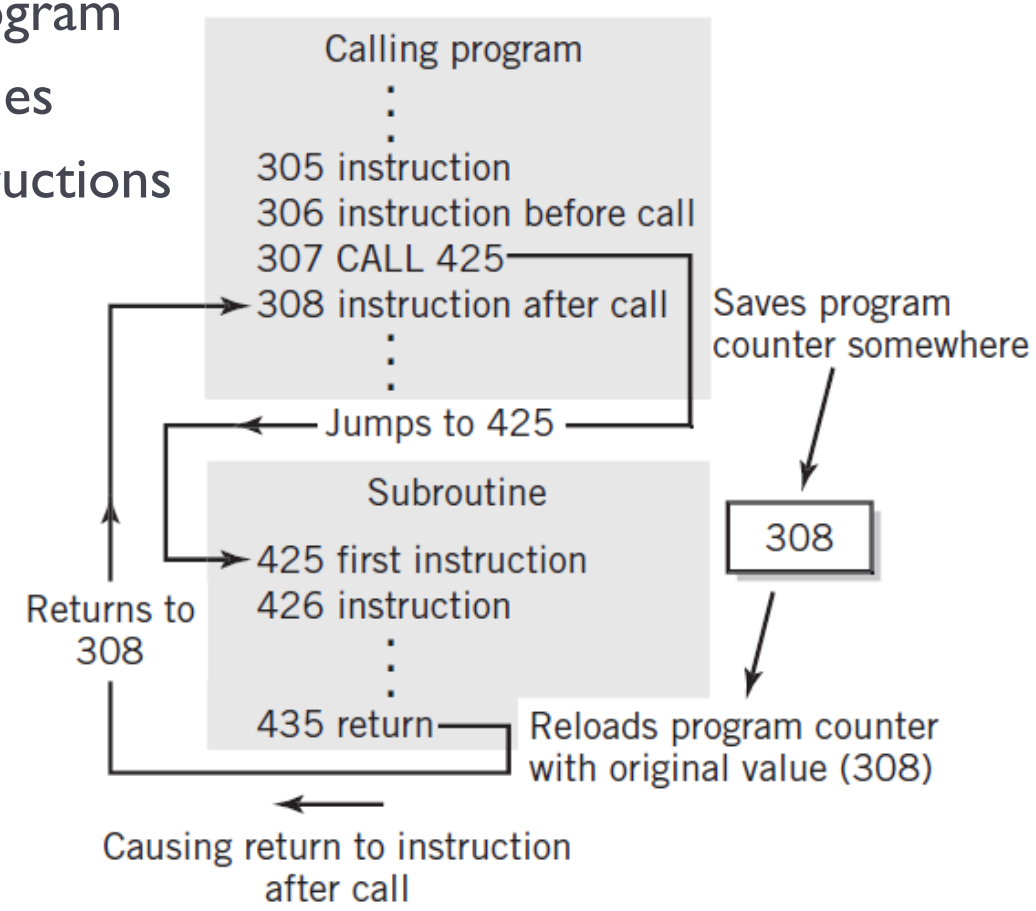
# INSTRUCTIONS

- Shift and Rotate Instructions
  - Means to implement multiplication, division and other operations



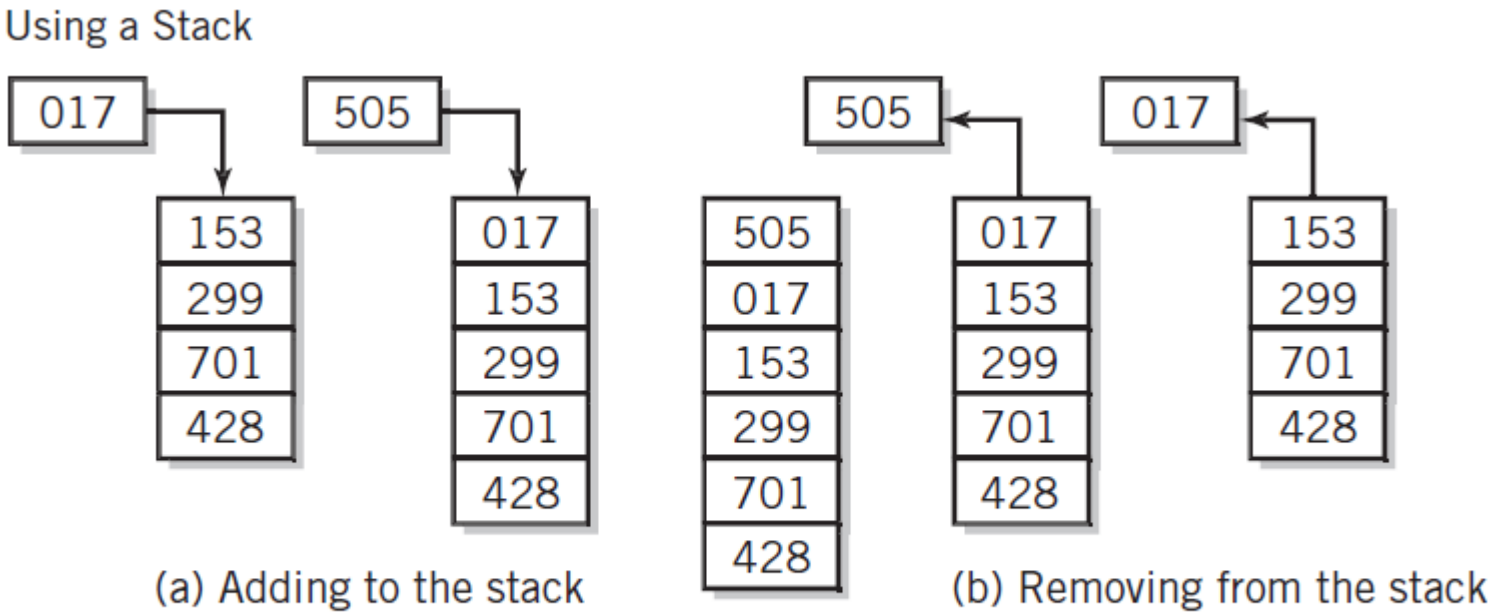
# INSTRUCTIONS

- Program Control Instructions
  - Control the flow of a program
  - Include jumps and branches
  - CALL and RETURN instructions



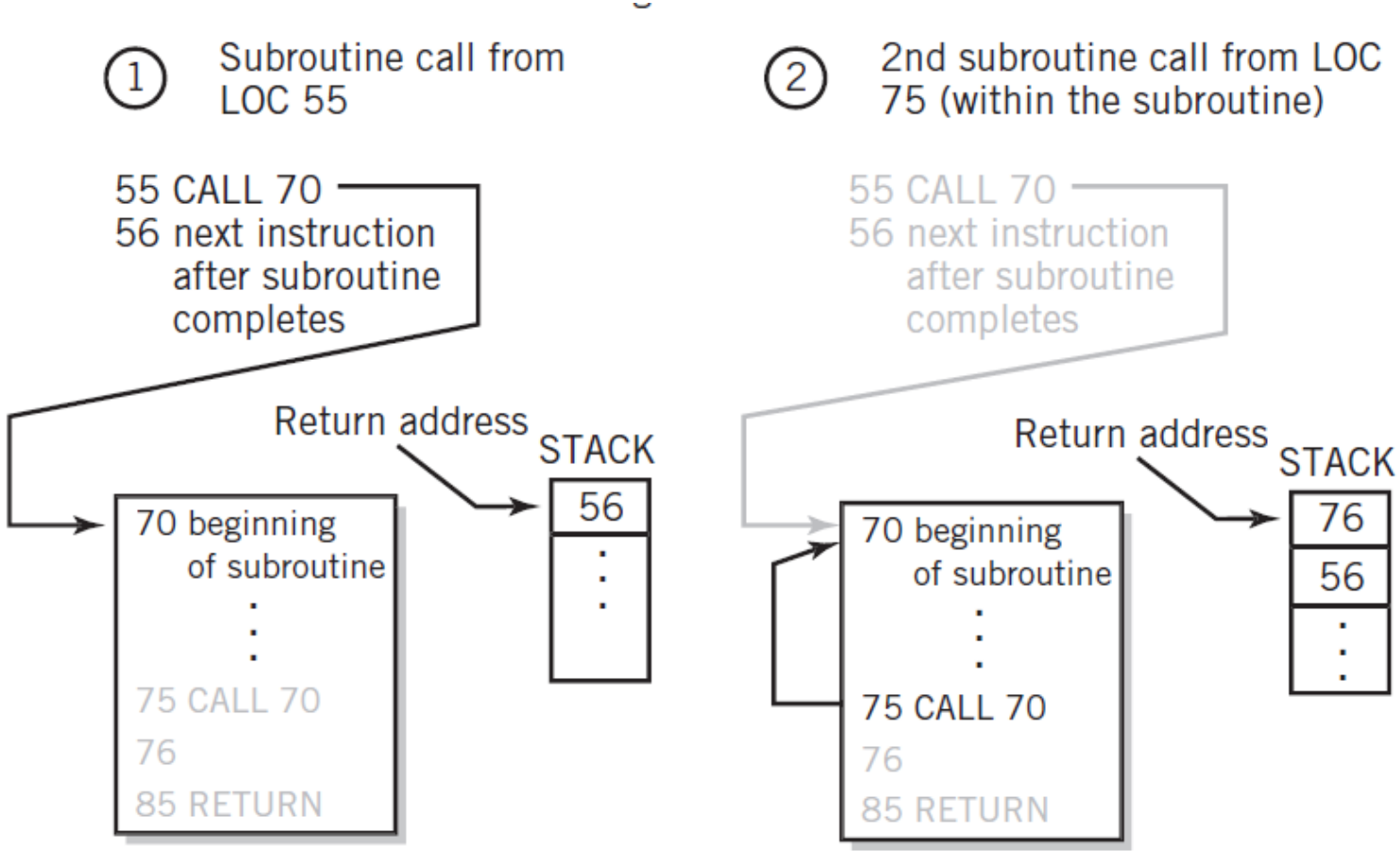
# INSTRUCTIONS

- Stack Instructions
  - Stack is used to store data when the most recently used data will also be the first needed, Last in First Out (LIFO)
  - PUSH, POP



# INSTRUCTIONS

- Stack Instructions



# MEMORY ENHANCEMENTS

- Memory is slow compared to CPU processing speeds
  - 2 Ghz CPU 1 cycle in ½ of a billionth of a second
  - 70 ns DRAM 1 access in 70 millionth of a second

- Methods to improve memory accesses
  - Wide Path Memory Access
  - Memory Interleaving
  - Cache Memory

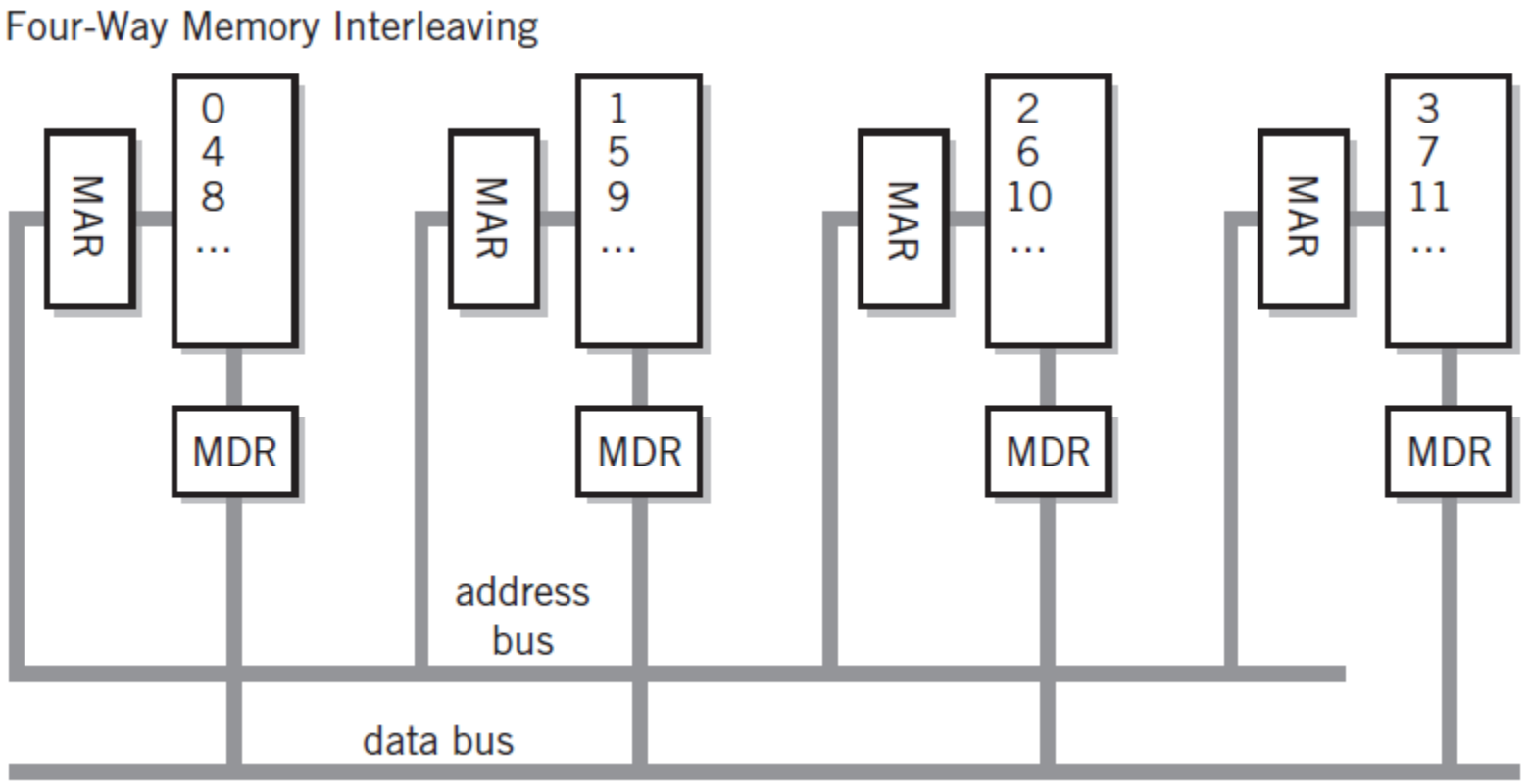
# WIDE PATH MEMORY ACCESS

- Retrieve multiple bytes instead of 1 byte at a time
- Wider bus data path and larger MDR
- Increased number of bytes  leads to increased complexity
- All retrieved bytes may not be used

# MEMORY INTERLEAVING

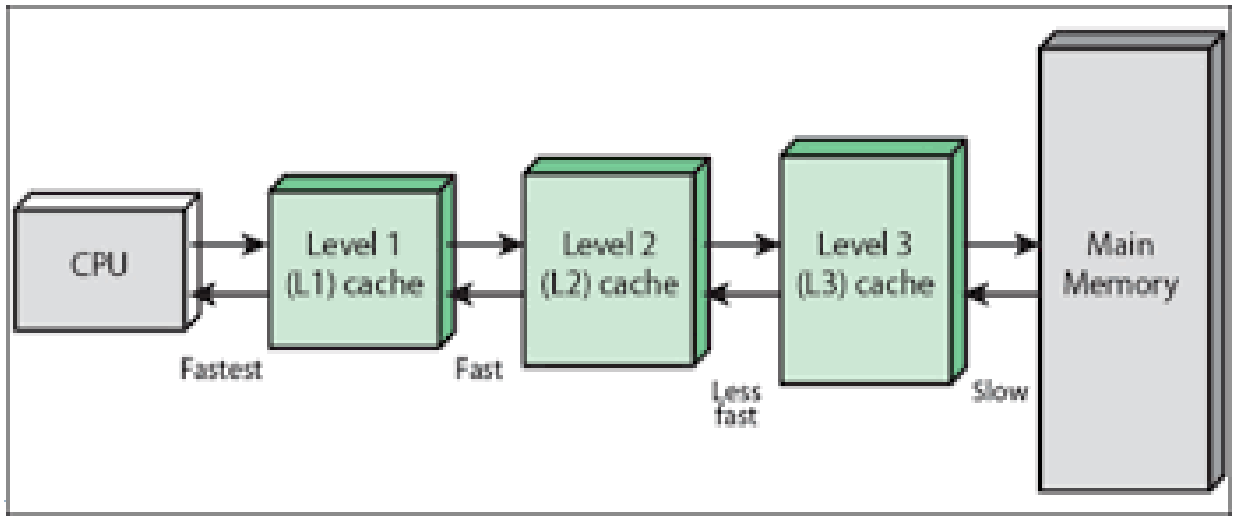
- Partition memory into subsections
- Each with own MAR and MDR
- Each section is accessed separately
- N-way Interleaving

# MEMORY INTERLEAVING



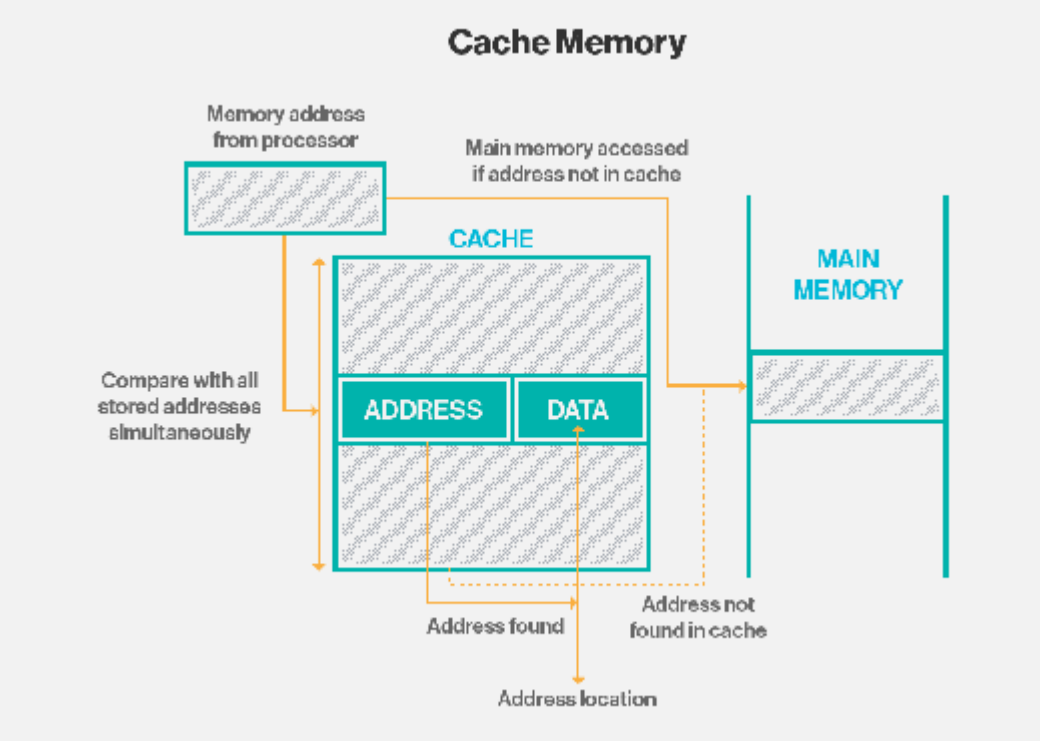
# CACHE MEMORY

- A small amount of high speed memory between CPU and memory
- Arranged in blocks: 8 or 16 bytes - Cache line
- Cache Line
  - Unit of transfer between storage and cache memory

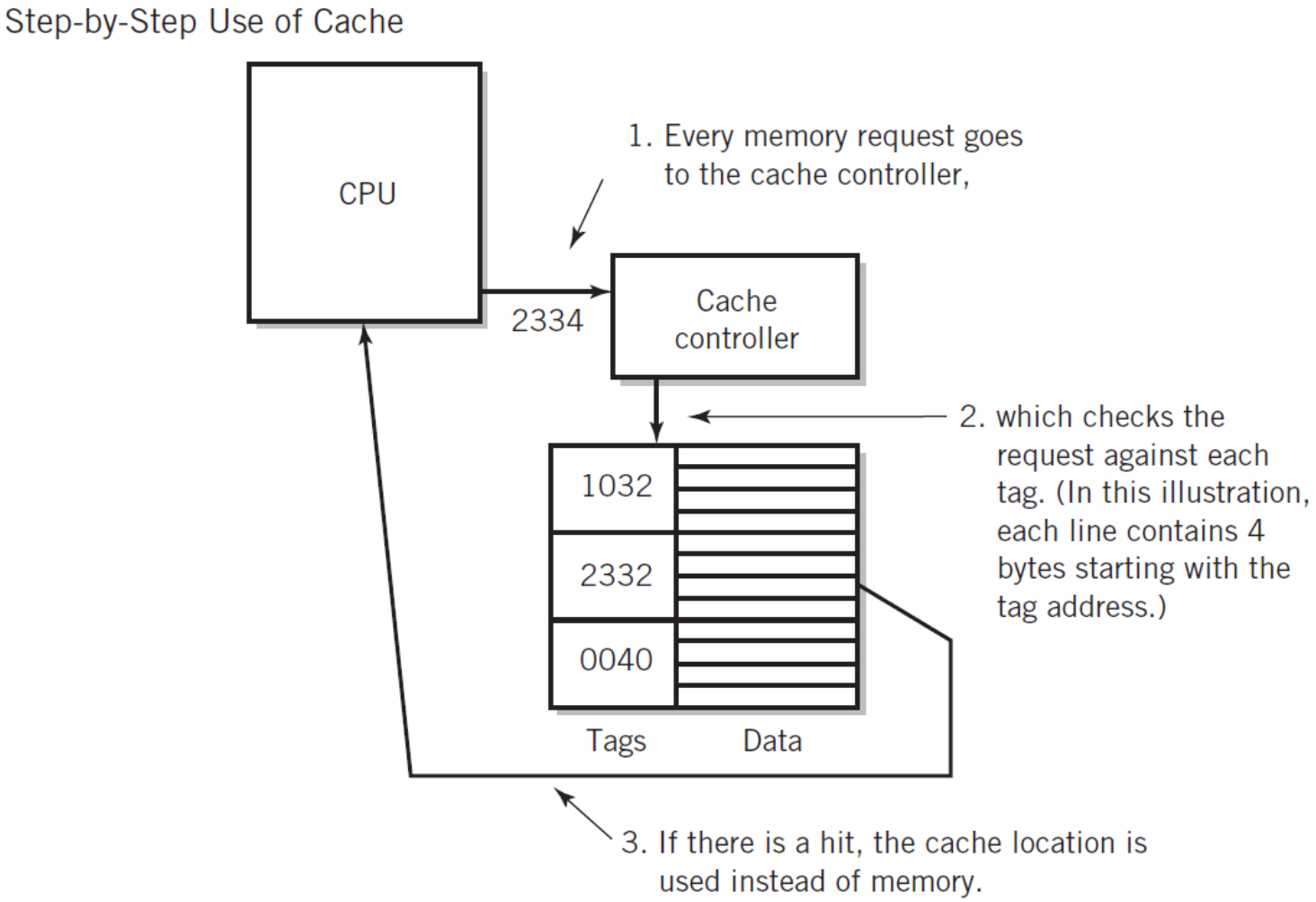


# CACHE MEMORY

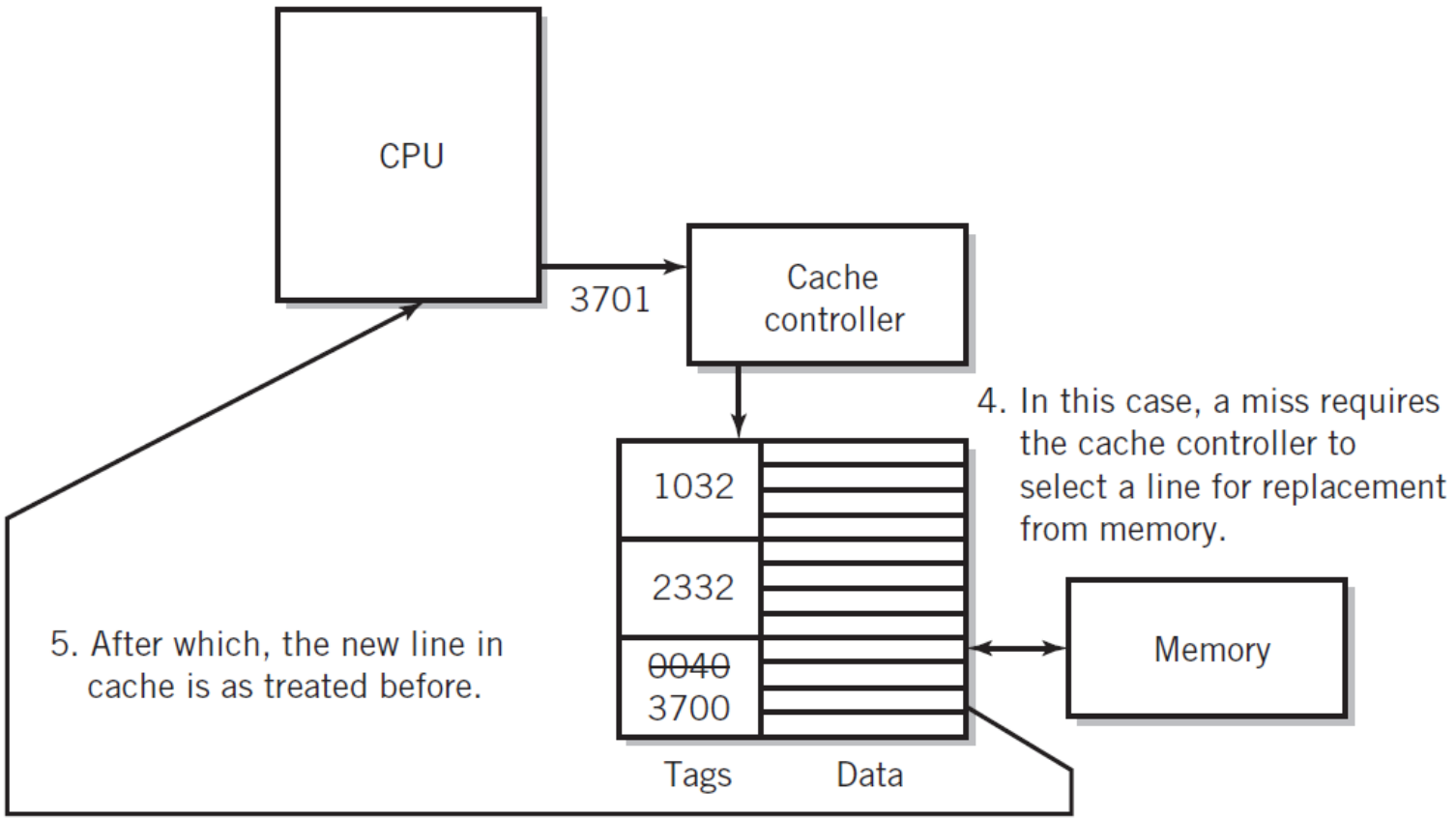
- Tags : pointer to location in main memory
  - Cache controller
  - hardware that checks tags



# CACHE HIT


Step-by-Step Use of Cache
CPU
1. Every memory request goes to the cache controller,
2334
Cache controller
2. which checks the request against each tag. (In this illustration, each line contains 4 bytes starting with the tag address.)
1032
2332
0040
Tags
Data
3. If there is a hit, the cache location is used instead of memory.

# CACHE MISS


CPU
3701
Cache controller
4. In this case, a miss requires the cache controller to select a line for replacement from memory.
1032
2332
0040
3700
Tags
Data
Memory
5. After which, the new line in cache is as treated before.

# THANK YOU

# REFERNCES


- Chapter 7 and 8: The Architecture of Computer Hardware, Systems Software & Networking: An Information Technology Approach -4th Edition, Irv Englander -John Wiley and Sons