數位系統設計實習
Final Project

指導老師：陳勇志 教授

Schedule

Week	Day	Lecture	Content	Note
1	09/02,03	1	Introduction, Verilog HDL (Gate level)	
2	09/09,10	2	Verilog HDL (Date flow level)	
3	09/16,17		No class	9/17 Moon Festival
4	09/23,24	3	Verilog HDL (Behavior level)	
5	09/30,10/01	4	Sequential logic, Latch and Flip-Flop	
6	10/07,08	5	Counter	
7	10/14,15	6	Shift Register, Johnson Counter	
8	10/21,22	7	FSM, Seven segment display, Binary to BCD	
9	10/28,29	8	SMIMS Development Board, LFSR	
10	11/04,05	9	LCD module	
11	11/11,12		Final project	
12	11/18,19		Final project	
13	11/20,21		Final project	
14	12/02,03		Final project	
15	12/09,10		Final project demo	Project deadline
16	12/16,17		Final exam	

Final Project Demo

- One person per group
- 6-min in-class presentation (Week 15: 12/9,10)
  - 3-min slide presentation
  - 3-min pre-recorded video demonstration

Deliveries

- **Complete all the submissions by the end of class (Week 15: 12/9,10)**
  - .dkp, .rbf, and presentation slide
    - Tar/zip them into a single file and submit it to Moodle
    - File name: Bxxxxxxxx_DEMO
  - Quartus project
    - Tar/zip the project into a single file and submit it to Moodle
    - File name: Bxxxxxxxx_林小明_Project
  - Demonstration video
    - Upload it to the following google drive
      - https://drive.google.com/drive/folders/1-6ffgyr2ZZ8HeunlSbzMsi0N_6YXuZFr?usp=sharing
    - File name:數位系統設計實習小影片_final_project_Bxxxxxxxx_林小明