數位系統設計實習

Lecture 1

Verilog HDL (Gate Level)

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實習課助教：黃柏皓

Chapter

- Introduce Verilog
- Verilog HDL (Gate Level)
- Quartus II
  - build a Project
  - simulate
- LAB1

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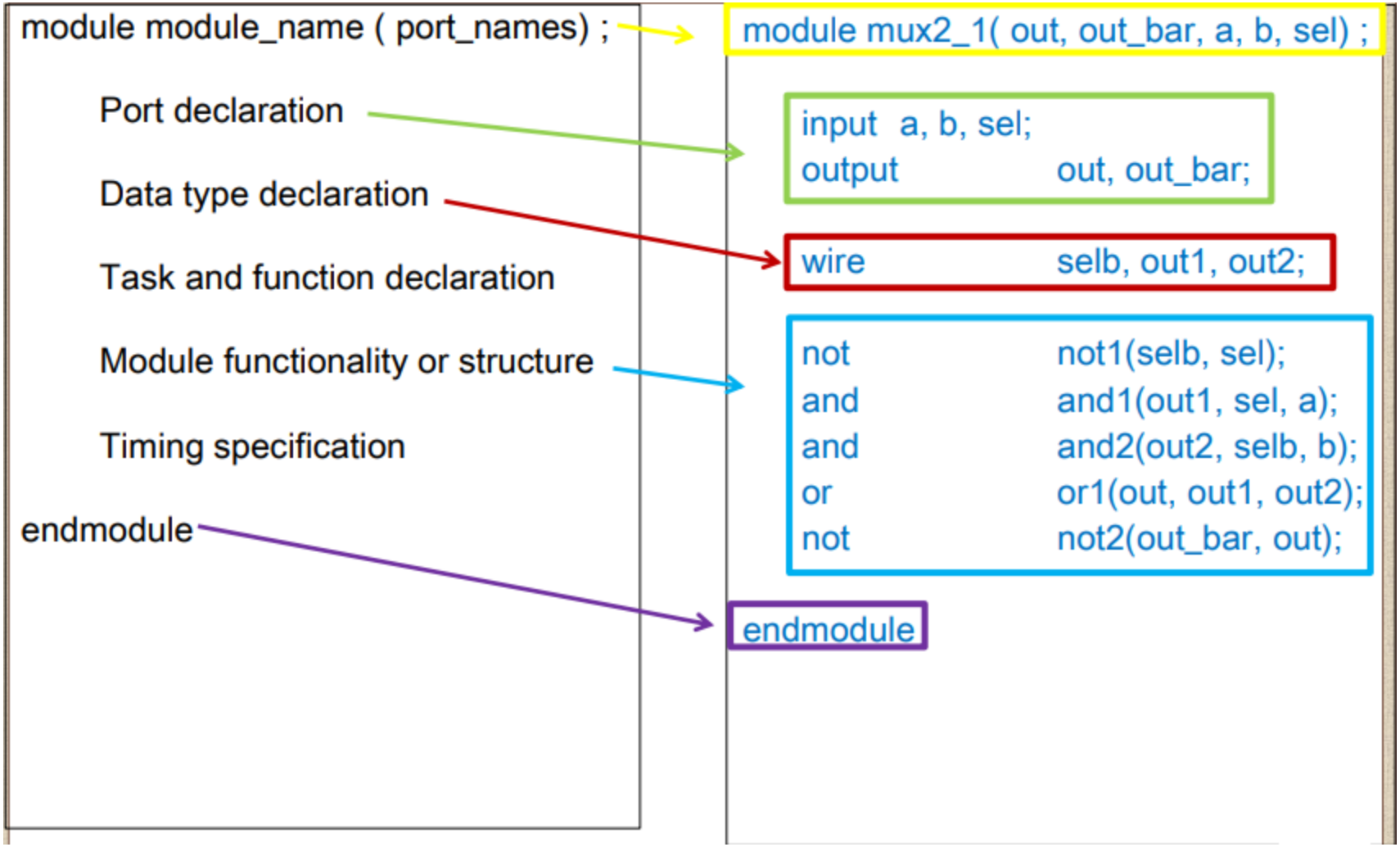
Introduce Verilog



Introduce verilog

- 空白(White space)

  -空格(blank space) , 定位字(tab), 換行(new line)都屬於空白字元。

- 註解(Comment)

  -單行註解--- //

  -多行註解--- /* */

- 關鍵字(keyword)

  -全部以小寫表示

  -又稱為保留字, 識別字的命名不可以和關鍵字相同, 必須避開以免造成混淆

  -如module, endmodule, input, output, begin, end, assign, always, initial, if, ...

Introduce verilog

- 識別字(identifier)

  -區分大小寫

  -第一個字元必須為字母,第二個之後可以為字母、數字、底線所組成

  -Example1和example1是二個不同的識別字

- 分號(;)

  -作敘述的分隔

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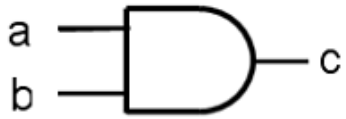
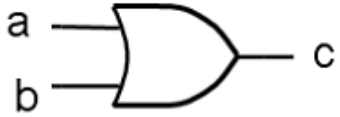
Verilog HDL

and




```
and (c,a,b);
```

or

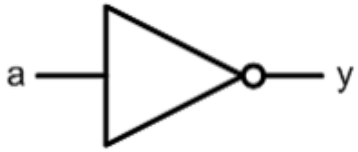



```
or (c,a,b);
```

nand

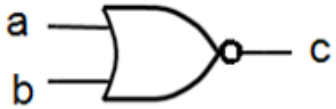

```
nand (c,a,b);
```

not




```
not (y,a);
```

nor

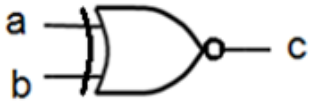



```
nor (c,a,b);
```

xor

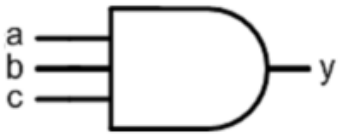

```
xor (c,a,b);
```

xnor




```
xnor (c,a,b);
```

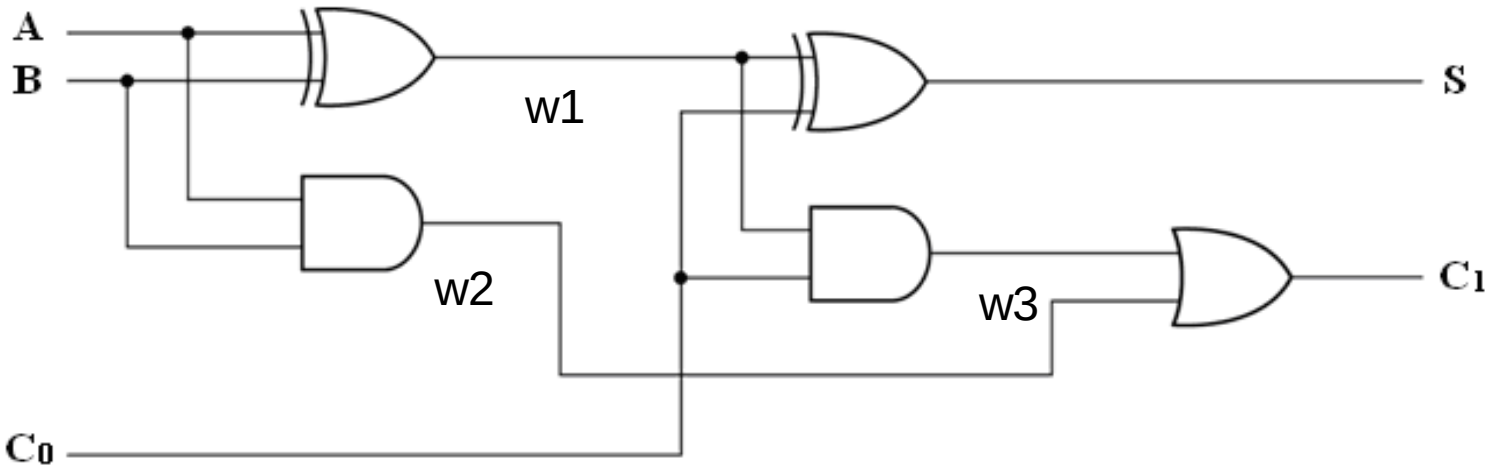
and




```
and (y,a,b,c);
```

Verilog HDL

- EX：Full adder



Verilog HDL

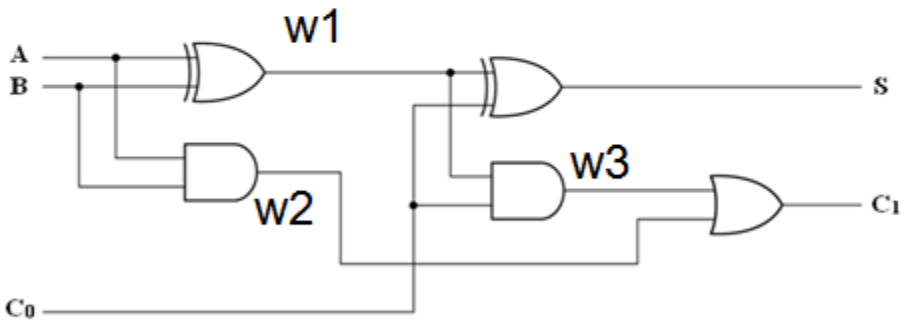

```
module fulladder(A, B, C0, C1, S);

input A, B, C0;
output S, C1;
wire w1, w2, w3;

xor  g1(w1, A, B);
xor  g2(S, w1, C0);
and g3(w2, A, B);
and g4(w3, w1, C0);
or   g5(C1, w3, w2);

endmodule
```

注意 module name 要跟 project 與.v檔檔名相同！



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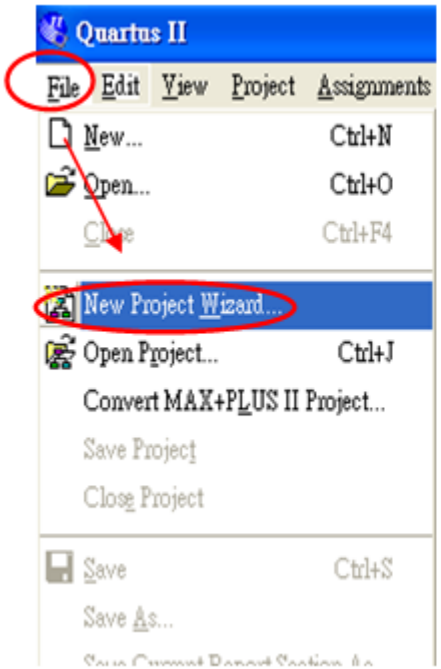
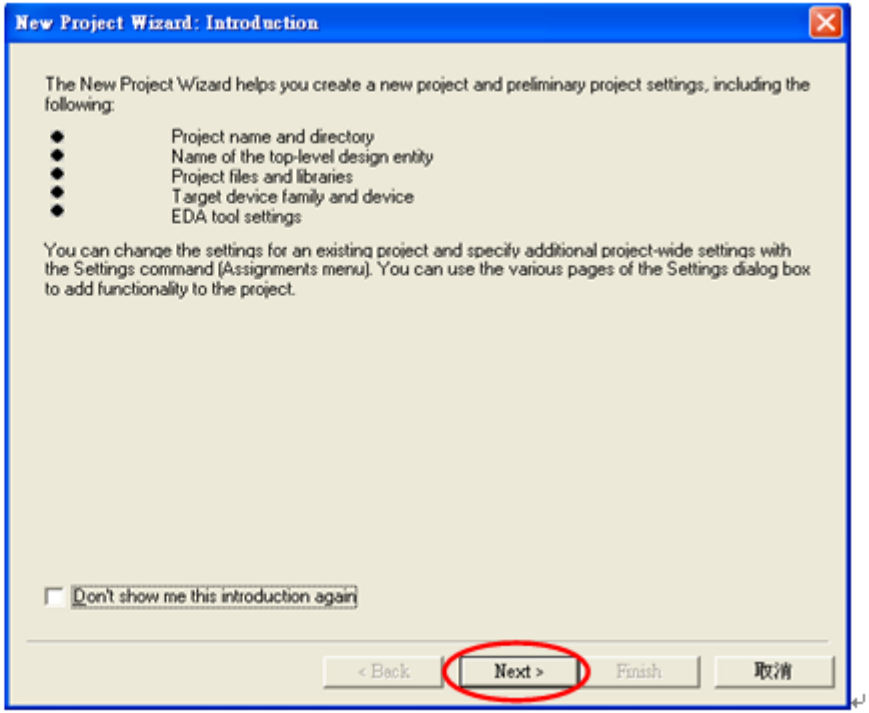
Quartus II - build a Project

- 專案開發流程(只有用波形模擬)：
  - 建立新專案(New project wizard)
  - 開新verilog檔案(.v檔)
  - 決定輸入與輸出腳位
  - 主程式
  - Compile(Compiler Tool)
  - 建立波形檔 (.vwf檔)
  - 模擬波形(Simulator Tool)
  - 儲存模擬結果報告(.vcd檔)

Quartus II - build a Project

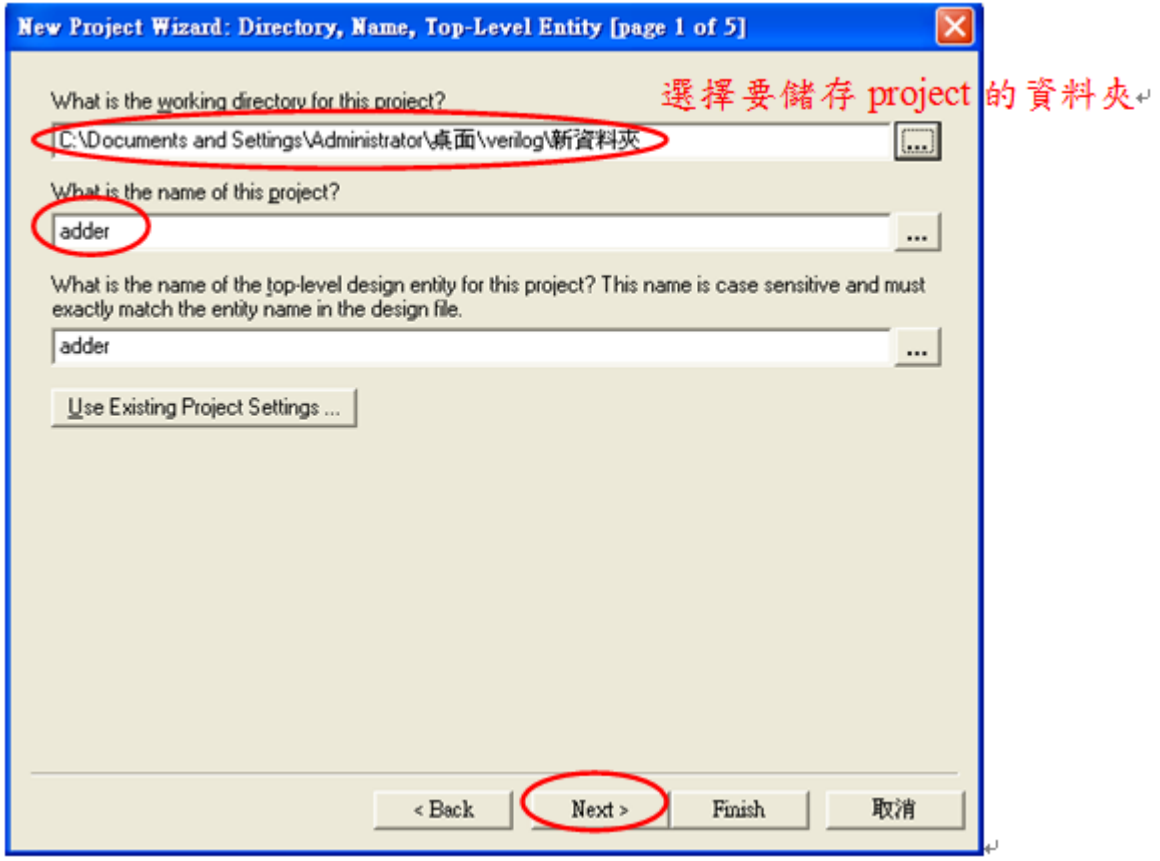
- 1.





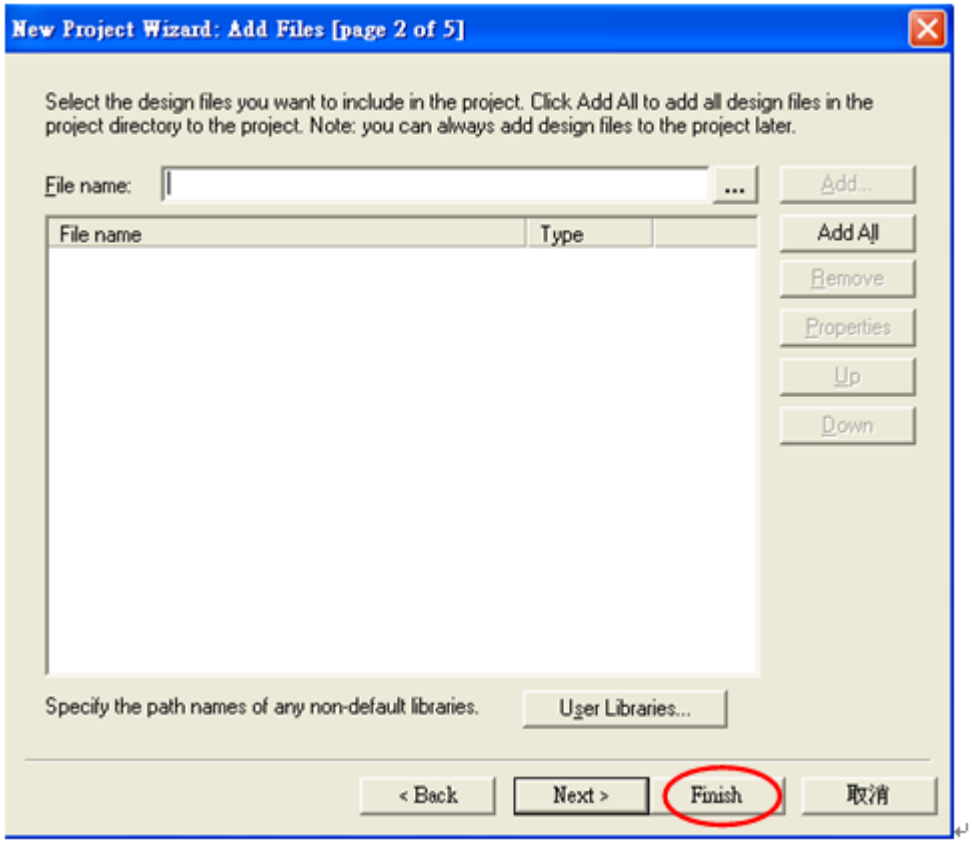
Quartus II - build a Project

- 2.



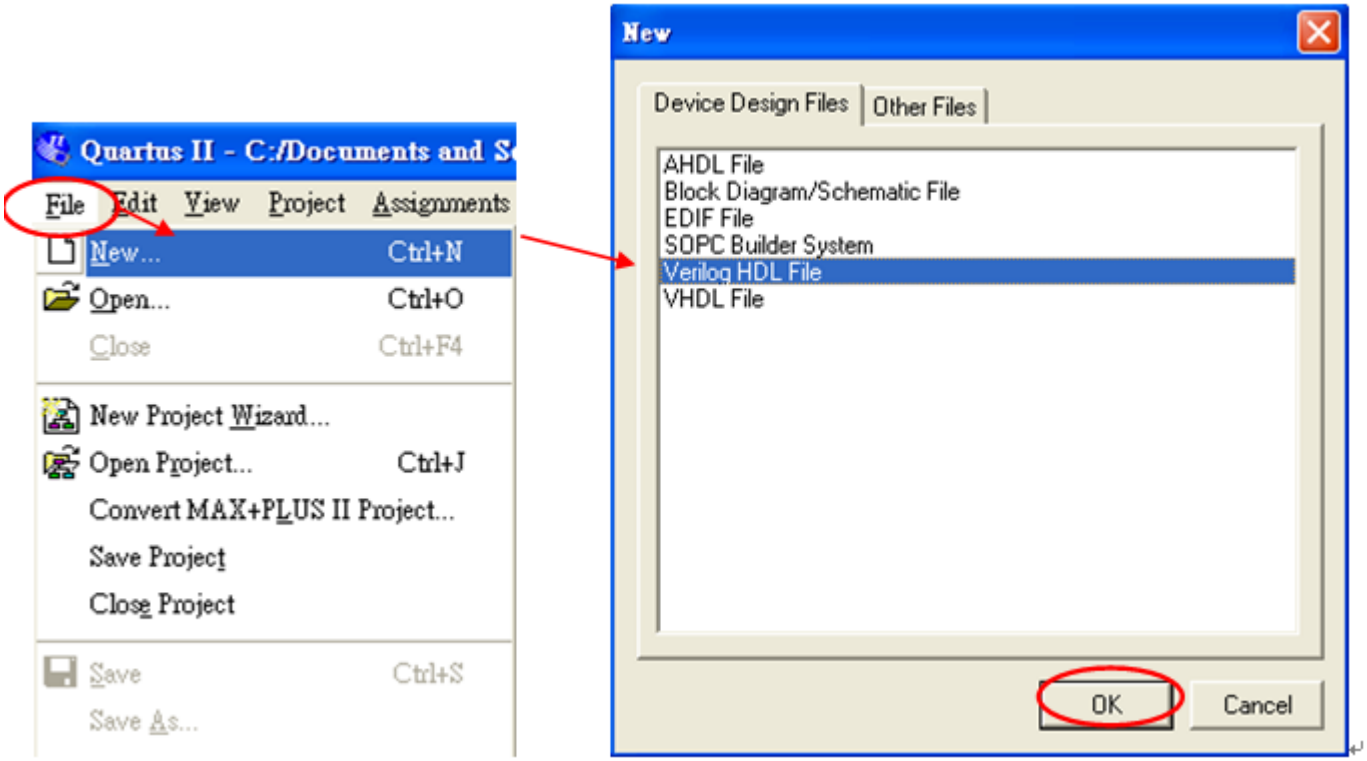
Quartus II - build a Project

- 3.



Quartus II - build a Project

- 4.



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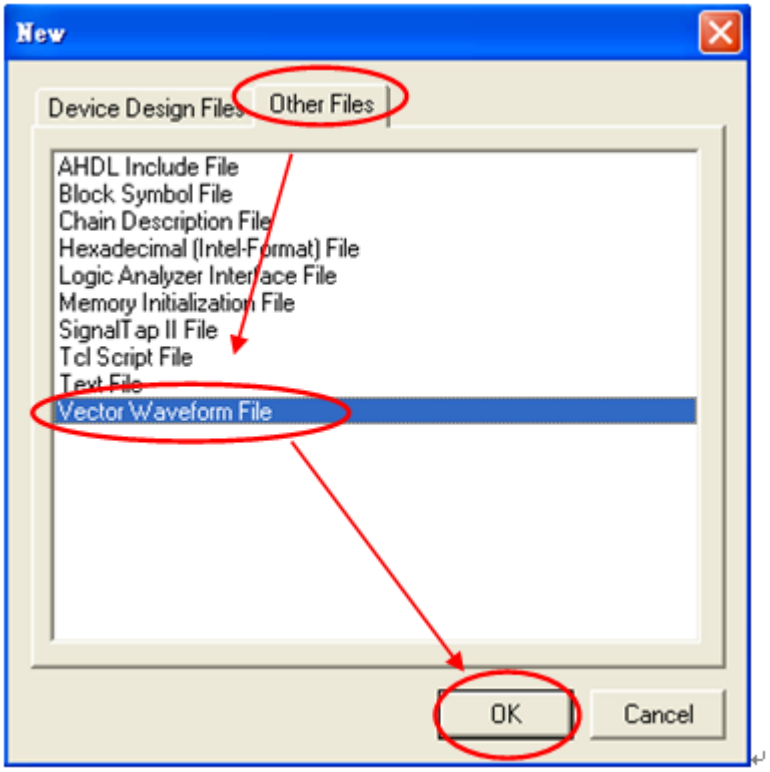
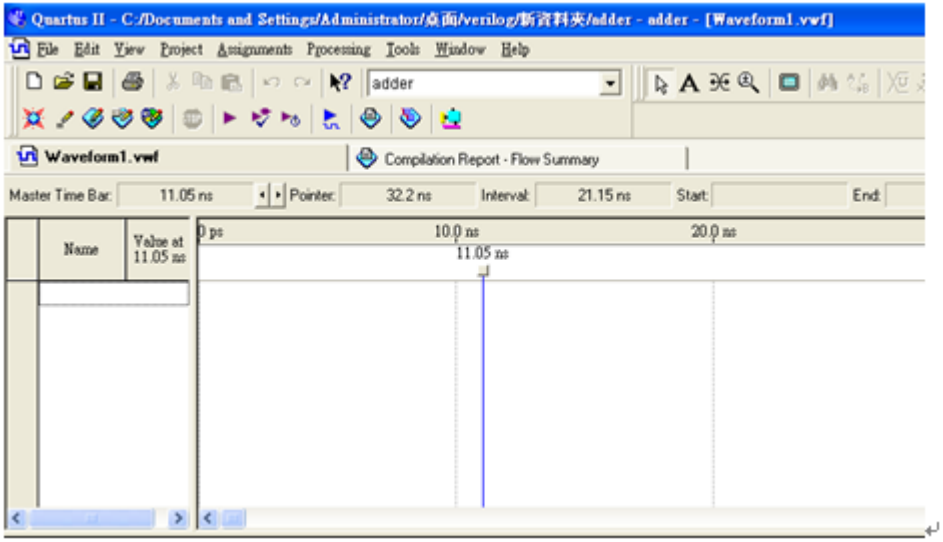
Quartus II - simulate

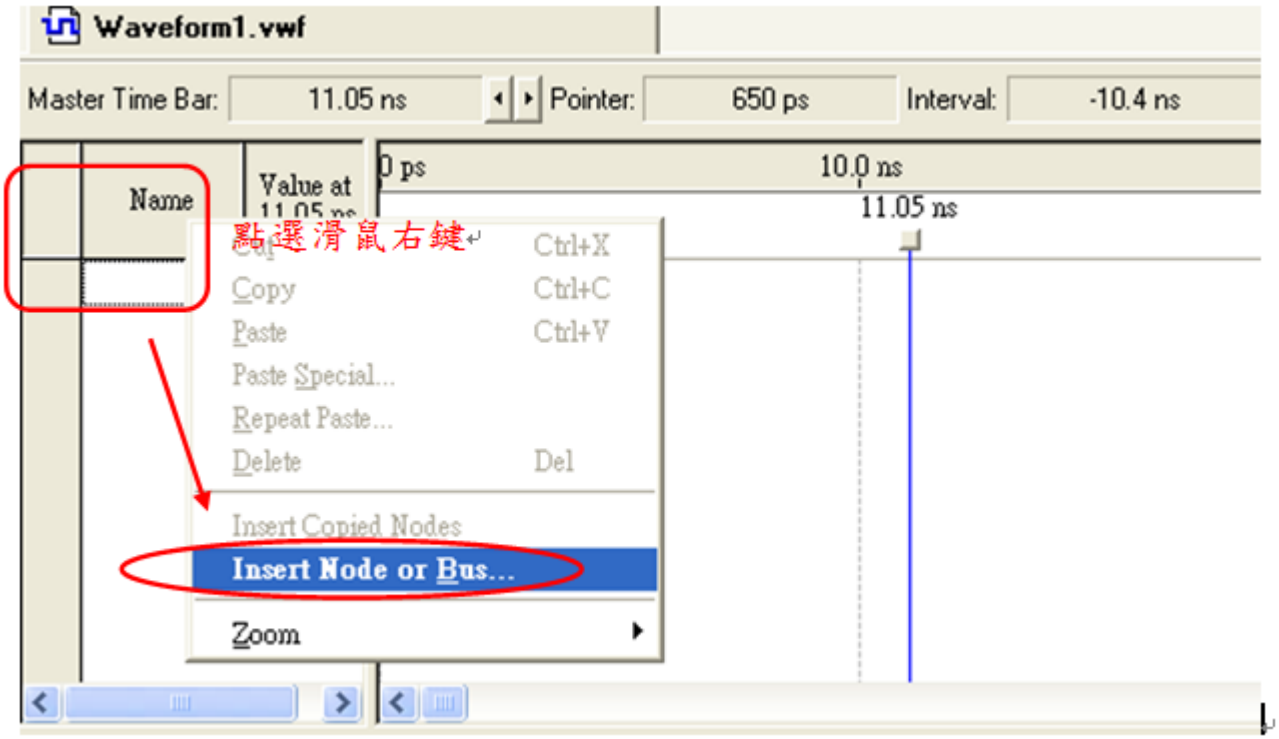
- 1. create a .vwf file





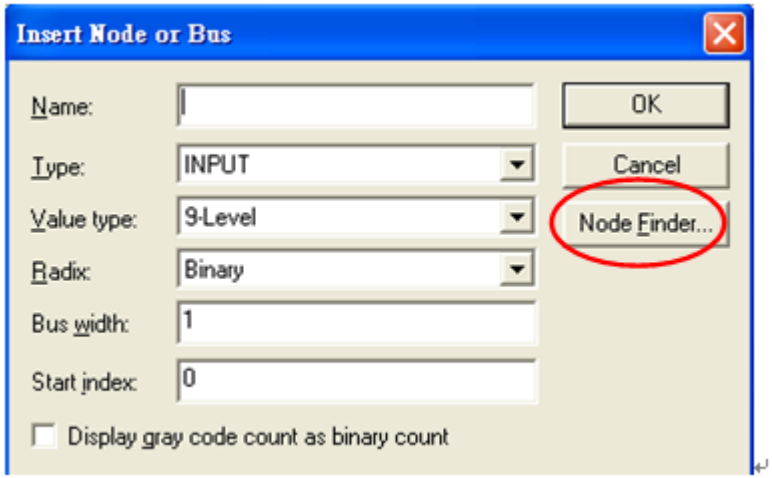
Quartus II - simulate

- 2.



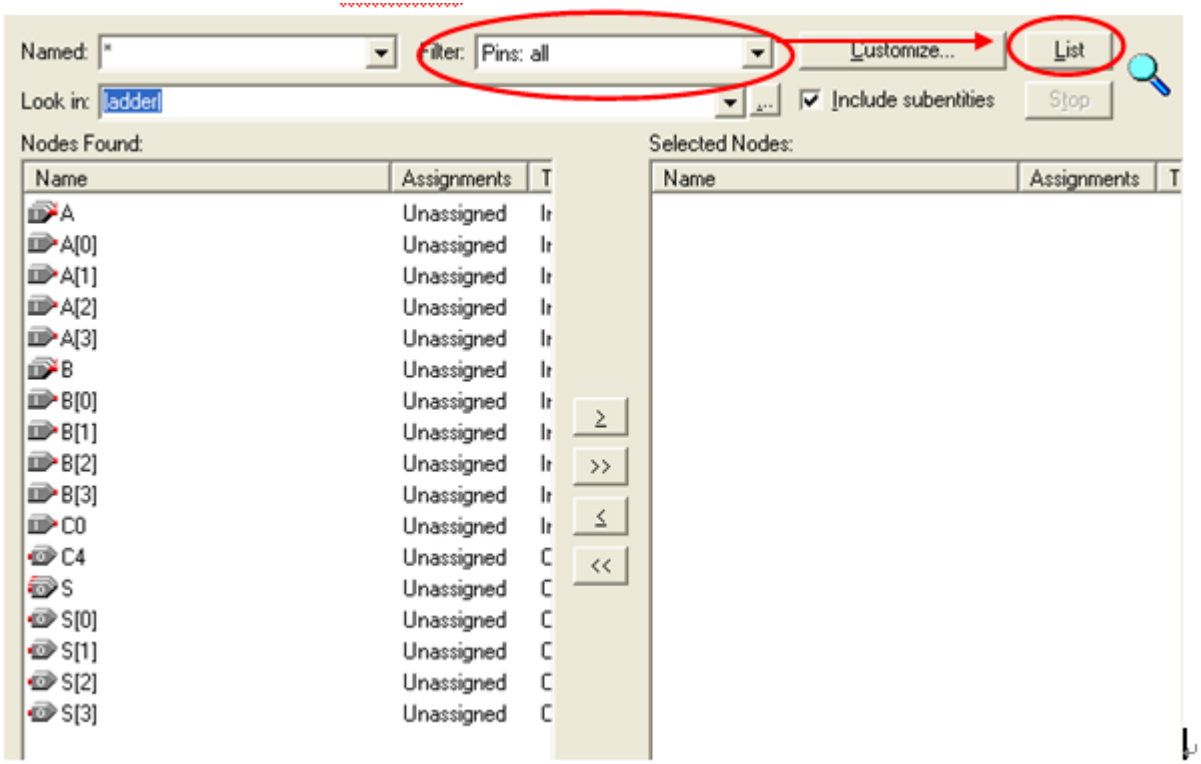
Quartus II - simulate

- 3.



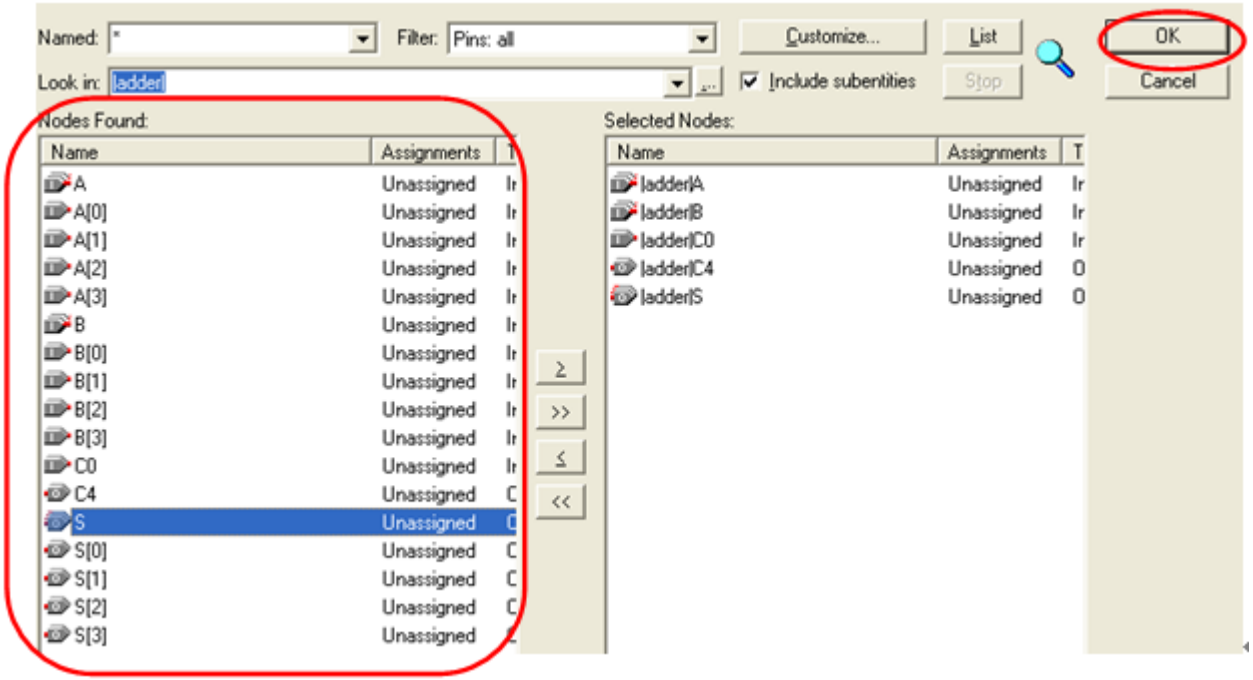
Quartus II - simulate

- 4.select the ports



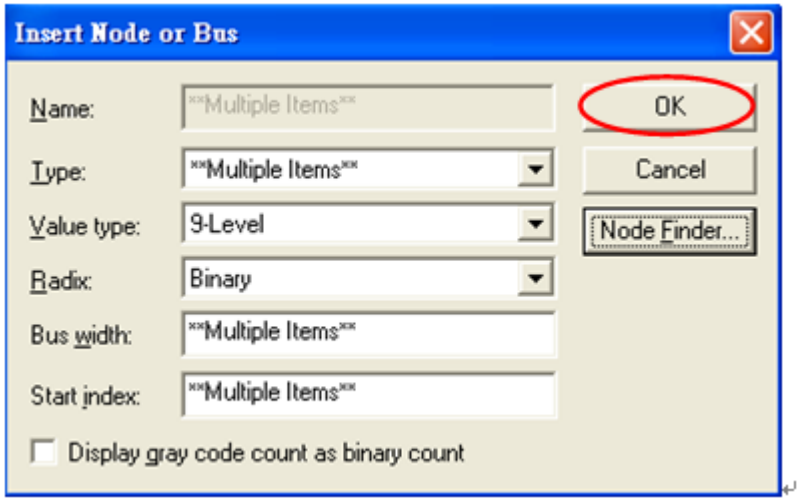
Quartus II - simulate

- 5.

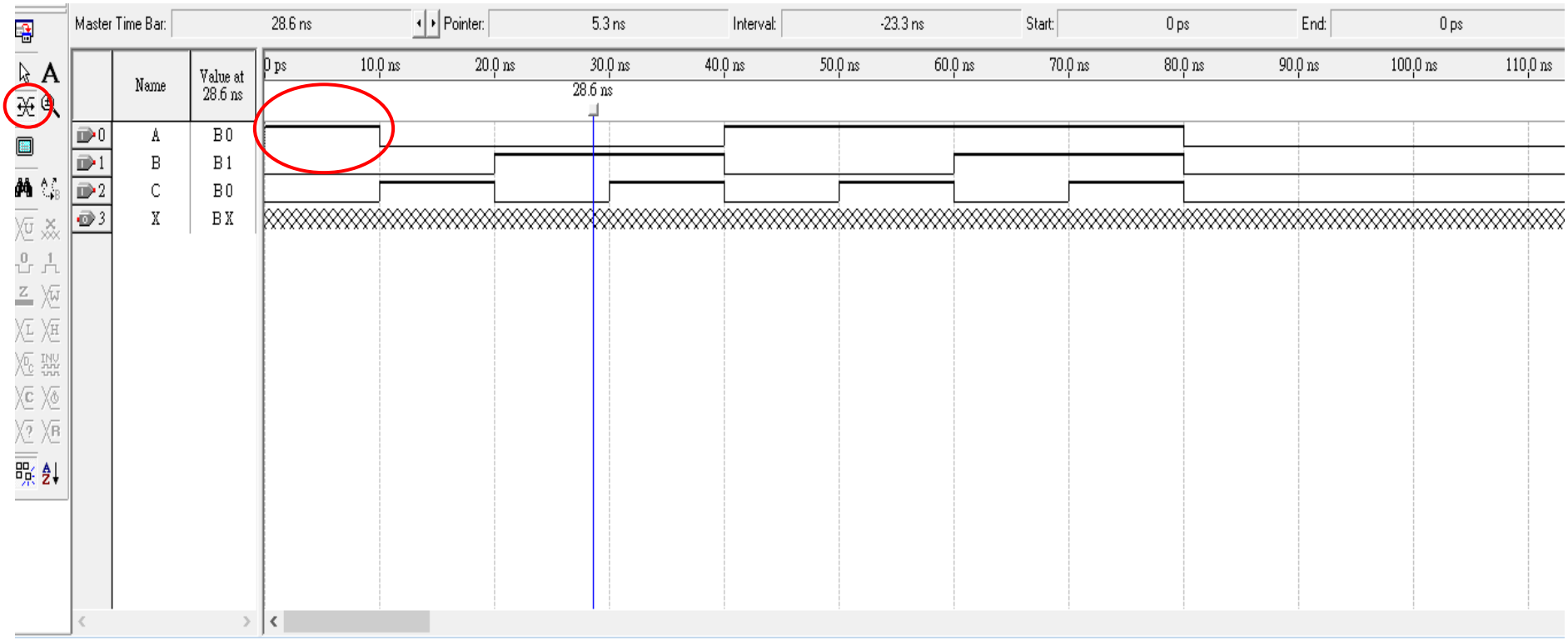


Quartus II - simulate

- 6.

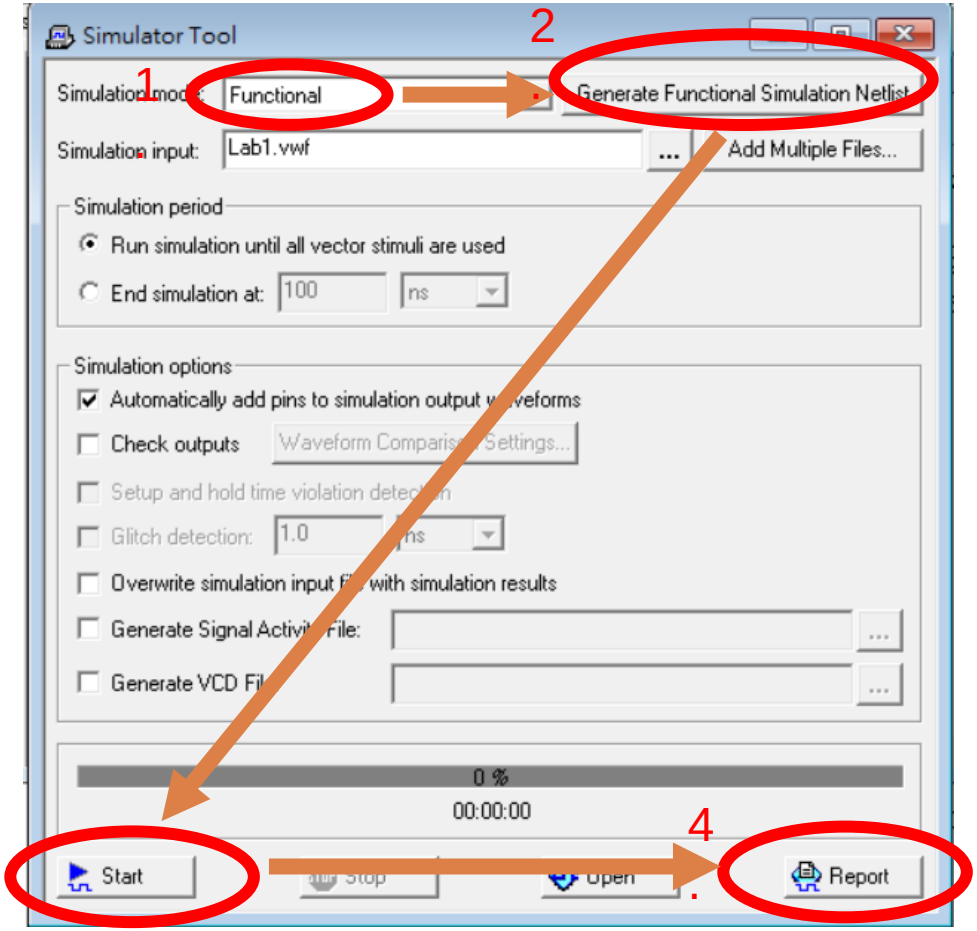


Quartus II - simulate



Quartus II - simulate

- 1.
  - 1. Choose FUNTIONAL
  - 2. Generate
  - 3. Start
  - 4. View Report



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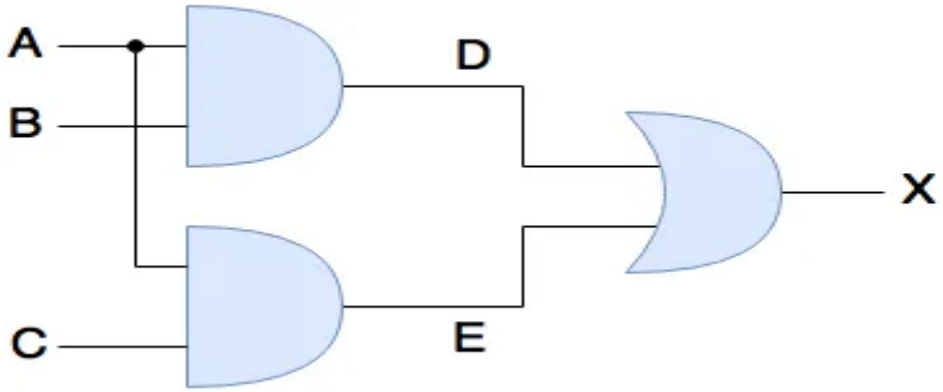
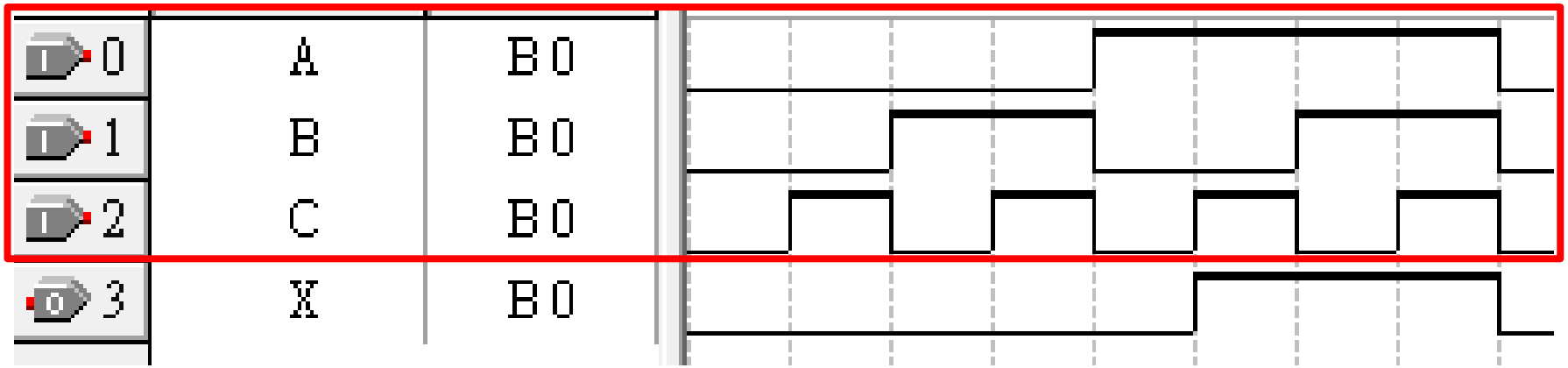
LAB 1

- 請使用Verilog HDL描寫出下圖之邏輯閘，並於QuartusⅡ 模擬訊號波型加以驗證結果。



LAB 1

- 課堂檢查



LAB1

下課前繳交至moodle：

上傳verilog.v

波形截圖