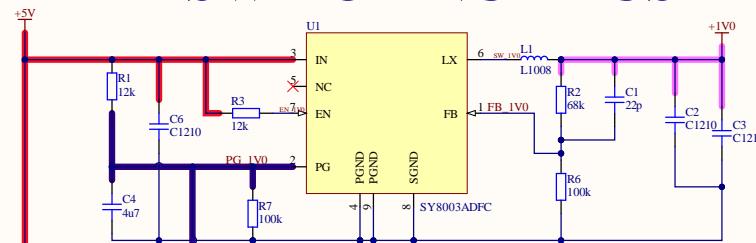
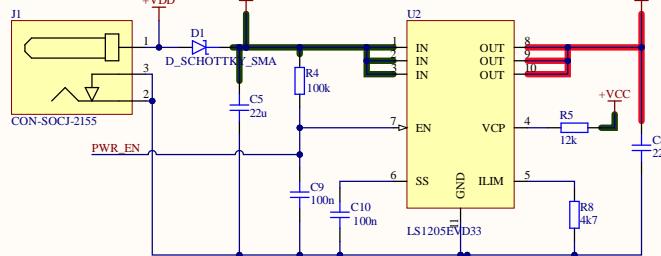
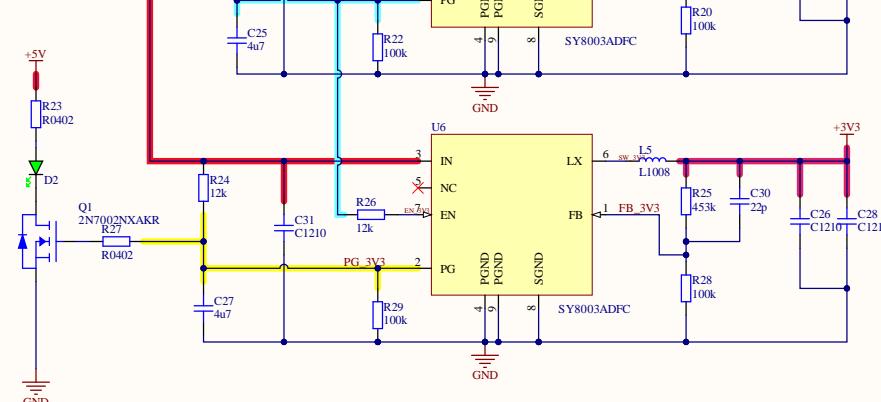
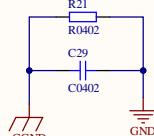
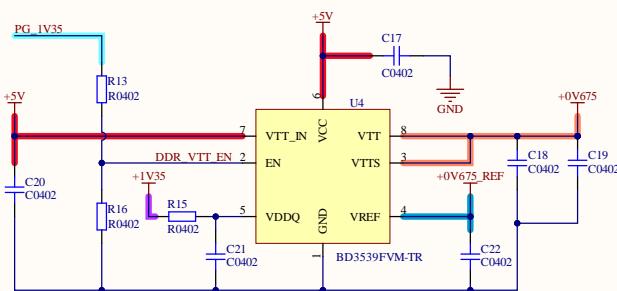


# [1] Power

## SWITCHING-REGS



## DDR3L-REG

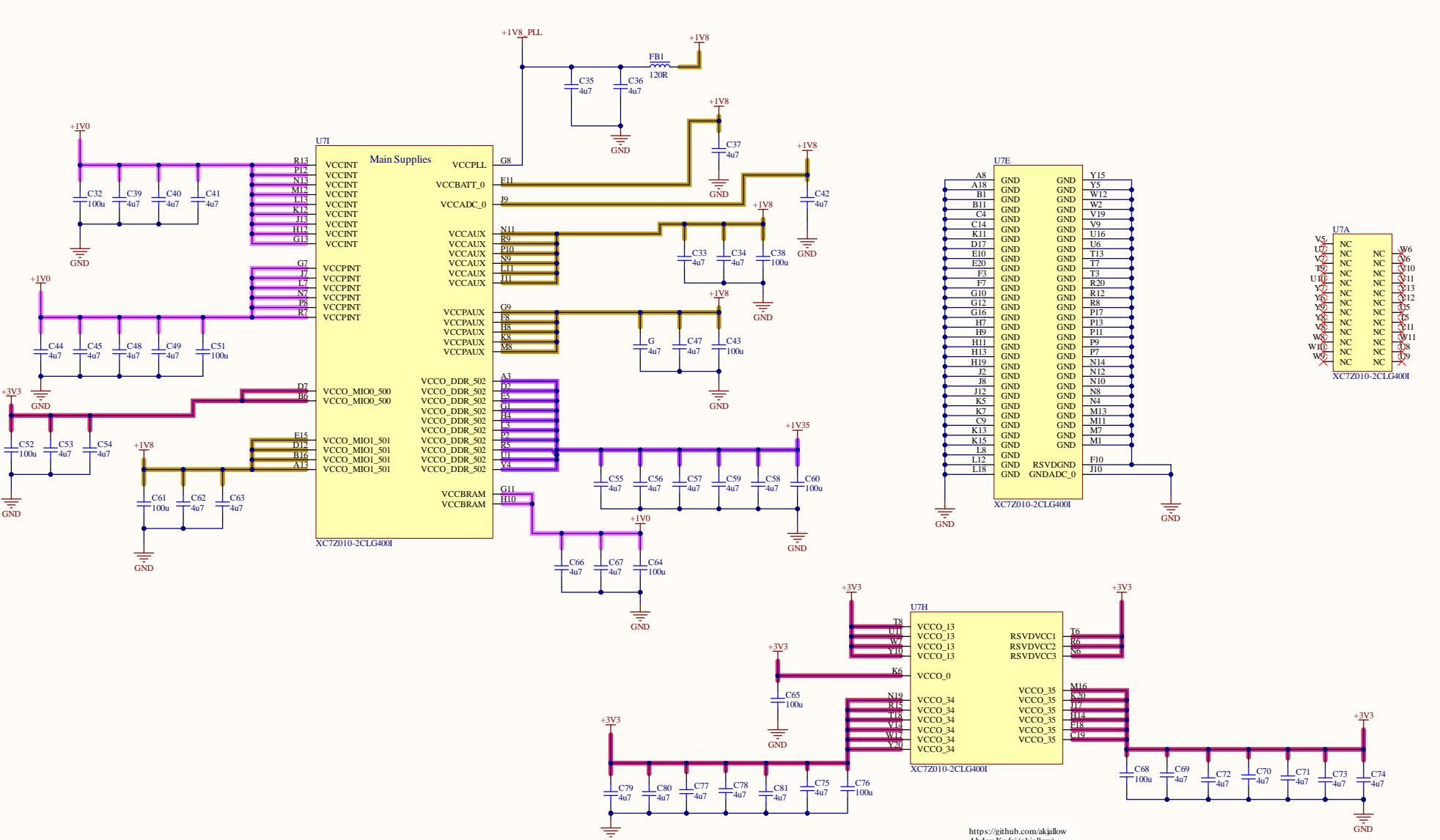


TITLE	Power Supplies		
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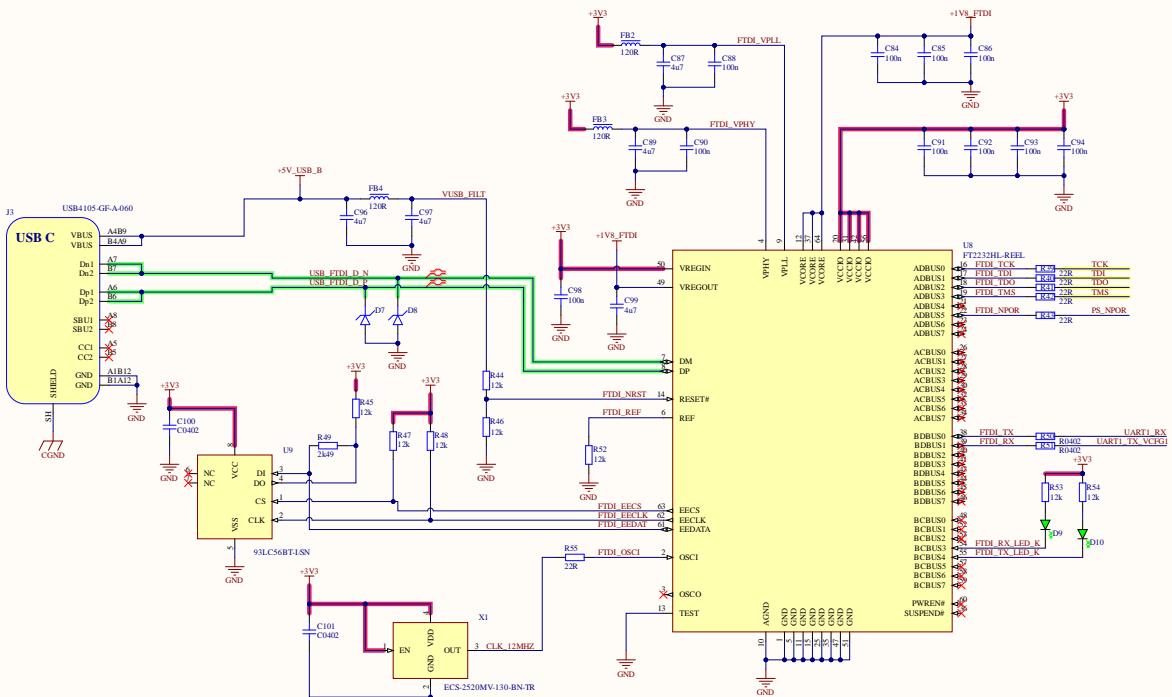
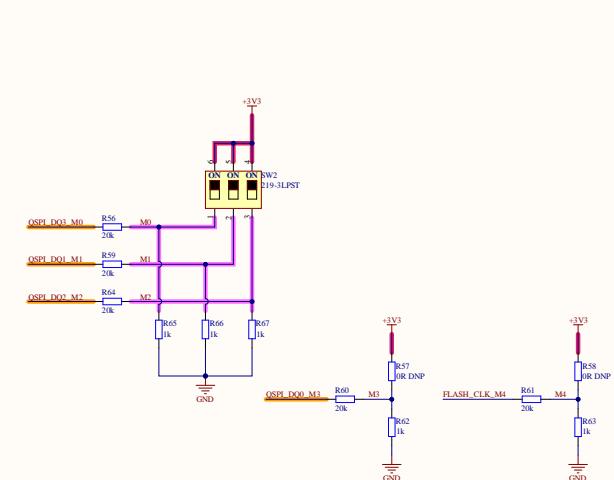
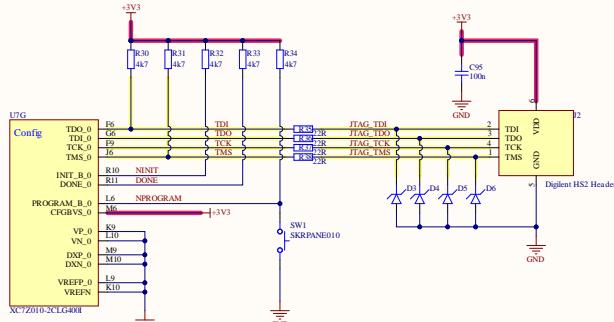
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## [2] Zynq Power and Decoupling

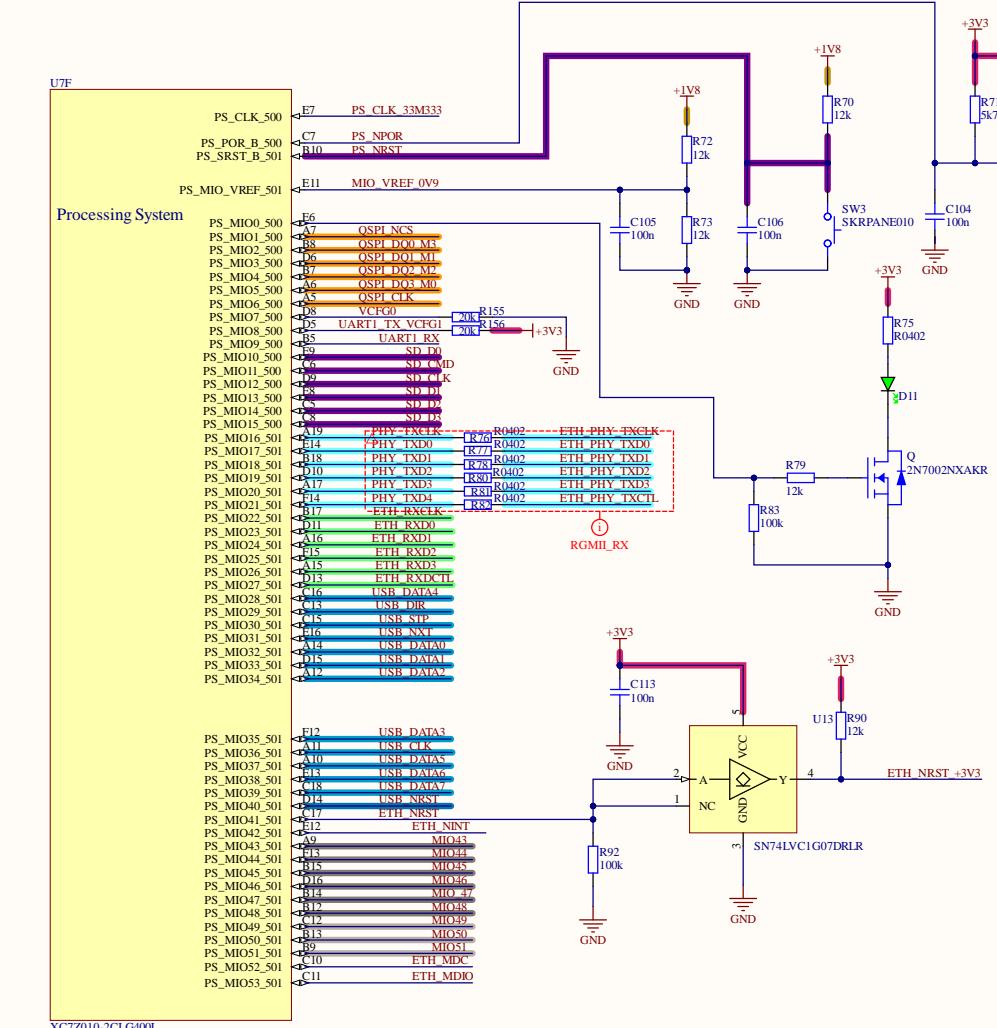


### [3] Zynq Config, JTAG, Debug

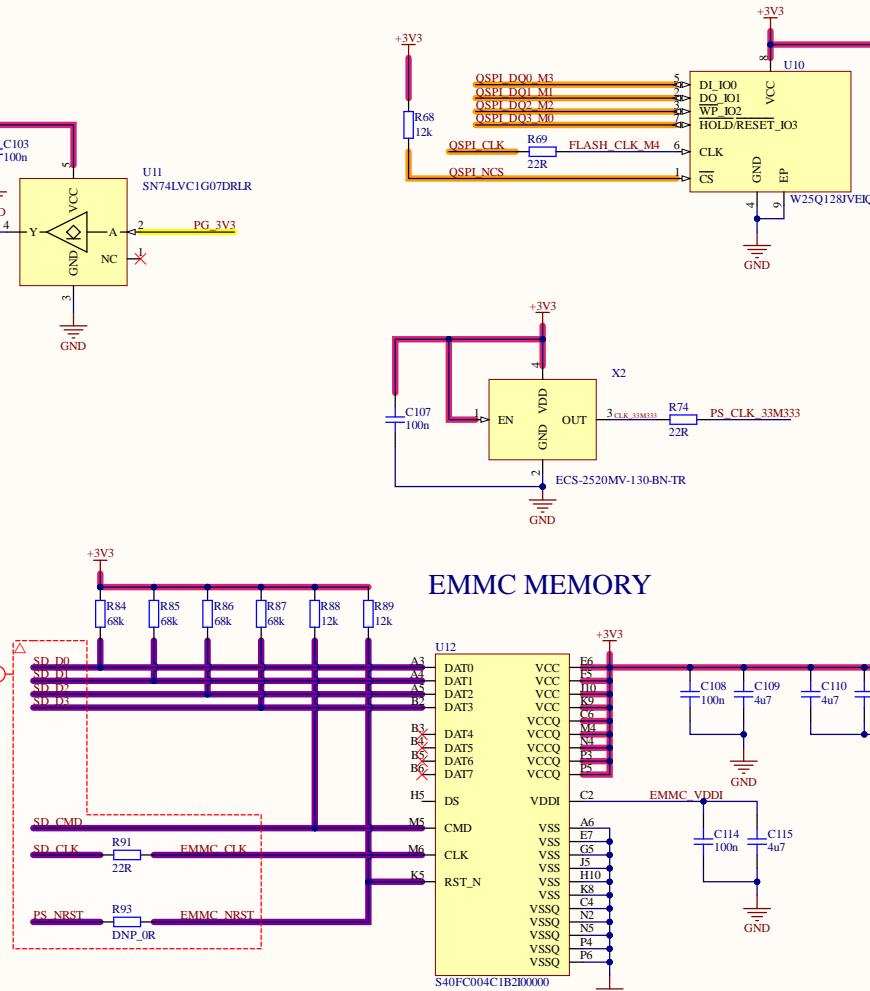
### FTDI JTAG Programmer and USB-to-UART



# [4] Zynq Processing System (PS)

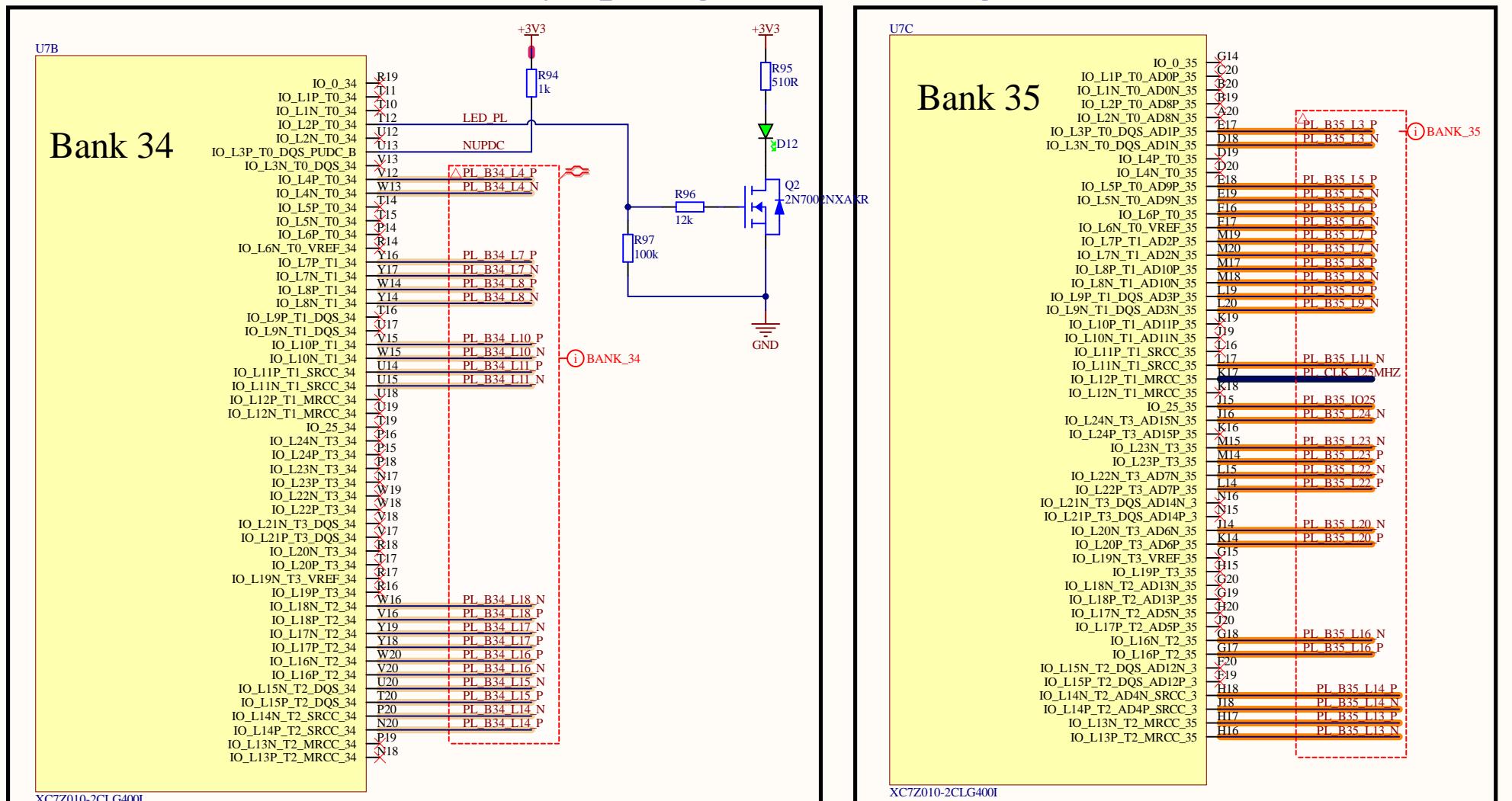


QSPI Flash Memory (128MBit)



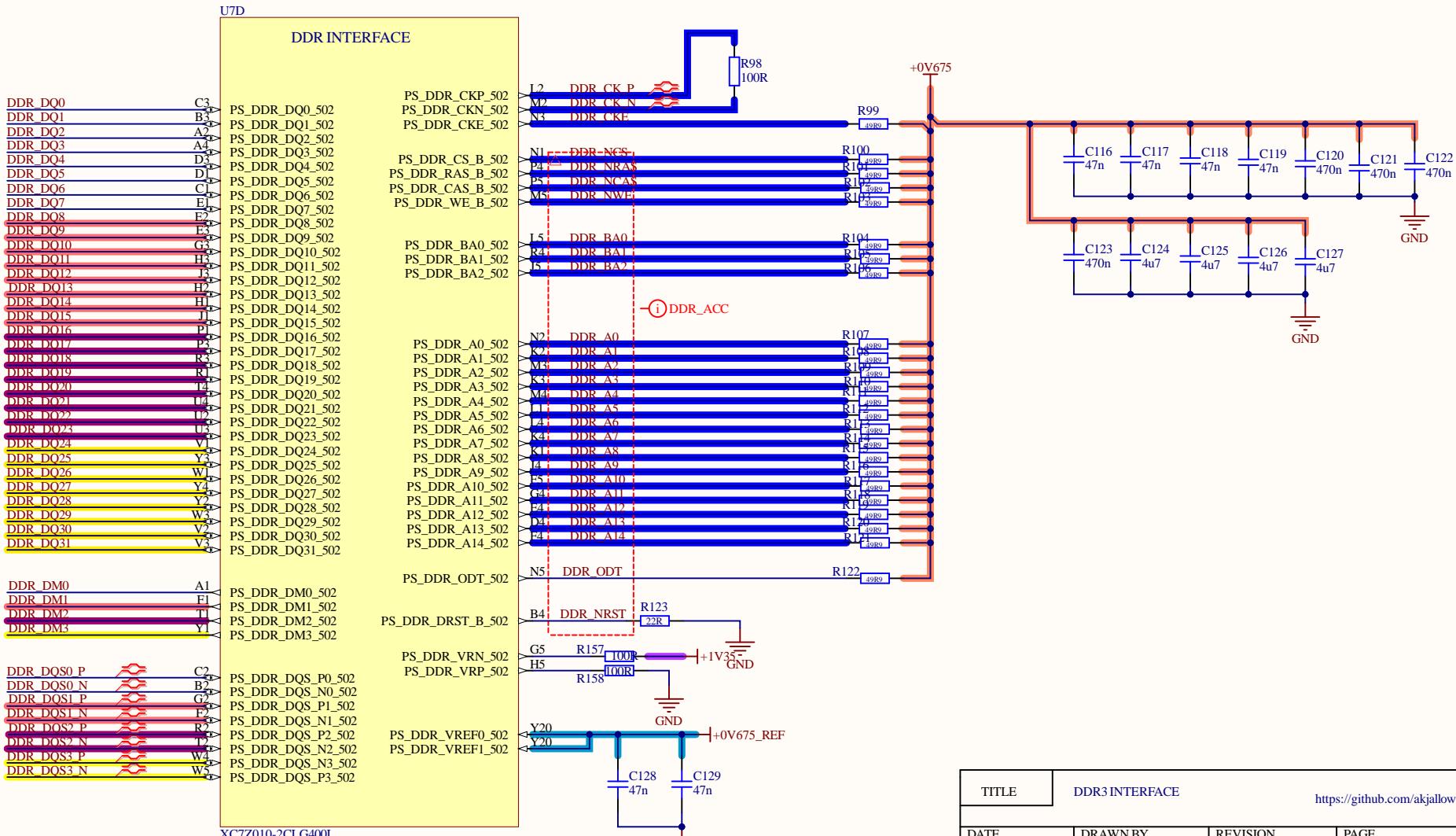
TITLE	ZYNQ PROCESSING SYSTEM	<a href="https://github.com/akjallow">https://github.com/akjallow</a>	
DATE	01/26	DRAWN BY Abdou Kadri(akjallow)	REVISION A

## [5] Zynq Programmable Logic (PL)

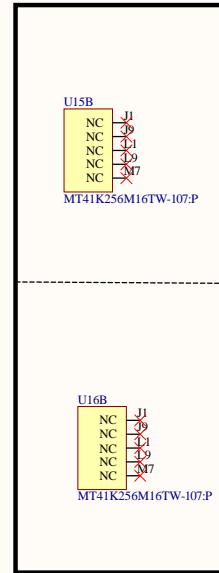
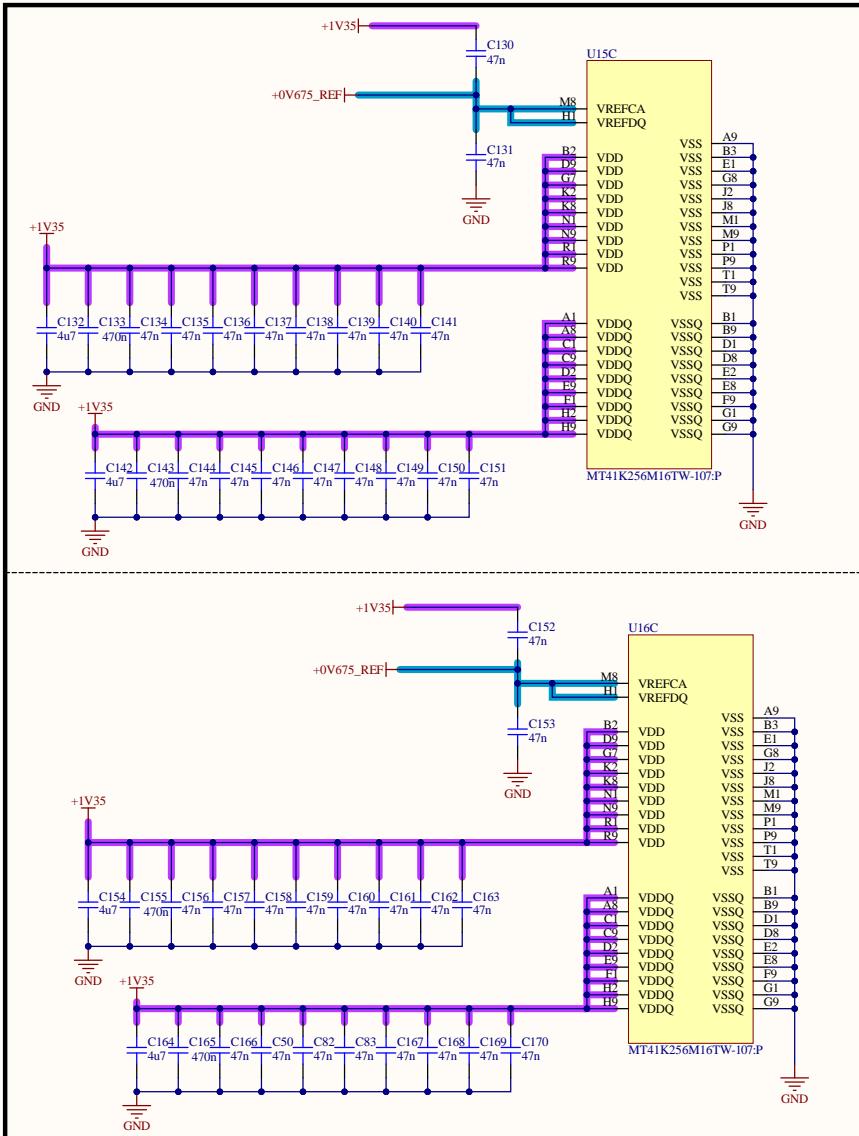
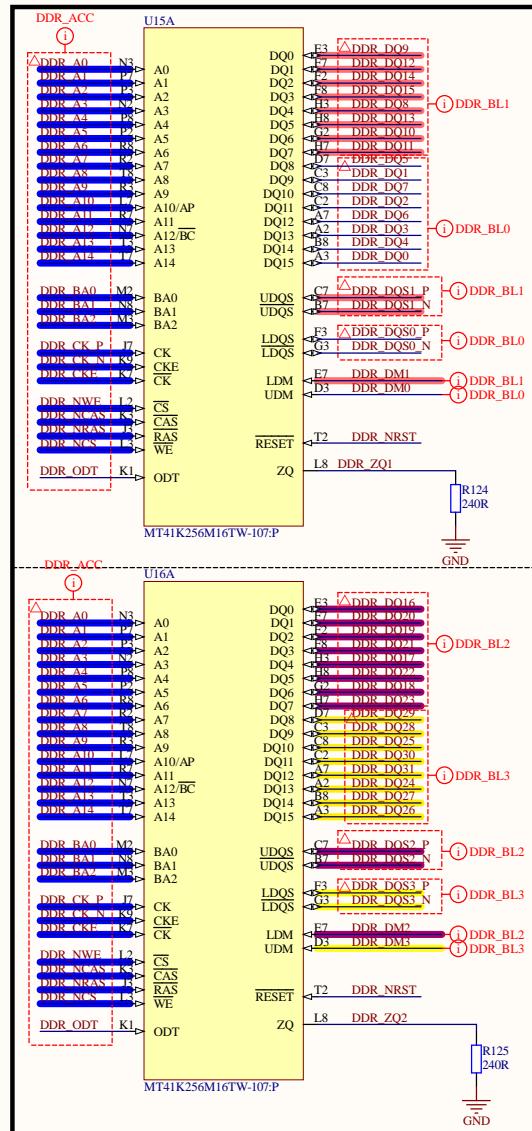


TITLE	ZYNQ PROGRAMMABLE LOGIC		
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# [6] Zynq DDR Interface & Termination

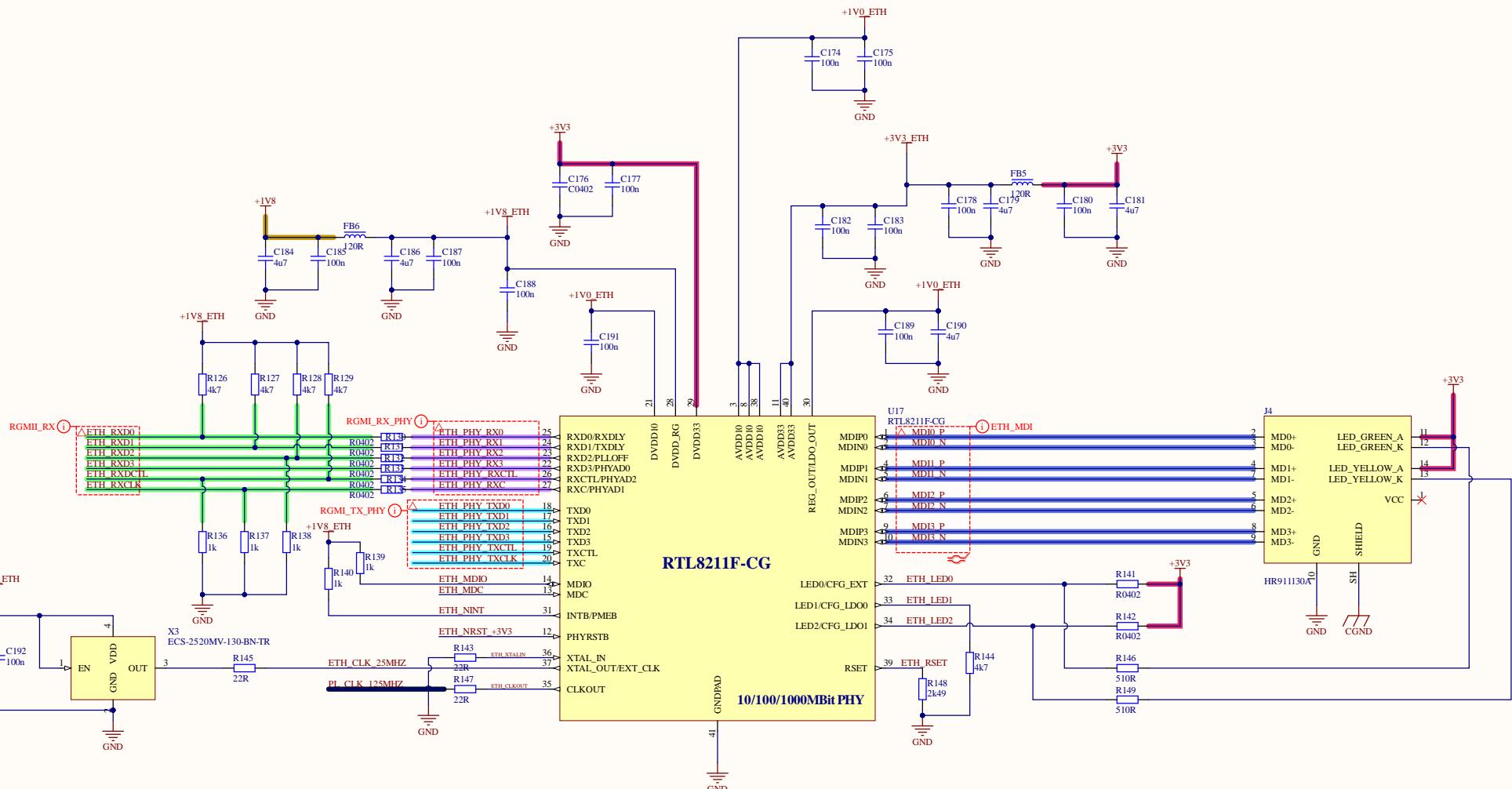


# [7] 1GB DDR3L Modules



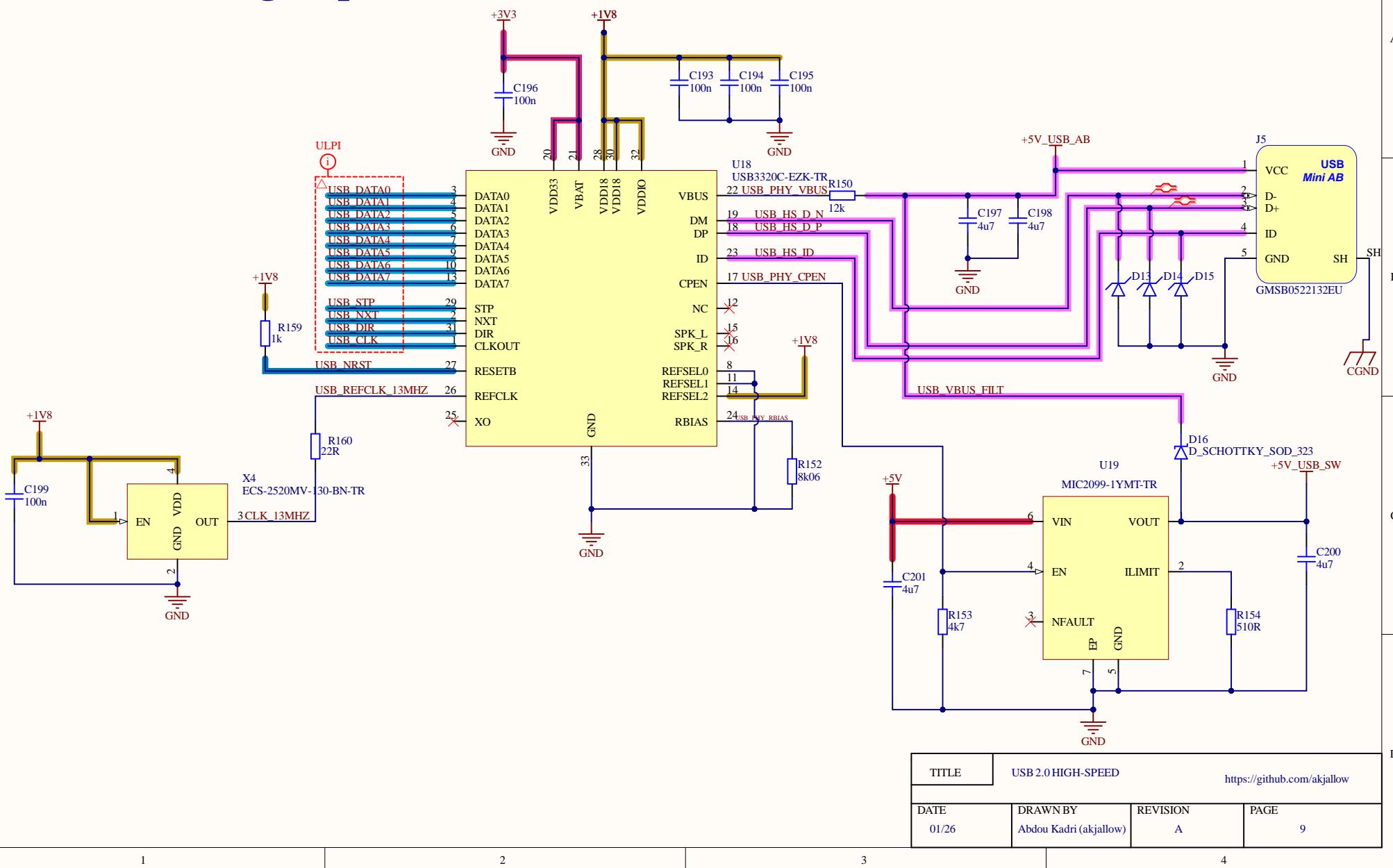
TITLE	DDR3L MODULES		
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# [8] Gigabit Ethernet



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## [9] USB 2.0 High-Speed (OTG)



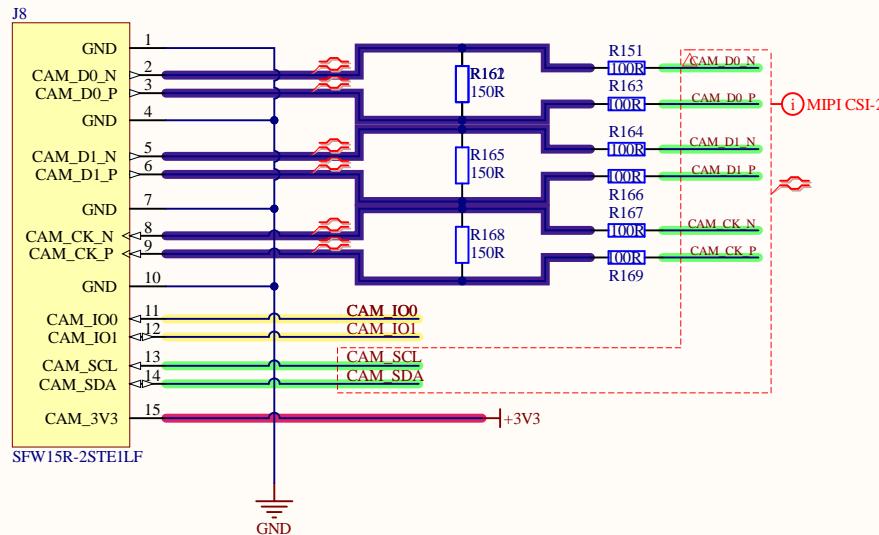
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# [10] CAMERA INTERFACE

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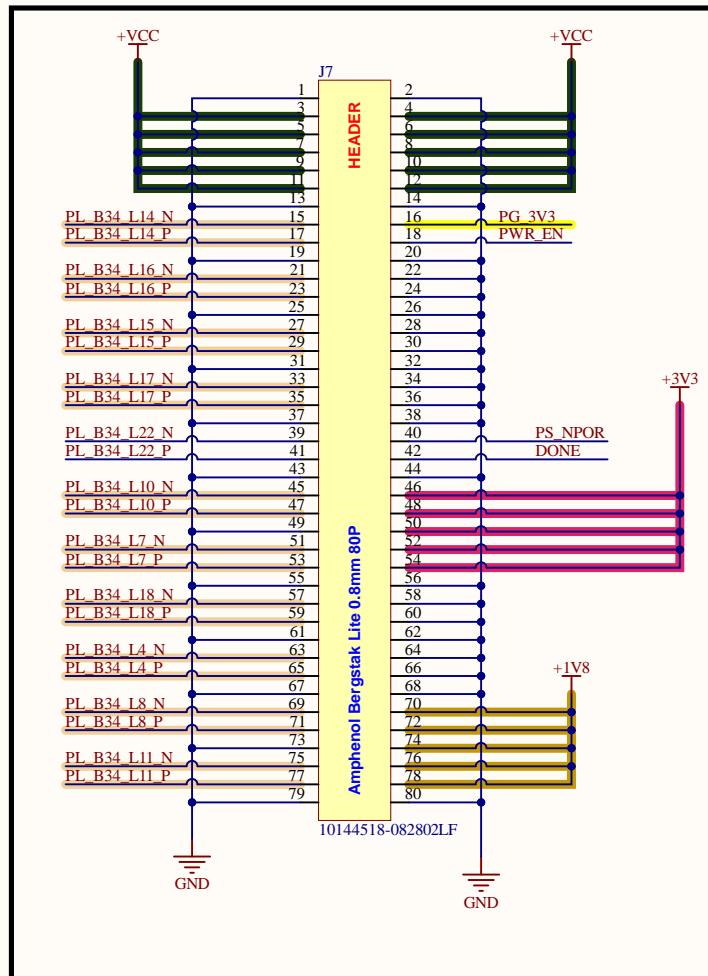
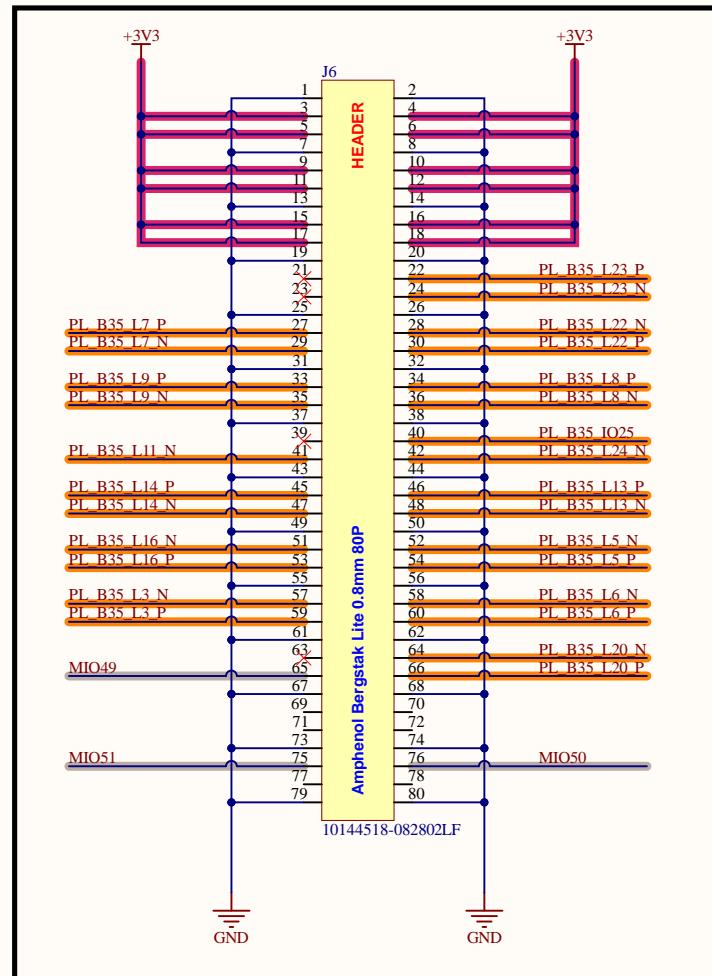
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# [10] Mezzanine Connectors

A



TITLE

MEZZANINE CONNECTORS

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