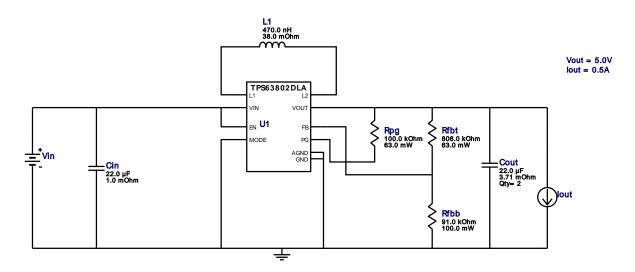


WEBENCH® Design Report

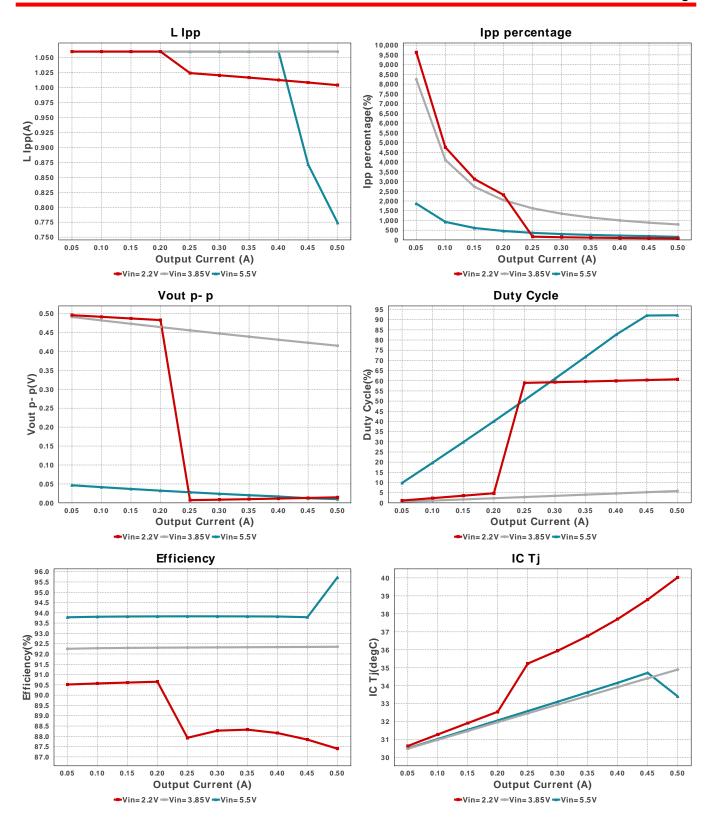
VinMin = 2.2V VinMax = 5.5V Vout = 5.0V lout = 0.5A Device = TPS63802DLAR
Topology = Buck_Boost
Created = 2021-01-05 01:02:19.036
BOM Cost = \$1.28
BOM Count = 8
Total Pd = 0.25W

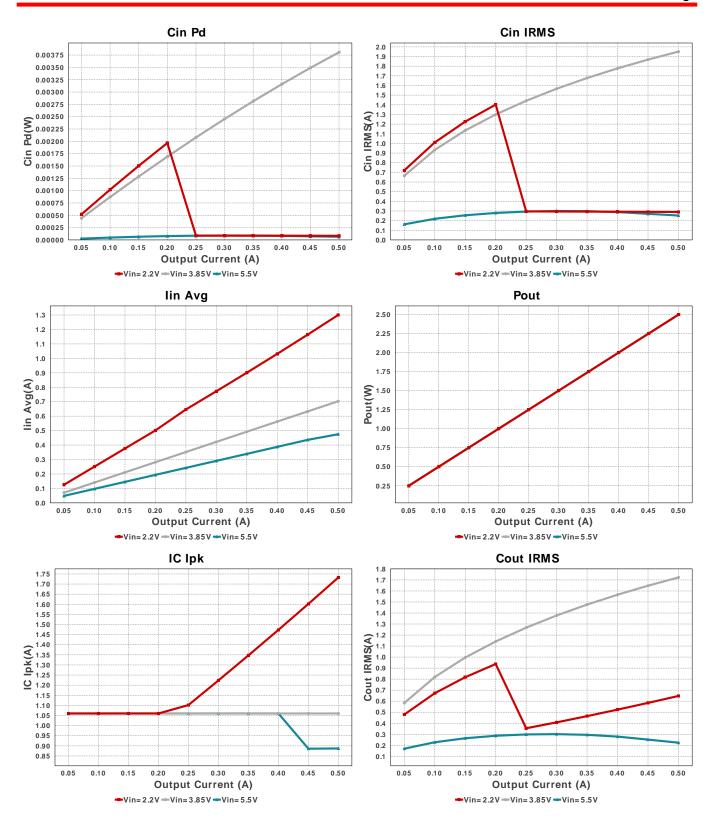
Design: 32 TPS63802DLAR TPS63802DLAR 2.2V-5.5V to 5.00V @ 0.5A

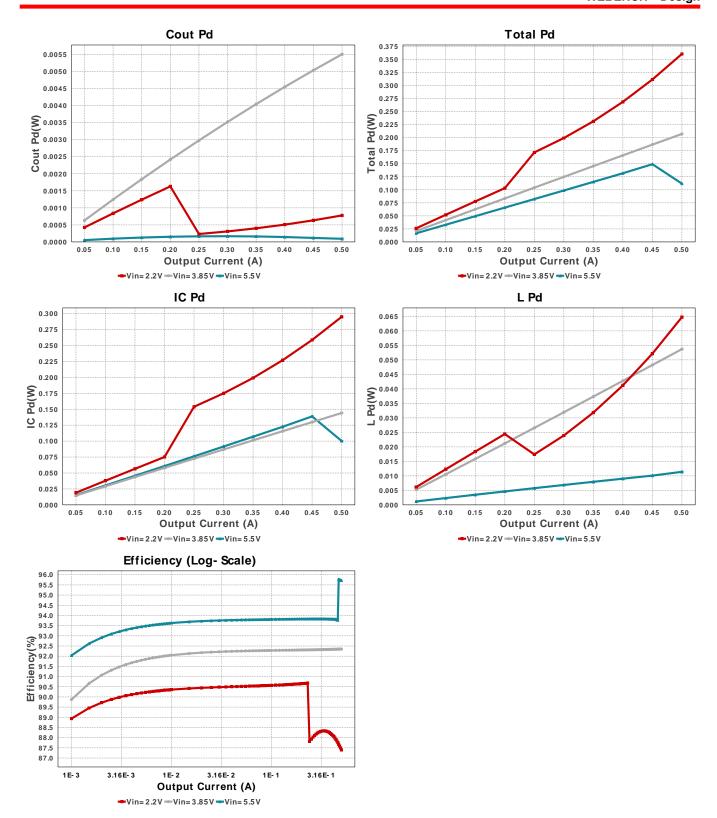


Electrical BOM

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cin	MuRata	GRM188R60J226MEA0D Series= X5R	Cap= 22.0 uF ESR= 1.0 mOhm VDC= 6.3 V IRMS= 6.0 A	1	\$0.05	0603 5 mm ²
Cout	TDK	C1608X5R1A226M080AC Series= X5R	Cap= 22.0 uF ESR= 3.71 mOhm VDC= 10.0 V IRMS= 2.69936 A	2	\$0.12	0603 5 mm ²
L1	TDK	NLCV32T-R47M-PFR	L= 470.0 nH 38.0 mOhm	1	\$0.10	NLCV32 13 mm ²
Rfbb	Yageo	RC0603FR-0791KL Series= ?	Res= 91.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm ²
Rfbt	Vishay-Dale	CRCW0402806KFKED Series= CRCWe3	Res= 806.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rpg	Vishay-Dale	CRCW0402100KFKED Series= CRCWe3	Res= 100.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
U1	Texas Instruments	TPS63802DLAR	Switcher	1	\$0.86	DLA0010A 12 mm ²







Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	2.078 A	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	4.32 mW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	1.416 A	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	3.72 mW	Capacitor	Output capacitor power dissipation
5.	IC lpk	1.06 A	IC	Peak switch current in IC
6.	IC Pd	182.76 mW	IC	IC power dissipation
7.	IC Tj	36.214 degC	IC	IC junction temperature
8.	IC Tolerance	5.0 mV	IC	IC Feedback Tolerance
9.	ICThetaJA	34.0 degC/W	IC	IC junction-to-ambient thermal resistance
10.	lin Avg	1.25 A	IC	Average input current

#	Name	Value	Category	Description
11.	Ipp percentage	842.155 %	Inductor	Inductor ripple current percentage (with respect to average inductor
				current)
12.	L Pd	59.822 mW	Inductor	Inductor power dissipation
13.	Cin Pd	4.32 mW	Power	Input capacitor power dissipation
14.	Cout Pd	3.72 mW	Power	Output capacitor power dissipation
15.	IC Pd	182.76 mW	Power	IC power dissipation
16.	L Pd	59.822 mW	Power	Inductor power dissipation
17.	Total Pd	250.64 mW	Power	Total Power Dissipation
18.	BOM Count	8	System Information	Total Design BOM count
19.	Duty Cycle	12.329 %	System Information	Duty cycle
20.	Efficiency	90.888 %	System	Steady state efficiency
20.	Lindency	JU.000 /0	Information	Gloddy State Childenby
21.	FootPrint	50.0 mm ²	System	Total Foot Print Area of BOM components
۷.	. 550 11110	50.0 11111	Information	Total 1 oot 1 mile 7 flow of Both components
22.	Frequency	110.102 kHz	System	Switching frequency
	Troquonoy	110.102 1012	Information	Simoning inequality
23.	lout	500.0 mA	System	lout operating point
			Information	31.
24.	L lpp	1.06 A	System	Peak-to-peak inductor ripple current
	• •		Information	
25.	Mode	PFM	System	Conduction Mode
			Information	
26.	Pout	2.5 W	System	Total output power
			Information	
27.	Total BOM	\$1.28	System	Total BOM Cost
			Information	
28.	Vin	2.2 V	System	Vin operating point
			Information	
29.	Vout	5.0 V	System	Operational Output Voltage
			Information	
30.	Vout Actual	4.929 V	System	Vout Actual calculated based on selected voltage divider resistors
			Information	
31.	Vout Tolerance	2.833 %	System	Vout Tolerance based on IC Tolerance (no load) and voltage divider
			Information	resistors if applicable
32.	Vout p-p	458.788 mV	System	Peak-to-peak output ripple voltage
			Information	

Design Inputs

Name	Value	Description	
lout	500.0 m	Maximum Output Current	
VinMax	5.5	Maximum input voltage	
VinMin	2.2	Minimum input voltage	
Vout	5.0	Output Voltage	
base_pn	TPS63802	Base Product Number	
source	DC	Input Source Type	
Та	30.0	Ambient temperature	

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 2.2V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum lout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

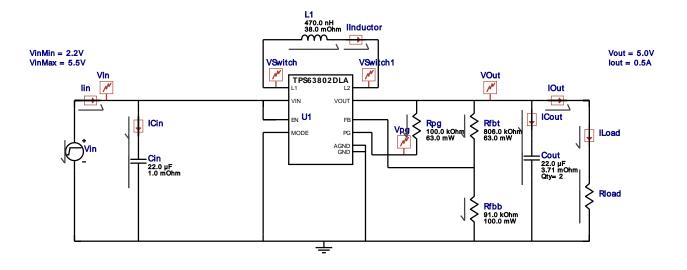


WEBENCH[®] Electrical Simulation Report

Design Id = 32

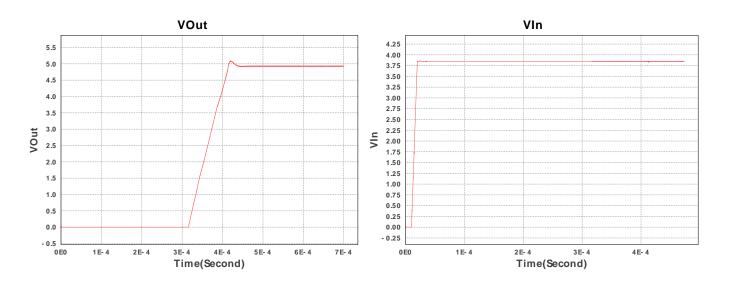
 $sim_id = 1$

Simulation Type = Startup



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Vzero1	Vmode	no description	0
2.	Vzero1	Ven	no description	0
3.	Rload	R	Load Resistance	10.0 Ohm



Design Assistance

- 1. Master key : B5D4E2491D752E31[v1]
- 2. **TPS63802** Product Folder: http://www.ti.com/product/TPS63802: contains the data sheet and other resources.

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