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1. Scope

Aim of this document is to describe suggestions and corrections that Telit advises to improve Ovoo Electronics B100AA application that integrates Telit GE910-QUAD V3 and BlueMod S50 modules.

2. Design review

Design review is based on the following received documentation:

- Schematic files: B151BA-R1.PDF, B100AA-R2.PDF
- Gerber file: none.
- Other: Telit Design Review R02 (Schematic).PDF

Summary Tables:

Schematic Review	P	F	I	MI	N/A
Power Supply			V		
SIM Pins	V				
Digital Pins		V			
Audio					V
RF			V	V	

PCB Layout Review	P	F	I	MI	N/A
General Placement					V
Antenna Waveguide					V
RF Aspects					V
Audio Aspects					V

P: Pass; F: Fail; I: Improvements possible; MI: Missing Information; N/A: Not Applicable

The following symbols will be used throughout the Design Review to indicate:

✓ OK: No design changes are required.

Tip: information or possible improvement, not mandatory but recommended.

⚠ Warning: if you don't follow the recommendation there's a risk of malfunctioning or issues during the homologation phase, strongly recommended.

Error: it's mandatory to follow the recommendation otherwise the module could be damaged or could not work properly or there's high probability of facing issues during the homologation phase.

? Missing Information: some relevant information is missing therefore the DR cannot be accurate on this item.

2.1. Schematic review

2.1.1. Power supply

⚠ Add 33pF capacitor to GND at modem's VAUX/PWRMON close to modem.

2.1.2. SIM pins

✓ Ok.

2.1.3. Digital pins

STOP For BlueMOd+S50 module, it is strongly recommended to use hardware flow control in both directions. Not using flow control can cause a loss of data.

⚠ BlueMod+S50 signals BOOT0 and TESTMODE# should be accessible to be set to high or low for invoking test modes required by the certification labs. Please use jumpers or resistor options here

ⓘ The optional MCU_HANGUP(GPIO4) connected to GPIO of the MCU feature is to close the link is provided.

ⓘ We recommend placing test points for BOOT0 pin, UART-RXD, UART-TXD, UART-RTS# and UART-CTS#. This will be useful for Regulatory approval purpose.

Test mode# Pin	BOOT0 Pin	Mode
LOW	LOW	Test mode (38400, 8N1)
LOW	HIGH	DTM (19200, 8N1)
HIGH	LOW	Firmware (115200, 8N1)
HIGH	HIGH	Bootloader

For more details on Test Mode, refer BlueMod+S50 HUG section 4.8.

ⓘ BlueMod+S50 SWDIO and SWCLK are reserved only for debugging purpose.
If you intend to use them for debugging purposes, make them available.

2.1.4. Audio pins

✓ N.A.

2.1.5. RF aspects

⚠ We suggest **making provision**, of 33pF filtering capacitors to GND also on power Sources and signals on input-output connectors (J2, J3,..).

? Looks the current design is using BlueMod+S50_AP variant. Antenna part number is missing in the schematics.

2.2. PCB Layout review

We don't have the PCB gerbers yet, but we will give you anyhow some useful general suggestions.

2.2.1. General placement

- As a general rule we suggest predisposing your PCB to optionally mount a metallic shield on top of noisy components (fast digital components, MCU, memories). This is a must in case of switching components, rectifiers and power amplifiers. For this purpose, components must be packet into well-defined areas surrounded with ground pads where you can eventually solder the shield. The shield options can be used, when needed, to suppress EMI fields that may interfere with the cellular reception/emission.

- Be aware that all PCBs placed close to GSM antenna must be RF proof and not only the PCB mounting the module; this means that all the PCB placed less than 30cm from the antenna must have shields over the noisiest components (switching, MCU, RAM, Ethernet PHY, etc..) and with the top and bottom layers mostly ground planes.

2.2.2. RF aspects

- The position of the external antenna with respect to other boards is of maximum importance, since conductive planes close to antenna modify the impedance sees by the antenna and any board of the system must be RF proof, not only the modem board.

- Move components, tracks, vias and connectors away from antenna area to reduce their coupling with RF signal; you can also bury tracks in the inner layers of a multi-layer PCB.

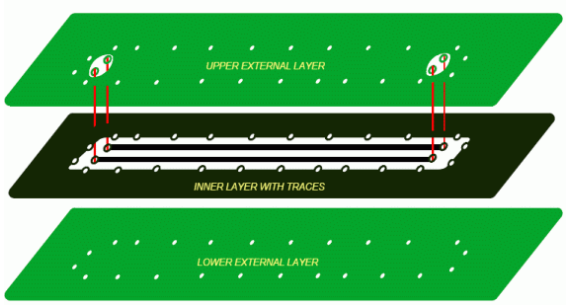
- We strongly suggest complying the following build-up and routing general rules for best RF performances (high RF receiver sensitivity, low spurious emissions) and also for best thermal behavior:

  - We advise using at least 4 layers PCB.
  - **Top and Bottom layers should be mainly a ground plane** interrupted just by component's pads, VIAs and RF antenna waveguide; just the minimum possible portion of tracks should be routed in these layers.
  - **Inner layers should be used for interconnections** and power planes; all empty spaces should be filled with GND.

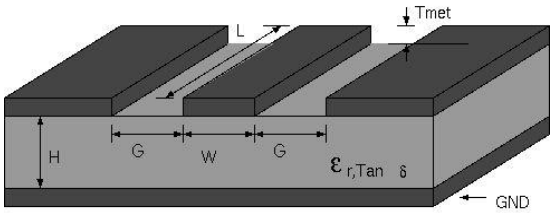
o All grounds, either planes or areas, in an all layers, must be well connected with each other, using large tracks and many conductive VIAs, in order to guarantee a strong equipotential node.
o PCB borders should be GND in all layers, wherever is possible. We suggest adding a series of conductive VIAs evenly distributed (e.g. every 2mm) all along the board edges, inside the border GND area.
o Noisy components should be shielded into a metallic shield if required.

- The Bypass capacitors must be placed close to the Telit modem's power input pads or at least on the same path. In case of switching power supply another Bypass low ESR capacitor must be placed close to the inductor output to cut the ripple.

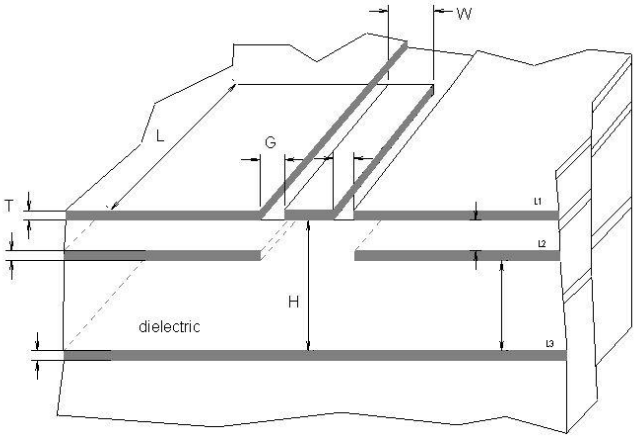
- It is not advisable to route analog or digital audio lines, memory address and data bus, fast digital signals, clocks, quartz, serial, USB and long signal tracks on an outer layer. It'll be better to bury it on an inner layer with a ground plane under and above it to shield the signal from RF and crosstalk, see figure below. USB data lines should be Differential Offset Coplanar Waveguide with 90 Ohms characteristic impedance.



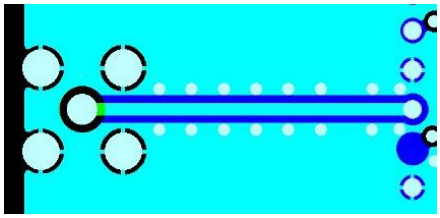
- The RF antenna track, and eventually any via connected to it, must be a homogeneous waveguide with 50 Ohm characteristic impedance; we suggest using the coplanar waveguide with ground model where the RF track has a **uniform ground** plane **underneath** and **surrounding** it as in figure below. Do not place signal lines and signal-VIAs crossing or close to RF lines in no one of waveguide's layers involved.



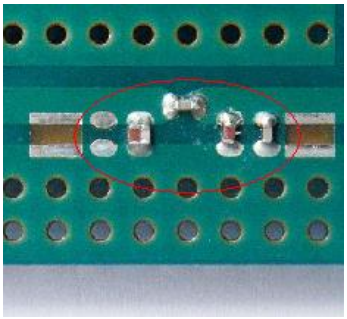
- When dielectric between 2 consecutive layers has not the desired height then for right impedance realization, you should remove the copper under RF line or pad, in one or more layers, to wider dielectric between antenna track and its reference ground plane, as example in figure below. The clearance in the internal layers must be wider than the W+2G. This is to avoid electric filed to close in internal layers instead of in the desired reference ground layer.



- We suggest shielding the waveguide by adding a series of conductive VIAs evenly distributed (e.g. every 2mm) all along the edges of the GND plane facing the coplanar waveguide (about 1mm from the edge), both sides. (see figure below). This improve line grounding and reduce signal coupling inside the PCB from adjacent tracks.



- If applicable, route RF matching network using as short as possible tracks and avoiding stubs, sharp bends and meanders.
  Figure below represents a layout example of the RF line matching network circuitry.



2.3. General comments

Please check and follow Telit Modem Integration Design Guide.
Review is related to received application information and the supposed use of it.

3. Quality record

This design review is registered internally in Bugzilla with ID #33285.
The customer request is registered internally in Salesforce with ID # 00201737.