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Contents

1. Scope

Aim of this document is to describe suggestions and corrections that Telit advises to improve Ovoo Electronics B100AA application that integrates Telit GE910-QUAD V3 and BlueMod S50 modules.

2. Design review

Design review is based on the following received documentation:

- Schematic files: B151BA-R2.PDF, B100AA-R4.PDF
- Gerber file: Gerber Files.
- Other: Telit Design Review R04 (Schematic).PDF

Summary Tables:

Schematic Review	P	F	I	MI	N/A
Power Supply	V				
SIM Pins	V				
Digital Pins	V				
Audio					V
RF				V	

PCB Layout Review	P	F	I	MI	N/A
General Placement		V			
Antenna Waveguide		V			
RF Aspects		V			
Audio Aspects					

P: Pass; F: Fail; I: Improvements possible; MI: Missing Information; N/A: Not Applicable

The following symbols will be used throughout the Design Review to indicate:

✓ OK: No design changes are required.

Tip: information or possible improvement, not mandatory but recommended.

⚠ Warning: if you don't follow the recommendation there's a risk of malfunctioning or issues during the homologation phase, strongly recommended.

Error: it's mandatory to follow the recommendation otherwise the module could be damaged or could not work properly or there's high probability of facing issues during the homologation phase.

? Missing Information: some relevant information is missing therefore the DR cannot be accurate on this item.

2.1. Schematic review

2.1.1. Power supply

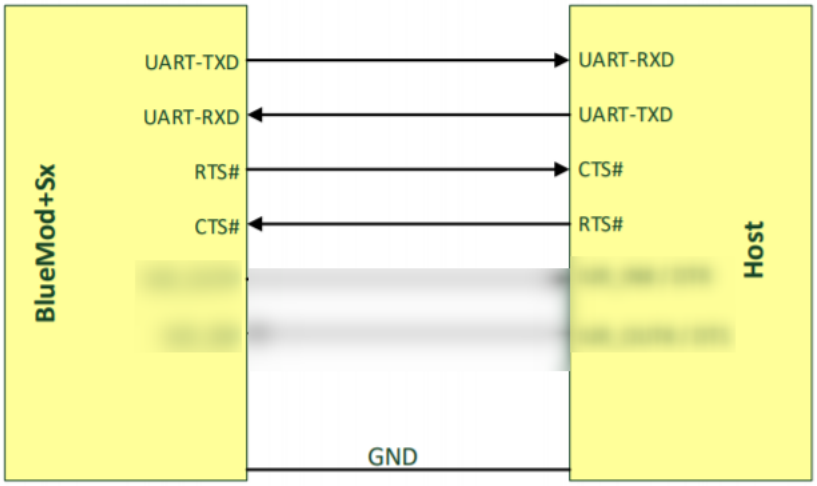
- Ok.

2.1.2. SIM pins

- Ok.

2.1.3. Digital pins

- Kindly make sure the BlueMod+S50 UART lines are connected to HOST MCU as shown below,



- We recommend placing test points for BOOT0 pin, UART-RXD, UART-TXD, UART-RTS# and UART-CTS#. This will be useful for Regulatory approval purpose.

Test mode# Pin	BOOT0 Pin	Mode
LOW	LOW	Test mode (38400, 8N1)
LOW	HIGH	DTM (19200, 8N1)
HIGH	LOW	Firmware (115200, 8N1)
HIGH	HIGH	Bootloader

For more details on Test Mode, refer BlueMod+S50 HUG section 4.8.

2.1.4. Audio pins

- ✓ N.A.

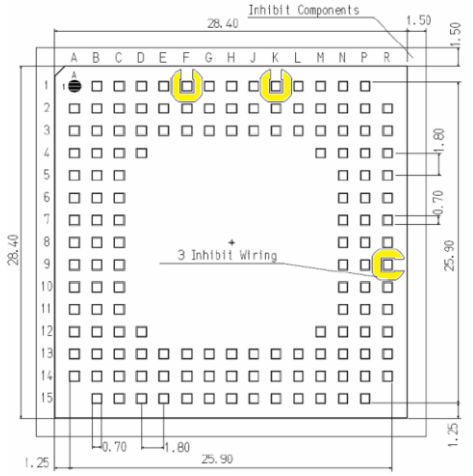
2.1.5. RF aspects

? Looks the current design is using BlueMod+S50_AP variant. Antenna part number is missing in the schematics.

2.2. PCB Layout review

2.2.1. General placement

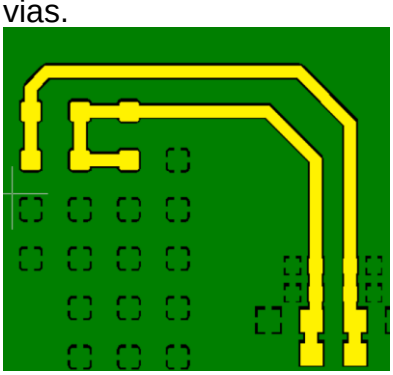
STOP Respect all the wiring inhibits regions, as shown in figure below. Remove copper, tracks and VIAs from there.



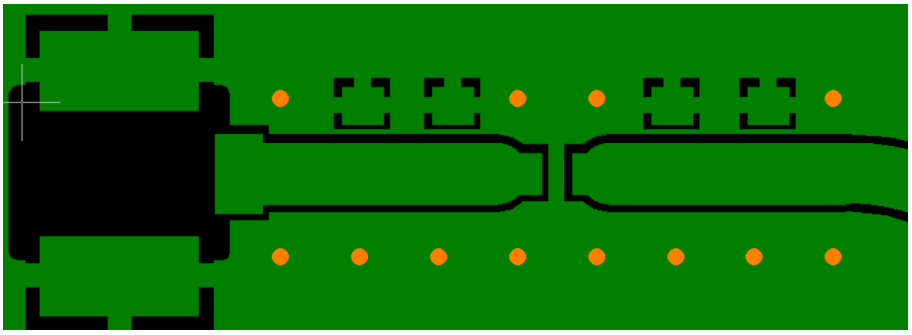
2.2.2. RF aspects

STOP Your design is not RF proof; the PCB has many tracks exposed creating loops that pick-up RF energy; they can generate high frequency intermodulation harmonics that irradiate very efficiently producing unwanted spurious emissions and furthermore it is lacking in RF decoupling.
Reroute the PCB design to have minimum lines running on external layers, burying the tracks in the inner layers and having all external layers and borders like ground

STOP Power tracks should not run on external layers. We strongly suggest burying power tracks in the inner layers and routing them directly to the component pads by using vias.



- Your RF line is a waveguide with characteristic impedance of about 50 Ohms, but it has not a uniform layout. We remind you that all waveguide parameters (**Width, Gap** and Height) must remain constant all track long, including the matching network pads otherwise this can lead to characteristic impedance discontinuities**.**
  In your waveguides, width and Gap change in several points along the track introducing discontinuities to the characteristic impedance.
  In order to avoid discontinuities, we suggest routing your waveguide as depicted below:



2.3. General comments

Please check and follow Telit Modem Integration Design Guide.
Review is related to received application information and the supposed use of it.

3. Quality record

This design review is registered internally in Bugzilla with ID #33285.
The customer request is registered internally in Salesforce with ID # 00201737.