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Contents

1. Scope

Aim of this document is to describe suggestions and corrections that Telit advises to improve Ovoo Electronics B100AA application that integrates a Telit GE910-QUAD V3 module.

2. Design review

Design review is based on the following received documentation:

- Schematic files: B100AA-R1.PDF
- Gerber file: none.
- Other: Telit Design Review R01 (Schematic).PDF

Summary Tables:

Schematic Review	P	F	I	MI	N/A
Power Supply				V	
SIM Pins			V		
Digital Pins		V			
Audio					V
RF			V		

PCB Layout Review	P	F	I	MI	N/A
General Placement					V
Antenna Waveguide					V
RF Aspects					V
Audio Aspects					V

P: Pass; F: Fail; I: Improvements possible; MI: Missing Information; N/A: Not Applicable

The following symbols will be used throughout the Design Review to indicate:

✓ OK: No design changes are required.

Tip: information or possible improvement, not mandatory but recommended.

⚠ Warning: if you don't follow the recommendation there's a risk of malfunctioning or issues during the homologation phase, strongly recommended.

STOP Error: it's mandatory to follow the recommendation otherwise the module could be damaged or could not work properly or there's high probability of facing issues during the homologation phase.

? Missing Information: some relevant information is missing therefore the DR cannot be accurate on this item.

2.1. Schematic review

2.1.1. Power supply

? Missing information on the 1V8 supply used for powering level shifter sides connected to the Telit modem.

2.1.2. SIM pins

⚠ C34 capacitor on SIMVCC shall be sized up to 1uF or 100nF.

2.1.3. Digital pins

STOP **In order to avoid back powering, it is strongly recommended to avoid having any HIGH logic level signal applied to the digital pins of the GE910 QUAD when the module is powered off or during an ON/OFF transition**. The +1V8 power circuitry is not necessary. **Use VAUX instead**.
If the external circuitry is used anyway, select one provided of enable pin, then use modem's VAUX to control its EN.
VAUX output pad is a 1V8@100mA power output specific for external use. **In this power configurations, level shifter protect modem against latch-up, since they follow modem power status**. When more than 60mA current is absorbed from VAUX, its heating generation contribution to the overall modem heating becomes not neglected.

STOP The use of open collector buffers or bidirectional voltage level translators with unidirectional signals is in principle correct but they are less immune to RF and dependent on Pull-Up/Down that could be present at any side of the voltage translator; some have different power range for both Vcca and Vccb, in some cases you must guarantee Vcca < Vccb, and their OE should be powered only from Vcca signal. We prefer unidirectional level shifters; if you anyway decide for bidirectional buffers, then those designed for PU/PD like **TXS, NXS, FXLA** and **NVT200x** are preferable, they work better if strong PU/PD are internally present like in some of our modems. **We strongly suggest using a dual supply buffer component for unidirectional signals like UART. Example of this are SN74AVC2T245, SN74AVC4T774 or SN74LVC2T45, for 5V signals. They are more immune to RF and are independent on Pull-Up or Pull-Down that could be present at any side of the voltage translator. Place 33pF on both power supplies.**
The Power bank side connected to the modem should be directly powered by modem's VAUX/PWRMON to prevent latch-up from happening.

2.1.4. Audio pins

✓ N.A.

2.1.5. RF aspects

⚠ We suggest **making provision**, of 33pF filtering capacitors to GND also on power Sources and signals on input-output connectors (J2, J3,..).

2.2. PCB Layout review

2.2.1. General placement

🛈 As a general rule we suggest predisposing your PCB to optionally mount a metallic shield on top of noisy components (fast digital components, MCU, memories). This is a must in case of switching components, rectifiers and power amplifiers. For this purpose, components must be packet into well-defined areas surrounded with ground pads where you can eventually solder the shield. The shield options can be used, when needed, to suppress EMI fields that may interfere with the cellular reception/emission.

🛈 Be aware that all PCBs placed close to GSM antenna must be RF proof and not only the PCB mounting the module; this means that all the PCB placed less than 30cm from the antenna must have shields over the noisiest components (switching, MCU, RAM, Ethernet PHY, etc..) and with the top and bottom layers mostly ground planes.

2.2.2. RF aspects

🛈 The position of the external antenna with respect to other boards is of maximum importance, since conductive planes close to antenna modify the impedance sees by the antenna and any board of the system must be RF proof, not only the modem board.

🛈 Move components, tracks, vias and connectors away from antenna area to reduce their coupling with RF signal; you can also bury tracks in the inner layers of a multi-layer PCB.

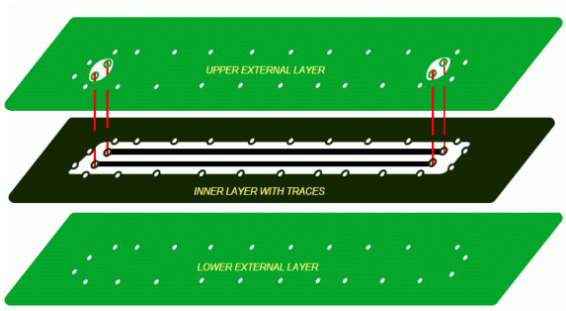
🛈 We strongly suggest complying the following build-up and routing general rules for best RF performances (high RF receiver sensitivity, low spurious emissions) and also for best thermal behavior:

- o We advise using at least 4 layers PCB.
- o **Top and Bottom layers should be mainly a ground plane** interrupted just by component's pads, VIAs and RF antenna waveguide; just the minimum possible portion of tracks should be routed in these layers.
- o **Inner layers should be used for interconnections** and power planes; all empty spaces should be filled with GND.
- o All grounds, either planes or areas, in an all layers, must be well connected with each other, using large tracks and many conductive VIAs, in order to guarantee a strong equipotential node.

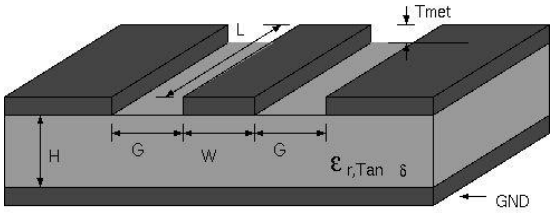
o PCB borders should be GND in all layers, wherever is possible. We suggest adding a series of conductive VIAs evenly distributed (e.g. every 2mm) all along the board edges, inside the border GND area.
o Noisy components should be shielded into a metallic shield if required.

- The Bypass capacitors must be placed close to the Telit modem's power input pads or at least on the same path. In case of switching power supply another Bypass low ESR capacitor must be placed close to the inductor output to cut the ripple.

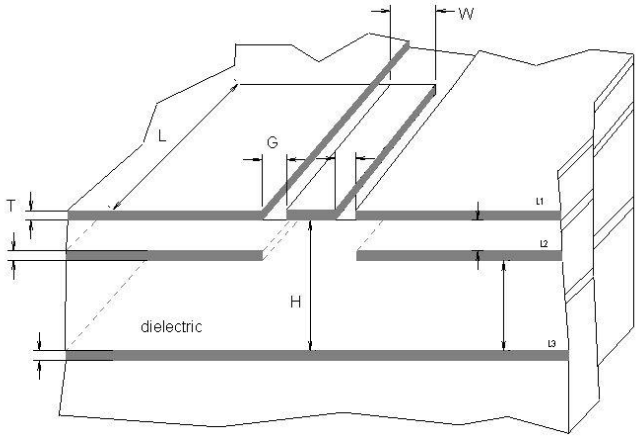
- It is not advisable to route analog or digital audio lines, memory address and data bus, fast digital signals, clocks, quartz, serial, USB and long signal tracks on an outer layer. It'll be better to bury it on an inner layer with a ground plane under and above it to shield the signal from RF and crosstalk, see figure below. USB data lines should be Differential Offset Coplanar Waveguide with 90 Ohms characteristic impedance.



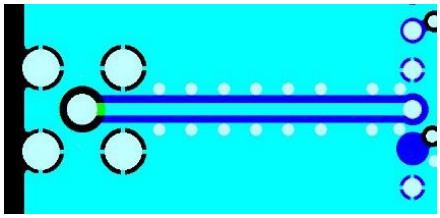
- The RF antenna track, and eventually any via connected to it, must be a homogeneous waveguide with 50 Ohm characteristic impedance; we suggest using the coplanar waveguide with ground model where the RF track has a **uniform ground** plane **underneath** and **surrounding** it as in figure below. Do not place signal lines and signal-VIAs crossing or close to RF lines in no one of waveguide's layers involved.



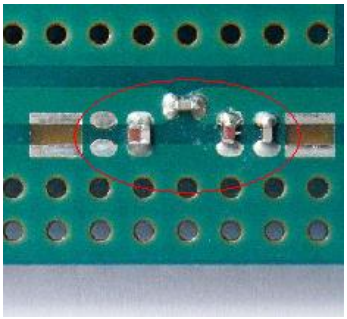
- When dielectric between 2 consecutive layers has not the desired height then for right impedance realization, you should remove the copper under RF line or pad, in one or more layers, to wider dielectric between antenna track and its reference ground plane, as example in figure below. The clearance in the internal layers must be wider than the W+2G. This is to avoid electric filed to close in internal layers instead of in the desired reference ground layer.



- We suggest shielding the waveguide by adding a series of conductive VIAs evenly distributed (e.g. every 2mm) all along the edges of the GND plane facing the coplanar waveguide (about 1mm from the edge), both sides. (see figure below). This improve line grounding and reduce signal coupling inside the PCB from adjacent tracks.



- If applicable, route RF matching network using as short as possible tracks and avoiding stubs, sharp bends and meanders.
  Figure below represents a layout example of the RF line matching network circuitry.



2.3. General comments

Please check and follow Telit Modem Integration Design Guide.
Review is related to received application information and the supposed use of it.

3. Quality record

This design review is registered internally in Bugzilla with ID #33285.
The customer request is registered internally in Salesforce with ID # 00201737.