Design Rules Verification Report

Filename : C:\Users\Mehmet Günce Akkoyun\AppData\Local\Temp\Releases\Snapshot\3\

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.1mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.77mm) (Max=0.77mm) (Preferred=0.77mm) (InNetClass('R7_Nets'))	0
Width Constraint (Min=0.1mm) (Max=1.5mm) (Preferred=0.2mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.175mm) (Conductor Width=0.2mm)	0
Minimum Annular Ring (Minimum=0.125mm) (All)	0
Minimum Annular Ring (Minimum=0.125mm) (((ObjectKind = 'Pad') OR (ObjectKind = 'Via')) And	0
Minimum Annular Ring (Minimum=0.125mm) (((ObjectKind = 'Pad') OR (ObjectKind = 'Via')) And	0
Hole Size Constraint (Min=0.15mm) (Max=5mm) (All)	0
Hole To Hole Clearance (Gap=0.35mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.08mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.1mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.2mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25mm) (Prefered=12.5mm) (All)	0
Total	0