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Contents

1. Scope

Aim of this document is to describe suggestions and corrections that Telit advises to improve **Ovoo Electronics "B106AA(V2)"** customer application that integrates Telit **GE910-QUAD V3** module.

2. Design review

Design review is based on the following received documentation:

- Schematic files: B106AA-R4.PDF
- Gerber file: none
- Other: Telit Design Review R04 (Schematic).pdf

Summary Tables:

Schematic Review	P	F	I	MI	N/A
Power Supply	√				
SIM Pins	√				
Digital Pins	√		√		
Audio					√
RF	√				

PCB Layout Review	P	F	I	MI	N/A
General Placement					√
Antenna Waveguide					√
RF Aspects					√
Audio Aspects					√

P: Pass; F: Fail; I: Improvements possible; MI: Missing Information; N/A: Not Applicable

The following symbols will be used throughout the Design Review to indicate:

√ OK: No design changes are required.

Tip: information or possible improvement, not mandatory but recommended.

Warning: if you don't follow the recommendation there's a risk of malfunctioning or issues during the homologation phase, strongly recommended.

Error: it's mandatory to follow the recommendation otherwise the module could be damaged or could not work properly or there's high probability of facing issues during the homologation phase.

? Missing Information: some relevant information is missing therefore the DR cannot be accurate on this item.

2.1. Schematic review

2.1.1. Power supply

- OK

2.1.2. SIM pins

- OK

2.1.3. Digital pins

- OK

For deep power saving when using *AT+CFUN=5*, the modem checks the DTR status. Only when DTR goes OFF, C108/DTR='HI' or floating, modem is allowed to enter into deep power saving mode; otherwise, if DTR is ON, C108/DTR='LOW' modem remains always awake. **Avoid leaving DTR opened or tied to fixed values, we suggest connecting, it to a controller to access the possibility of going into power saving mode**.
In case of another power saving mode, *AT+CFUN=0 or 9*, the modem checks RTS transition from RTS (OFF)='HI' to RTS(ON)='LOW'. Again, RTS shall not tied to fix values but controlled by your uP.

2.1.4. Audio pins

- N.A

2.1.5. RF aspects

- Ok

2.2. PCB Layout review

We do not have the PCB yet, but we will provide few general considerations that shall be taken into account when designing the PCB for your convenience.

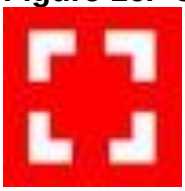
2.2.1. General placement

We strongly suggest adding the outline trace to mount a metallic shield on top of Fast digital, MCU, Memories and *Power Supply components area* to reduce spurious emissions on any board of the system. It is a must in case of switching components, rectifiers and power amplifiers. You can do this by packing components in well-defined

areas surrounded with ground pads where you can eventually solder the shield. The shield options can be used if needed to suppress EMI fields that may interfere with the cellular reception/emission.

- Once below the component is all ground, the PADs GND and VBATT should be done with thermal relief, like in figure below, otherwise having a big plane can create high thermal dissipation with consequently bad soldering due to a different local solder temperature profile.

Figure 16. GROUND and VBATT thermal relief Pad layout.



2.2.2. RF aspects

- The Ground of the PCB or Chip RF antenna is part of antenna when using a monopole, especially the part that lies in front of the monopole. Leave a wide ground area, without components and tracks, of at least 5mm, in front of antenna on all layers, on the internal layers the width could be less.

- If antenna is placed directly on onboard connector, it is important to consider leaving a wide ground area for it.

- The position of the external antenna with respect to boards is of maximum importance and any board of the system must be RF proof, not only the modem board.

- Move components, tracks, vias and connectors away from antenna area to reduce their coupling with RF signal; you can also bury them in the inner layers of a multi-layer PCB.

- We strongly suggest following these PCB design rules. Use at least 4 layers. External layers must be mainly ground planes with tracks buried in the inner layers as indicated in the following rules:

  - Top Layer: **mainly ground plane interrupted just by component** pads and RF antenna tracks.
  - INNER Layers: mainly interconnection tracks and power planes, **under the RF tracks only ground plane is allowed.**
  - Bottom Layer: **mainly ground plane interrupted just by component** pads and RF antenna tracks.

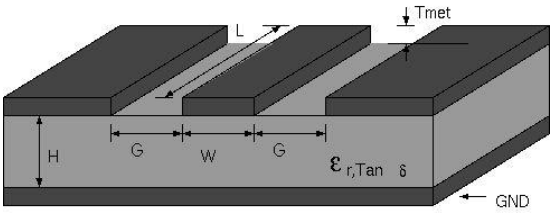
- All the PCB borders should be ground on ALL layers, with a fence of GND vias one each 2mm. All the ground, either planes or areas, must be well connected with VIAs to

guarantee a strong equipotential node. Avoid unconnected copper islands and signal or vias on PCB border.
The only exceptions are eventually the antenna's areas where ground and ground vias are in the ground surface facing the antenna monopole. Remove tracks and pads that are on the edge of the PCB, moving them to internal layers.

- Top and Bottom layers should be mainly a ground plane interrupted just by component's pads, vias and RF tracks, with several vias to interconnect all ground planes. In this way the signal tracks are more protected from picking up RF due to the Faraday-Cage effect. Long exposed tracks can easily pick-up RF power and especially in your case with many RF power sources you can generate high frequency intermodulation harmonics that the same exposed tracks can then irradiate very efficiently.

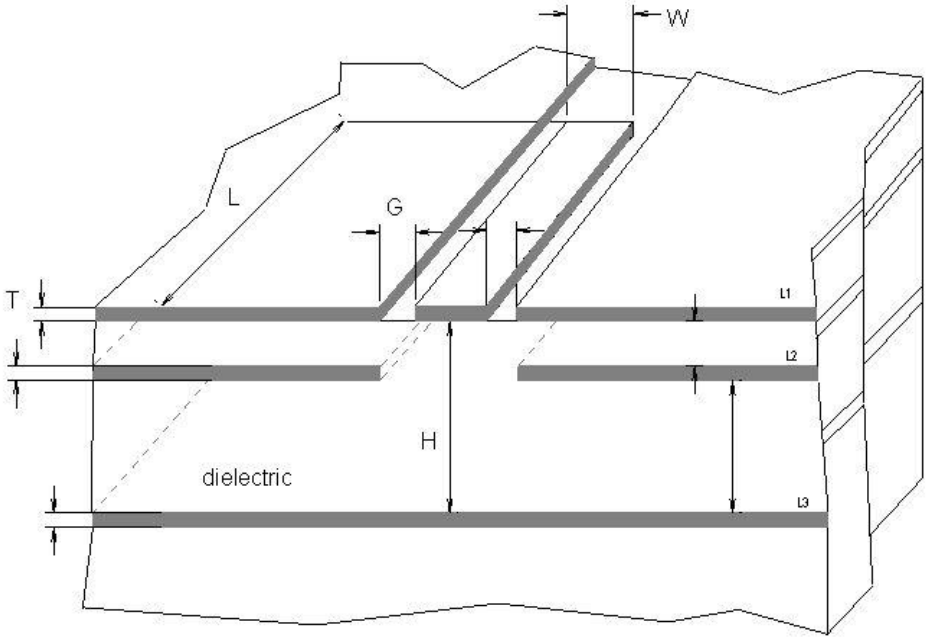
- The RF antenna track, and eventually any via connected to it, must be a homogeneous waveguide with 50 Ohm characteristic impedance; we suggest using the coplanar waveguide with ground model where the RF track has a **uniform ground** plane **underneath** and **surrounding** it as in figure below. Do not place signal lines and signal-VIAs crossing or close to RF lines in no one of waveguide's layers involved.

Figure 18. RF layout of Coplanar with Ground (CPW) Waveguide model.



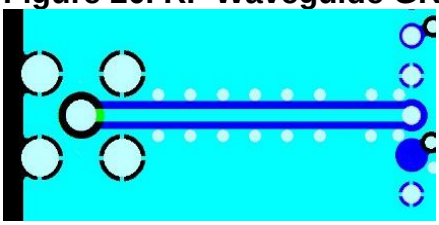
- If dielectric between 2 consecutive layers, as could be Layer1 and Layer2, is not enough for right impedance realization, then you can remove the copper under RF line or pad, in this case on Layer2, to have wider dielectric between Layer1 and Layer3, as example in figure below.

Figure 19. RF Waveguide typical layout.



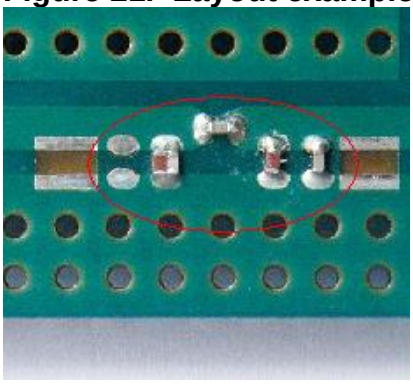
The ground in front of PCB antenna, surrounding and under waveguide must be well connected each other. Use many vias, every 2mm maximum, to connect ground layer with all other ground planes and layers as example in figure below.

Figure 20. RF Waveguide GROUND realization.



Route RF matching network using as short as possible tracks and avoiding bends and stubs.
Figure below represents a layout example of the RF line matching network circuitry.

Figure 21. Layout example RF line matching.



2.2.3. Audio aspects

- N.A.

2.3. General comments

Please check and follow *Telit Modem Integration Design Guide*.

Review is related to received application information and the supposed use of it.

3. Quality record

This design review is registered internally in Bugzilla with ID #32846.
The customer request is registered internally in Salesforce with ID #00157856.