Implementing a Single Stage fully differential folded cascode Amplifier with Gain Boosting Technique

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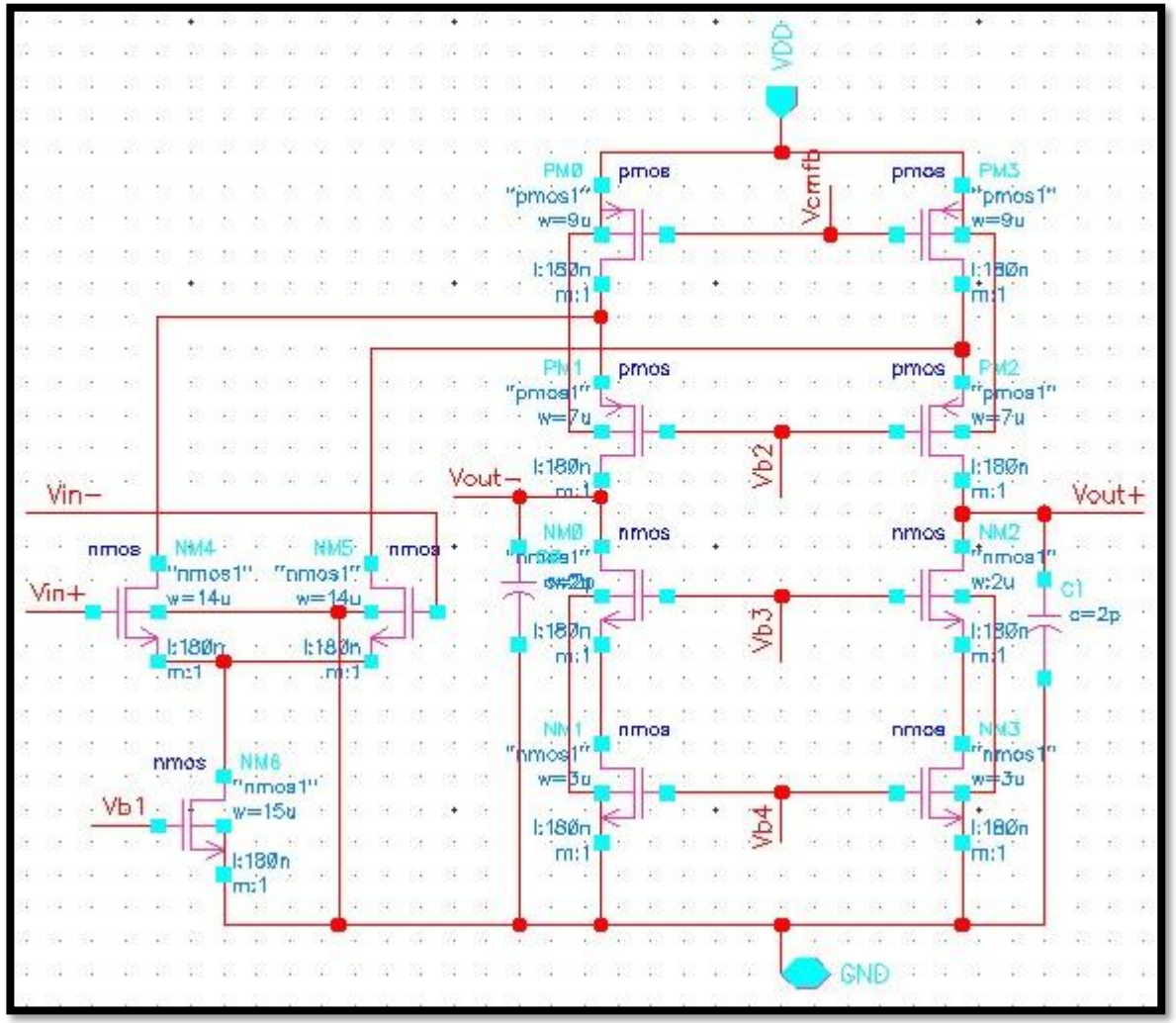
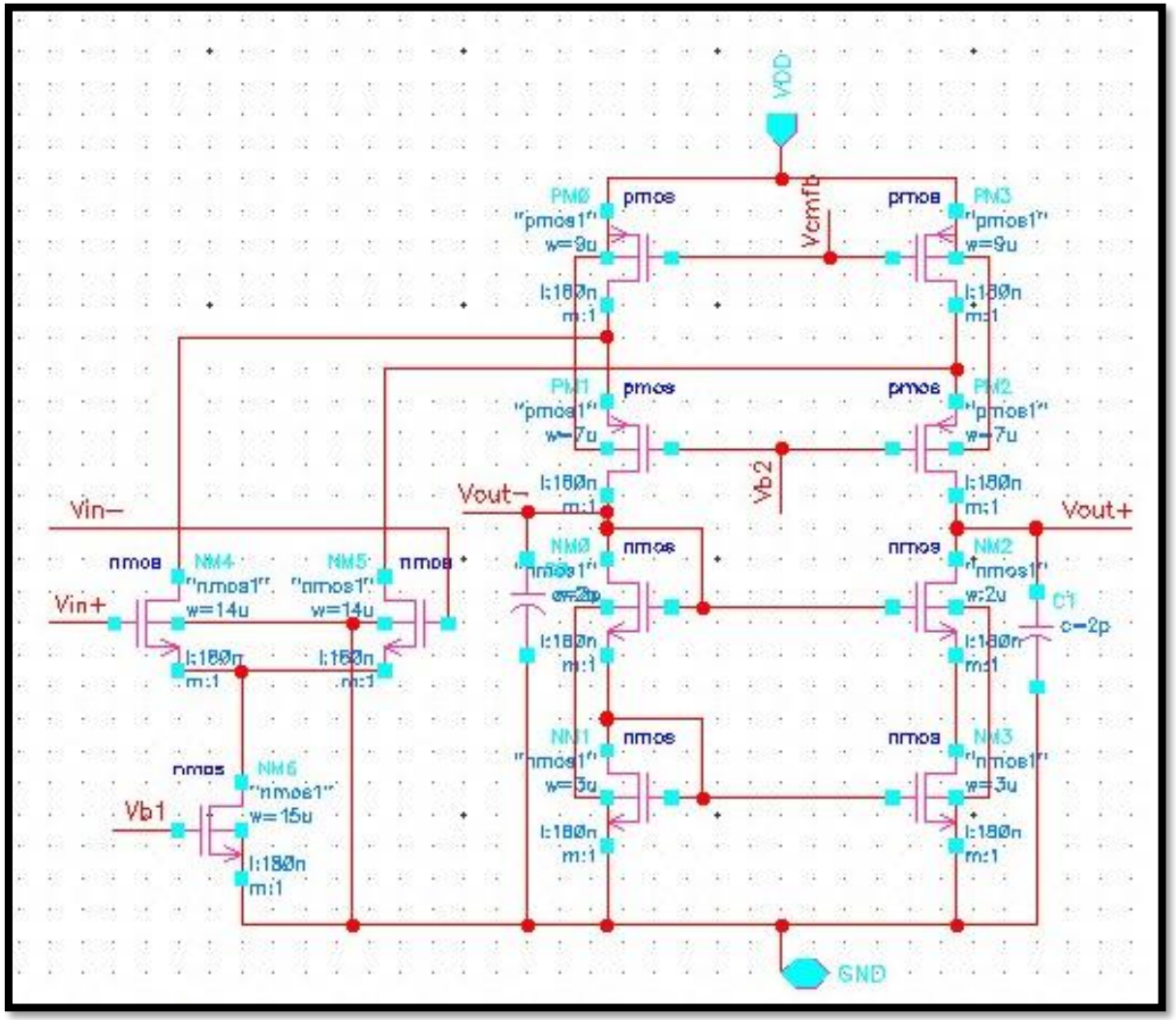
Fully Differential Folded Cascode (1/2)



- The circuit shows implementation of a fully differential folded cascode structure.
- Our initial attempt was to do analysis on fully differential structure without any gain boosting employed and compare how the gain is enhanced and other parameters are varied as we moved towards gain boosted topology.
- But the problem with this circuit was how to do biasing at the gate terminals of transistors.
- To provide a solution for biasing we moved to our next circuit.

Fully Differential Folded Cascode (2/2)

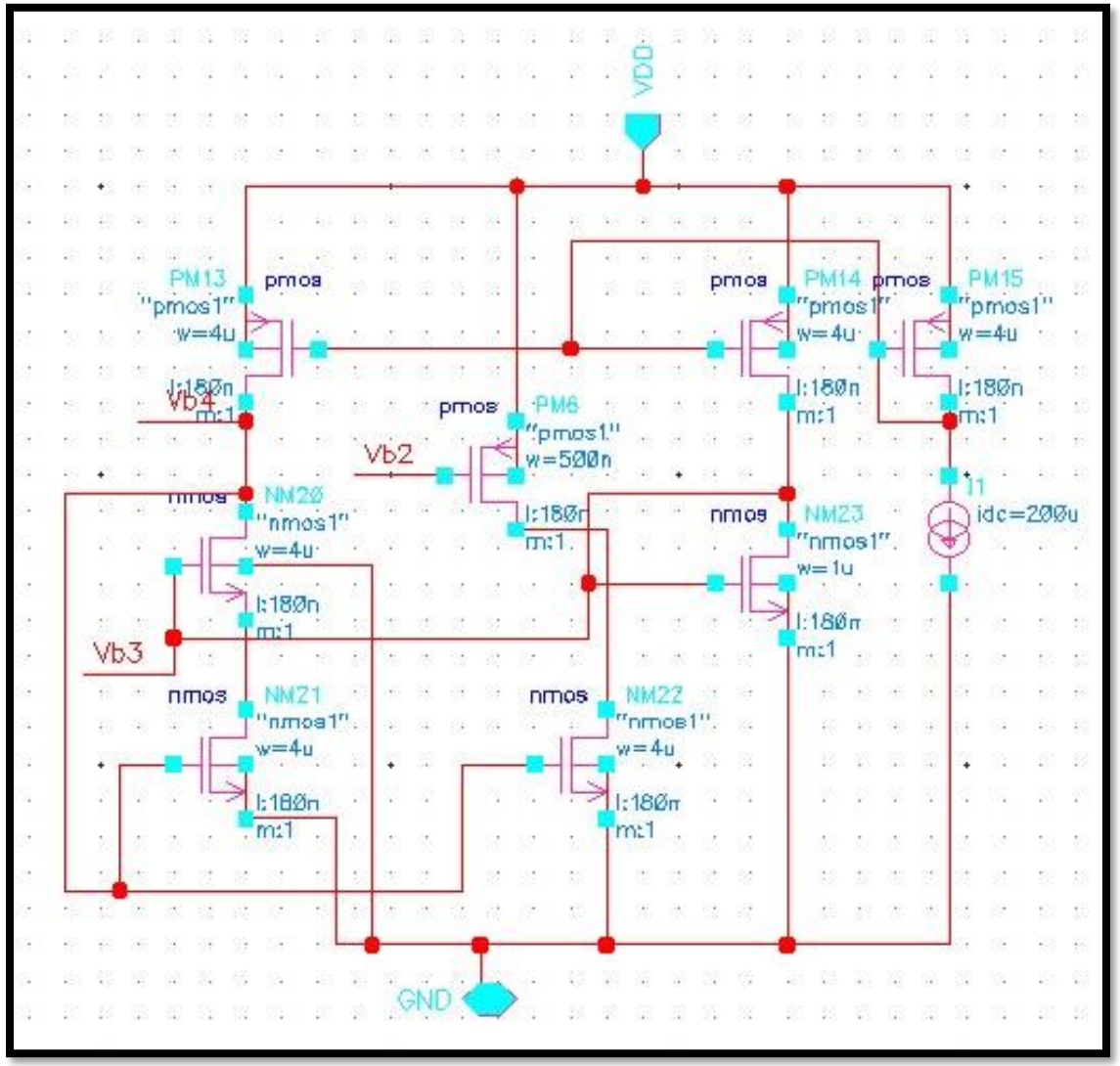


- To solve for the problem we faced earlier, we moved at this topology, i.e. we made the two NMOS transistors as diode connected transistors by connecting their gate and drain terminals same as connected in cascode current mirror. Biasing problem for the stack nmos is solved over here. But over here the issue faced is that -

  Vout(min) = 2*Vov + Vt

- hence Vout(min) is increased To get the maximum swing Vout(min) should be 2Vov but over here it is greater by a factor of Vt, due to which the swing of our circuit is reduced.
- So enhancement in circuit has to be done so that there is an improvement in the circuit swing. This made us move towards other modification.

Wide Range Cascode Current Mirror



- In this modification, we introduced a wide range cascode current mirror. This circuit helped us to provide the bias for the bottom stacked NMOS transistors we can also bias the above PMOS transistors with the similar scheme, so we can use a PMOS with similar bias current to bias the PMOS stack.
- Also this circuit enabled us to increase the swing of the circuit, as over here-

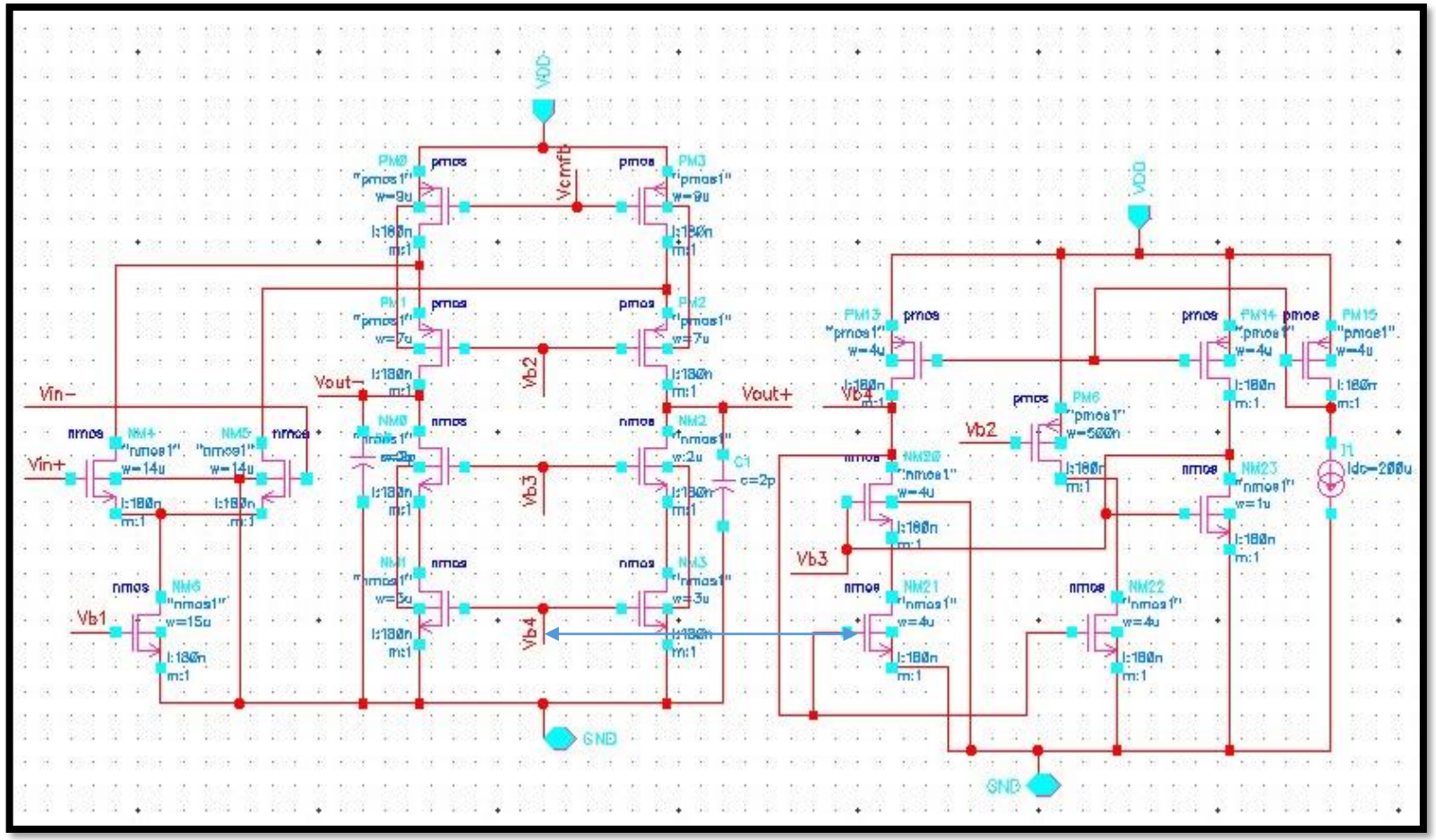
  Vout(max) = VDD- 2*Vov

  Vout(min) = 2*Vov
- Thereby when we see at the total output swing it is-

  = Vout(max)-Vout(min)

  =VDD- 4*Vov
- Hence this circuit enabled us to increase the swing as well as provide the biasing to the gate of differential transistors.

Fully Differential Amplifier and Wide Range Cascode Current Mirror Circuit



- In this implementation, we have shown how cascading of both wide range cascode current mirror and the fully differential folded cascode is done.
- This structure is implemented, providing the biasing at the respective mentioned gate terminals
- Also helping us to increase the overall swing at the output of the structure.

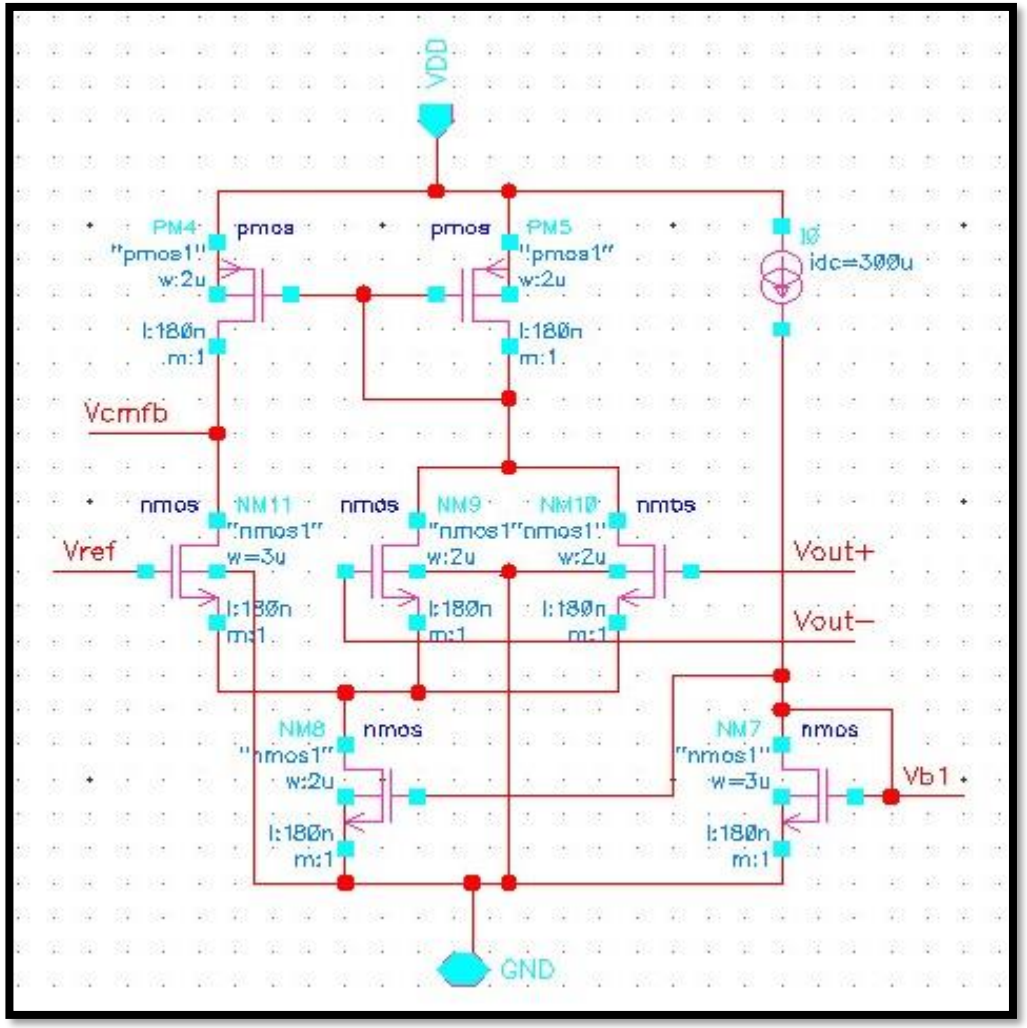
Common Mode Feedback Circuit

- A common mode feedback circuit comprises of a common mode detector which senses the output common mode voltage and it is connected in negative feedback to control output common mode voltage .

Need of Common Mode Feedback Circuit

- A common mode feedback circuit is required to stabilize the output common mode voltage of fully differential circuits.
- While designing fully differential circuits for example a folded cascode fully differential circuit, then in that circuit the current in the above PMOS stack must be equal to the current in the below NMOS stack.
- If both the currents are not equal then either the output voltage keeps on rising until the above PMOS goes into triode region and output gets very close to VDD rail or the output voltage keeps on falling until the below NMOS goes into triode region and output gets very close to GND rail.
- So from the above discussion it is evident that the common mode feedback circuit is the **necessity** for fully differential circuits.

Common mode feedback circuit



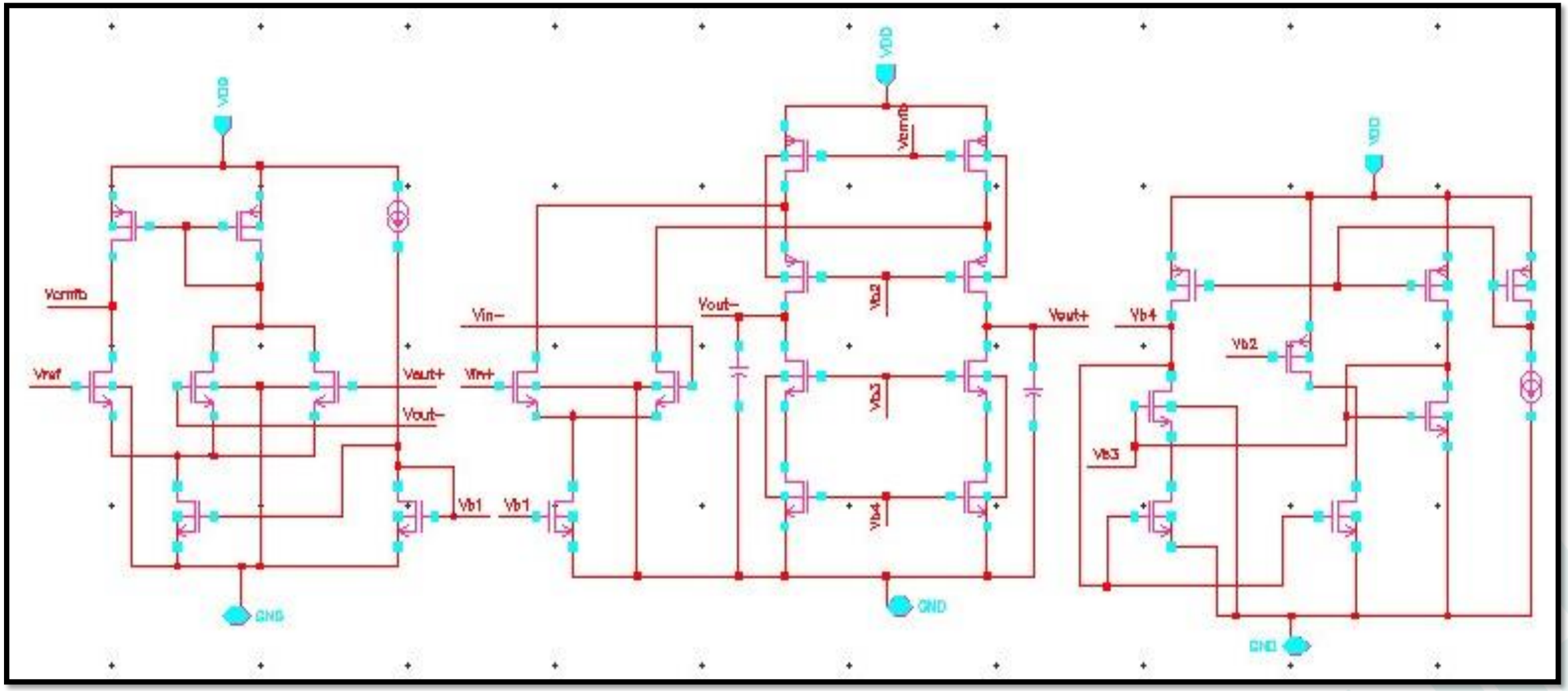
Selection of Common mode detector circuit

- So we can make common mode detector as either **PMOS load and NMOS input type** or **NMOS load and PMOS input type.**
- Here in our circuit as we supposed to provide bias for the pmos load i.e the gate voltage for both the PMOS's.
- So therefore the dc point of the output of common mode feedback circuit is supposed to be close to the bias point of the gate of PMOS, therefore we are using here **PMOS load and NMOS input type common mode detector circuit.**
- Since we able to achieve symmetric swing as compared to VDD i.e.

  Vout(max) = VDD- 2*Vov **Vout(min) = 2*Vov**

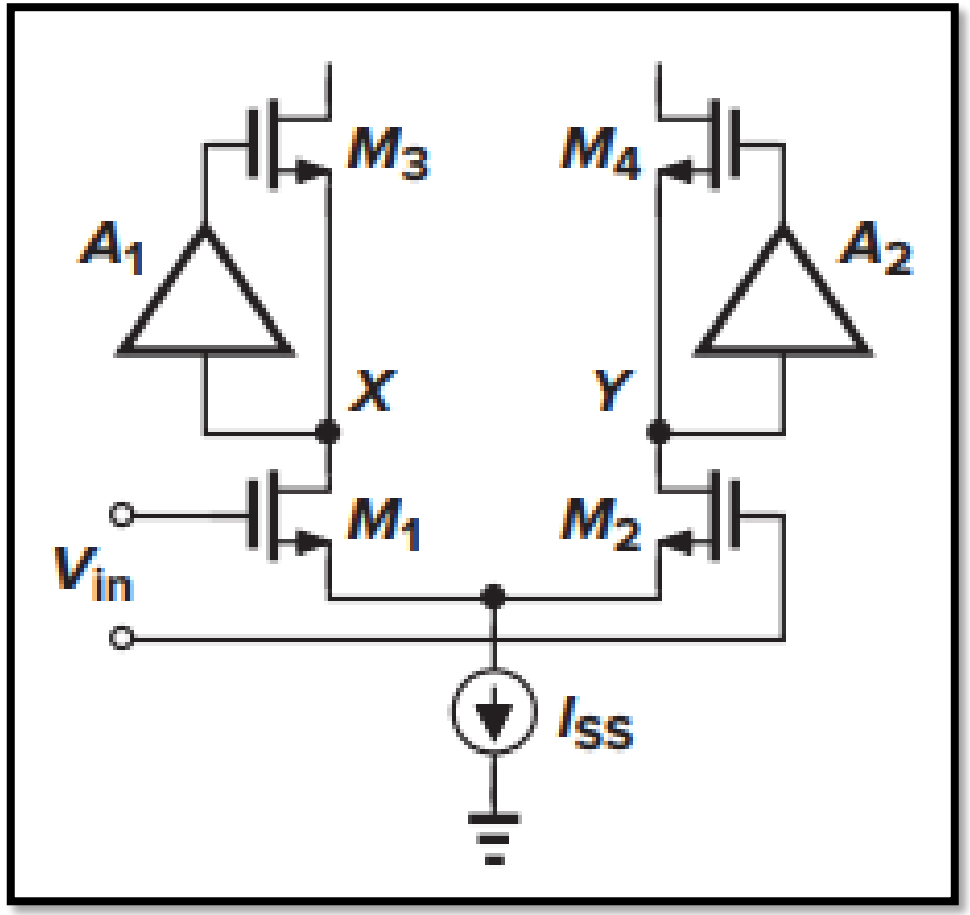
  Therefore a good biasing point will be **(Vout(max)+Vout(min))/2** which is basically VDD/2 approximately, so thats why we kept our **Vref = VDD/2**

Fully Differential Amplifier with Wide Range Cascode Current Mirror and Common mode Feedback Circuit



Gain Boosting Circuit (1/4)

- If the gain boosted structure is implemented by a single input and single output auxiliary amplifier structure, for both the transistors.



Gain Boosting Circuit (2/4)

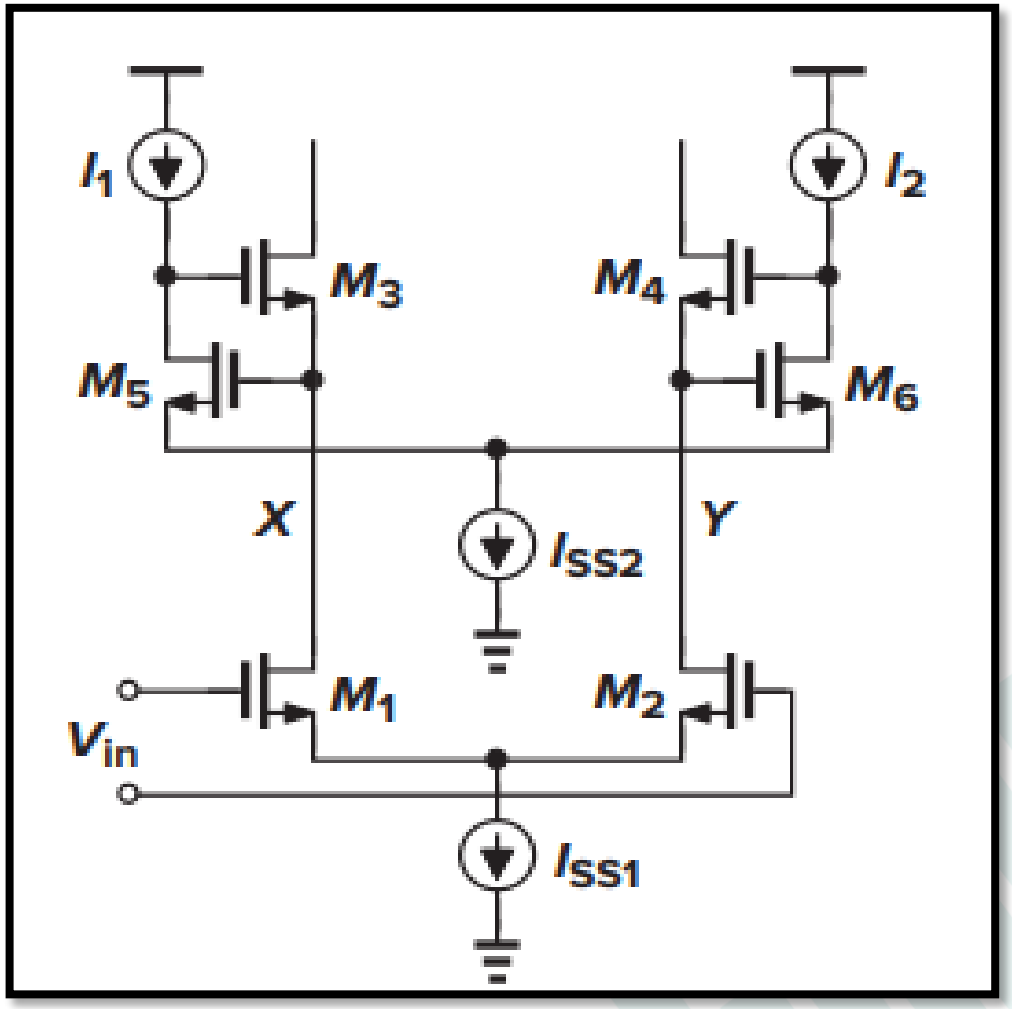
- Further if the auxiliary amplifiers are replaced by differential amplifier structure, then

  Vout(min) = Vov3+Vgs5+VIss2

  (as Vgs5>Vov1)

- Therefore this lead to increase in Vout(min), which leads to reduction in the output swing.

- If M5 and M6 transistors is replaced by a pmos differential, it solves the problem as minimum input CM level of a folded-cascode stage using a PMOS input pair can be zero.



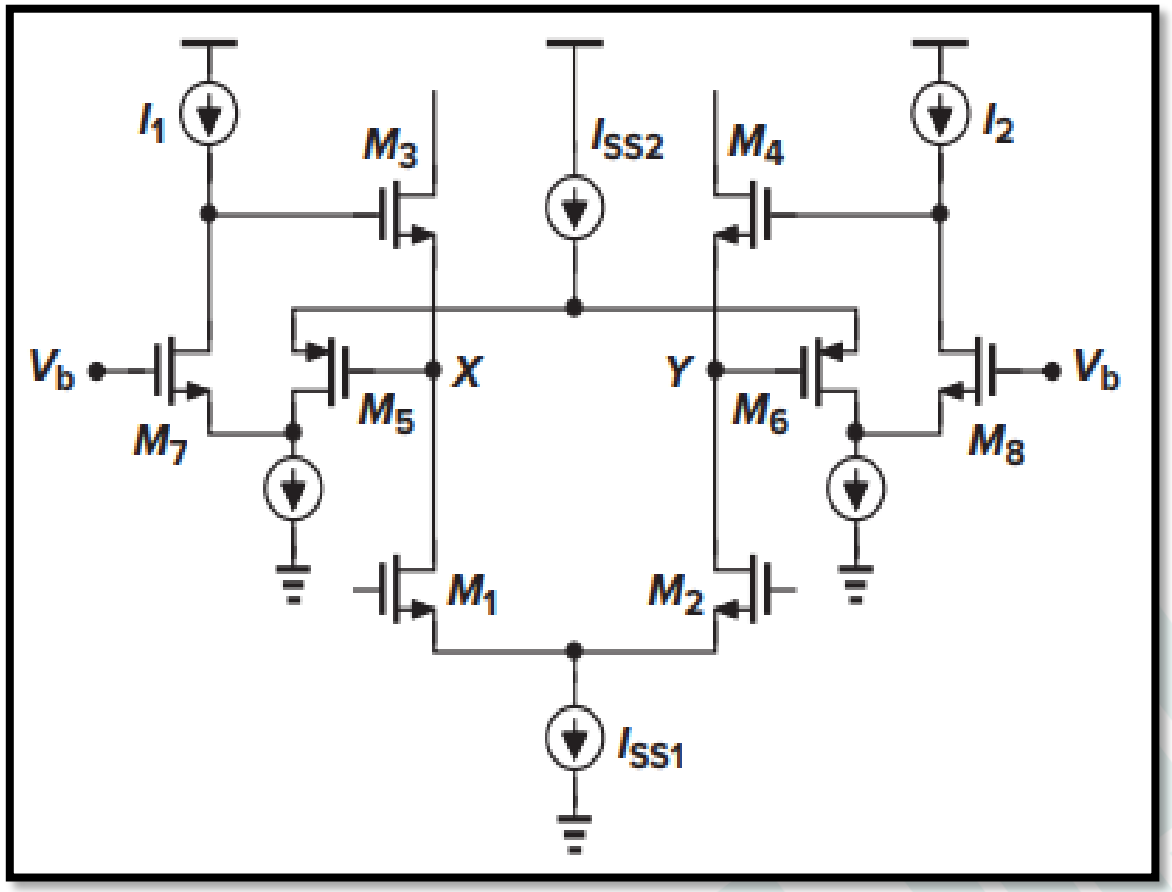
Gain Boosting Circuit (3/4)

- If M5 and M6 transistors is replaced by a pmos differential input pair,

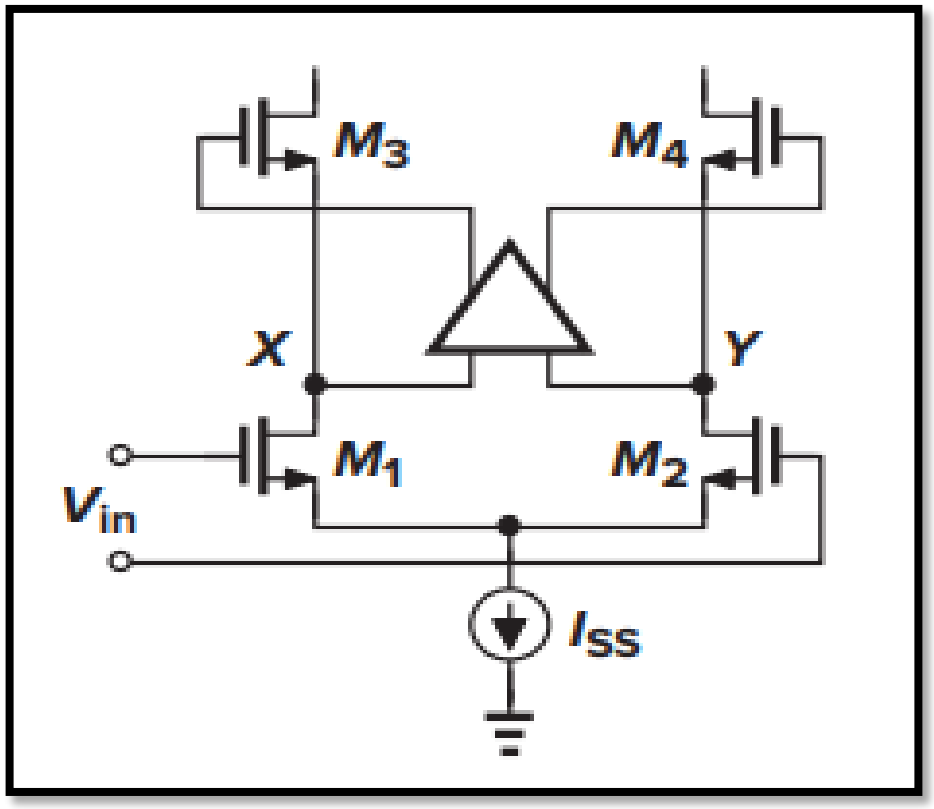
  Now

  Vout(min)=Vov3+Vov1+VIss2

- Hence this causes reduction in Vout(min), which causes increase in swing. Therefore we use **Differential Input and Differential Output Auxiliary Amplifier** as shown in the next slide.

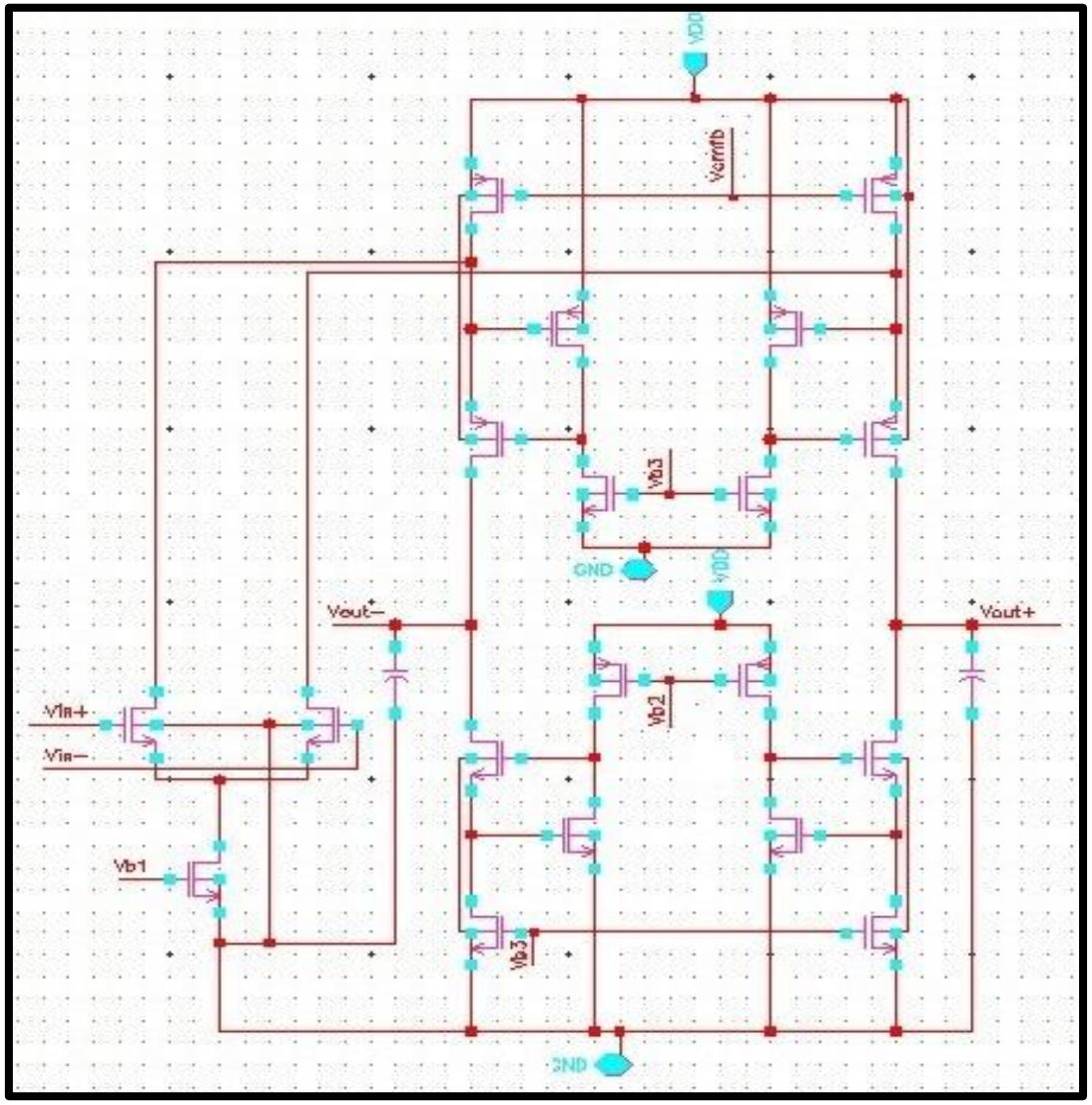


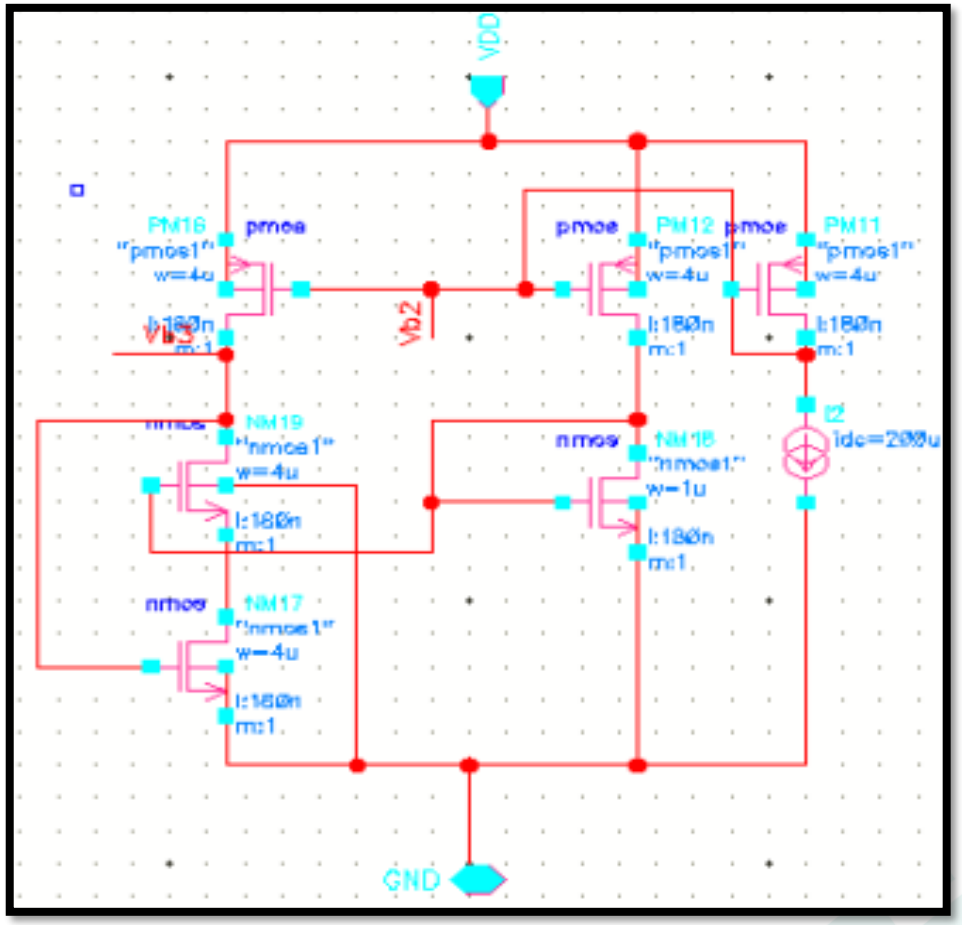
Gain Boosting Circuit (4/4)



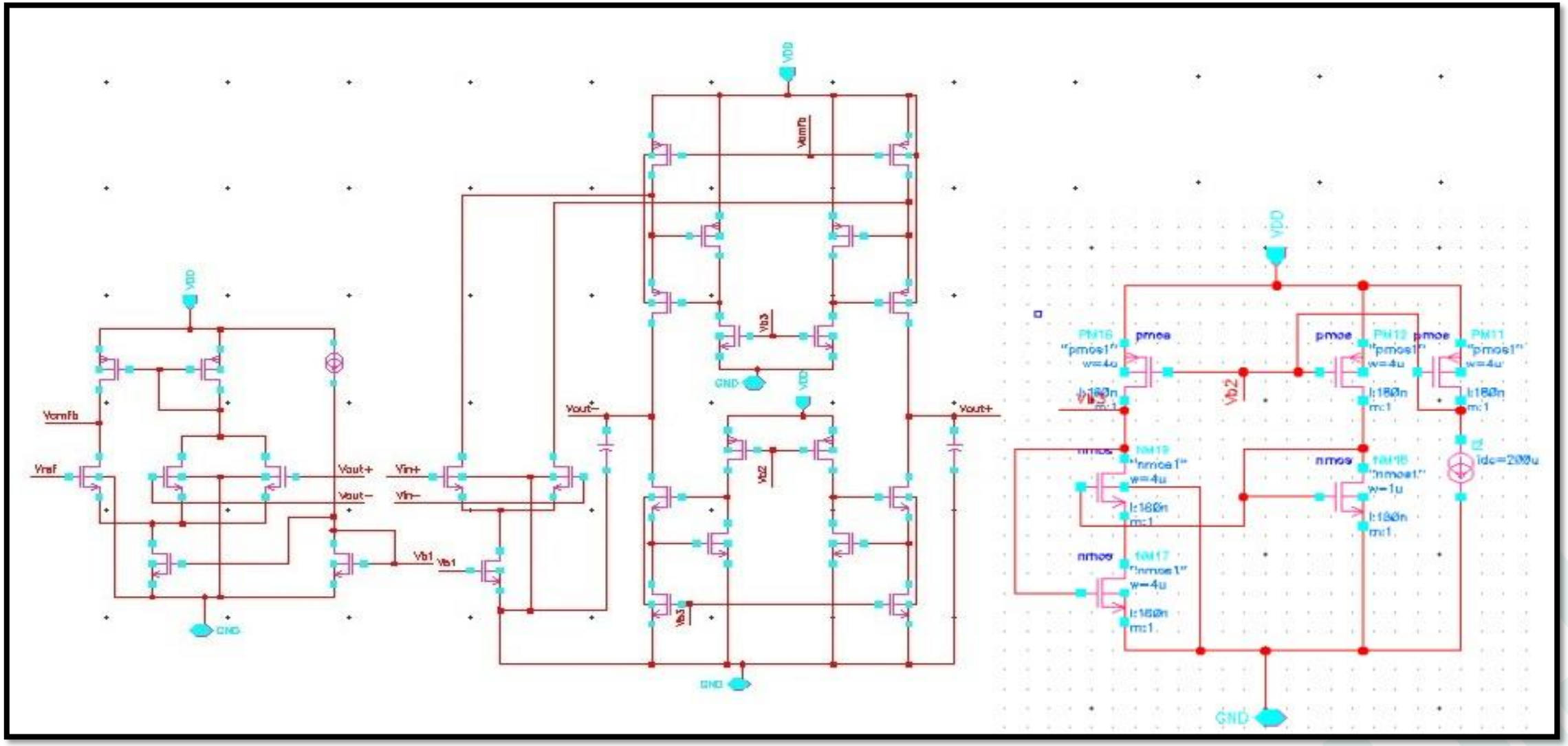
- Similarly for the nmos stack auxiliary amplifier is implemented by pmos differential input pair, in pmos stack is auxiliary amplifier is implemented by nmos differential input pair

Gain boosting Technique Implemented in Fully Differential Circuit and Wide Range Cascode Current Mirror

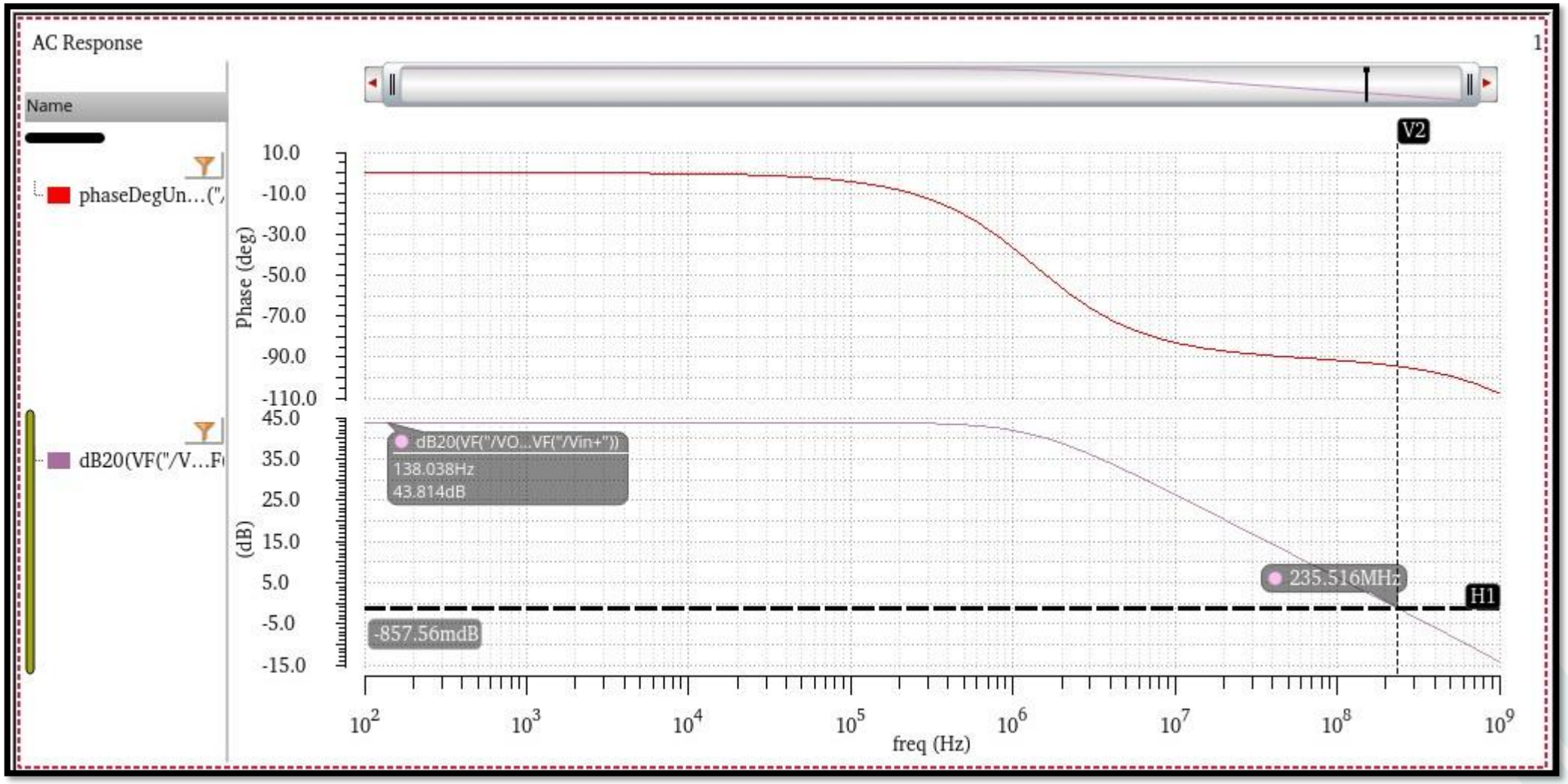




Fully Differential Gain Boosted Wide Range Cascode Amplifier with Common Mode Feedback Circuit

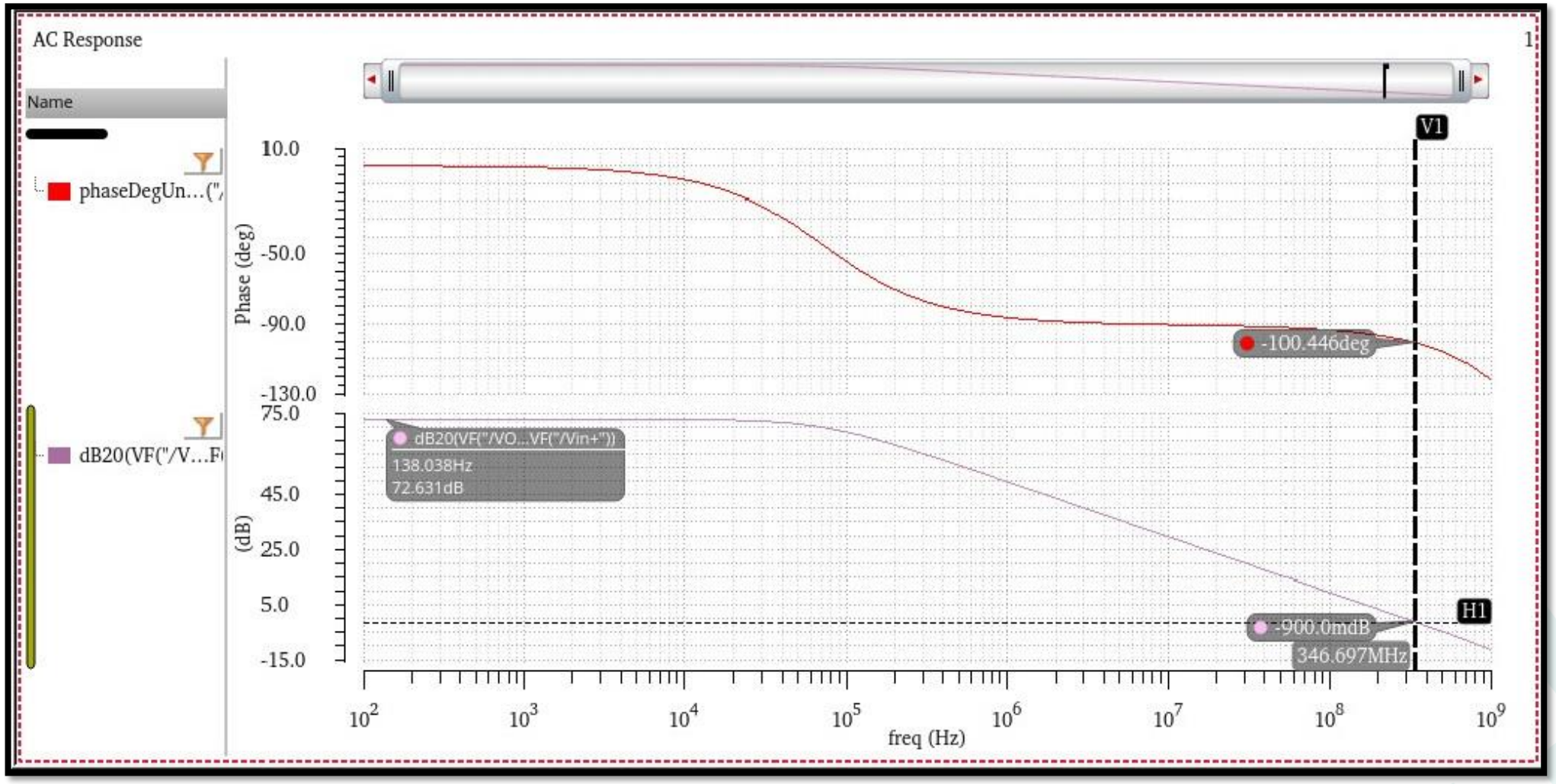


Simulation Results



Folded Cascode Amplifier

Simulation Results

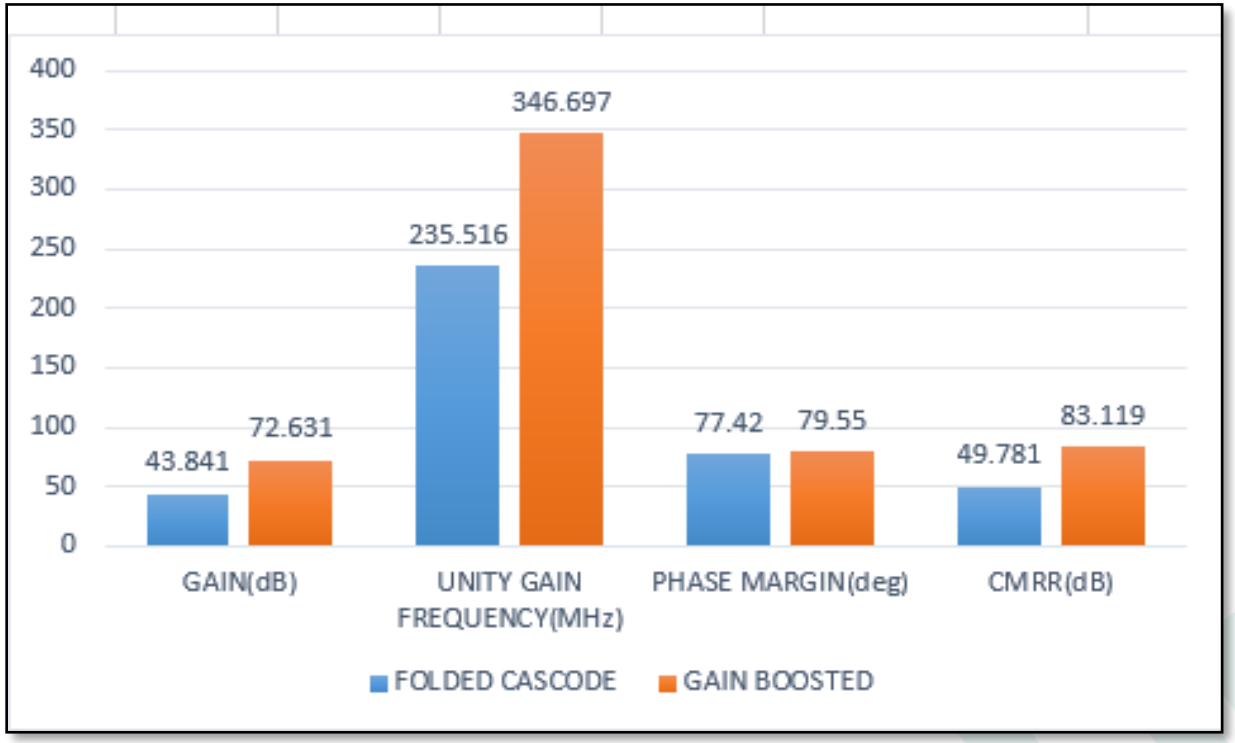


Folded Cascode Amplifier with Gain Boosting

Conclusion

COMPARISON BETWEEN FOLDED CASCODE AND GAIN BOOSTED		
Parameters	FOLDED CASCODE	GAIN BOOSTED
GAIN	43.841 dB	72.631 dB
UNITY GAIN FREQUENCY	235.516 MHz	346.697 MHz
PHASE MARGIN	77.42 deg	79.55 deg
CMRR	49.781 dB	83.119 dB

Parameters	This Work	References
DC GAIN(db)	72.631 dB	95 dB
UNITY GAIN FREQUENCY(MHz)	346.697 MHz	412 MHz
PHASE MARGIN (deg)	79.55 deg	75 deg
LOAD CAPACITOR(pF)	2 pF	1.9 pF
POWER SUPPLY(V)	3 V	3 V



Issues Faced

- We first attempted to bias the transistors by using constant voltage sources. However, it was neither an ideal nor a good design. As a result, we experimented with Simple Cascode Current Mirror, but after using cascode current mirror, we did not get full output swing. Then later on we employed wide range cascode current mirror, and got the full output swing . that's why we finally bias the transistors by wide range cascade current mirror.
- Firstly we decided to bias our circuit by resistive sensing but then later on we found out that implementing resistive sensing as a common mode detector can be of a huge fuss as it reqires large number of transistors. So we bias our circuit by a simple common mode detector. Hence connecting Vcmfb bias voltage to bias gate voltage of pmos transistor hence making a common mode feedback circuit.
- Initially we decided to use a single ended structure but cmrr was less in a single ended structure, so we moved towards at fully differential structure, also to bias the ckt, CMFB bias cannot be applied in a single ended structure.