AOI222 : Domino Style

Group Number: 15

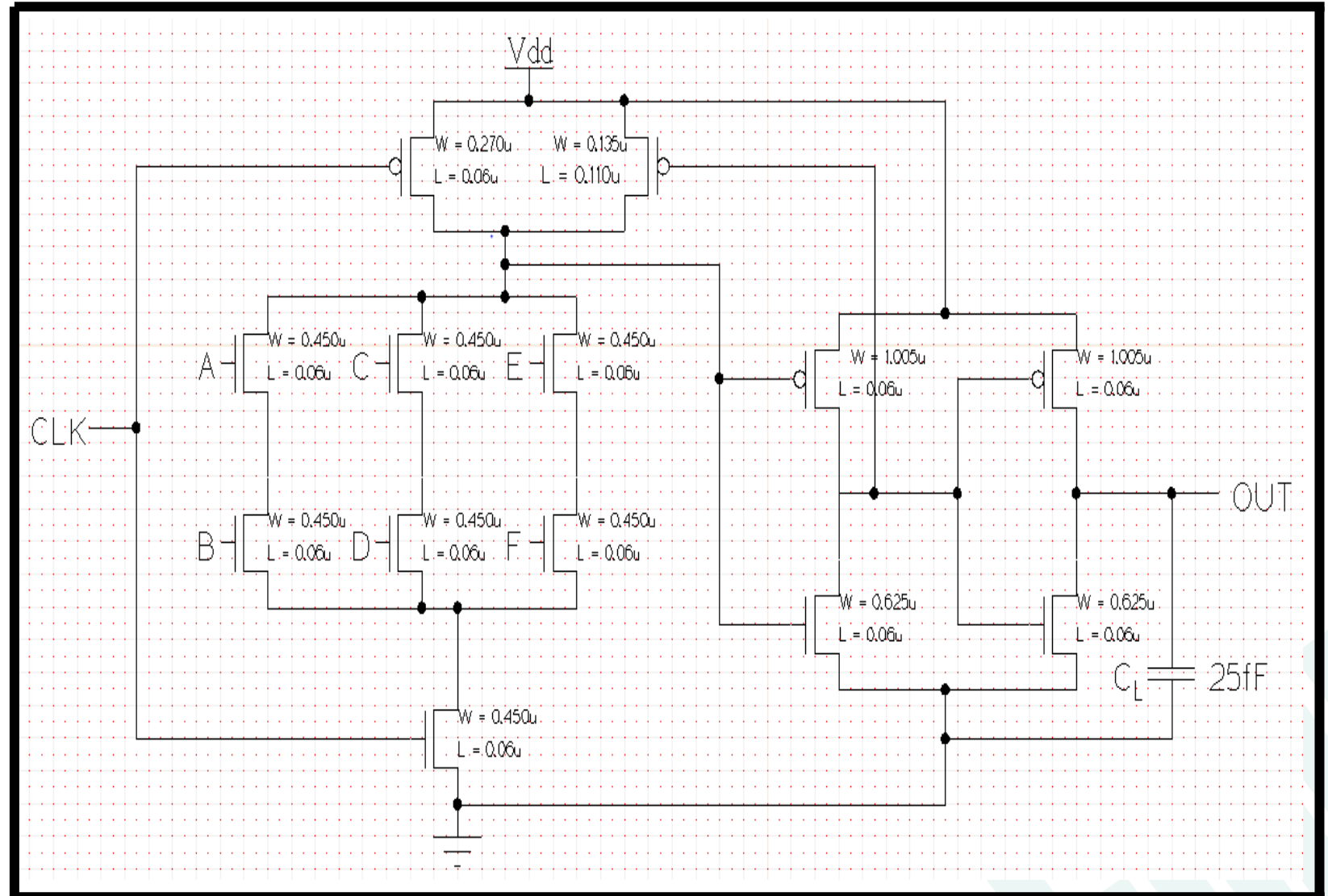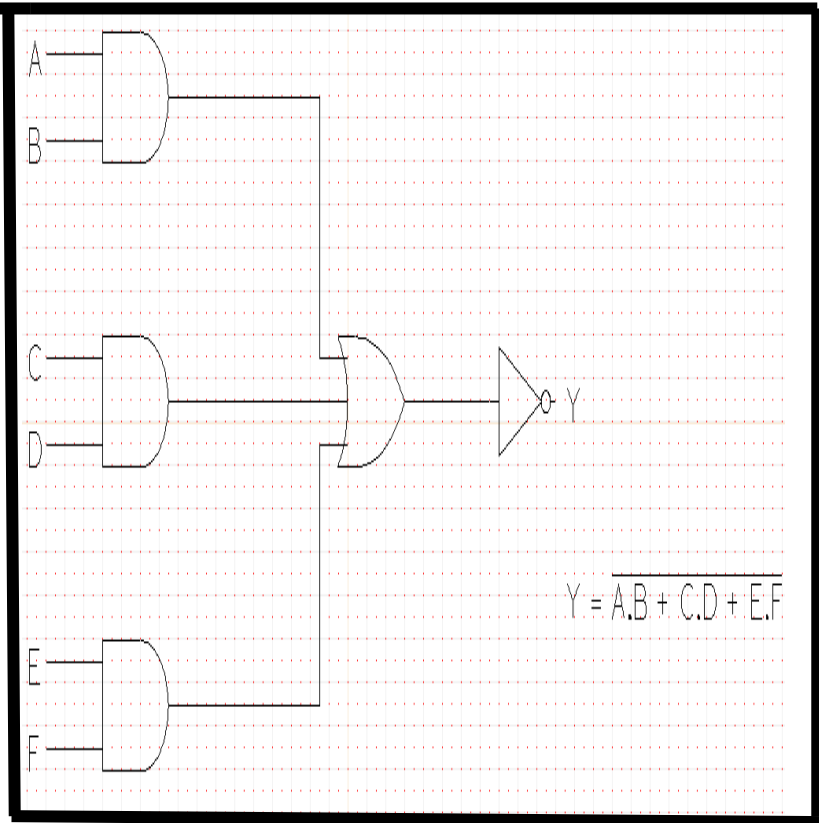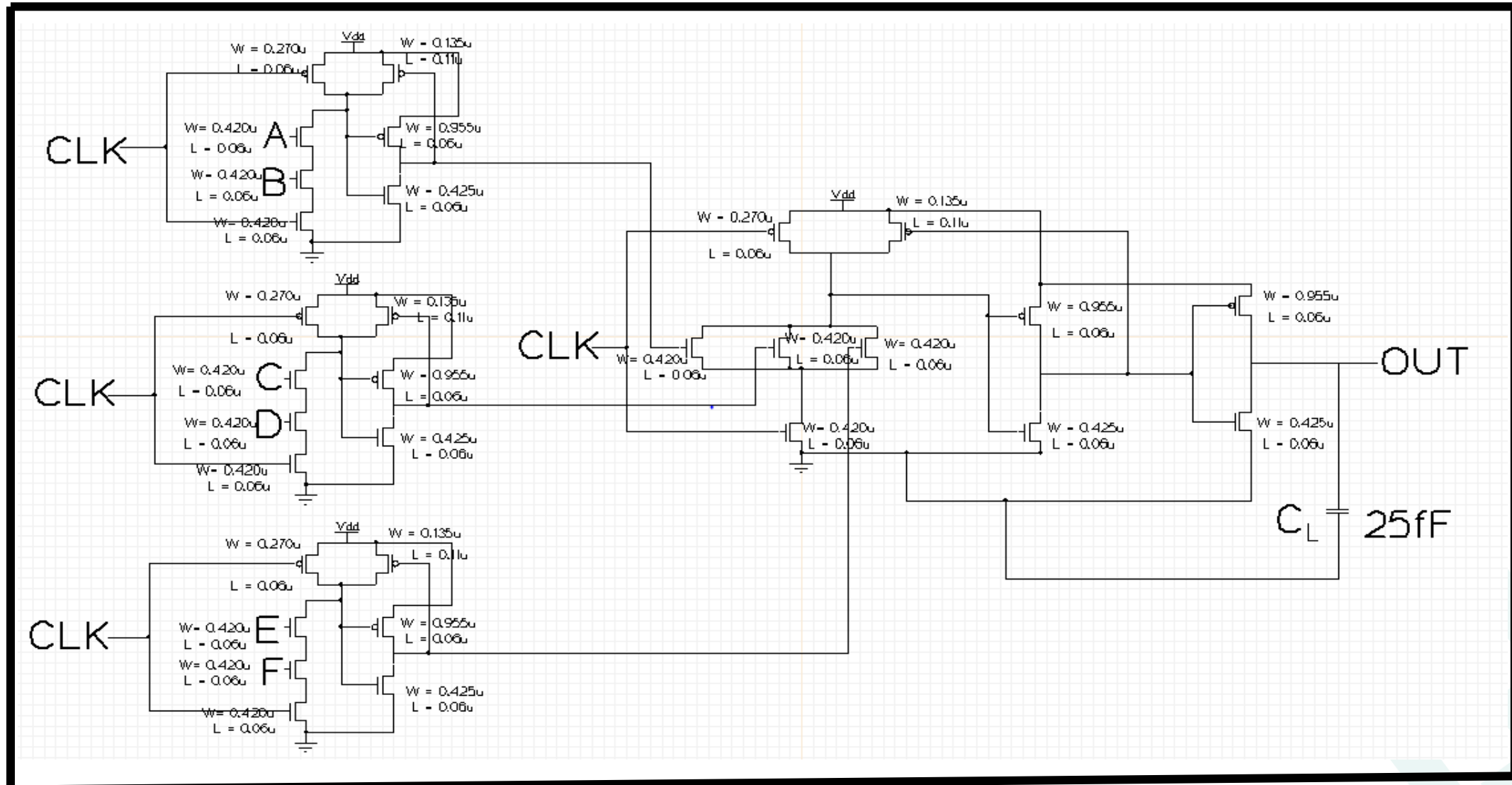Group Members :

- Aayushi Gupta – MT21215
- Aakash Gupta – MT21150
- Nikhil Pratap Singh- MT21199
- Aniket Vijayaraj- 2019145

IIID

INDRAPRASTHA INSTITUTE *of*
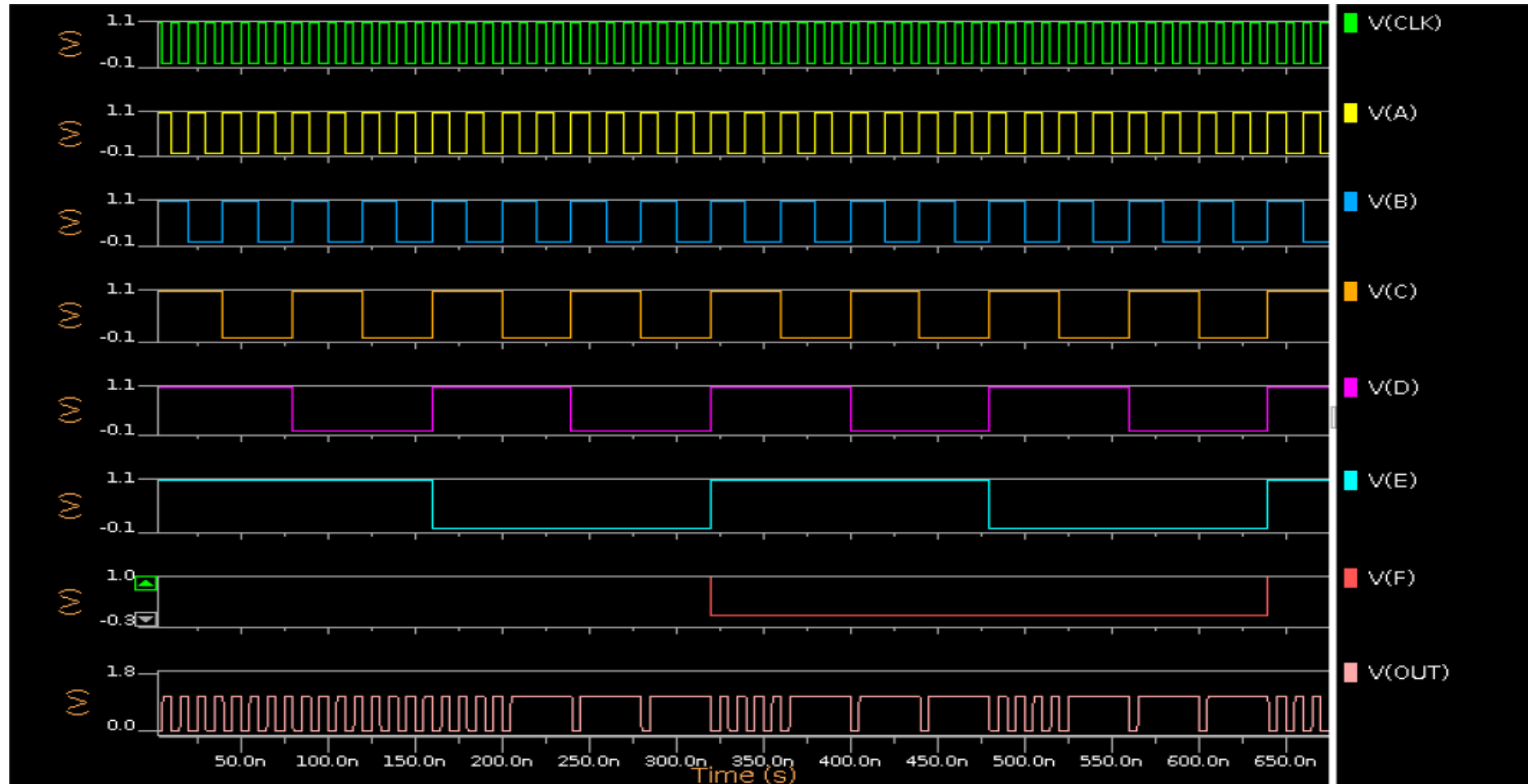INFORMATION TECHNOLOGY
DELHI

Schematic and Sizing (Complex Gate)

$Y = \overline{A.B + C.D + E.F}$

SIMULATION WAVEFORMS

After comparing waveforms for both complex and non-complex both were found to be same.

Stick Diagram
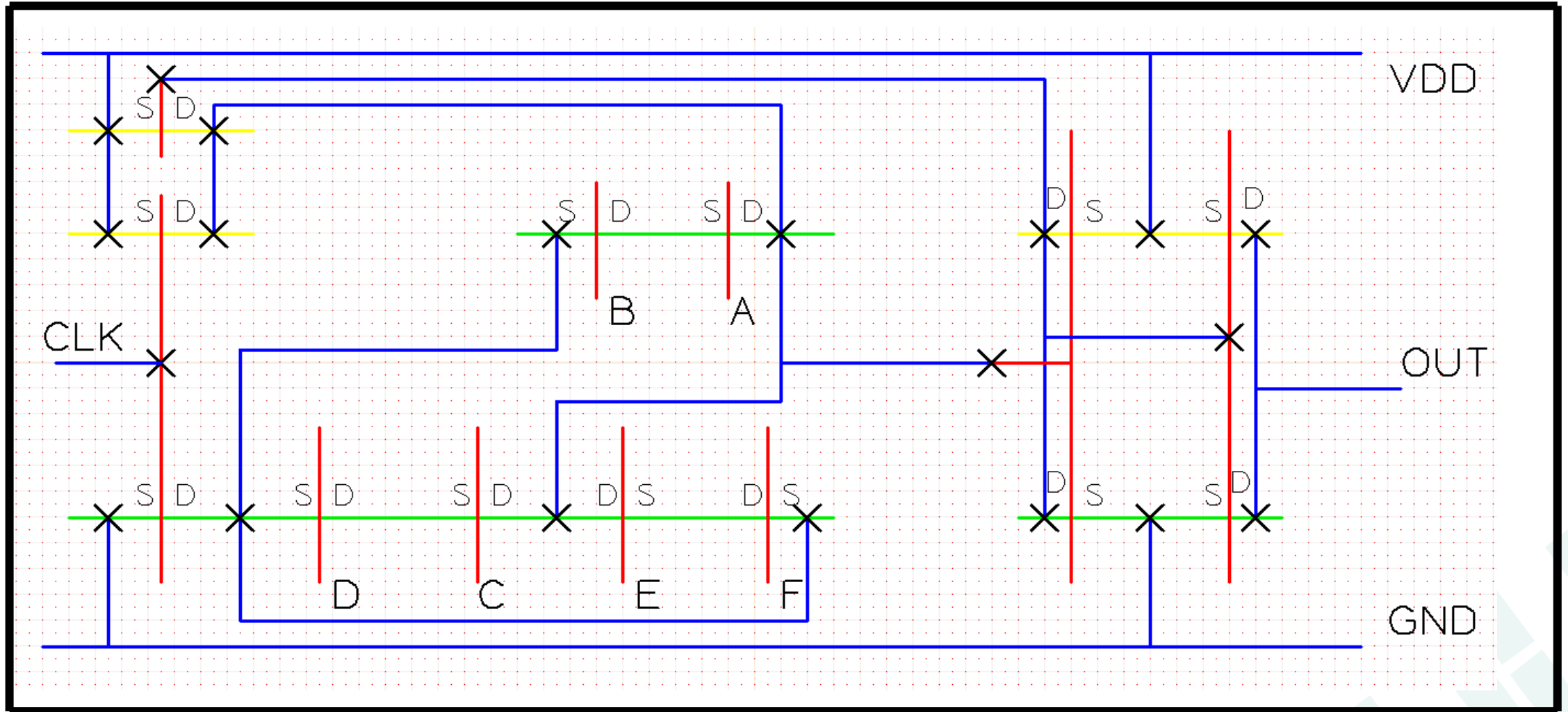
ANALYSIS:
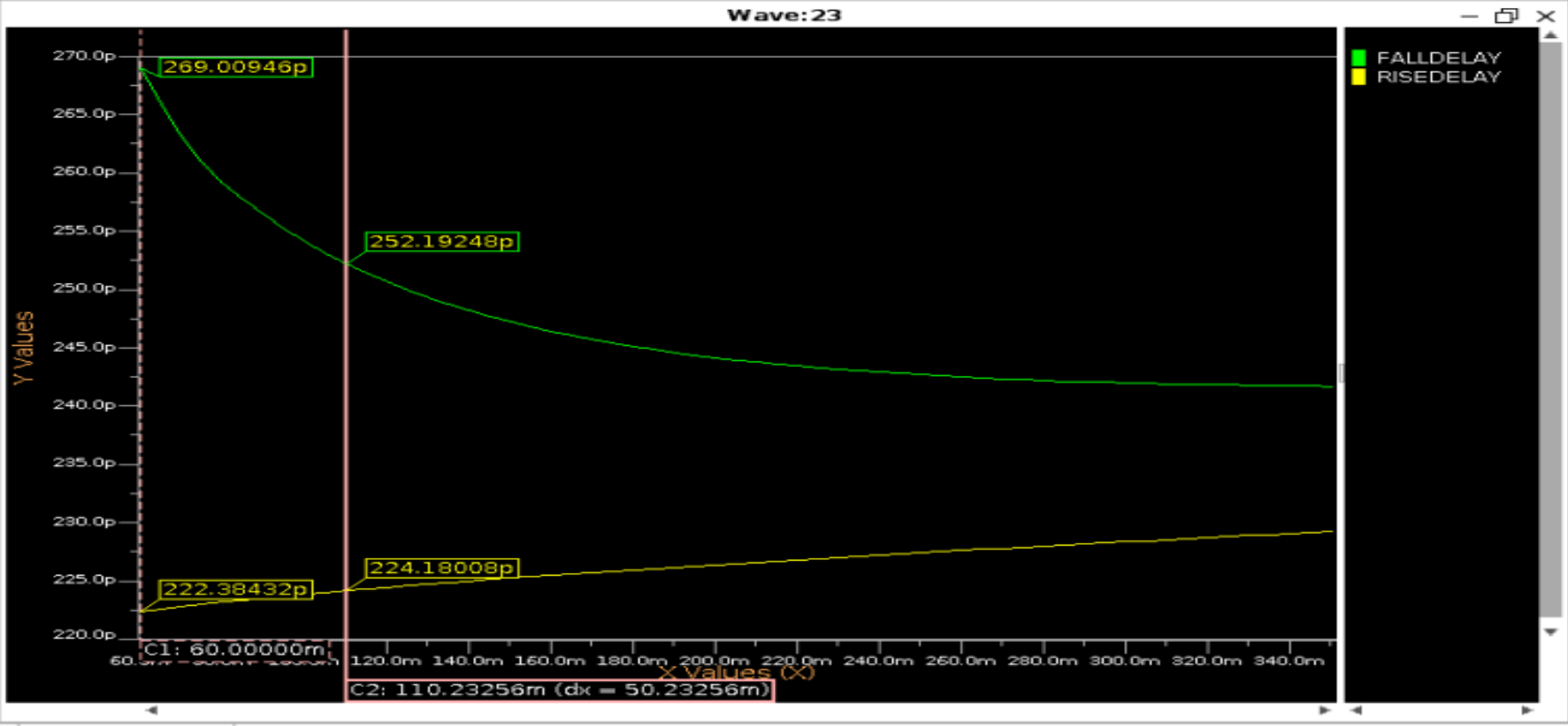
Parameters / Length	L=0.06	L=0.07	L=0.08	L=0.09	L=0.10	L=0.11	L=0.12	L=0.13	L=0.14	L=0.15
Fall Delay	2.69E-10	2.63E-10	2.59E-10	2.56E-10	2.54E-10	2.52E-10	2.51E-10	2.49E-10	2.48E-10	2.47E-10
Rise Delay	2.22E-10	2.23E-10	2.23E-10	2.24E-10	2.24E-10	2.24E-10	2.24E-10	2.25E-10	2.25E-10	2.25E-10

Initially:
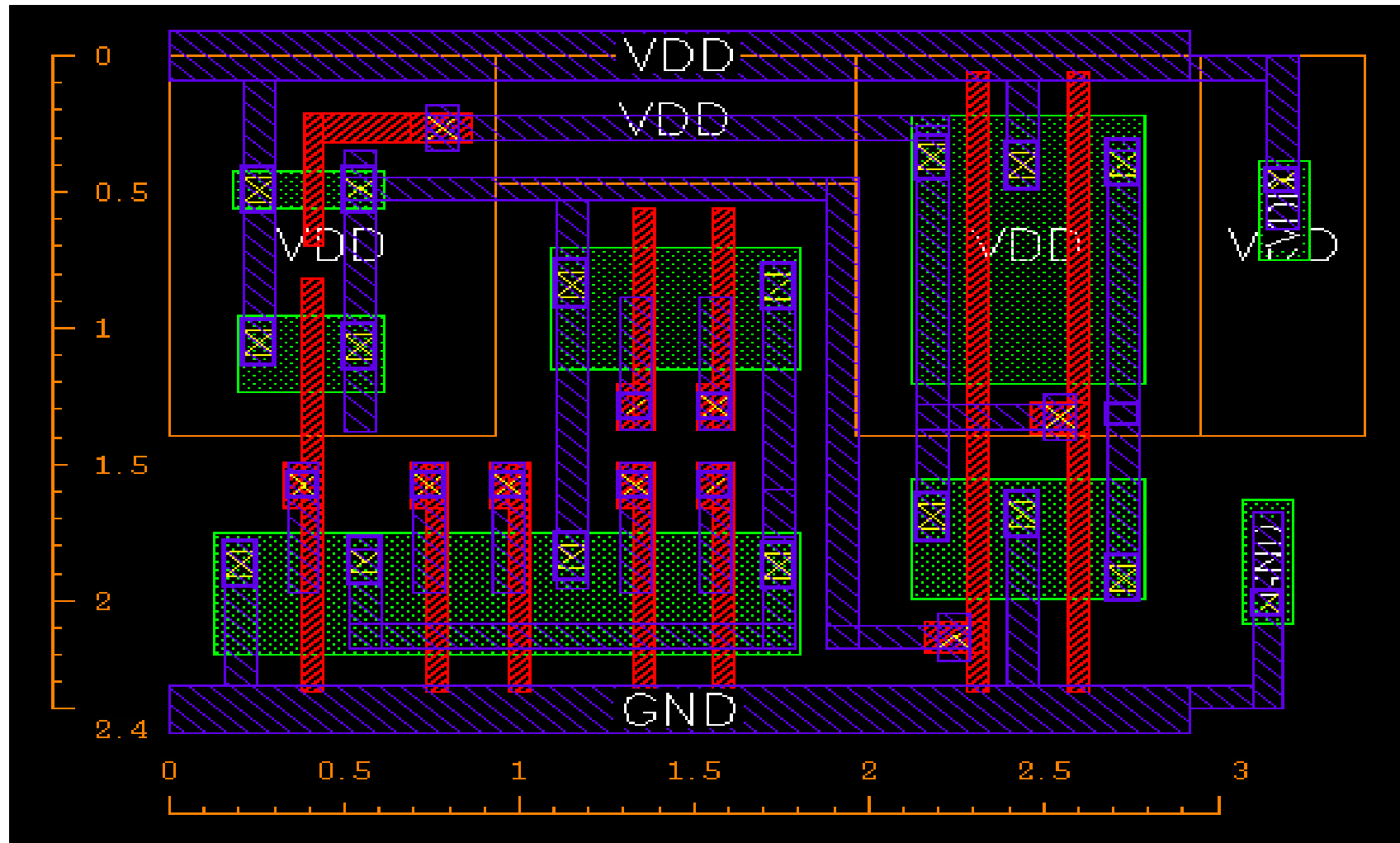
Layout Complex

Area=6.72μm^2.
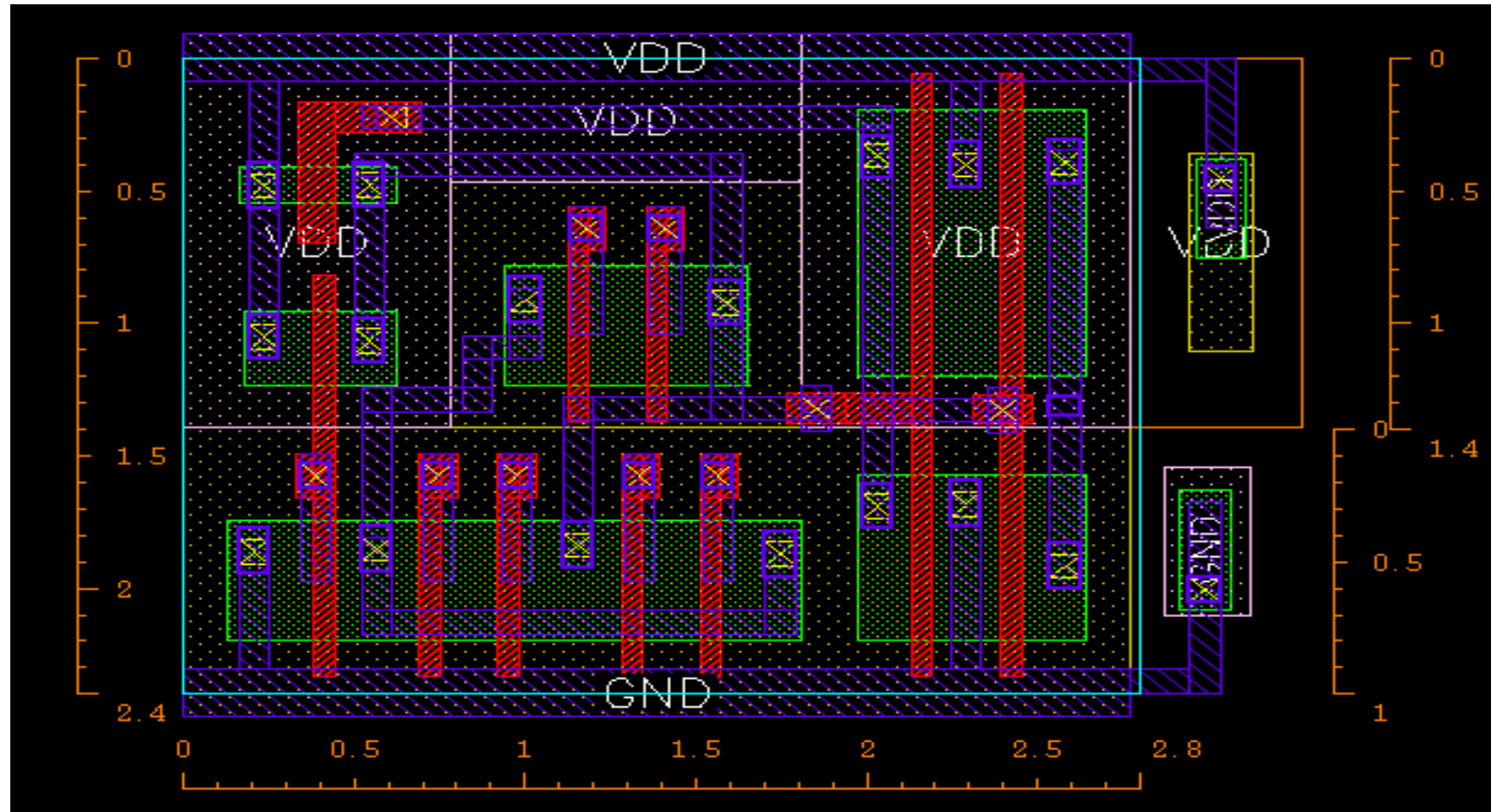
Layout without PP and NP

DRC, LVS clean and PEX Results of Complex Logic

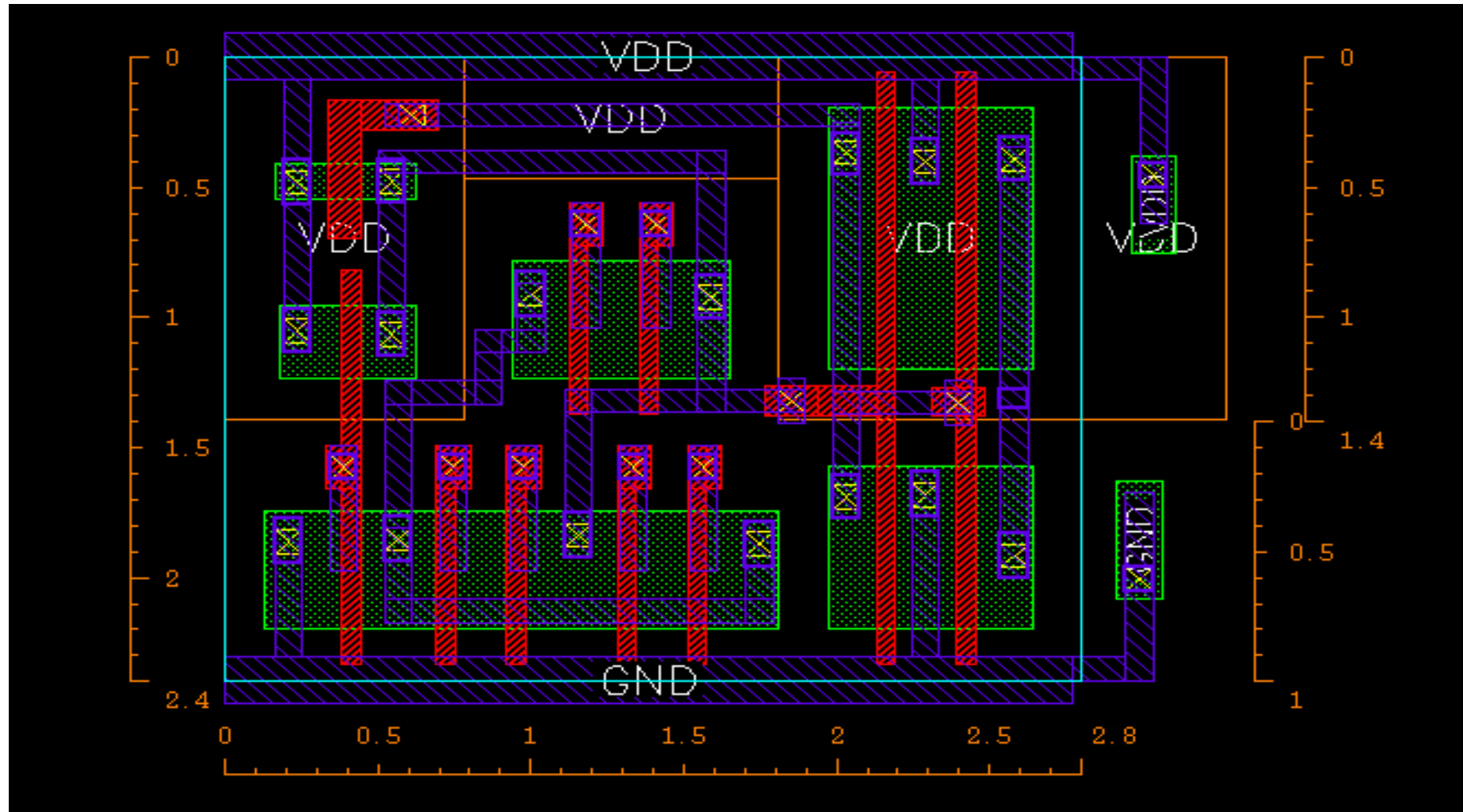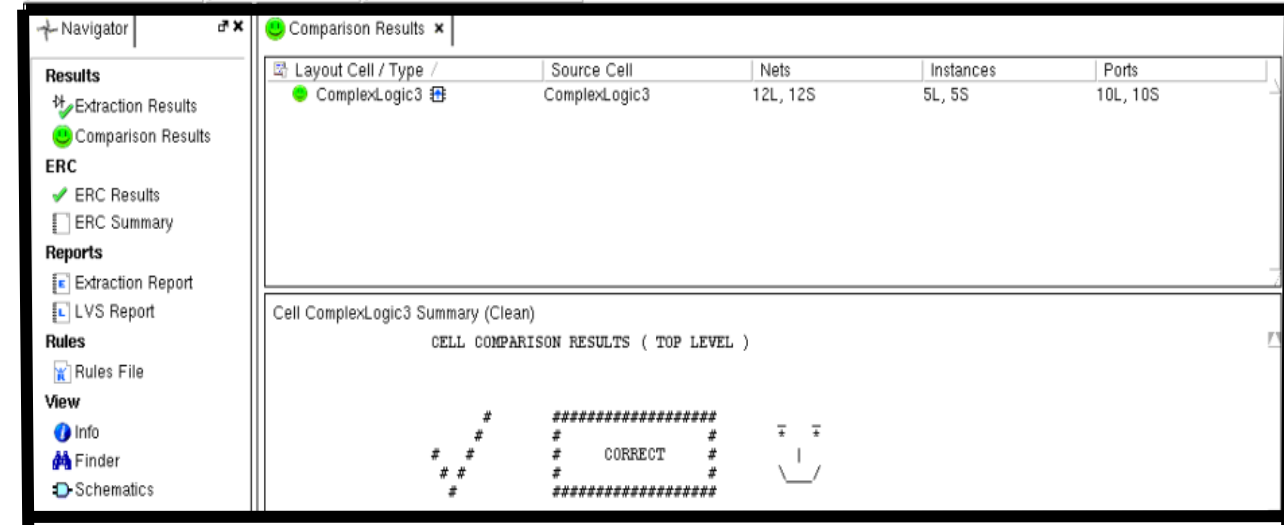| No.	Layout Net	Source Net	R Count	L Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	CLK	CLK	6	4	0.00000	3.00069E-16	3.00069E-16
2	2	net143	20	8	4.64544E-19	1.07597E-15	1.07643E-15
3	D	D	2	0	0.00000	2.46091E-16	2.46091E-16
4	C	C	2	0	0.00000	2.33875E-16	2.33875E-16
5	B	B	2	0	0.00000	2.10607E-16	2.10607E-16
6	E	E	2	0	0.00000	2.47464E-16	2.47464E-16
7	A	A	2	0	2.24340E-19	2.20548E-16	2.20773E-16
8	F	F	2	0	1.94653E-19	2.20271E-16	2.20466E-16
9	9	net140	25	10	5.30598E-20	1.10054E-15	1.10059E-15
10	10	net138	17	8	0.00000	5.92712E-16	5.92712E-16
11	OUT	OUT	4	2	2.18629E-20	2.65772E-16	2.65793E-16
12	GND	GND	15	0	3.28588E-19	8.35222E-16	8.35551E-16
13	VDD	VDD	16	0	1.81191E-19	8.45491E-16	8.45672E-16
14	40	net148	0	0	0.00000	8.89292E-18	8.89292E-18
15	41	net149	0	0	0.00000	3.44880E-18	3.44880E-18
16	42	net147	0	0	0.00000	8.86857E-18	8.86857E-18

Initially:
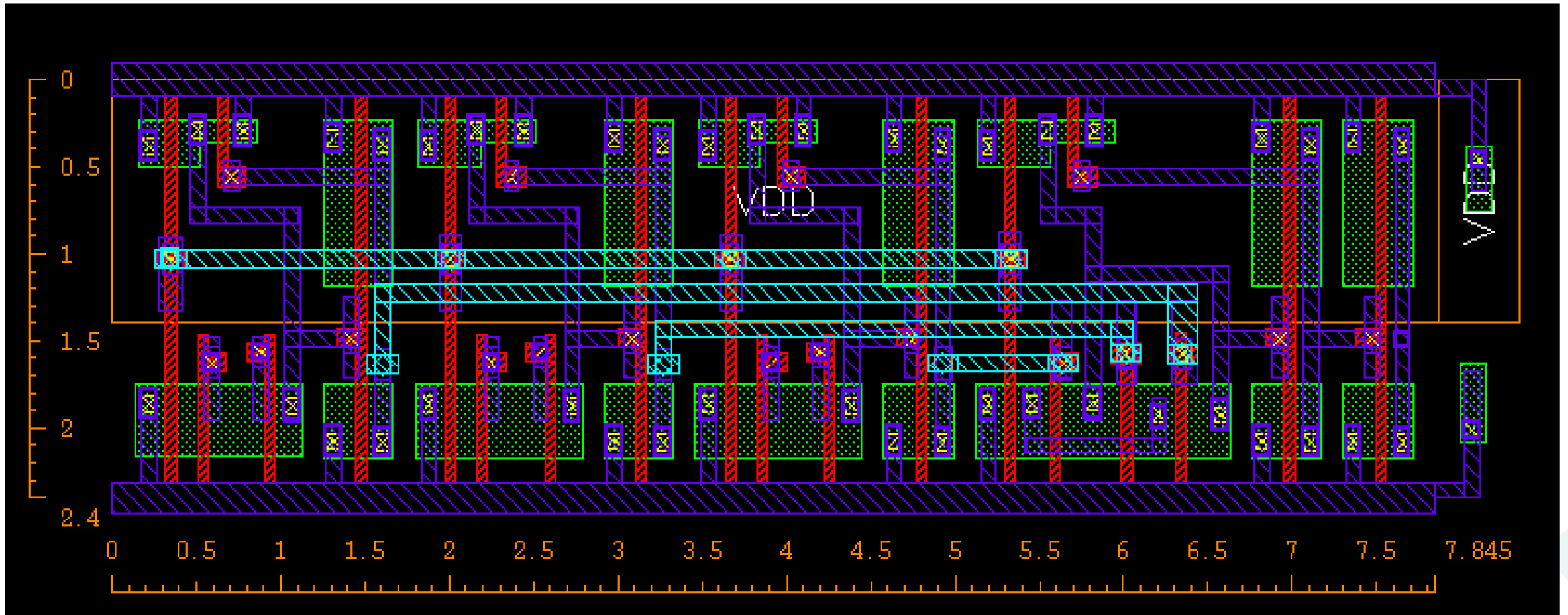
Non-Complex layout
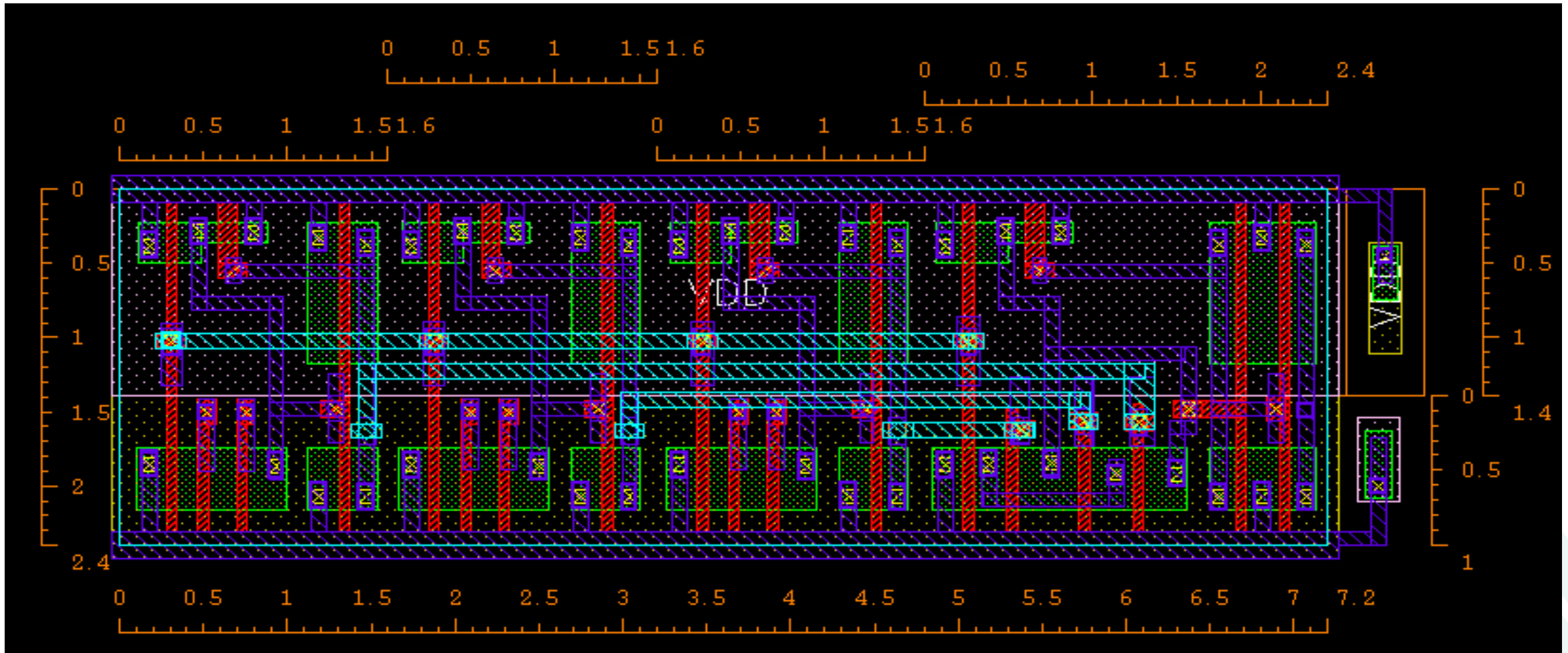
Area = 17.28 μm^2

Layout without PP and NP

DRC, LVS clean and PEX Results of Non-Complex Logic

Calibre - RVE v2020.3_38.22 : NonComplexLogic3.drc.results
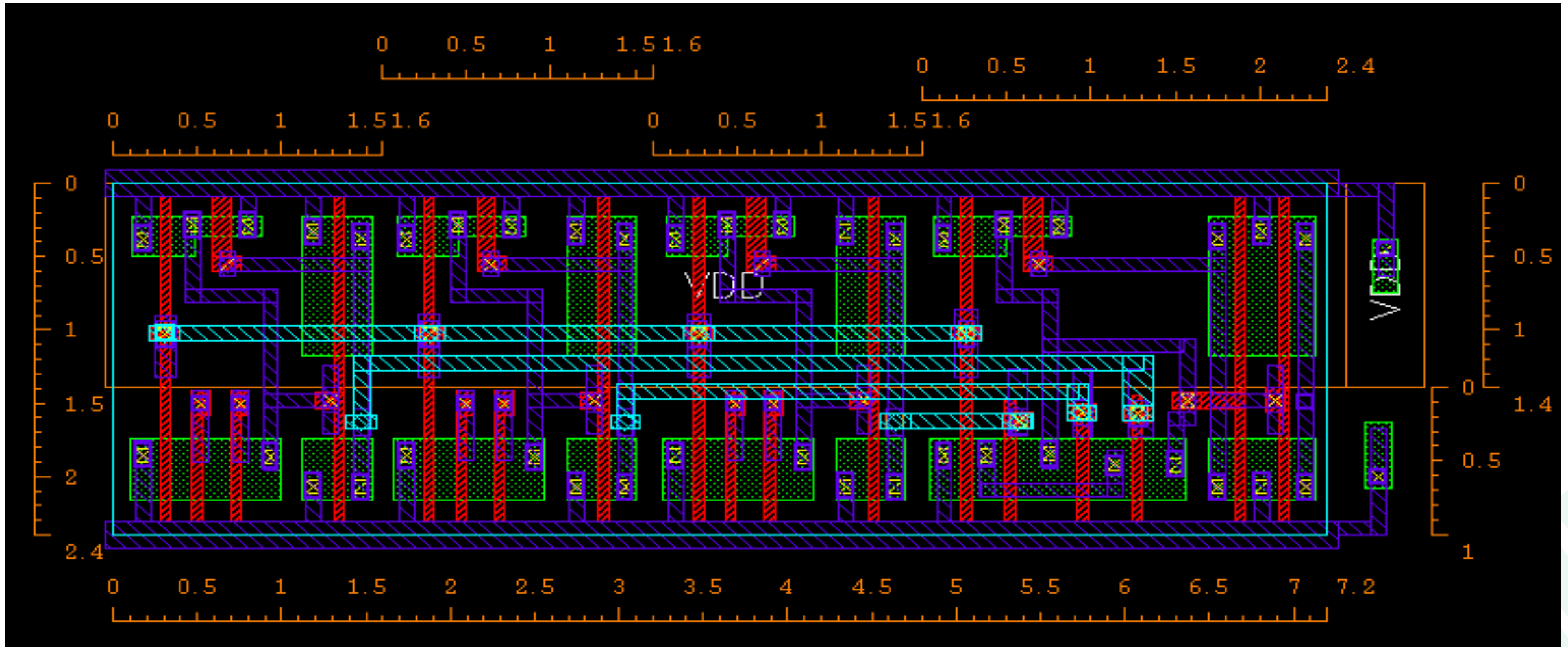
File View Highlight Tools Window Setup Help

Search

Filter: Show Unresolved   No Results Found

Check / Cell   Results

Navigator

Comparison Results

Results
- Extraction Results
- Comparison Results

ERC
- ERC Results
- ERC Summary

Reports
- Extraction Report
- LVS Report

Rules
- Rules File

View
- Info
- Finder
- Schematics

Setup

Layout Cell / Type	Source Cell	Nets	Instances	Ports
NonComplexLogic3	NonComplexLogic3	18L, 18S	17L, 17S	10L, 10S

Cell NonComplexLogic3 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

```
        #          ###################
        #          #                  #
  #  #  #          #      CORRECT      #
    # #  #         #                  #
        #          ###################
```

No.	Layout Net	Source Net	R Count	L Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	CLK	CLK	27	19	4.08640E-19	2.08626E-15	2.08667E-15
2	B	B	3	2	0.00000	2.02024E-16	2.02024E-16
3	3	net352	27	13	1.23768E-18	1.75514E-15	1.75638E-15
4	A	A	3	2	0.00000	2.19046E-16	2.19046E-16
5	5	net346	19	8	1.11809E-19	7.75315E-16	7.75427E-16
6	D	D	3	2	0.00000	2.03351E-16	2.03351E-16
7	7	net354	27	13	5.02563E-19	1.39737E-15	1.39788E-15
8	C	C	3	2	0.00000	2.17609E-16	2.17609E-16
9	9	net348	19	8	2.20953E-20	7.75862E-16	7.75884E-16
10	F	F	3	2	1.41978E-19	2.06243E-16	2.06385E-16
11	11	net353	21	9	7.49245E-19	1.00140E-15	1.00215E-15
12	E	E	3	2	1.41978E-19	2.19166E-16	2.19308E-16
13	13	net347	19	8	3.63401E-19	7.90630E-16	7.90993E-16
14	14	net361	24	11	8.61512E-19	9.37036E-16	9.37898E-16
15	15	net358	27	12	3.00064E-19	1.07031E-15	1.07061E-15
16	16	net356	7	3	3.20136E-20	3.26701E-16	3.26733E-16
17	OUT	OUT	4	2	4.15316E-19	3.08126E-16	3.08542E-16
18	GND	GND	51	0	4.31078E-19	2.04022E-16	2.04065E-16
19	VDD	VDD	73	0	1.16278E-18	2.94654E-15	2.94770E-15
20	71	net375	0	0	0.00000	2.60487E-18	2.60487E-18
21	73	net377	0	0	0.00000	2.50273E-18	2.50273E-18
22	75	net379	0	0	0.00000	2.50273E-18	2.50273E-18

SIMULATION RESULTS:

Conditions	Parameters	COMPLEX		NON-COMPLEX	
		PRE-Layout	POST-Layout	PRE-Layout	POST-Layout
Contamination Delay (Tcd) B,D,F = 1 & A,C,E = 0 → 1	FALL Delay	6.82E-11	6.93E-11	1.02E-10	1.08E-10
	RISE Delay	8.29E-11	8.75E-11	9.48E-11	1.00E-10
PVT - FF, 1.32, -40	Trise	6.47E-11	6.25E-11	6.48E-11	6.67E-11
	Tfall	4.74E-11	4.84E-11	7.05E-11	7.21E-11
Propagation Delay (Tpd) D,F = 0 , A,C,E = 1 , B = 0 → 1	FALL Delay	2.52E-10	2.41E-10	3.16E-10	3.30E-10
	RISE Delay	2.24E-10	2.24E-10	2.51E-10	2.71E-10
PVT - SS, 1.08, 125	Trise	1.42E-10	1.43E-10	1.55E-10	1.45E-10
	Tfall	1.25E-10	1.16E-10	1.67E-10	1.75E-10
PVT - FF, 1.32, 125	ILEAK(Pre-Charge)	7.99E-08	8.66E-08	1.98E-07	2.30E-07
	ILEAK(Evaluate)	1.43E-07	1.68E-07	1.89E-07	2.27E-07
PVT – TT, 1.2, 25	Pstatic	2.79E-09	4.05E-10	1.94E-08	5.16E-08
	Pdynamic	1.11E-06	1.12E-06	1.66E-06	1.79E-06

CONCLUSION

- Area of the layout is optimized by :-

  1. Sharing the diffusion layers wherever possible.

  2. Removing the metal layer running vertically by adjusting the stick diagram.

  3. Keeping minimum DRC between Poly to Poly by placing vias vertically and making vertical contact pins.

- Improved overall Delay performance of our design by increasing Keeper length to an optimum value of L=110nm.

- It is observed that the delays for Complex logic are less than that of Non-Complex logic and similar trend is followed in both Pre layout and Post layout.

- The propagation delay for Complex logic is observed to be better after PEX.

- Area and power consumed are lesser in Complex logic implementation as compared to Non-Complex logic implementation.