Replica Column for Write

ECE-611 (Memory Design and Test)

Aakash Gupta (MT21150)

Neeraj (MT21156)

Prapti Makkar (MT21202)

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Problem Statement

SPECIFICATIONS

- 6 sigma qualification
- Layout should be as close to the real SRAM cell layout.
- no change in the active layer, minimal change in the poly layer.
- no change in the internal contacts.

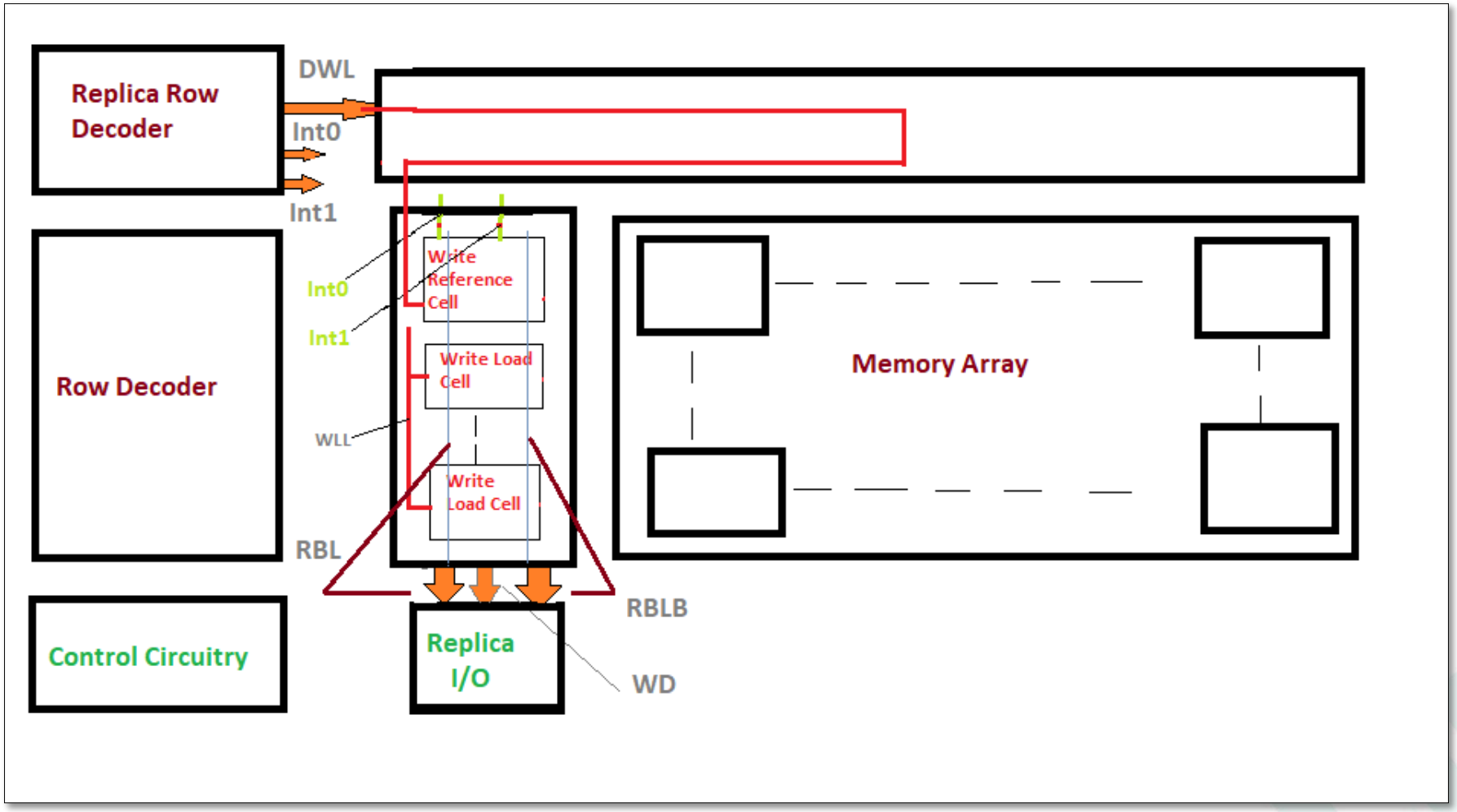
UNDERSTANDING FROM PROBLEM STATEMENT

The replica column provides the worst case delay for the write operation to complete. So, we have to use the same 6T SRAM Bitcell as used by the 6T SRAM Bitcell array team and then performed the six sigma qualification for the same to ensure that the worst case cell delay(six sigma) in the actual 6T SRAM Bitcell array should be less than the time required for generating the write detect signal in replica column in addition with the minimum time required to reset WL and to switch off the Write Driver.

Challenges

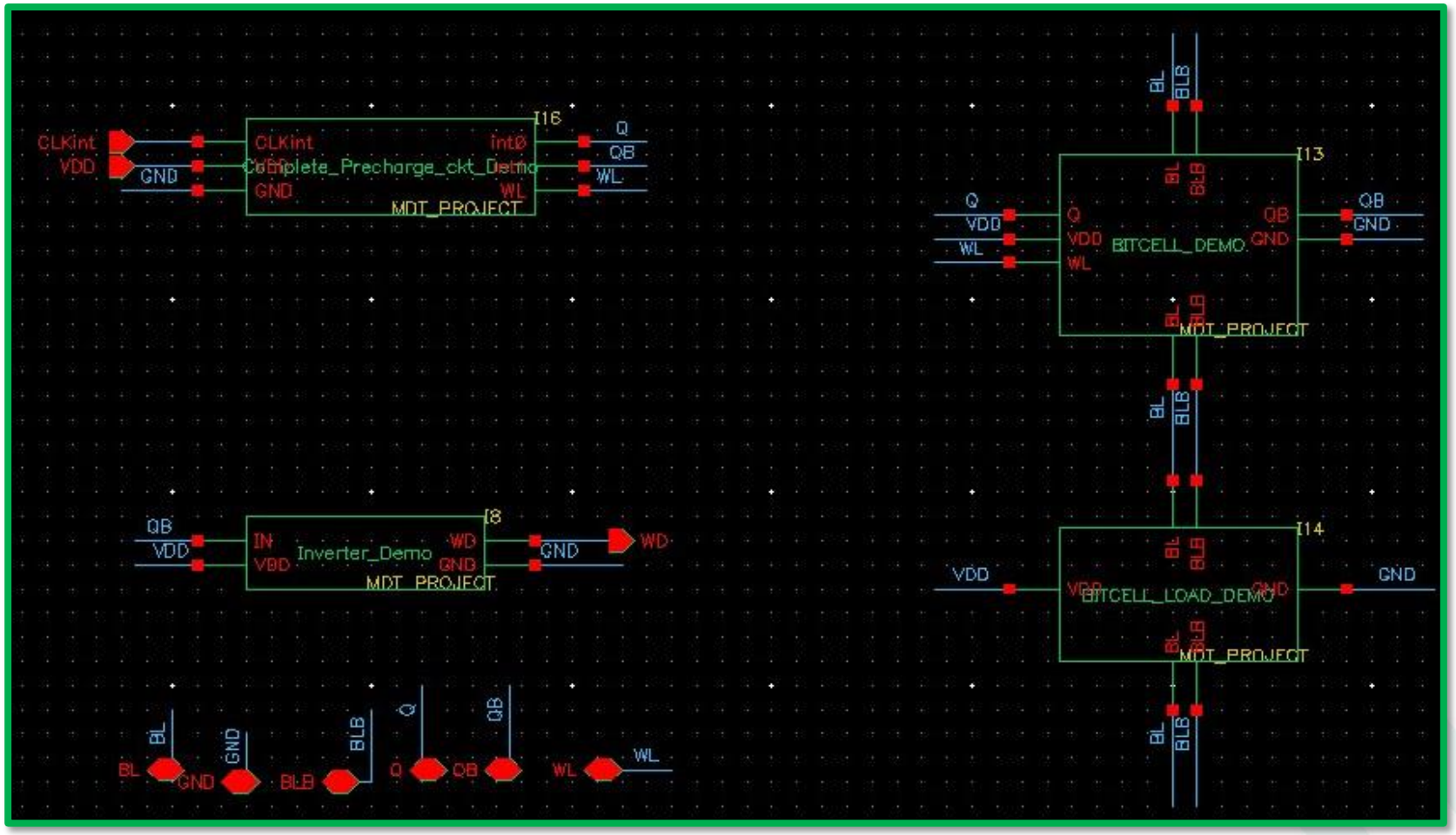
- Routing in the layout for connections of the signals from different circuits.
- softchk and supply abort errors in LVS.
- Strap cells realization after fixed intervals.
- Manual repetition of the bitcells to make column.
- Shorting of word lines in the discharge cells.
- Sizing changed multiples times after getting different constraints with with teams.

Design Schematic (1)



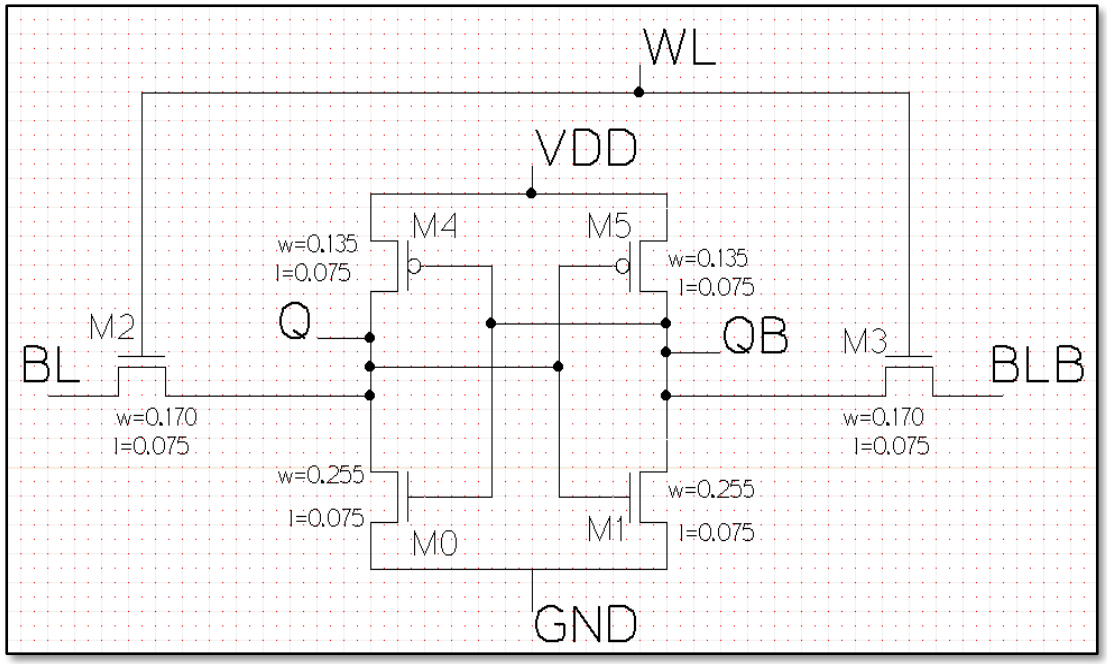
Top Level Architecture

Design Schematic (2)

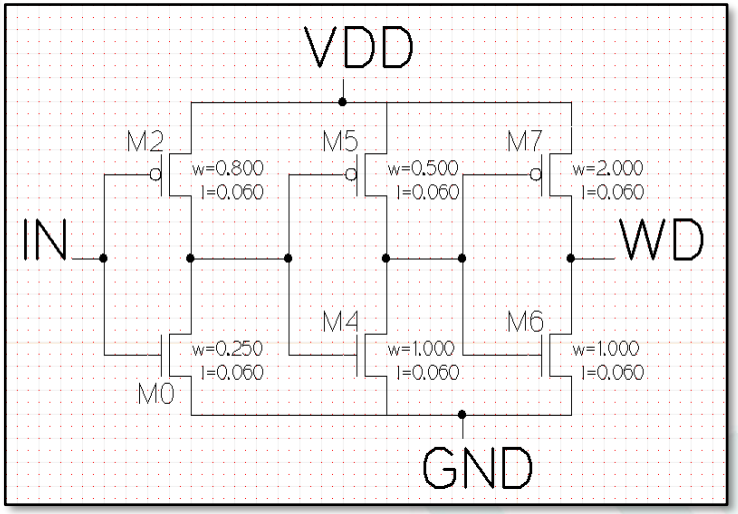


[Complete schematic symbol view]

Design Schematic (3)

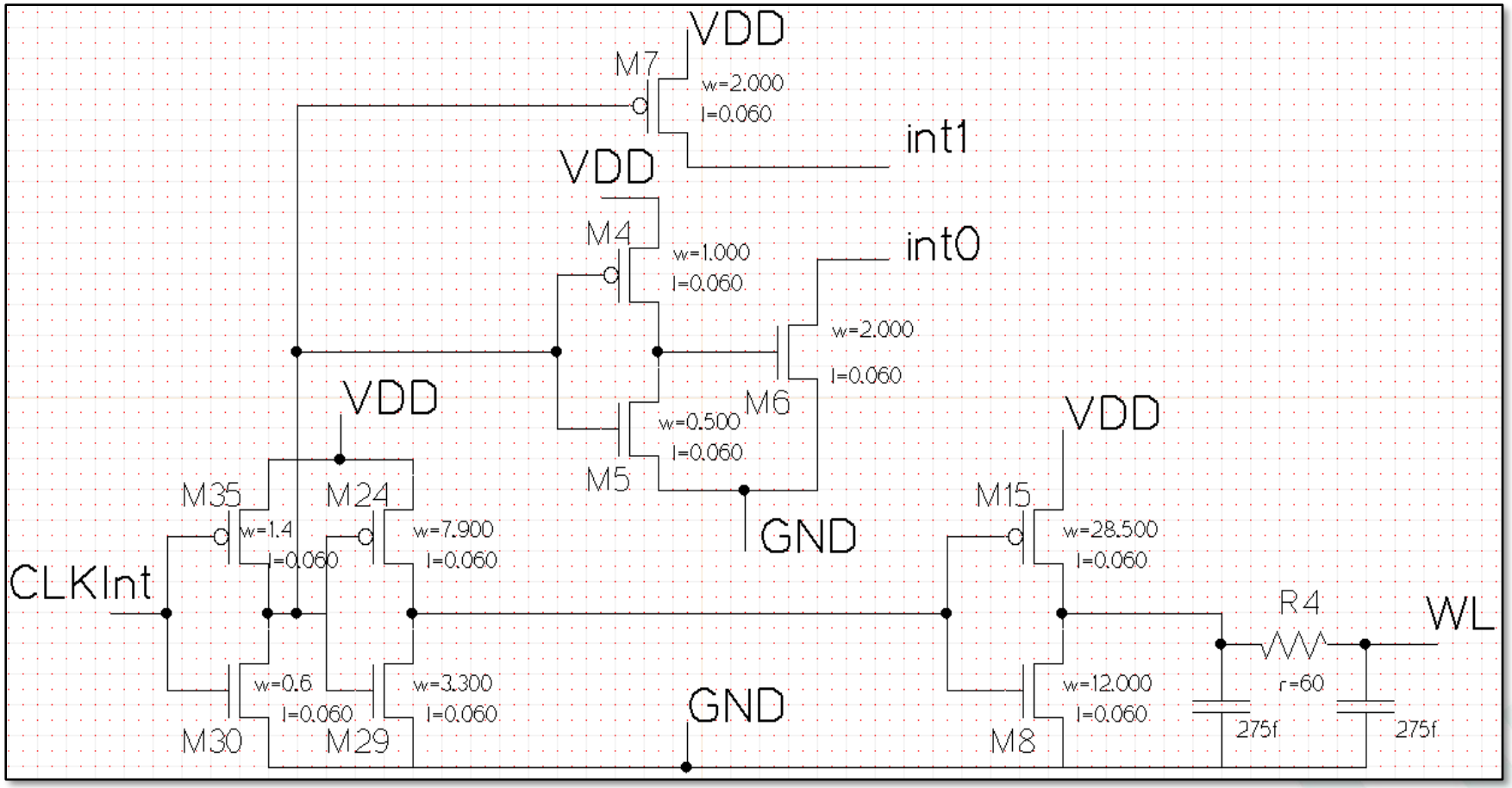


6T SRAM Bitcell schematic (Reference cell)



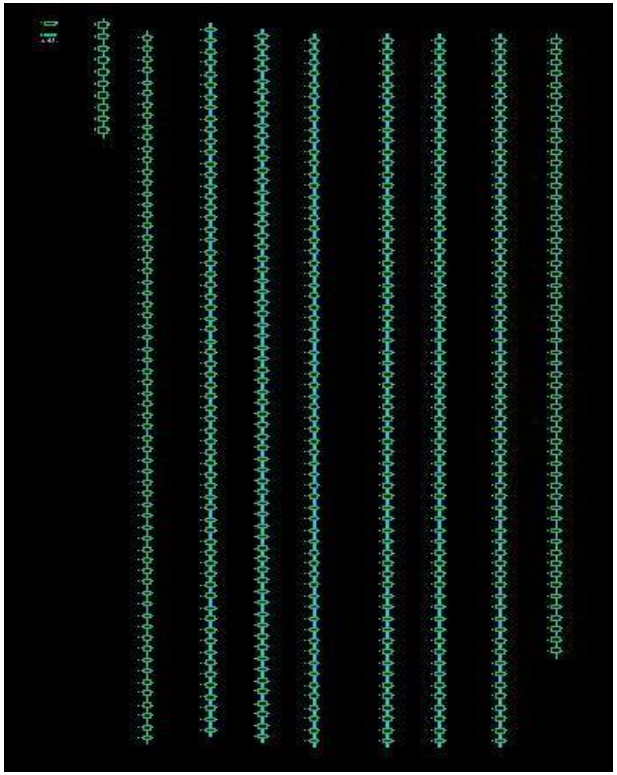
Write Detect (WD) signal generation circuit

Design Schematic (4)



Dummy WL generation and internal nodes precharge circuit

Design Schematic (5)



Complete schematic symbol view (with 512 bitcell column)

PU	PD	PG
W= 0.135 L= 0 .075	W= 0.255 L= 0.075	W= 0.170 L= 0.075

Instance Name	Width	Length
For Precharge Circuit		
M4	1.000	0.060
M5	0.500	0.060
M7	2.000	0.060
M8	12.000	0.060
M15	28.500	0.060
M24	7.900	0.060
M29	3.300	0.060
M30	0.600	0.060
M35	1.400	0.060
For Write Detect Circuit		
M0	0.250	0.060
M2	0.800	0.060
M4	1.000	0.060
M5	0.500	0.060
M6	1.000	0.060
M7	2.000	0.060

Verification Plan (1)

- **PVT:** We are using the PVT condition SS,1.08,125C which is the worst case PVT for the delays.
- **STIMULI:**

STIMULI	Rise Time	Fall Time	ON Time/Time Period	Delays
CLKint	80ps	50ps	370ps/1ns	CLK to CLKint = 130ps
WL	196ps	202ps	430ps/1ns	CLKint to WL = 257ps
BLB	100ps	100ps	400ps/1ns	CLKint to BLB = 150ps
BL	DC supply (precharged to SUPPLY voltage)			

Verification Plan (2)

- **Results need to measure:** We have to generate a write detect signal and measure the following delays to satisfy the constraint shown.

$$t_{WC} < t_{WD} + \min(t_{WL,reset}, t_{WD,reset})$$ **(Desired Result)**

where,

t_{WC} : CLKint to Worst case cell delay

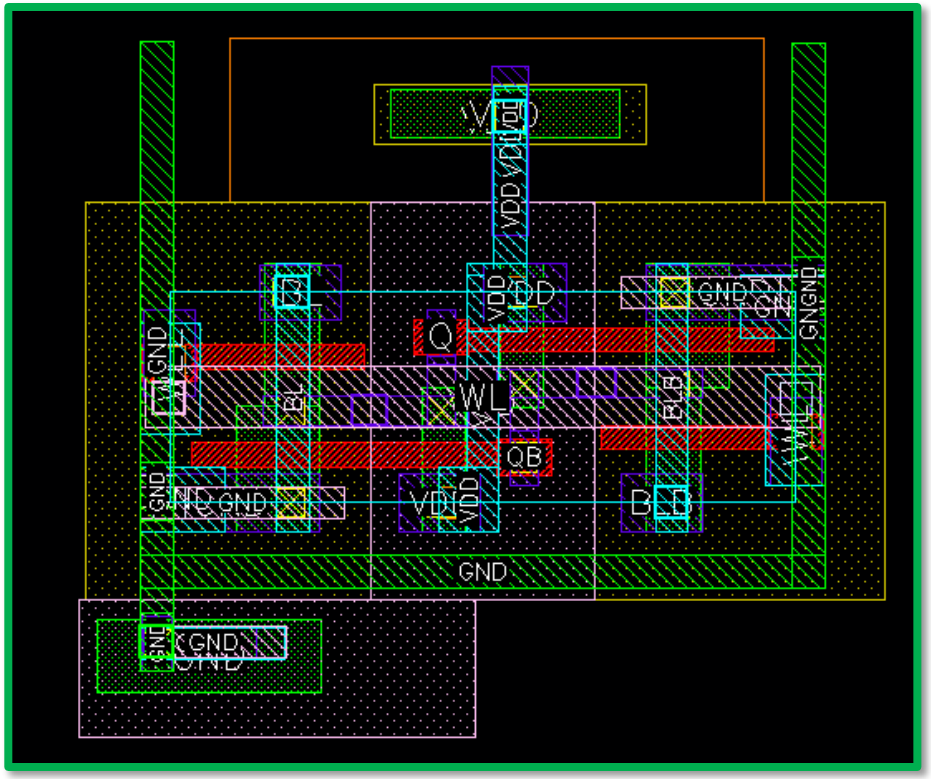
t_{WD} : CLKint to WD delay

$t_{WL,reset}$: WD to WL OFF delay

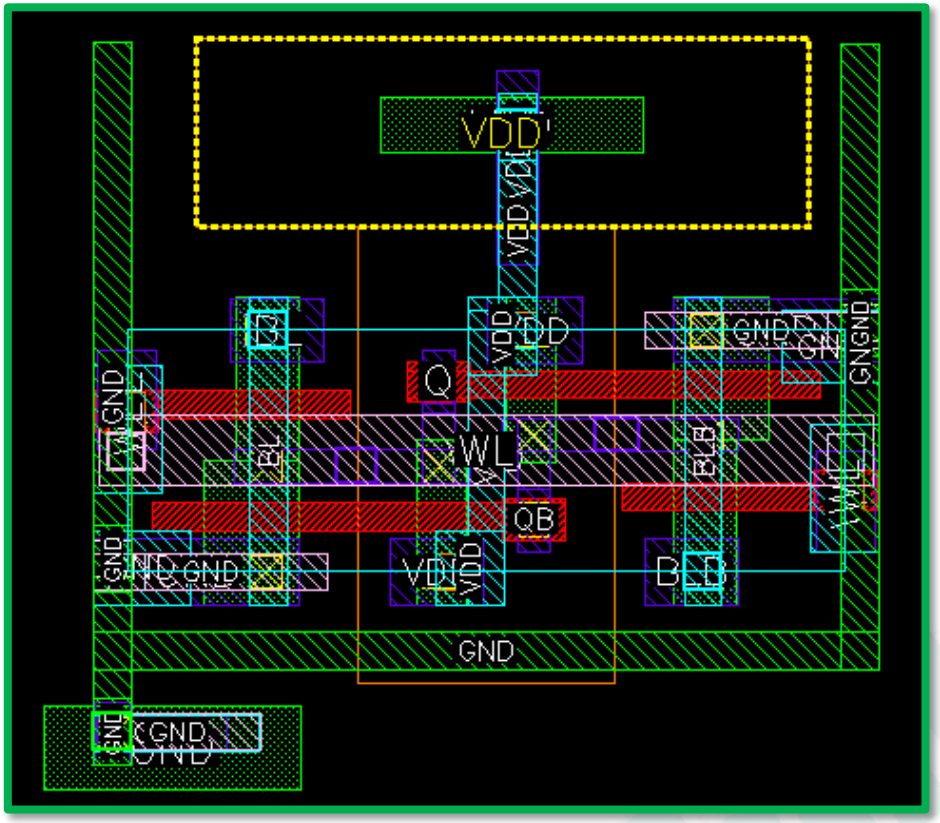
$t_{WD,reset}$: WD to Write Driver OFF delay

- **Modifications done for achieving specifications:**
  - 1st parameters that we have used is the discharged cell in the replica Column.
  - Initially we were using 4 discharge cells but then we increase it to 8 in order to decrease CLKint to WD delay.
  - With the above optimizations the size of the precharge circuit also got changed.

LAYOUT (1)

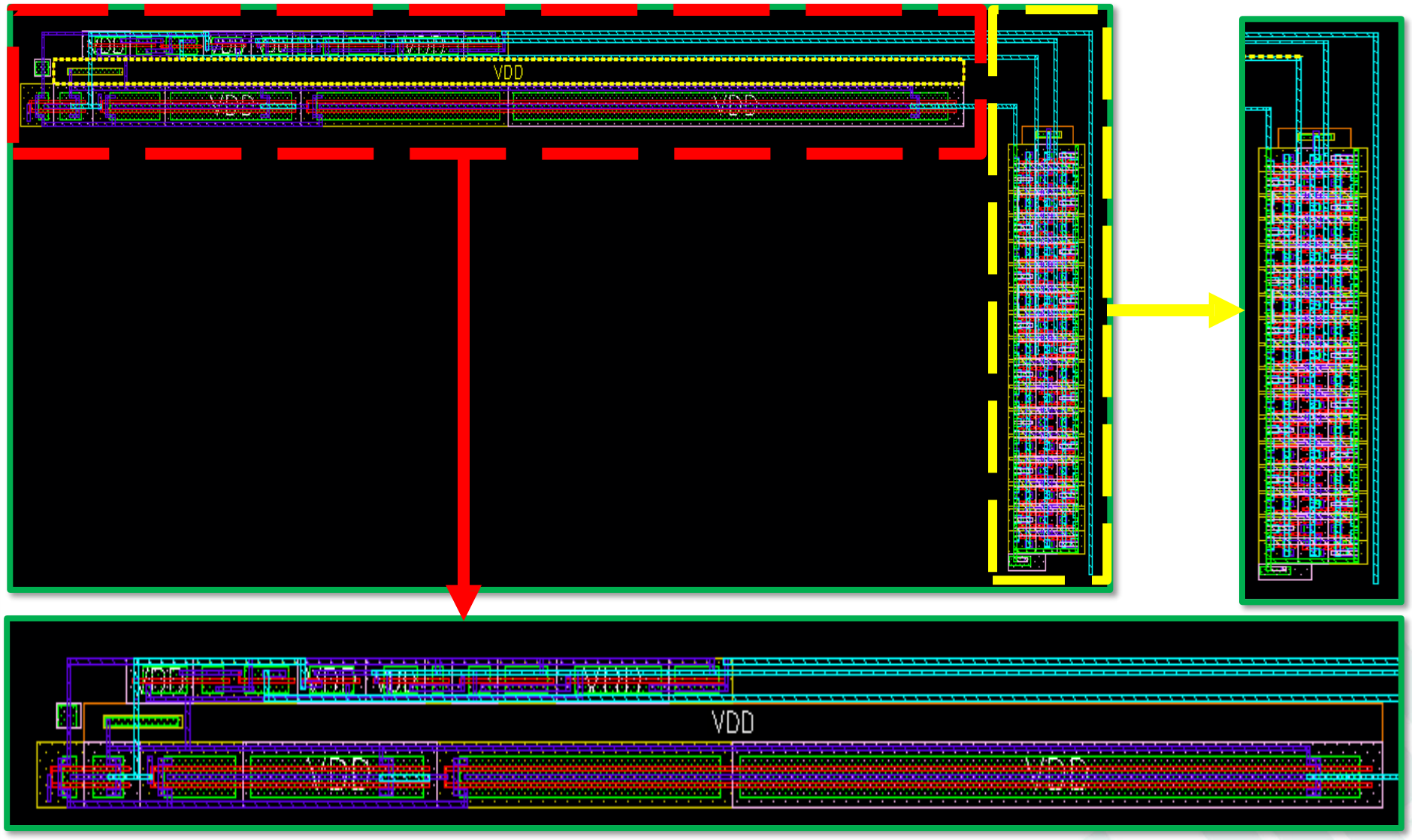


6T SRAM Bitcell (Reference cell)



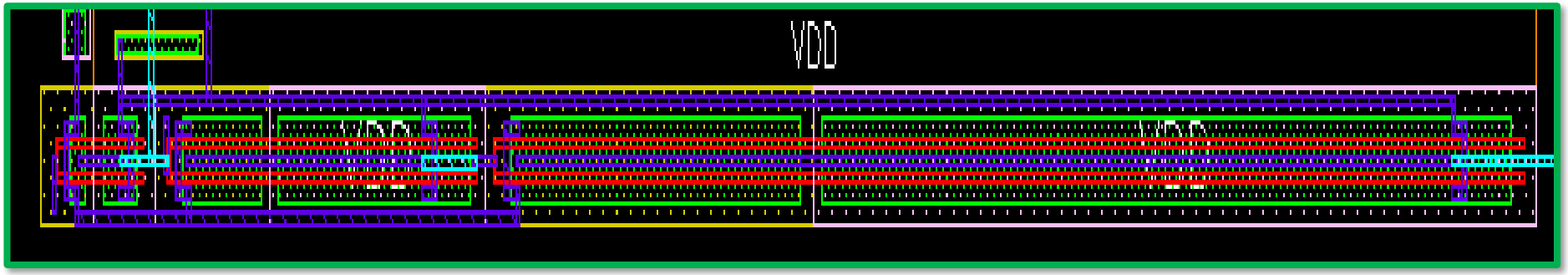
6T SRAM Bitcell (Reference cell) without PP and NP layer

LAYOUT (2)

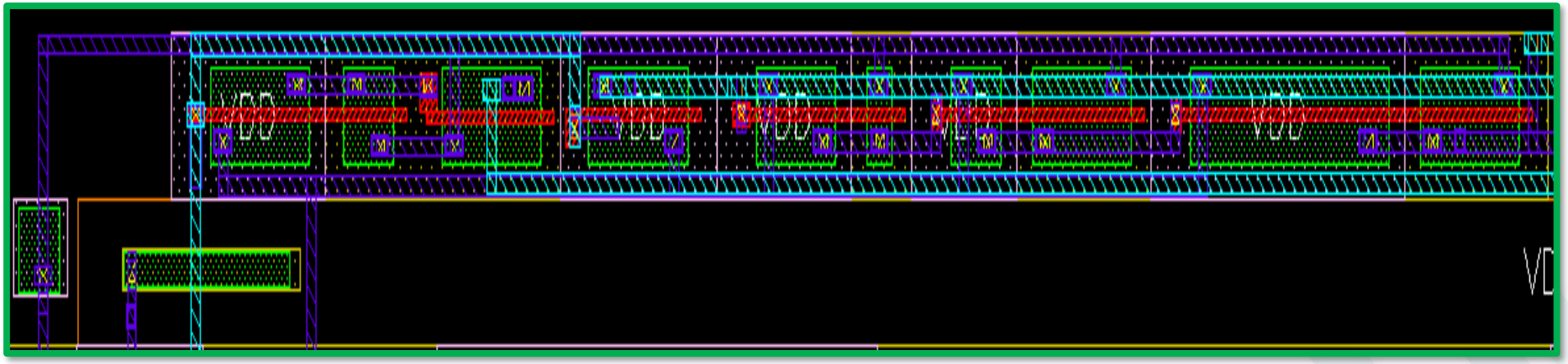


Complete Layout with 8 discharge cells and 8 load cells

LAYOUT (3)

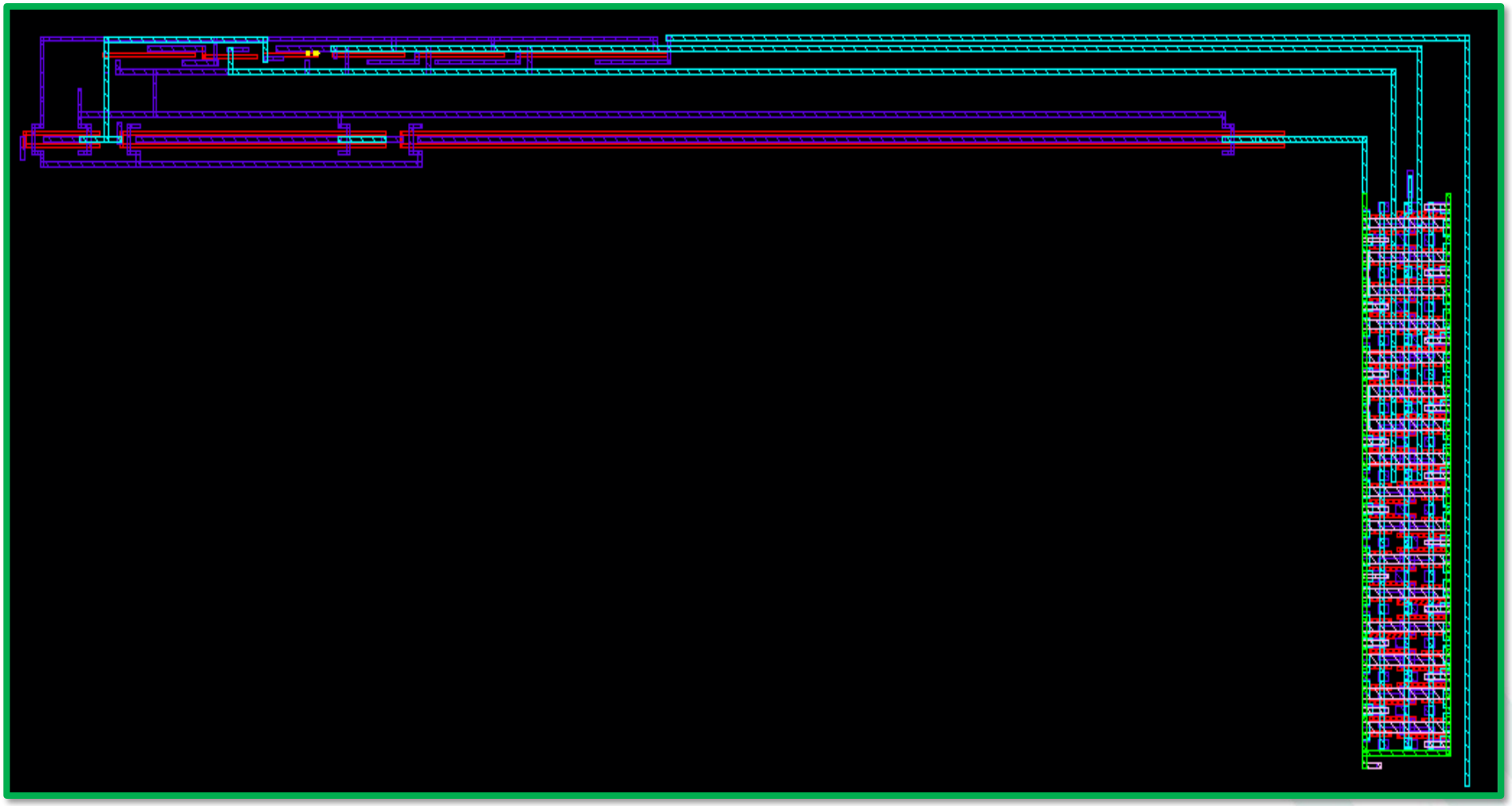


Zoomed in view of the Dummy WordLine Generation Circuit



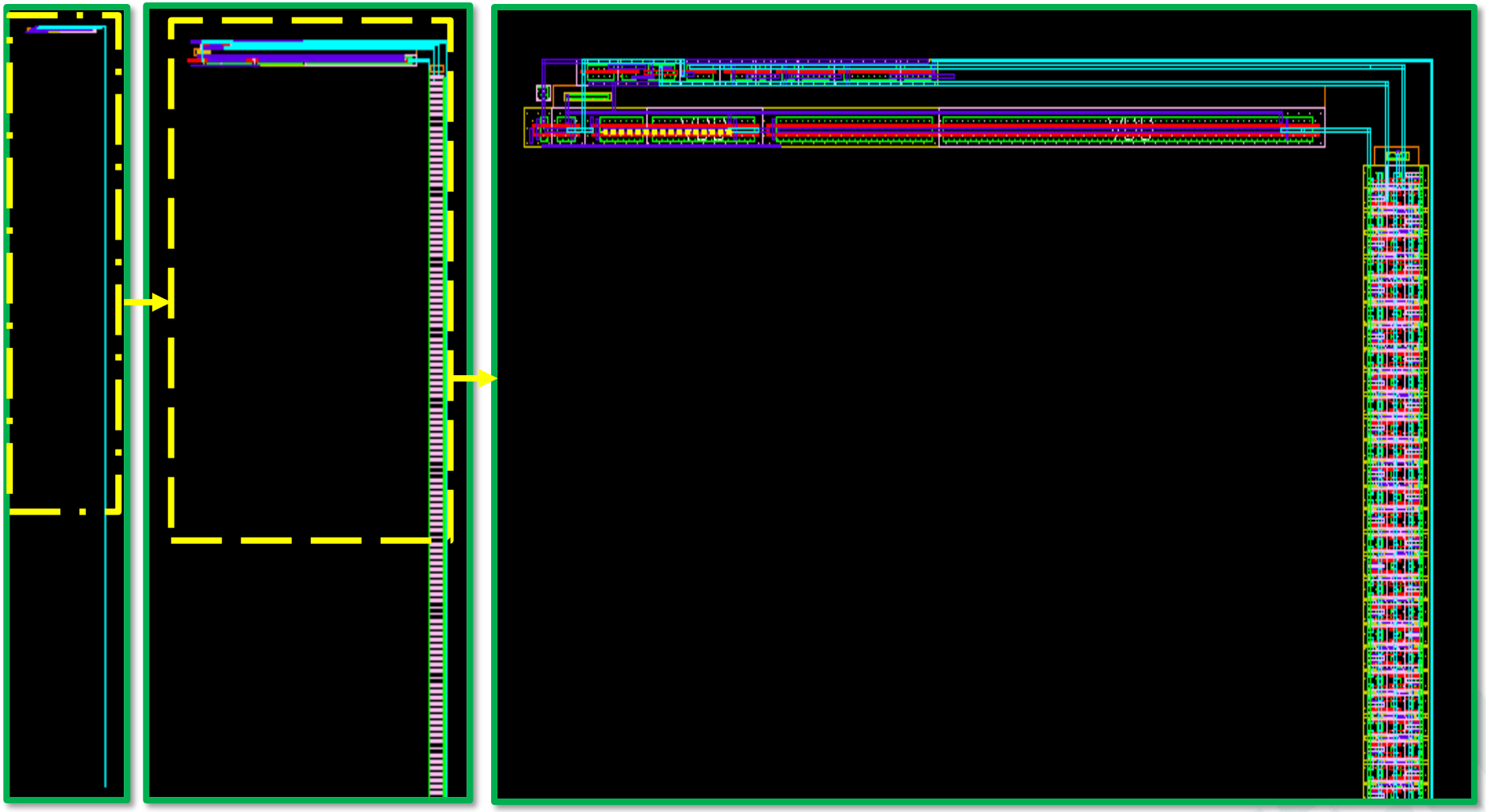
Zoomed in view of the Internal nodes Precharge Circuit along with Write Detect Signal Generation circuit

LAYOUT (4)



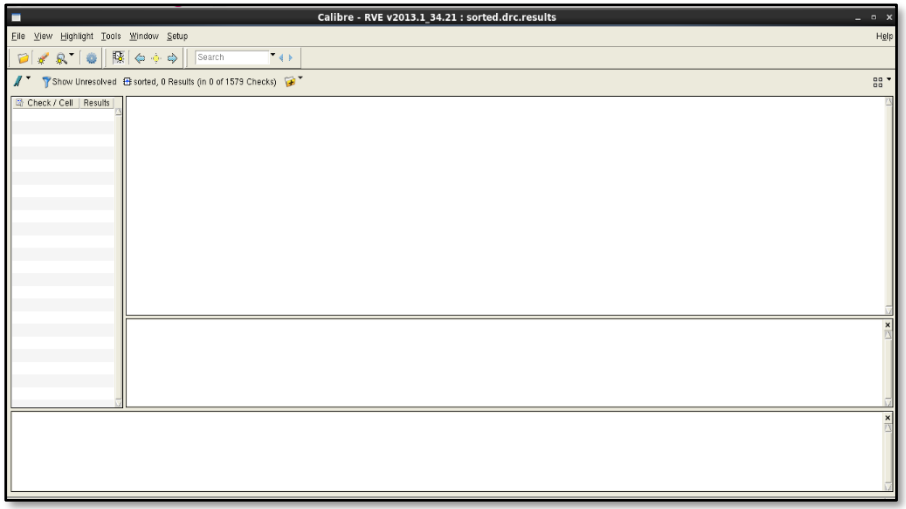
Complete Layout with 8 discharge cells and 8 load cells without PP and NP layers

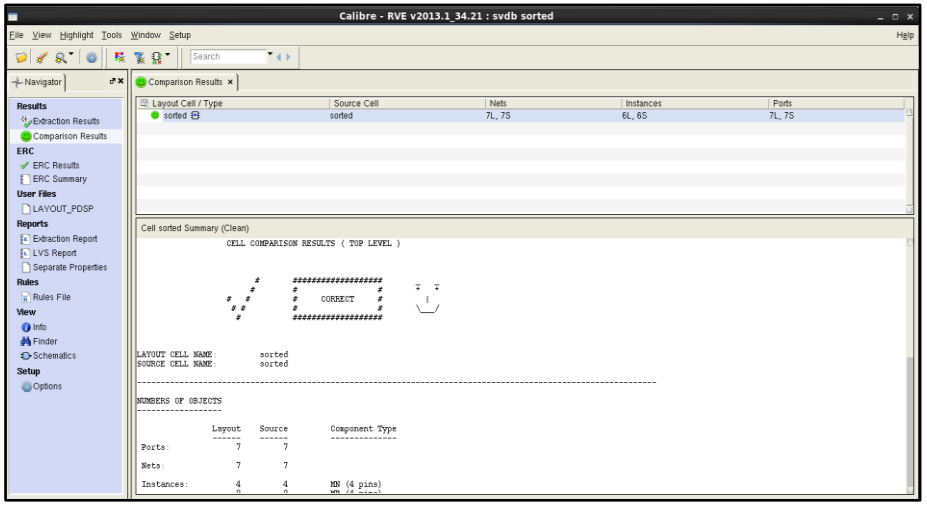
LAYOUT (5)



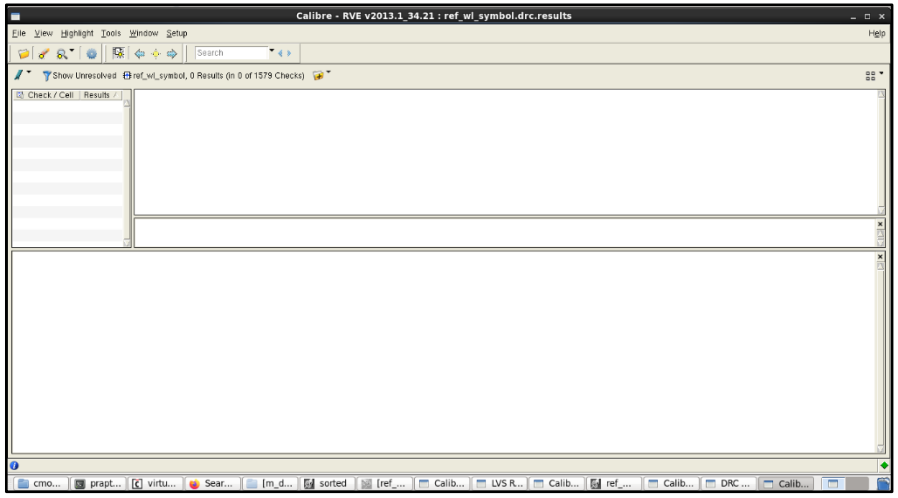
Complete Layout with 8 discharge cells and 504 load cells i.e a total of 512 cells

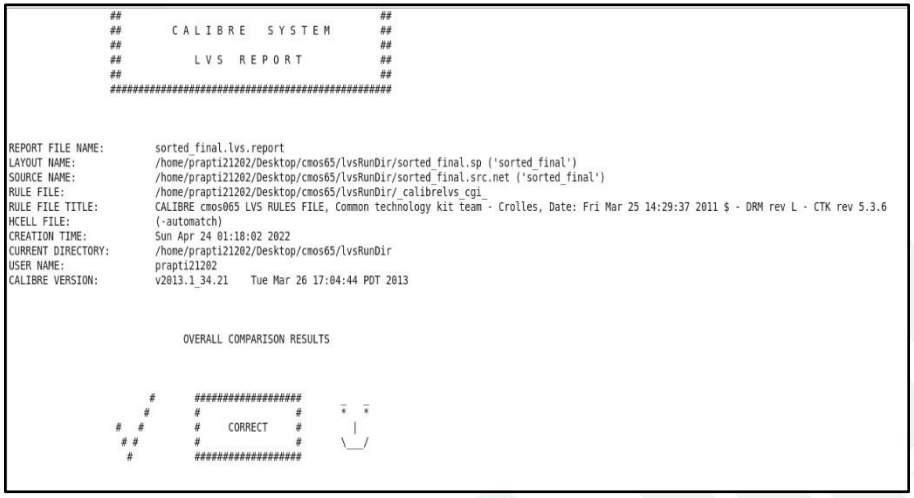
DRC & LVS Clean Results





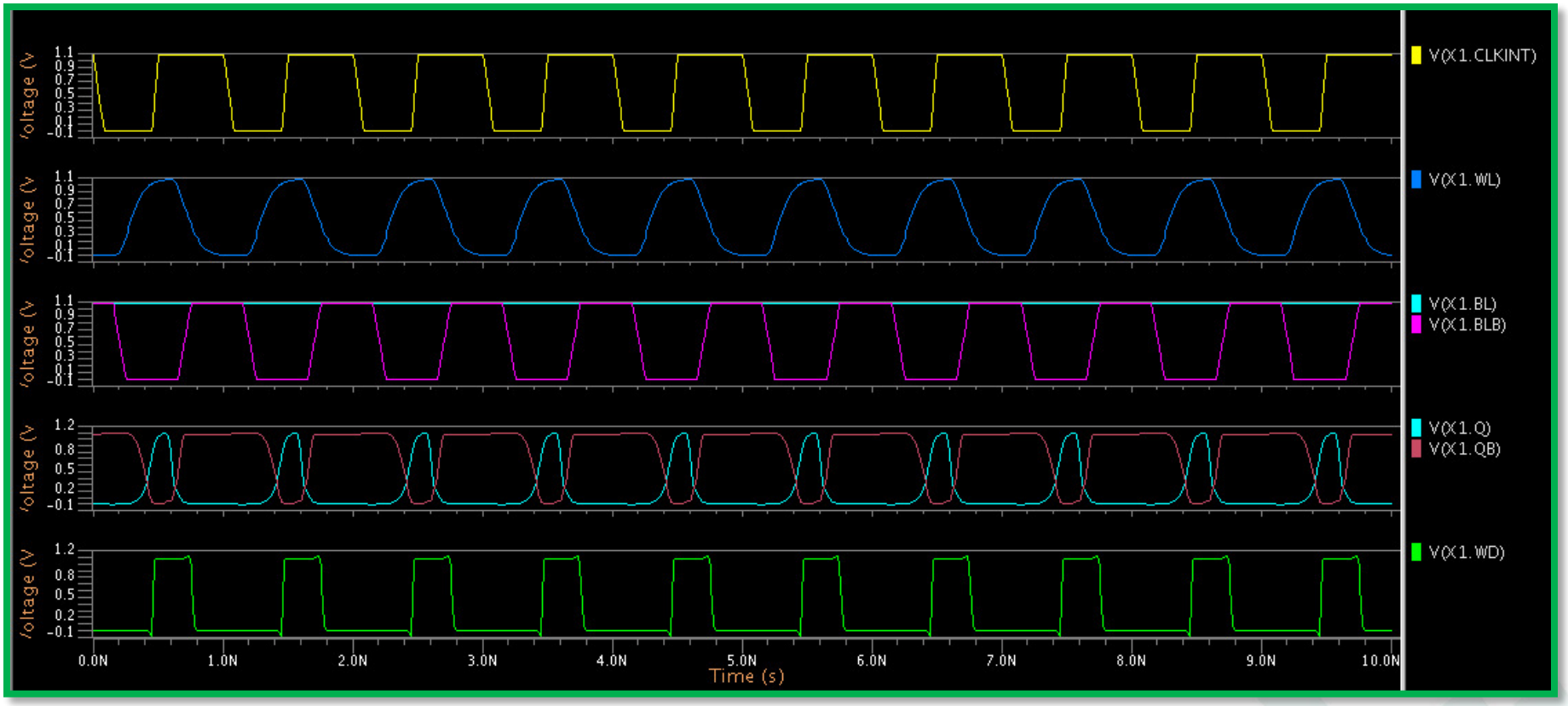
DRC & LVS Results of 6T SRAM Bitcell (Reference cell)





DRC & LVS Results of Complete Layout

RESULTS (1)

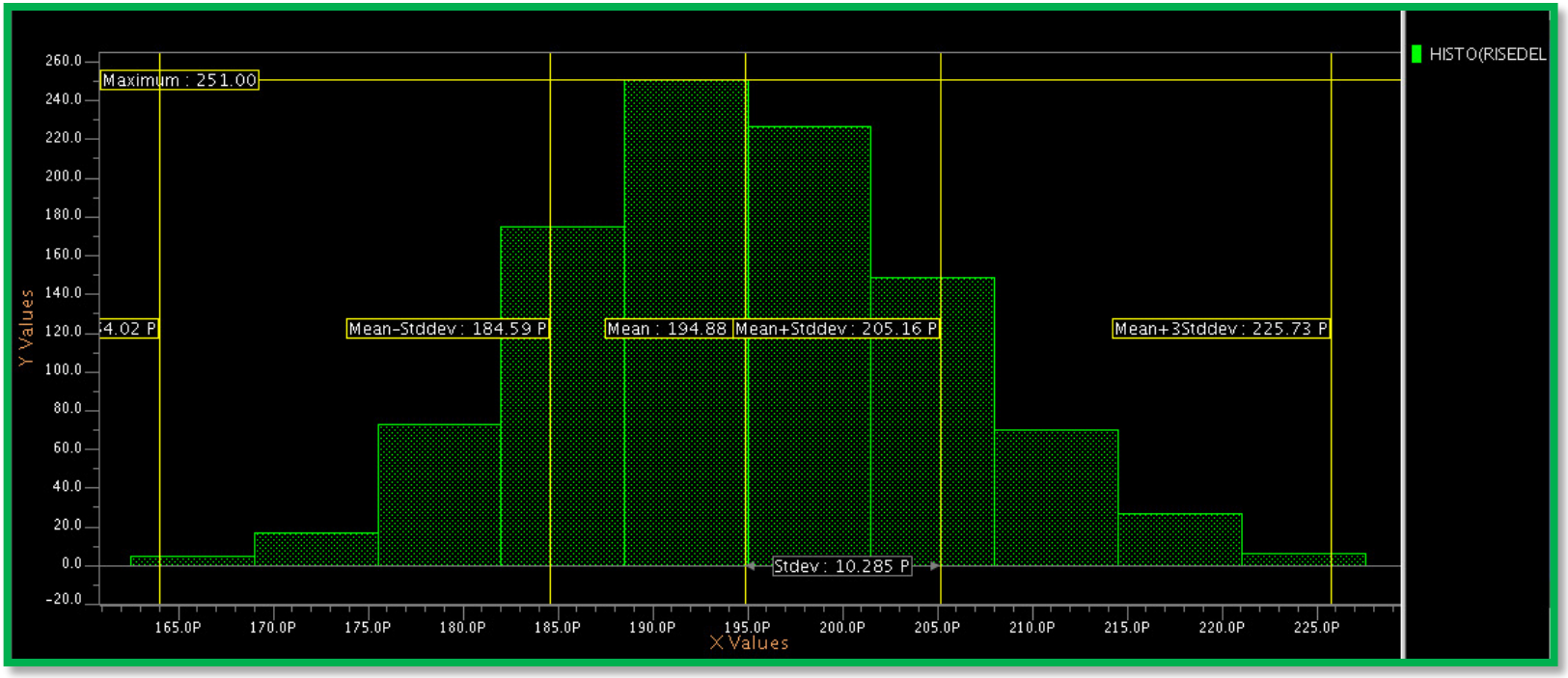


Waveforms after applying stimuli for verifying the functionality of the circuit

(Keeping 8 discharge cells and 504 Load cells)

RESULTS (2)

WL to worst case cell delay : 194ps



Monte Carlo results for worst case cell delay (WL to Q):

Mean = 194.88ps

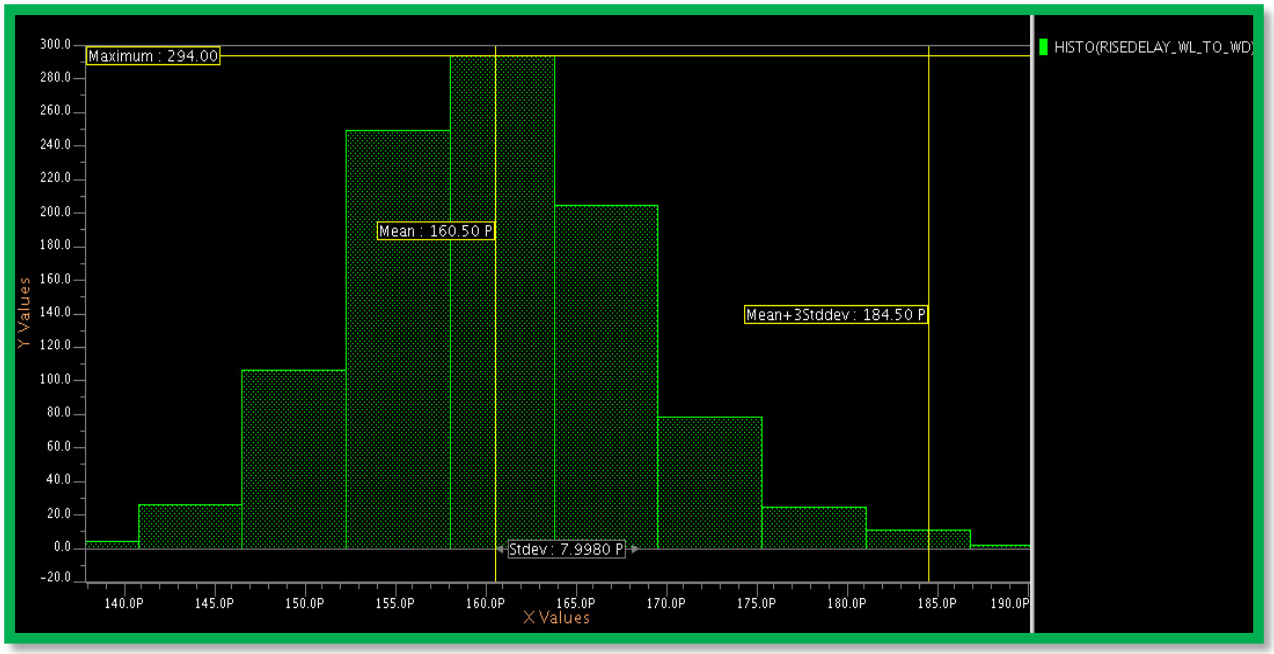
Sigma = 10.285ps

Mean + 6*Sigma = 256.59ps

Determined at SS, 125, 1.08

RESULTS (3)

WL to WD delay : 160ps (for 8 discharging cells)



Monte Carlo results for WL to WD delay (for 8 discharging cells) (SS,125,1.08):
Mean = 160.5ps
Sigma = 7.99ps
Mean – 6*sigma = 112.5ps

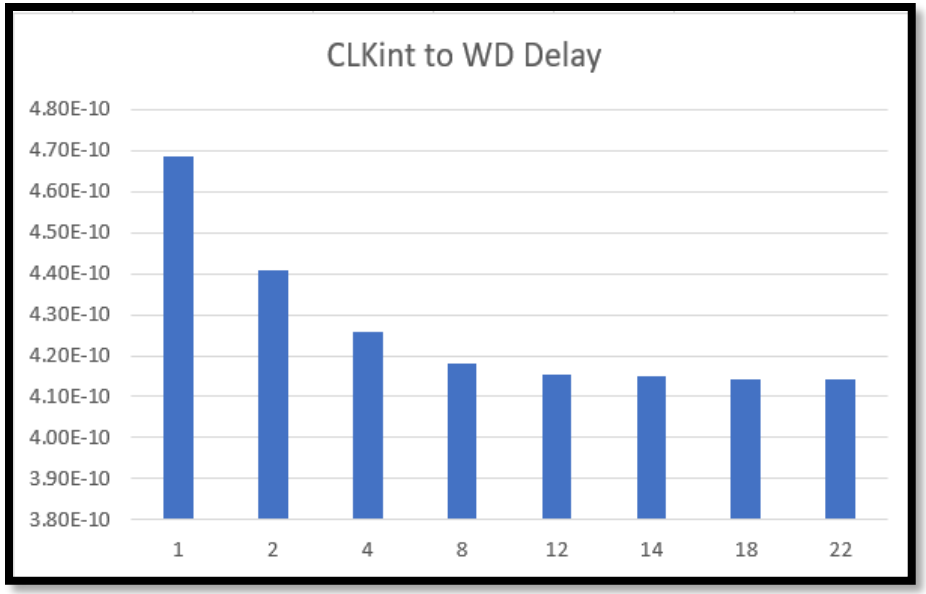
WD to WL OFF delay(best case) = (WD to RESET) + (RESET to CLKint) + (CLKint to WL off)
= 83ps + 253ps
= 336ps

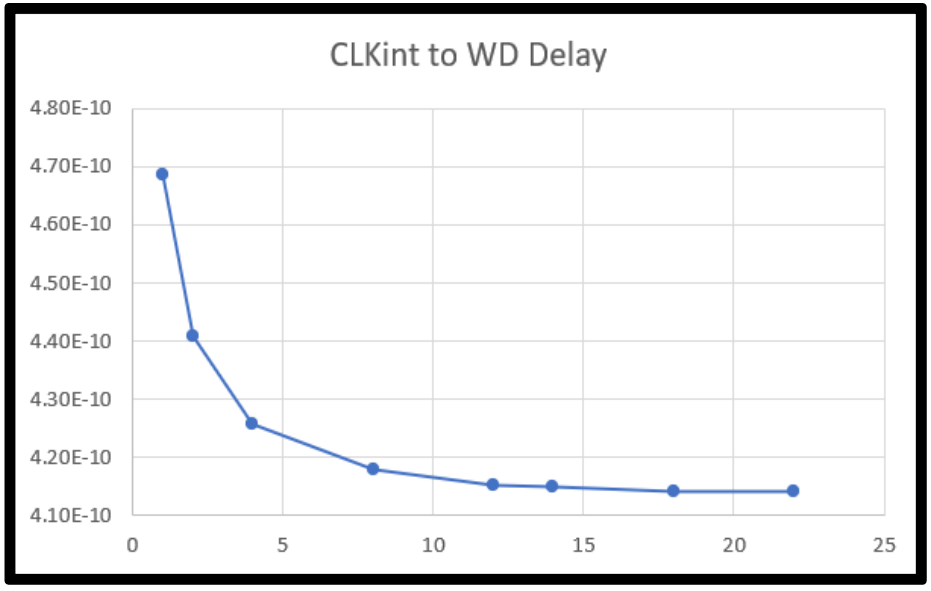
Taking these delays in consideration, the following constraint is satisfied.

$$t_{WC} < t_{WD} + \min(t_{WL,reset} , t_{WD,reset})$$

RESULTS (4)

Number of Discharge cells	CLKint to WD Delay
1	4.69E-10
2	4.41E-10
4	4.26E-10
8	4.18E-10
12	4.15E-10
14	4.15E-10
18	4.14E-10
22	4.14E-10





As we can see from the above bar graph with the increase in number of discharge cells the CLKint to WD delay decreases significantly initially but after 8 discharge cells it becomes constant approximately, hence we have considered 8 discharge cells in our circuit.

Conclusions and Future Plans (1)

What worked:

We satisfied the timing constraints worst case delay is not such small that the word line goes off before the completion of the write operation.

What did not work:

We were getting some erc like softchk and supply aborting while doing the LVS of the Dummy word line generation circuit but finally we removed them by making the fresh layout.

Answer the Whys:

Supply aborted errors were coming due to the multiple declaration of the same pin and softchk errors were coming due to the stamping on the nets.

Conclusions and Future Plans (2)

New skills:

- We have learned about the mpar, how it can replicate the same behavior as we as bit lines see load of 504 bit cells hence we can simply use mpar instead of connecting 504 bit cells load.
- Practical knowledge of signal flow in write operation and delays involved Main purpose of replica bit cell is to replicate the same behavior as that of the array and as well as to create the reset signal which actually resets the clock internal and reset the clock for particular cycle.
- Replica is basically required to track the delays appropriately within the memory for a particular cycle for different cut sizes of the particular memory.

Future work:

Future extension: will work on the layout for further optimization

Publication.

scope : yes

References

- Zhao-Yong Zhang, Li-Jun Zhang, Yi-Ping Zhang, Rui-Feng Huang, Shou-Dao Wu and Jian-Bin Zheng, "A 55nm ultra high density twoport register file compiler with improved write replica technique," 2011 9th IEEE International Conference on ASIC, 2011, pp. 303-306, doi: 10.1109/ASICON.2011.6157182.
- B. S. Amrutur and M. A. Horowitz, "A replica technique for wordline and sense control in low-power SRAM's," in IEEE Journal of SolidState Circuits, vol. 33, no. 8, pp. 1208-1219, Aug. 1998, doi: 10.1109/4.705359.
- Shyh-Chyi Yang, Hao-I Yang, Ching-Te Chuang and Wei Hwang, "Timing control degradation and NBTI/PBTI tolerant design for Write-replica circuit in nanoscale CMOS SRAM," 2009 International Symposium on VLSI Design, Automation and Test, 2009, pp. 162-165, doi: 10.1109/VDAT.2009.5158120