

GROUP 17

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VDF PROJECT

PART 1

PROBLEM NUMBER - 7

If C=8'h00 TO 8'h59, 4-bit ring counter

C=8'h78 TO 8'h90, 4x1 Mux

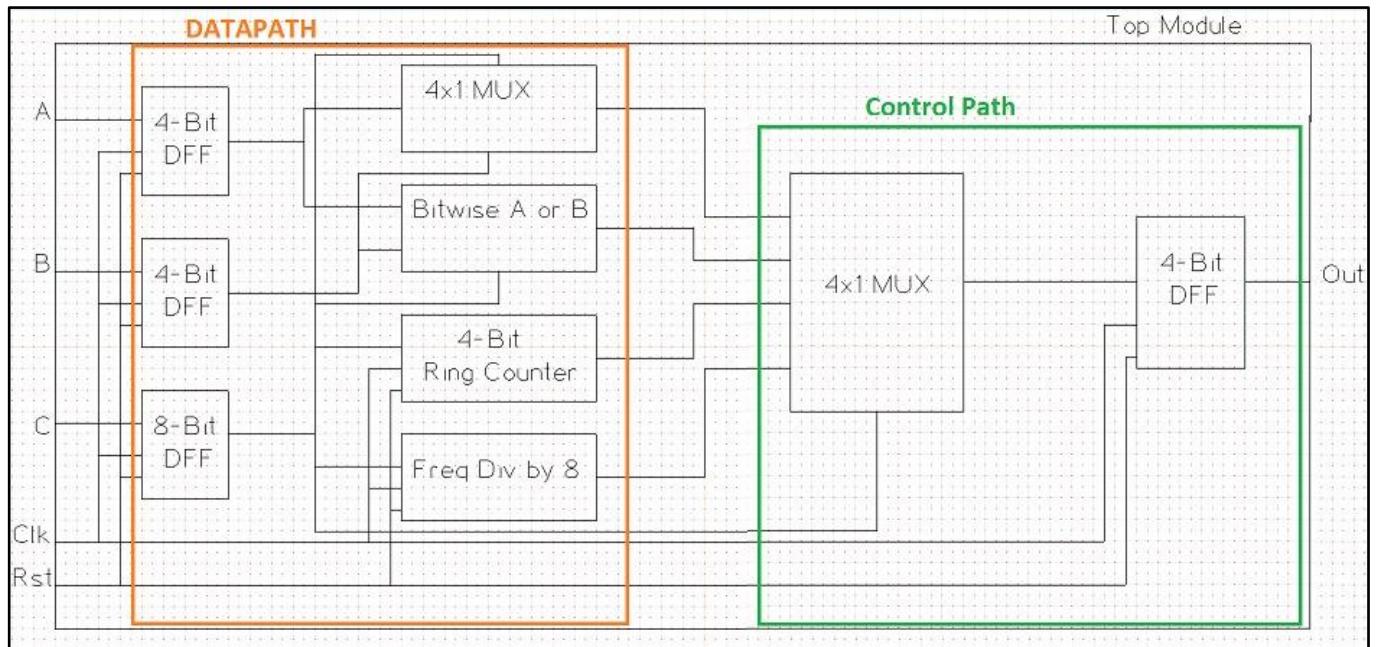
C=8'hB1 TO 8'hED, frequency divider by 8

Else, bitwise A OR B

STEP – 1

SPECIFICATIONS & ASSUMPTIONS

GENERAL BLOCK DIAGRAM OF OUR DESIGN



SPECIFICATIONS

- **PROBLEM STATEMENT**

If C=8'h00 TO 8'h59, 4-bit ring counter
 C=8'h78 TO 8'h90, 4x1 Mux
 C=8'hB1 TO 8'hED, frequency divider by 8
 Else, bitwise A OR B

- **INPUT & OUTPUT PORTS**

A, B, C, rst and **clk** are input ports where,

- **A [3:0]** and **B [3:0]** are constituting data path with size **4 bits**.
- **C [7:0]** is a control signal constituting Control path with size **8 bits**.
- **rst** is used as a reset signal and **clk** is used as a clock signal with size **1 bit** each.
- The design is a **synchronous design**.

OUT [3:0] is an output port with size **4 bits**.

- **FUNCTIONAL BEHAVIOUR OF CIRCUIT**

Port C will decide the functionality of our circuit. If C is between 8'h00 to 8'h59 then a 4-bit ring counter will be implemented and we will get the output of ring counter at the ouput port OUT. Similarly, if C is between 8'h78 to 8'h90 then 4x1 Mux will be implemented and according to inputs we will get the output. If C is between 8'hB1 to 8'hED then we will implement frequency divider by 8 circuit. If the control signal does not satisfy any condition mentioned above then bitwise A or B will be performed and correspondingly, we will get the output.

- 1 clock cycle **latency** is observed.

- **TOOLS USED**

All the steps are performed in Cadence tools (SimVision, ICCR, Genus, Conformal and Tempus).

ASSUMPTIONS

- Inputs A and B are first passed through DFFs and further operation on them is performed based on the control signal C. C is also connected to a DFF first. Synchronous reset (rst) is used in the design. Output is also connected through the DFF.
- C is an 8 bit control signal which will cover all the cases given in the problem statement.
- A and B both are of size 4 bits because all the outputs can be obtained with this size.
- When a 4 bit ring counter has to be executed then we need only clk and rst signals to obtain the desired result irrespective of the value of A and B signal.
- For implementing the 4x1 Mux, we are using input A as an input to the mux as A[0], A[1], A[2] and A[3]. Last two bits of input B are used as a 2 bit select line.
- For implementing the frequency divider by 8 circuit, a 4 bit upcounter is designed with mod number 8 and a 4 bit output is obtained at the output as 0 or 1.
- 4 bit input A and B are used as an input to the bitwise OR operation and a 4 bit output is obtained correspondingly.

STEP – 2

SIMULATION AND COVERAGE ANALYSIS

VERILOG CODE:

```
//----- Top Module-----
module group17(
    input clk,           // declaration of input and outputs
    input rst,
    input [3:0]A,
    input [3:0]B,
    input [7:0]C,
    output [3:0]OUT
);
    wire [1:0]flag;

    control_path cp (clk, rst, C, flag);      // instantiating control path
    data_path dp (A, B, clk, rst, flag, OUT); // instantiating data path

endmodule
//----- Control Path-----

module control_path(
    input clk,
    input rst,
    input [7:0]C,
    output reg [1:0]flag
);           // declaration of control path module

    wire [7:0]c;

    DFF8 D1 (clk, C, c);

    always@(*)
    begin
        if(c<=8'h59)
        begin
            flag=2'b00;    //4-bit ring counter
        end
        else if(c>=8'h78 && c<=8'h90)
        begin
            flag=2'b01;  //4x1 Mux
        end
        else if(c>=8'hB1 && c<=8'hED)
        begin
            flag=2'b10;      //frequency divider by 8
        end
        else // bitwise A OR B
        begin
            flag=2'b11;      //bitwise A OR B
        end
    end

```

```

end
end
endmodule
//-----Data Path-----

module data_path(
input [3:0]A,
input [3:0] B,
input clk,
input rst,
input [1:0]flag,
output [3:0]OUT
);
    // declaration of data path
reg [3:0]out;
wire [3:0] a;
wire [3:0] b;
wire [3:0]out1,out4;
wire out2,out3;
DFF4 D2(clk, A, a); // 4 bit DFF is instantiated to PIPO input A
DFF4 D3(clk,B,b); // 4 bit DFF is instantiated to PIPO input B
Rcounter4 c1(clk,rst,out1); // Instantiating ring counter
mux4 m1(a,b[1:0],out2); // Instantiating 4x1 mux
freq_div f1(clk,rst,out3); // Instantiating frequency divider by 8 design
bitwise_xor x1(a,b,out4); // Instantiating bitwise xor
always @(*)
begin
case (flag) // according to flag status output of a module will be given to output.
2'b00: begin
    out=out1 ; //4-bit ring counter
end

2'b01: begin
    out=out2; //4x1 Mux
end

2'b10: begin
    out={{3{1'b0}},out3}; //frequency divider by 8
end

2'b11: begin
    out=out4; //bitwise A OR B
end
endcase
end
DFF4 D4(clk,out,OUT); // 8 bit DFF is instantiated to PIPO output OUT
endmodule
//-----D flip flop 4 bits-----

```

```

module DFF4(
    input clk,
    input [3:0]D,
    output reg [3:0]Q
);
    always@(posedge clk)
    begin

```

```

Q<=D;          // 4 bit DFF
end
endmodule
//-----D flip flop 8 bits-----

module DFF8(
  input clk,
  input [7:0]D,
  output reg [7:0]Q
);
  always@(posedge clk)
  begin
    Q<=D;          // 8 bit DFF
  end
endmodule
//-----Ring counter-----

module Rcounter4(
  input clk,
  input rst,
  output reg [3:0]out1
);
  always @ (posedge clk)
  begin
    if(rst == 1'b1) begin          // synchronous reset
      out1 <= 4'b0001; end
    else begin
      out1 <= {out1[2:0],out1[3]}; end
    end
  endmodule
//-----MUX-----

module mux4(
  input [3:0]A,
  input [1:0]sel,      // select signal is assumed to be 2 LSB of input B
  output reg out2
);
  always @ (A,sel) begin
    case (sel)
      2'b00 :begin
        out2 = A[0];
      end

      2'b01 :begin
        out2 = A[1];
      end

      2'b10 :begin
        out2 = A[2];
      end
    endcase
  end

```

```

2'b11 :begin
    out2 = A[3];
end

default :out2 = 4'b0000;

endcase
end
endmodule
//-----Frequency Divider-----
module freq_div (
    input clk,
    input rst,
    output out3
);
reg [3:0]temp;
always @ (posedge clk)
begin
if(rst)           // synchronous reset
    temp <=4'b0000;
    else
    temp <= temp + 1;
end
assign out3=temp[2];
endmodule

//-----BITWISE XOR-----
module bitwise_xor(
    input [3:0] a,
    input [3:0] b,
    output [3:0] out4
);
    assign out4 = a ^ b;    // xor operation
endmodule

```

TESTBENCH FOR CHECKING THE FUNCTIONALITY OF THE DESIGN

```

module group17_tb();
reg [3:0] A,B;
reg[7:0] C;
wire [3:0] out;
reg rst,clk;
group17 DUT(clk,rst,A,B,C,out);
initial begin
clk=1'b0;
forever #5 clk=~clk;
end

initial begin

```

```
$dumpfile("group17.vcd");
$dumpvars(0,group17_tb);
#700 $finish;
end

initial
begin

A = 4'b0000; B = 4'b0000;
C = 8'h10;
#5 rst = 1'b1;
#10 rst = 1'b0;
#15 A = 4'b1101; B = 4'b1011;
#15 A = 4'b0101; B = 4'b1010;
#30 rst = 1'b1;
#15 rst = 1'b0;

#15 C = 8'h79;
#15 A = 4'b0000; B = 4'b0000;
#15 rst = 1'b1;
#15 rst = 1'b0;
#15 A = 4'b1010; B = 4'b1000;
#30 A = 4'b1011; B = 4'b1001;
#15 A = 4'b1011; B = 4'b1010;
#30 A = 4'b0010; B = 4'b1111;

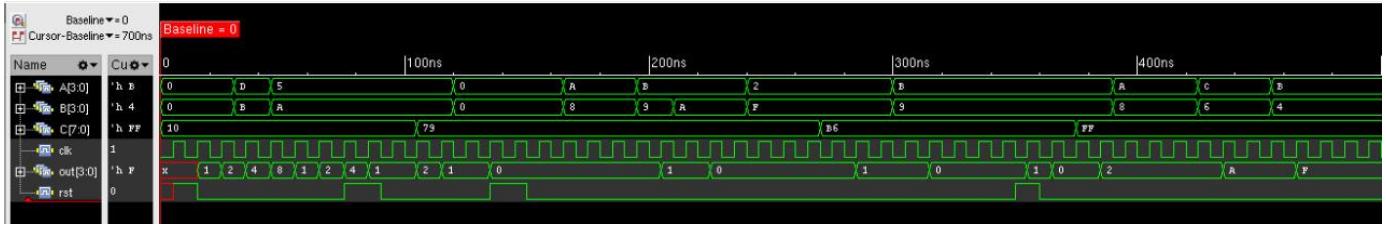
#30 C = 8'hb6;
#15 rst = 1'b0;
#15 A = 4'b1011; B = 4'b1001;
#50 rst = 1'b1;
#10 rst = 1'b0;

#15 C = 8'hFF;
#15 A = 4'b1010; B = 4'b1000;
#35 A = 4'b1100; B = 4'b0110;
#30 A = 4'b1011; B = 4'b0100;

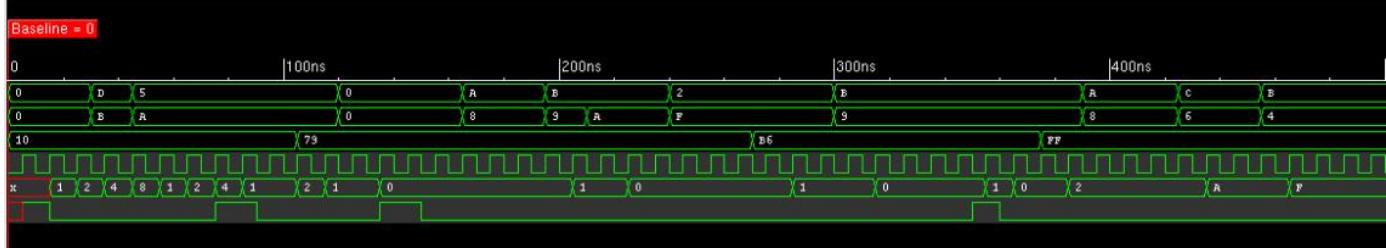
end

endmodule
```

SIMULATION RESULTS AND ANALYSIS

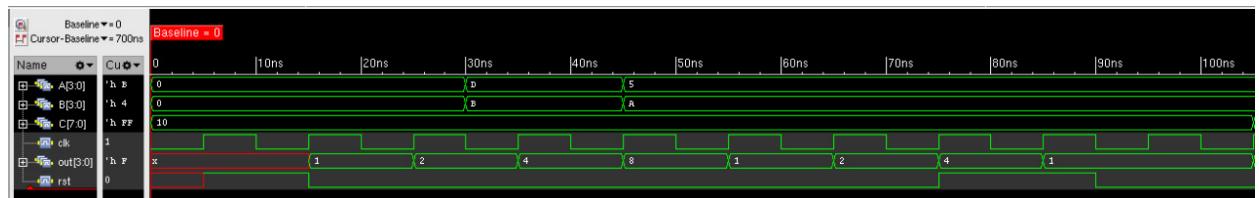


Zoomed view



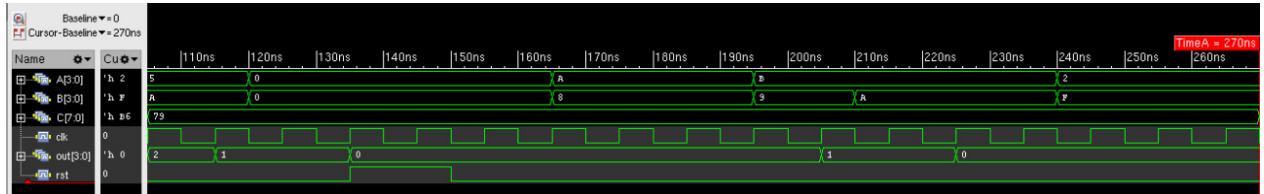
- A and B are initialized with value 4'b0000 and C with 8'h10 (**4-bit ring counter** will be executed). Clock period is taken as 10ns with 50% duty cycle. Reset (rst) is set high at 5ns.
 - There is a clock latency of 1 clock cycle. Therefore, ring counter starts its functionality at 15ns. As shown in the waveform, output OUT goes from 1 -> 2 -> 4 -> 8 after each clock cycle irrespective of input A and B which satisfies the given specifications.
 - rst is set high from 75ns to 90ns which resets the output of ring counter to 4'b0001 until rst goes low.
 - At 105ns, C changes to 8'h79 which will execute the **4x1 mux**.
When A = 4'b0000 and B = 4'b0000, OUT = 4'b0000 (select line is 00, A[0] is selected at the output). Similarly, corresponding to each input given in this range is observed to be correct according to 4x1 mux.
 - At 270ns, C changes to 8'hB6 which will execute the operation of frequency divider by 8 circuit which is working as an 8 bit upcounter till 375ns.
 - As C goes to 8'hFF, bitwise OR operation is performed on input A and B.
When A is 4'hA and B is 4'h8 then OUT is 4'h2 till 385ns. The output is changing according to inputs subsequently till 550ns which satisfies the desired functionality.

1. Ring Counter Functionality



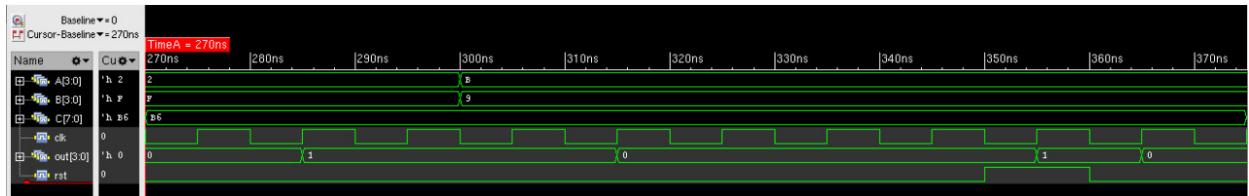
$C=8'h10$ is within the range of ring counter. Due to latency of 1 clock cycle, ring counter is starting at 2nd posedge of clock at 15ns. Output OUT goes from 1, 2, 4, 8 and then again 1, 2, 4 until rst goes high. At 75ns, rst goes high and hence output restarts from 1 at next posedge of clock (synchronous reset).

2. 4x1 Mux Functionality



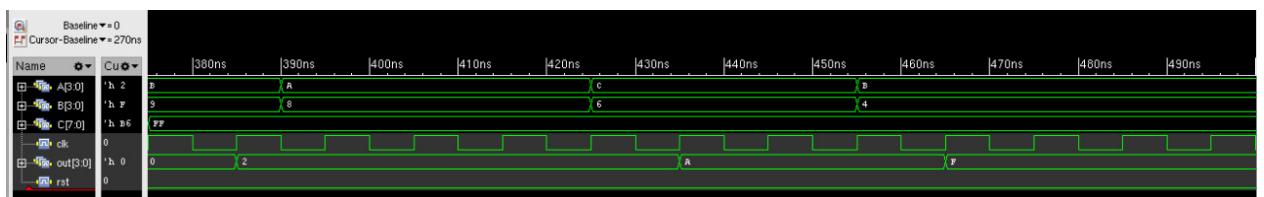
$C = 8'h79$ is within the range of 4x1 mux. Initially, when input $A = 4'h5$ and $B = 4'hA$, we can observe the output as 1. Since, $A = 4'b0101$ and $B = 4'b1010$, hence, $OUT = 4'b0001$ (select line is 10, $A[2]$ is selected at the output). Similarly, for other inputs functionality is coming out to be correct.

3. Frequency Divider Functionality



We can observe from the waveform that when C is in the range of frequency divider by 8 circuit then 8 bit upcounter functionality is obtained and the cycle gets reset to 0 when reset goes high.

4. Bitwise XOR Functionality



When C is $8'hFF$ then bitwise xor operation is performed on A and B . When A is $4'hB$ and B is $4'h9$ then output is $4'h4$. Similarly, for $A = 4'hA$ and $B = 4'h8$ the output OUT is $4'h2$ and so on.

TESTBENCHES AND CODE COVERAGE RESULTS

I. Testbench – 1

```
module group17_tb();
    reg [3:0] A,B;
    reg[7:0] C;
    wire [3:0] out;
    reg rst,clk;
    group17 DUT(clk,rst,A,B,C,out);
    initial begin
        clk=1'b0;
        forever #5 clk=~clk;
    end

    initial begin
        $dumpfile("group17.vcd");
        $dumpvars(0,group17_tb);
        #555 $finish;
    end

    initial
        begin
            A = 4'b0000; B = 4'b0000; C = 8'h00;
            #5 rst = 1'b1;
            #10 rst = 1'b0;
            #50 C = 8'h43;
            #20 rst = 1'b1;
            #15 rst = 1'b0;

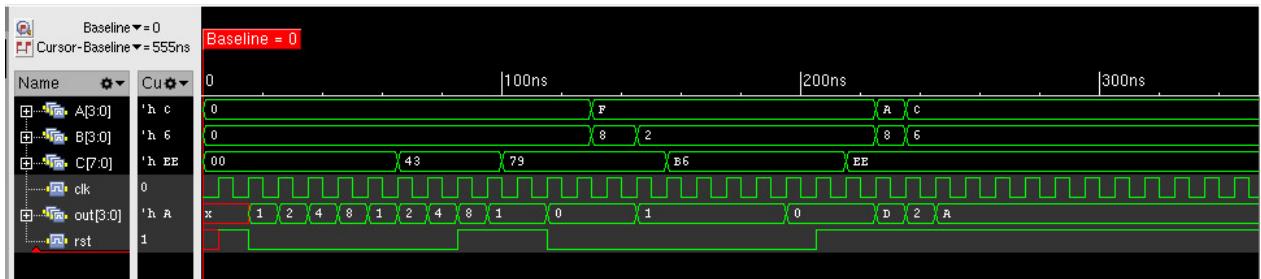
            A = 4'b0000; B = 4'b0000; C = 8'h79;
            rst = 1'b1;
            #15 rst = 1'b0;
            #15 A = 4'b1111; B = 4'b1000;
            #15 A = 4'b1111; B = 4'b0010;

            #10 C = 8'hb6;
            #50 rst = 1'b1;

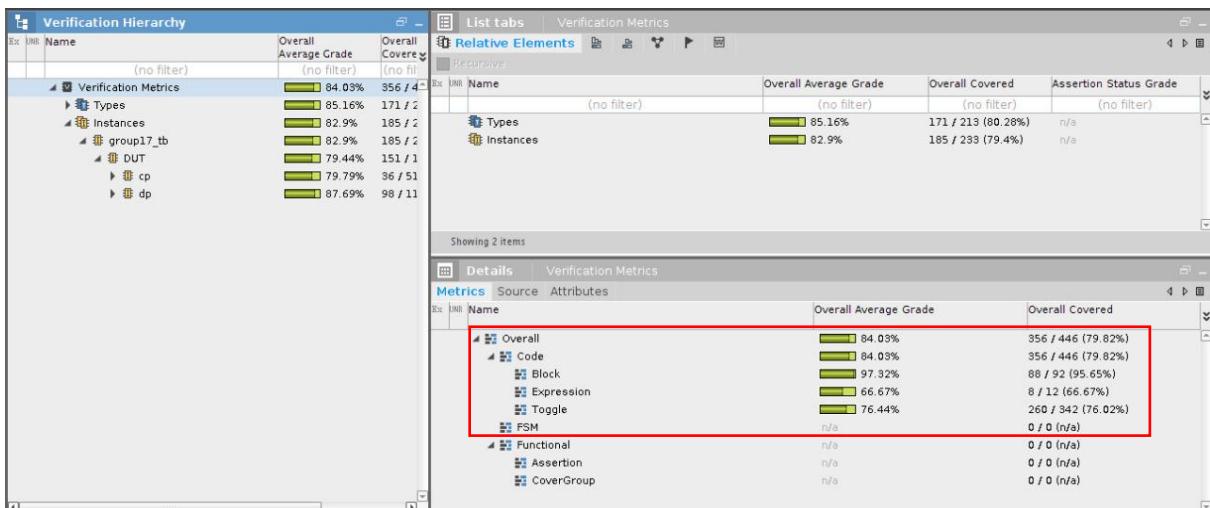
            #10 C = 8'hEE;
            #10 A = 4'b1010; B = 4'b1000;
            #10 A = 4'b1100; B = 4'b0110;

        end
    endmodule
```

Simulation Results



Coverage Report



Metrics Report - Metrics Tree

Current Node: [/Verification Metrics/Types](#)

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	Types	85.16%	171 / 213 (80.28%)	n/a

Sub-Nodes:

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	group17_tb	86.36% (85%)	34 / 40 (85%)	n/a
None	none	group17	70.83%	17 / 24 (70.83%)	n/a
None	none	control_path	77.22%	24 / 33 (72.73%)	n/a
None	none	DFF8	82.35%	12 / 18 (66.67%)	n/a
None	none	data_path	90.79%	37 / 44 (84.09%)	n/a
None	none	DFF4	100%	10 / 10 (100%)	n/a
None	none	Rcounter4	100%	9 / 9 (100%)	n/a
None	none	mux4	69.05%	9 / 13 (69.23%)	n/a
None	none	freq_div	100%	10 / 10 (100%)	n/a
None	none	bitwise_xor	75%	9 / 12 (75%)	n/a

Coverage Color Legend

0	<25	<50	<75	<100	100	n/a	Not Scored
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Metrics Report - Metrics Tree

Current Node: [/Verification Metrics](#)

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	Verification Metrics	84.03%	356 / 446 (79.82%)	n/a

Sub-Nodes:

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	Types	85.16%	171 / 213 (80.28%)	n/a
None	none	Instances	82.9%	185 / 233 (79.4%)	n/a

Coverage Color Legend

0	<25	<50	<75	<100	100	n/a	Not Scored
---	-----	-----	-----	------	-----	-----	------------

Toggle	Block	Expression	name
71.43% (5/7)	66.67% (4/6)	n/a	mux4

Uncovered Toggle Detail Report, Type Based

Type name: mux4
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered signal bits: 2 of 7
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 1 of 7
Number of signal bits partially toggled(fall): 0 of 7

Hit(Full)	Hit(Rise)	Hit(Fall)	Signal
0	1	0	A[3]
0	0	0	sel[0]

Uncovered Block Detail Report, Type Based

Type name: mux4
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered blocks: 2 of 6
Number of unreachable blocks: 0

Count	Block	Line	Kind	Origin	Source Code
0	3	152	a case item of	147	2'b01 :begin
0	5	160	a case item of	147	2'b11 :begin

Coverage Summary Report, Type-Based

Toggle	Block	Expression	name
64.71% (11/17)	100.00% (1/1)	n/a	DFF8

Uncovered Toggle Detail Report, Type Based

Type name: DFF8
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered signal bits: 6 of 17
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 6 of 17
Number of signal bits partially toggled(fall): 0 of 17

Hit(Full)	Hit(Rise)	Hit(Fall)	Signal
0	1	0	D[7]
0	1	0	D[5]
0	1	0	D[2]
0	1	0	Q[7]
0	1	0	Q[5]
0	1	0	Q[2]

Coverage Summary Report, Type-Based

Toggle	Block	Expression	name
75.00% (9/12)	n/a	n/a	bitwise_xor

Uncovered Toggle Detail Report, Type Based

Type name: bitwise_xor
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered signal bits: 3 of 12
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 2 of 12
Number of signal bits partially toggled(fall): 0 of 12

Hit(Full)	Hit(Rise)	Hit(Fall)	Signal
0	1	0	a[3]
0	1	0	b[2]
0	0	0	b[0]

Coverage Summary Report, Type-Based

Toggle	Block	Expression	name
65.00% (13/20)	100.00% (7/7)	66.67% (4/6)	control_path

Uncovered Toggle Detail Report, Type Based

Type name: control_path
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered signal bits: 7 of 20
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 7 of 20
Number of signal bits partially toggled(fall): 0 of 20

Coverage Summary Report, Type-Based

Toggle	Block	Expression	name
65.00% (13/20)	100.00% (7/7)	66.67% (4/6)	control_path

Uncovered Toggle Detail Report, Type Based

Type name: control_path
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered signal bits: 7 of 20
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 7 of 20
Number of signal bits partially toggled(fall): 0 of 20

Hit(Full)	Hit(Rise)	Hit(Fall)	Signal
0	1	0	C[7]
0	1	0	C[5]
0	1	0	C[2]
0	1	0	flag[1]
0	1	0	c[7]
0	1	0	c[5]
0	1	0	c[2]

Uncovered Expression Detail Report, Type Based

Type name: control_path
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered expressions: 2 of 6
Number of unreachable expressions: 0

```

index | grade | line | expression
1.1  | 66.67% (2/3) | 37 | (c >= 8'h78) && (c <= 8'h90)
2.1  | 66.67% (2/3) | 41 | (c >= 8'hb1) && (c <= 8'hex)

index: 1.1 grade: 66.67% (2/3) line: 37 source: else if(c>=8'h78 && c<=8'h90) //4x1 Mux
(c >= 8'h78) && (c <= 8'h90)

<--1----> <--2---->
index | hit | <1> <2>
1.1.1 | 0 | 0 |
index: 2.1 grade: 66.67% (2/3) line: 41 source: else if(c>=8'hB1 && c<=8'hED) //frequency divider by 8
(c >= 8'hb1) && (c <= 8'hex)

<--1----> <--2---->
index | hit | <1> <2>
2.1.1 | 0 | 0 |

```

Coverage Summary Report, Type-Based

Toggle	Block	Expression	name
81.58% (31/38)	100.00% (6/6)	n/a	data_path

Uncovered Toggle Detail Report, Type Based

Type name: data_path
File name: [/home/prapti21202/VDF_PROJECT/rtl/vc.v](#)
Number of uncovered signal bits: 7 of 38
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 5 of 38
Number of signal bits partially toggled(fall): 0 of 38

Hit(Full)	Hit(Rise)	Hit(Fall)	Signal
0	1	0	A[3]
0	1	0	B[2]
0	0	0	B[0]
0	1	0	flag[1]
0	1	0	a[3]
0	1	0	b[2]
0	0	0	b[0]

Analysis

For the testbench 1, we are getting overall average code coverage as 84.03%. Block coverage is 97.32%, expression coverage is 66.67% and toggle coverage is coming out to be 76.44%. In the above detailed report, we can see the cases which are not covered in the testbench causing incomplete coverage. For the mux4 module, both

toggle and block coverage is not covered because few cases of select line are not covered by toggling the input 0 -> 1 and 1 -> 0 in the testbench. All lines or cases were also not covered for the mux4 module shown in block coverage report.

In the bitwise xor operation also all cases for input A and B are not covered by toggling the inputs. Toggle report for datapath, controlpath and DFF8 is shown above. There is also uncovered expression detail report which shows that C (the control signal) is not covered by all the cases. All these cases we tried to achieve in the next testbench written.

II. Testbench-2

```
module group17_tb();
reg [3:0] A,B;
reg[7:0] C;
wire [3:0] out;
reg rst,clk;
group17 DUT(clk,rst,A,B,C,out);
initial begin
clk=1'b0;
forever #5 clk=~clk;
end

initial begin
$dumpfile("group17.vcd");
$dumpvars(0,group17_tb);
#555 $finish;
end

initial
begin
A = 4'b0000; B = 4'b0000; C = 8'h00;
#5 rst = 1'b1;
#10 rst = 1'b0;
#50 C = 8'h43;
#5 A = 4'b0101; B = 4'b1010; C = 8'h01;
#20 rst = 1'b1;
#15 rst = 1'b0;

A = 4'b0000; B = 4'b0000; C = 8'h79;
rst = 1'b1;
#15 rst = 1'b0;
#15 A = 4'b0000; B = 4'b1000; C = 8'h78;
#15 A = 4'b1111; B = 4'b1000;
#10 A = 4'b0000; B = 4'b0010; C = 8'h87;
#15 A = 4'b1111; B = 4'b0010;
#15 A = 4'b0000; B = 4'b1101; C = 8'h79;
```

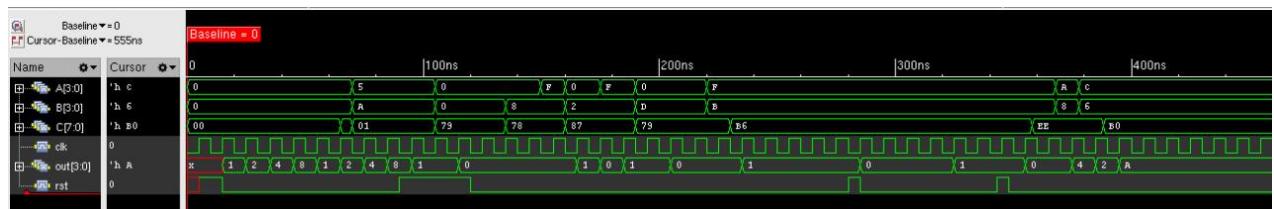
```
#15 A = 4'b0000; B = 4'b1101;
#15 A = 4'b1111; B = 4'b1011;
```

```
#10 C = 8'hb6;
#50 rst = 1'b1;
#5 rst = 1'b0;
#58 rst = 1'b1;
#5 rst = 1'b0;
```

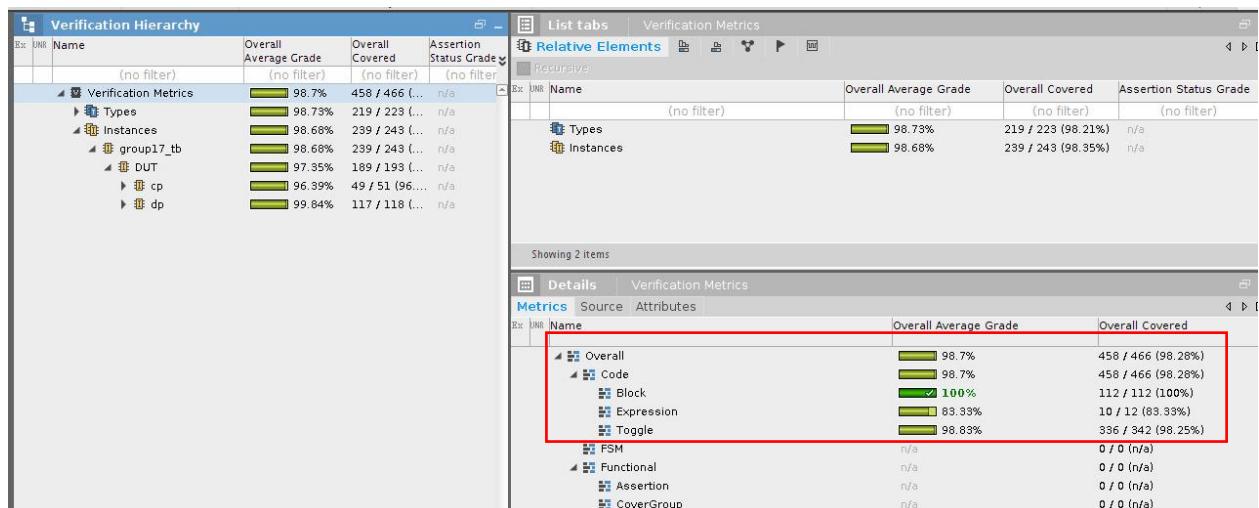
```
#10 C = 8'hEE;
#10 A = 4'b1010; B = 4'b1000;
#10 A = 4'b1100; B = 4'b0110;
#10 C = 8'hB0;
```

```
end
endmodule
```

Simulation Results



Coverage Report



Metrics Report - Metrics Tree

Current Node: /Verification Metrics

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	Verification Metrics	98.7%	458 / 466 (98.28%)	n/a

Sub-Nodes:

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	Types	98.73%	219 / 223 (98.21%)	n/a
None	none	Instances	98.68%	239 / 243 (98.35%)	n/a

Coverage Color Legend

0 <25 <50 <75 <100 100 n/a Not Scored

Metrics Report - Metrics Tree

Current Node: /Verification Metrics/Types

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	Types	98.73%	219 / 223 (98.21%)	n/a

Sub-Nodes:

Exclusion Rule Type	UNR	Name	Overall Average Grade	Overall Covered	Assertion Status Grade
None	none	group17_tb	100%	50 / 50 (100%)	n/a
None	none	group17	95.83%	23 / 24 (95.83%)	n/a
None	none	control_path	92.78%	31 / 33 (93.94%)	n/a
None	none	DFF8	100%	18 / 18 (100%)	n/a
None	none	data_path	98.68%	43 / 44 (97.73%)	n/a
None	none	DFF4	100%	10 / 10 (100%)	n/a
None	none	Rcounter4	100%	9 / 9 (100%)	n/a
None	none	mux4	100%	13 / 13 (100%)	n/a
None	none	freq_div	100%	10 / 10 (100%)	n/a
None	none	bitwise_xor	100%	12 / 12 (100%)	n/a

Coverage Color Legend

0 <25 <50 <75 <100 100 n/a Not Scored

Uncovered Toggle Detail Report, Type Based

Type name: data_path
File name: /home/prapti21202/VDF PROJECT/rtl/vc.v
Number of uncovered signal bits: 1 of 38
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 1 of 38
Number of signal bits partially toggled(fall): 0 of 38

Hit(Full)	Hit(Rise)	Hit(Fall)	Signal
0	1	0	flag[1]

Uncovered Toggle Detail Report, Type Based

Type name: control_path
File name: /home/prapti21202/VDF PROJECT/rtl/vc.v
Number of uncovered signal bits: 1 of 20
Number of unreachable signal bits: 0
Number of signal bits partially toggled(rise): 1 of 20
Number of signal bits partially toggled(fall): 0 of 20

Hit(Full)	Hit(Rise)	Hit(Fall)	Signal
0	1	0	flag[1]

Type name: control_path
File name: /home/prapti21202/VDF PROJECT/rtl/vc.v
Number of uncovered expressions: 1 of 6
Number of unreachable expressions: 0

```

index | grade      | line    | expression
-----|-----|-----|-----
1.1   | 66.67% (2/3) | 37     | (c >= 8'h78) && (c <= 8'h90)

index: 1.1 grade: 66.67% (2/3) line: 37 source: else if(c>=8'h78 && c<=8'h90) //4x1 Mux
(c >= 8'h78) && (c <= 8'h90)
<----1---->      <----2---->
index      | hit      | <1> <2>
-----|-----|-----'&&'|
1.1.1   | 0       | 0     -

```

Analysis

In this testbench (2), overall average code coverage coming out to be is 98.7% with block coverage as 100%, expression coverage as 83.33% and toggle coverage as 98.83%. We have improved the block coverage to 100% by adding the uncovered cases for the same in mux4 and bitwise. Expression coverage is also improved by using more cases. Toggle coverage is improved to 98.83% by adding the cases which were not toggling before in mux and bitwise xor operation. Reset signal is also appropriately applied in all the cases. Only few cases in control and datapath are not covered (flag signal) which we tried to achieve in 3rd testbench).

III. Testbench-3

```
module group17_tb();
reg [3:0] A,B;
reg[7:0] C;
wire [3:0] out;
reg rst,clk;
group17 DUT(clk,rst,A,B,C,out);
initial begin
clk=1'b0;
forever #5 clk=~clk;
end

initial begin
$dumpfile("group17.vcd");
$dumpvars(0,group17_tb);
#555 $finish;
end

initial
begin

A = 4'b0000; B = 4'b0000; C = 8'h00;
#5 rst = 1'b1;
#10 rst = 1'b0;
#50 C = 8'h43;
#5 A = 4'b0101; B = 4'b1010; C = 8'h01;
#20 rst = 1'b1;
#15 rst = 1'b0;

A = 4'b0000; B = 4'b0000; C = 8'h79;
rst = 1'b1;
#15 rst = 1'b0;
#15 A = 4'b0000; B = 4'b1000; C = 8'h78;
#15 A = 4'b1111; B = 4'b1000;
#10 A = 4'b0000; B = 4'b0010; C = 8'h87;
#15 A = 4'b1111; B = 4'b0010;
#15 A = 4'b0000; B = 4'b1101; C = 8'h79;
#15 A = 4'b0000; B = 4'b1101;
#15 A = 4'b1111; B = 4'b1011;

#10 C = 8'hb6;
#50 rst = 1'b1;
#5 rst = 1'b0;
#58 rst = 1'b1;
#5 rst = 1'b0;

#10 C = 8'hEE;
#10 A = 4'b1010; B = 4'b1000;
#10 A = 4'b1100; B = 4'b0110;
#10 C = 8'hB0;
```

```

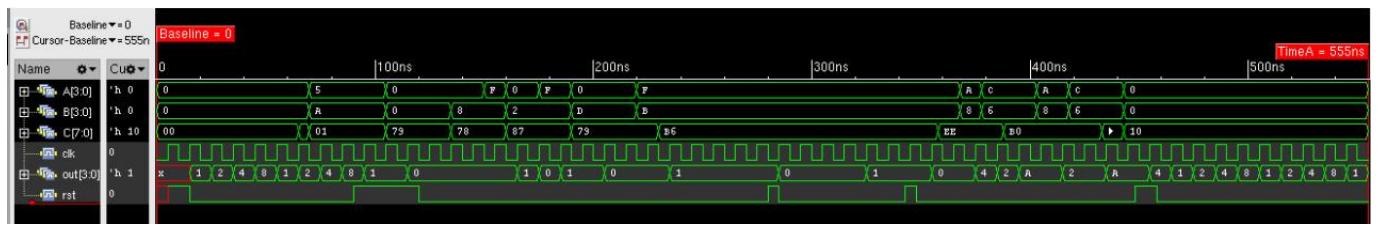
#15 A = 4'b1010; B = 4'b1000;
#15 A = 4'b1100; B = 4'b0110;
#15 C = 8'h77;
#10 A = 4'b1111; B = 4'b1111;

A = 4'b0000; B = 4'b0000; C = 8'h10;
#5 rst = 1'b1;
#10 rst = 1'b0;

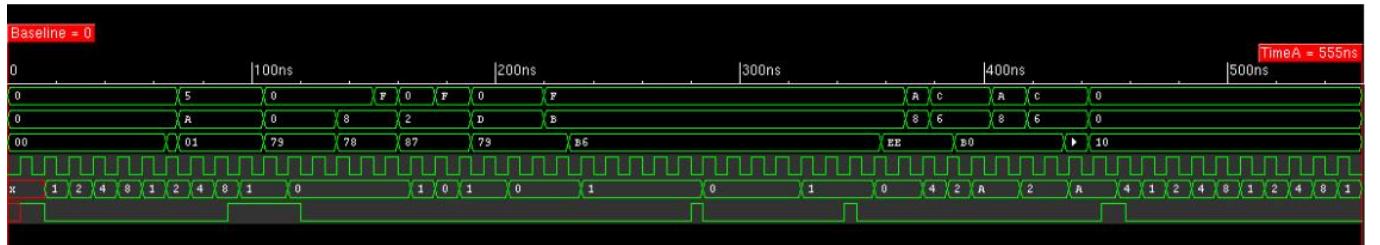
end
endmodule

```

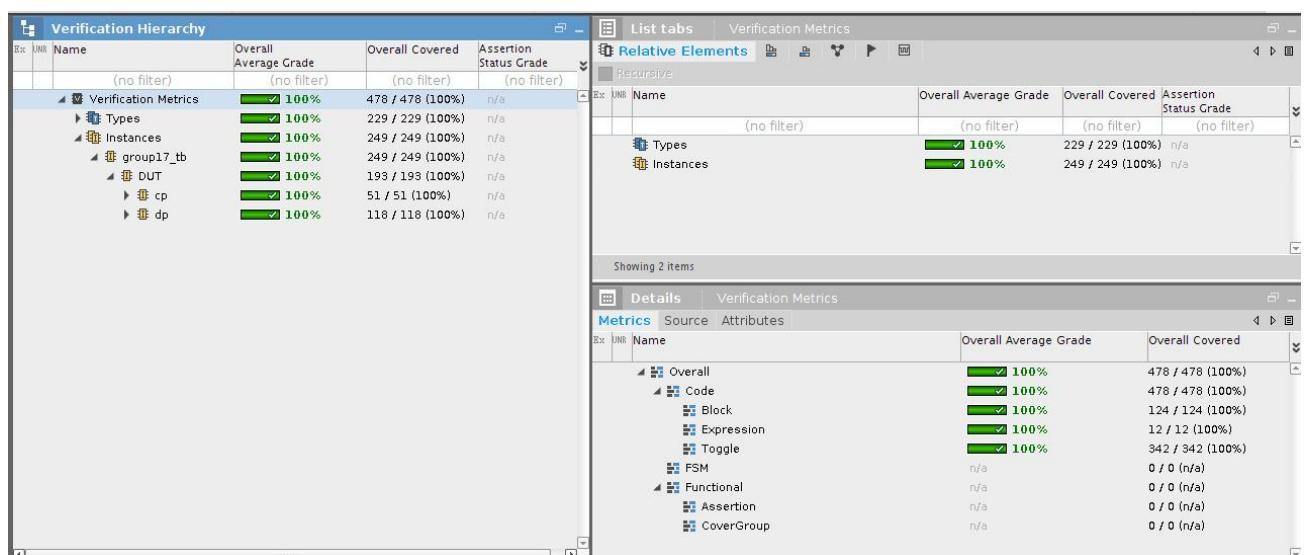
Simulation Results



Zoomed view



Coverage Report



Analysis

For the testbench 3, we have achieved 100% overall code coverage. Block, Expression and Toggle coverages are 100% covered. We have updated the testbench for this according to the previous coverage report so as to include all the cases.

STEP – 3

SYNTHESIS

TOOL USED: Cadence Genus

All three cases are described below:

CASE-1: SYNTHESIS FOR MINIMUM AREA AND RELAXED TIMING CONSTRAINT

In order to synthesize for the minimum area, Relaxed time constraints are used. As shown in the constraint file the time period is taken as sufficiently large which results in sufficient positive slack and hence as there is no slack violation or strict restrictions on slack violations the tool optimize for the minimum area by instantiating the smaller cells from the library that can also be seen in the generated cell report attached after the synthesis.

CONSTRAINT FILE

```
#generating clock
create_clock -name clk -period 15 -waveform {0 7.5} [get_ports "clk"]
set_propagated_clock [get_clocks "clk"]

#setting constraints on the clock
set_clock_transition 0.03 [get_clocks "clk"]
set_clock_uncertainty -setup 0.02 [get_clocks "clk"]
set_clock_uncertainty -hold 0.02 [get_clocks "clk"]

#input delays at different ports
set_input_delay -max 0.5 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -min 0.24 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -max 0.30 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -min 0.23 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -max 0.26 [get_ports "C"] -clock [get_clocks "clk"]
set_input_delay -min 0.11 [get_ports "C"] -clock [get_clocks "clk"]
set_input_delay 0.36 [get_ports "rst"] -clock [get_clocks "clk"]

#input transitions at different port
set_input_transition 0.06 [get_ports "A"]
set_input_transition 0.03 [get_ports "B"]
set_input_transition 0.06 [get_ports "C"]
set_input_transition 0.03 [get_ports "rst"]

#setting output constraints
set_output_delay 0.3 [get_ports "OUT"] -clock [get_clocks "clk"]
set_load 0.10 [get_ports "OUT"]
```

AREA REPORT

```
=====
Generated by:          Genus(TM) Synthesis Solution 19.13-s073_1
Generated on:          Apr 08 2022 04:45:57 pm
Module:                group17
Technology library:   slow
Operating conditions: slow (balanced_tree)
Wireload mode:        enclosed
Area mode:            timing library
=====

Instance  Module  Cell Count Cell Area Net Area Total Area Wireload
-----
group17          73      644.122  0.000   644.122 <none> (D)
  cp_D1  DFF8      8      127.159  0.000   127.159 <none> (D)
  dp_c1 Rcounter4  8      81.745  0.000   81.745 <none> (D)
  dp_f1 freq_div   10     71.906  0.000   71.906 <none> (D)
  dp_D4 DFF4_17    4      63.580  0.000   63.580 <none> (D)
  dp_D3 DFF4_18    4      63.580  0.000   63.580 <none> (D)
  dp_D2 DFF4       4      63.580  0.000   63.580 <none> (D)

(D) = wireload is default in technology library
```

TIMING REPORT

```
=====
Generated by:          Genus(TM) Synthesis Solution 19.13-s073_1
Generated on:          Apr 08 2022 04:45:57 pm
Module:                group17
Technology library:   slow
Operating conditions: slow (balanced_tree)
Wireload mode:        enclosed
Area mode:            timing library
=====

Pin           Type      Fanout Load Slew Delay Arrival
              (fF)  (ps)  (ps)  (ps)
-----
(clock clk)  launch
cp_D1
  Q_reg[2]/CK
  Q_reg[2]/Q    DFFQX1      2  4.2  57 +322   322 F
cp_D1/Q[2]
g887/A
g887/Y    NOR2XL      2  5.4  182 +156   478 R
g886/A
g886/Y    INVX1       1  2.8   66 +53    532 F
g874/A2
g874/Y    OAI31X1     2  3.3  152 +132   664 R
g872/B
g872/Y    NOR2XL      1  2.7   75 +69    733 F
g869/A1
g869/Y    OAI21X1     1  2.8   91 +93    826 R
g865/B1
g865/Y    AOI32X1     4 10.9  312 +150   976 F
g864/B
g864/Y    NOR2BX1    4  7.9  192 +198  1173 R
g859/B1
g859/Y    AOI32X1     1  2.8  174 +95   1268 F
g858/B0
g858/Y    OAI31X1     1  2.8  174 +78   1347 R
g857/B0
g857/Y    AOI21X1     1  2.7   95 +58   1404 F
g856/B0
g856/Y    OAI2BB1X1   1  1.6   52 +55   1460 R
dp_D4/D[0]
  Q_reg[0]/D <<< DFFQX1
  Q_reg[0]/CK setup
                           30 +173  1633 R
-----
(clock clk)  capture
               uncertainty
                           15000 R
                           -20  14980 R

Cost Group : 'clk' (path_group 'clk')
Timing slack : 13347ps
Start-point : cp_D1/Q_reg[2]/CK
End-point   : dp_D4/Q_reg[0]/D
```

POWER REPORT

Instance: /group17

Power Unit: W

PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	2.66315e-06	2.95229e-05	5.05651e-06	3.72426e-05	83.46%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	9.35870e-07	2.84025e-06	1.13096e-06	4.90708e-06	11.00%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	2.47320e-06	2.47320e-06	5.54%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	3.59902e-06	3.23631e-05	8.66067e-06	4.46228e-05	100.00%
Percentage	8.07%	72.53%	19.41%	100.00%	100.00%

CELL REPORT

=====

Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 04:45:57 pm
Module: group17
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library

=====

Gate	Instances	Area	Library
A022XL	3	22.707	slow
AOI21X1	2	9.083	slow
AOI21XL	1	4.541	slow
AOI31X1	1	6.055	slow
AOI32X1	3	20.436	slow
CLKINVX1	2	4.541	slow
DFFQX1	26	413.267	slow
DFFQXL	1	15.895	slow
INVX1	3	6.812	slow
INVXL	3	6.812	slow
MX2X1	1	6.812	slow
MXI2XL	2	12.110	slow
NAND2XL	2	6.055	slow
NOR2BX1	4	18.166	slow
NOR2XL	7	21.193	slow
NOR4BX1	1	6.812	slow
OAI21X1	3	13.624	slow
OAI21XL	1	4.541	slow
OAI2BB1X1	1	5.298	slow
OAI31X1	3	18.166	slow
OR2X1	1	4.541	slow
XOR2XL	2	16.652	slow
total	73	644.122	

Type	Instances	Area	Area %
sequential	27	429.162	66.6
inverter	8	18.166	2.8
logic	38	196.794	30.6
physical_cells	0	0.000	0.0
total	73	644.122	100.0

CASE-2: SYNTHESIS FOR TIGHT TIMING CONSTRAINT, SLIGHT -VE SLACK

In order to synthesize for the best timing case, tighter time constraints are used. As shown in the constraint file the time period is decreased significantly such that the slack becomes the slight negative value .as the slack is a negative value so there is a restriction on tool now, to avoid the violations tool has to instantiate bigger cells for the library and hence the area requirement will be increased automatically, same can be proved through the cell and the timing reports attached.

CONSTRAINT FILE

```
#generating clock
create_clock -name clk -period 4.927 -waveform {0 2.4635} [get_ports "clk"]
set_propagated_clock [get_clocks "clk"]

#setting constraints on the clock
set_clock_transition 3 [get_clocks "clk"]
set_clock_uncertainty -setup 1 [get_clocks "clk"]
set_clock_uncertainty -hold 0.2 [get_clocks "clk"]

#input delays at different ports
set_input_delay -max 2 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -min 0.5 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -max 2 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -min 0.5 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -max 2 [get_ports "C"] -clock [get_clocks "clk"]
set_input_delay -min 0.5 [get_ports "C"] -clock [get_clocks "clk"]
set_input_delay 1 [get_ports "rst"] -clock [get_clocks "clk"]

#input transitions at different port
set_input_transition 3 [get_ports "A"]
set_input_transition 3 [get_ports "B"]
set_input_transition 3 [get_ports "C"]
set_input_transition 3 [get_ports "rst"]

#setting output constraints
set_output_delay 3 [get_ports "OUT"] -clock [get_clocks "clk"]
set_load 1 [get_ports "OUT"]
```

AREA REPORT

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
group17		78	763.712	0.000	763.712	<none> (D)
dp_D4	DFF4_17	8	184.684	0.000	184.684	<none> (D)
cp_D1	DFF8	8	127.159	0.000	127.159	<none> (D)
dp_c1	Rcounter4	8	81.745	0.000	81.745	<none> (D)
dp_f1	freq_div	10	71.906	0.000	71.906	<none> (D)
dp_D3	DFF4_18	4	63.580	0.000	63.580	<none> (D)
dp_D2	DFF4_	4	63.580	0.000	63.580	<none> (D)

(D) = wireload is default in technology library

TIMING REPORT

Timing Report Summary						
Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)
(clock clk)	launch				0	R
dp_D4						
Q_reg[0]/CK				3000		0 R
Q_reg[0]/Q	DFFX2	1	13.2	87	+525	525 R
g6/A					+0	525
g6/Y	BUFX20	1	1000.0	427	+404	928 R
dp_D4/Q[0]						
OUT[0]	<<< interconnect			427	+0	928 R
	out port				+0	928 R
(best_timing.sdc_line_22_29_1)	ext delay				+3000	3928 R
(clock clk)	capture					4927 R
	uncertainty				-1000	3927 R
<hr/>						
Cost Group : 'clk' (path group 'clk')						
Timing slack : -1ps (TIMING VIOLATION)						
Start-point : dp_D4/Q_Reg[0]/CK						
End-point : OUT[0]						

← Timing Violation

POWER REPORT

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	2.97896e-06	2.14362e-04	4.06963e-06	2.21411e-04	56.03%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	2.40992e-06	3.16830e-05	1.32113e-04	1.66206e-04	42.06%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	7.51309e-06	7.51309e-06	1.90%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
<hr/>					
Subtotal	5.38888e-06	2.46045e-04	1.43696e-04	3.95130e-04	99.99%
Percentage	1.36%	62.27%	36.37%	100.00%	100.00%
<hr/>					

CELL REPORT

=====			
Generated by:			Genus(TM) Synthesis Solution 19.13-s073_1
Generated on:			Apr 06 2022 02:36:16 pm
Module:			group17
Technology library:			slow
Operating conditions:			slow (balanced_tree)
Wireload mode:			enclosed
Area mode:			timing library
=====			
Gate	Instances	Area	Library
ADDHXL	1	12.110	slow
AOI21X1	1	4.541	slow
AOI21XL	2	9.083	slow
AOI22X1	1	6.055	slow
AOI31X1	2	12.110	slow
AOI32X1	1	6.812	slow
BUFX20	4	102.938	slow
CLKINVX1	1	2.271	slow
DFFQX1	23	365.583	slow
DFFX2	4	81.745	slow
INVX1	3	6.812	slow
INVXL	3	6.812	slow
MX2X1	1	6.812	slow
NAND2BX1	1	4.541	slow
NAND2XL	5	15.138	slow
NOR2BX1	3	13.624	slow
NOR2XL	7	21.193	slow
OAI21X1	6	27.248	slow
OAI21XL	1	4.541	slow
OAI2BB1XL	1	5.298	slow
OAI31X1	2	12.110	slow
OAI32X1	1	6.812	slow
OR2XL	1	4.541	slow
XNOR2XL	3	24.978	slow

total	78	763.712	
Type	Instances	Area	Area %
sequential	27	447.328	58.6
inverter	7	15.895	2.1
buffer	4	102.938	13.5
logic	40	197.551	25.9
physical cells	0	0.000	0.0

total	78	763.712	100.0

CASE-3: SYNTHESIS FOR INTERMEDIATE TIMING CONSTRAINT, INTERMEDIATE SLACK

This is the intermediate case of the above two cases in this we have written our constraint file such that the slack doesn't become negative and hence the tool will not be restricted to instantiate bigger cells from the library and also the slack is not over positive such that tool will instantiate the smallest possible cells ,hence we can say this is the kind of trade-off between the above cases which results in area and slack in between of the above two cases as shown in the cell and the timing reports.

CONSTRAINT FILE

```
#generating clock
create_clock -name clk -period 11 -waveform {0 5.5} [get_ports "clk"]
set_propagated_clock [get_clocks "clk"]

#setting constraints on the clock
set_clock_transition 3 [get_clocks "clk"]
set_clock_uncertainty -setup 1 [get_clocks "clk"]
set_clock_uncertainty -hold 0.2 [get_clocks "clk"]

#input delays at different ports
set_input_delay -max 2 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -min 0.5 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -max 2 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -min 0.5 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -max 2 [get_ports "C"] -clock [get_clocks "clk"]
set_input_delay -min 0.5 [get_ports "C"] -clock [get_clocks "clk"]
set_input_delay 1 [get_ports "rst"] -clock [get_clocks "clk"]

#input transitions at different port
set_input_transition 3 [get_ports "A"]
set_input_transition 3 [get_ports "B"]
set_input_transition 3 [get_ports "C"]
set_input_transition 3 [get_ports "rst"]

#setting output constraints
set_output_delay 3 [get_ports "OUT"] -clock [get_clocks "clk"]
set_load 1 [get_ports "OUT"]
```

AREA REPORT

```
=====
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 04:45:28 pm
Module: group17
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----
group17 73 680.453 0.000 680.453 <none> (D)
cp_D1 DFF8 8 127.159 0.000 127.159 <none> (D)
dp_D4 DFF4_17 4 99.911 0.000 99.911 <none> (D)
dp_c1 Rcounter4 8 81.745 0.000 81.745 <none> (D)
dp_f1 freq_div 10 71.906 0.000 71.906 <none> (D)
dp_D3 DFF4_18 4 63.580 0.000 63.580 <none> (D)
dp_D2 DFF4 4 63.580 0.000 63.580 <none> (D)

(D) = wireload is default in technology library
```

TIMING REPORT

```
=====
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 04:45:28 pm
Module: group17
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
```

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)
(clock clk)	launch					0 R
dp_D4						
Q_reg[0]/CK			3000			0 R
Q_reg[0]/Q	DFFHQX8	1	1000.0	1017	+1294	1294 R
dp_D4/Q[0]						
OUT[0]	<<< interconnect			1017	+0	1294 R
	out port				+0	1294 R
(compromised_case.sdc_line_26_29_1)	ext delay				+3000	4294 R
						- - -
(clock clk)	capture					11000 R
	uncertainty				-1000	10000 R

Cost Group : 'clk' (path_group 'clk')						
Timing slack : 5706ps						
Start-point : dp_D4/Q_reg[0]/CK						
End-point : OUT[0]						

POWER REPORT

Instance: /group17

Power Unit: W

PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	3.43519e-06	1.00856e-04	5.91685e-05	1.63460e-04	94.10%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	9.44421e-07	4.33880e-06	1.57645e-06	6.85967e-06	3.95%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	3.37991e-06	3.37991e-06	1.95%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	4.37961e-06	1.05195e-04	6.41249e-05	1.73699e-04	100.00%
Percentage	2.52%	60.56%	36.92%	100.00%	100.00%

CELL REPORT

```
=====
Generated by: Genus(TM) Synthesis Solution 19.13-s073_1
Generated on: Apr 08 2022 04:45:28 pm
Module: group17
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
```

Gate Instances Area Library

A022X1	3	22.707	slow
AOI21X1	2	9.083	slow
AOI21XL	1	4.541	slow
AOI31X1	1	6.055	slow
AOI32X1	3	20.436	slow
CLKINVX1	2	4.541	slow
DFFHQX8	4	99.911	slow
DFFQX1	23	365.583	slow
INVX1	3	6.812	slow
INVXL	3	6.812	slow
MX2X1	1	6.812	slow
MXI2XL	2	12.110	slow
NAND2XL	2	6.055	slow
NOR2BX1	4	18.166	slow
NOR2XL	7	21.193	slow
NOR4BX1	1	6.812	slow
OAI21X1	3	13.624	slow
OAI21XL	1	4.541	slow
OAI2BB1X1	1	5.298	slow
OAI31X1	3	18.166	slow
OR2XL	1	4.541	slow
XOR2XL	2	16.652	slow

total	73	680.453
-------	----	---------

Type Instances Area Area %

sequential	27	465.493	68.4
inverter	8	18.166	2.7
logic	38	196.794	28.9
physical cells	0	0.000	0.0

total	73	680.453	100.0
-------	----	---------	-------

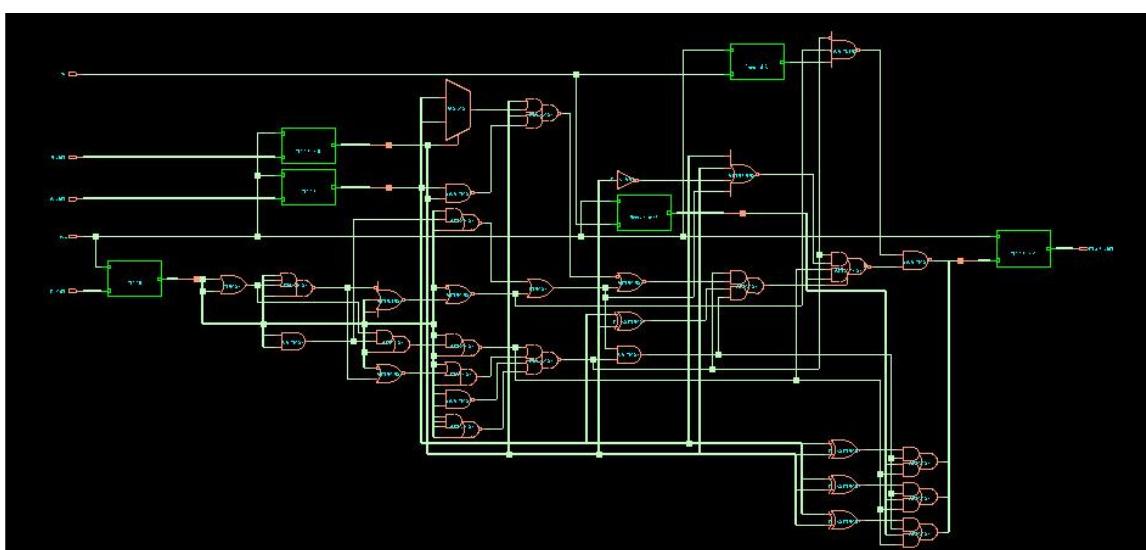
QoR ANALYSIS AND COMPARISION

QoR	CASE 1 MINIMUM AREA	CASE 2 BEST TIMING	CASE 3 COMPROMISED CASE
AREA (um ²)	644.122	763.712	680.453
SLACK (ps)	13347	-1	5706
NO. OF CELLS	73	78	73

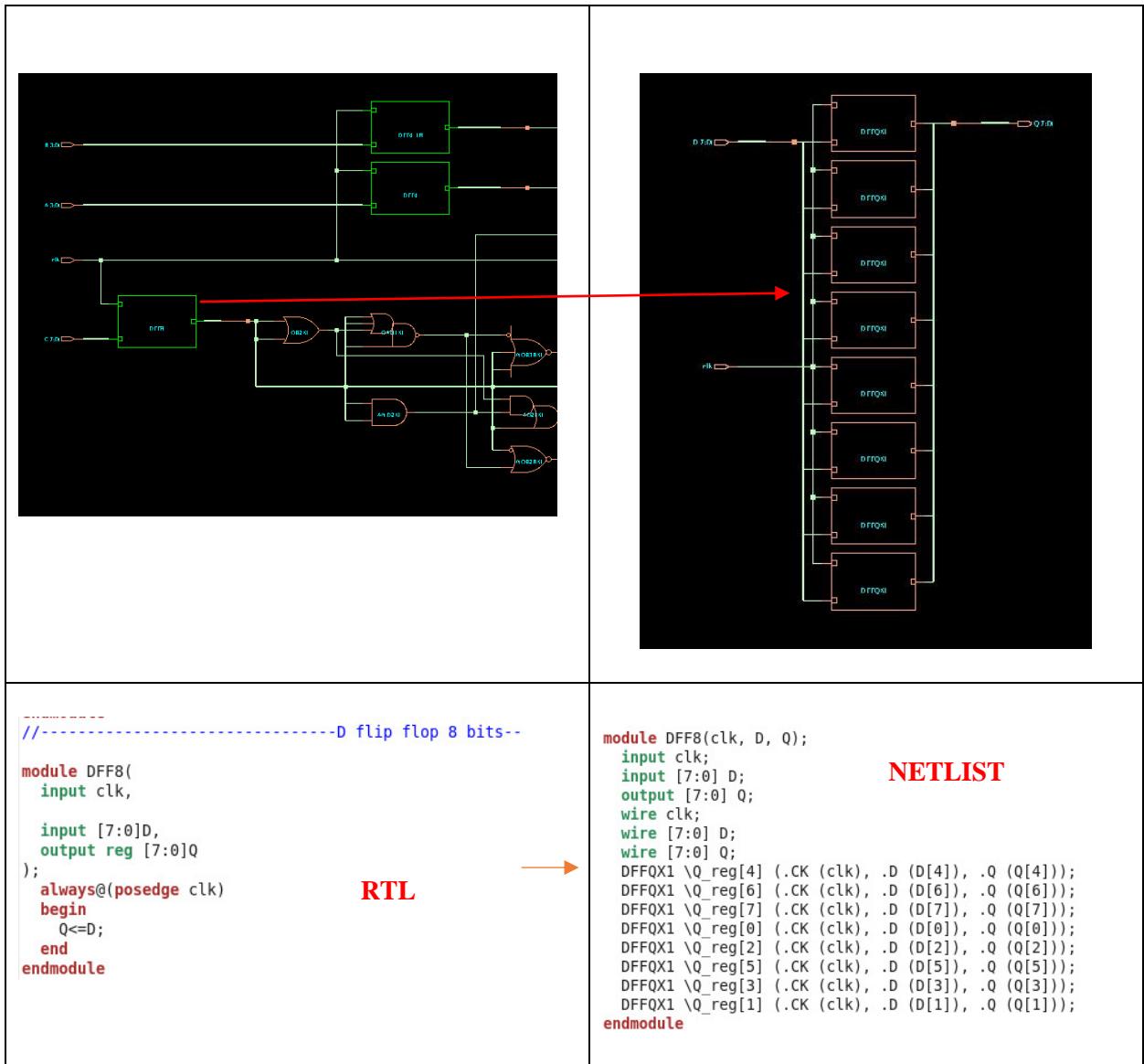
- Minimum area obtained is 644.122 unit², Slack is 13347ps and number of cells used is 73 in case-1. We kept the constraints relaxed in this case so that the tool will map to the smaller area cells to met the constraints. To achieve this, time period of clock is kept 15 unit.
- In case-2, we needed to obtain slight negative slack (-1ps). To achieve this, we kept the timing constraints tight in this case by reducing the time period of the clock so as to decrease the required time such that slack becomes negative. Area is 763.712 unit² which is increased as compared to minimum area constraint (case-1). The tool has used large size cells in this case to prevent slack violation. Hence, area is coming out to be large in this case. Also, the number of cells used in increased in this case to 78.
- Case-3 is compromised case between best timing and minimum area. For that purpose, we kept the constraints between both the cases. We can observe the area, slack and number of cells used are all moderate values (i.e., between the two extreme cases).
- We can observe that changing the clock period has made significant changes in the QoR results.

RTL TO NETLIST MAPPING

The netlist for the written RTL code is generated by the tool and the schematic for the same is shown after the optimization. After optimization some modules like bitwise xor in our RTL are optimized by the tool and hence no separate blocks are shown for them and the rest modules are shown below with the corresponding netlist generated along with their schematic.

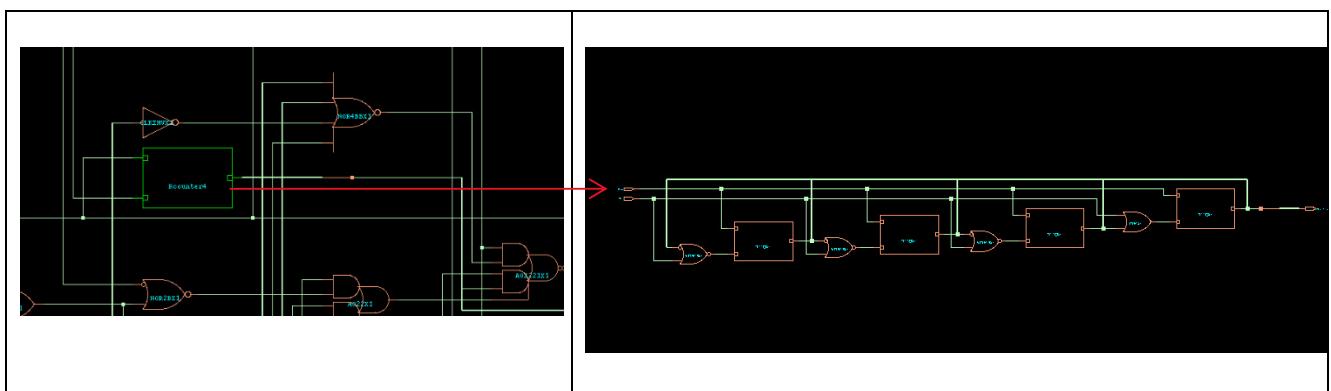


- [RTL MODULE: DFF8](#)



Module DFF8 in RTL is mapped to 8 DFFs in the netlist with appropriate pin connections shown in the netlist and schematic.

- [RTL MODULE: Rcounter4](#)



```

//-----Ring counter-----
module Rcounter4(
    input clk,
    input rst,
    output reg [3:0]out1
);

    always @ (posedge clk)
    begin
        if(rst == 1'b1) begin
            out1 <= 4'b0001;
        end
        else begin
            out1 <= {out1[2:0],out1[3]};
        end
    end
endmodule

```

RTL

```

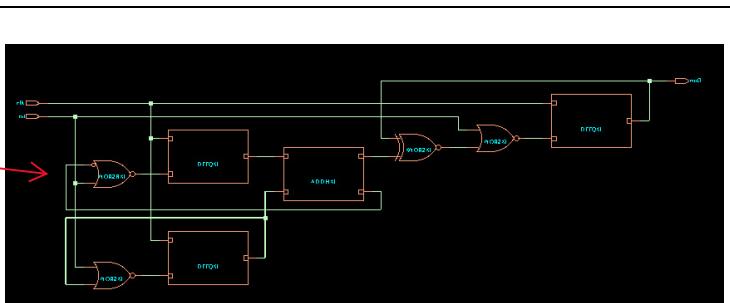
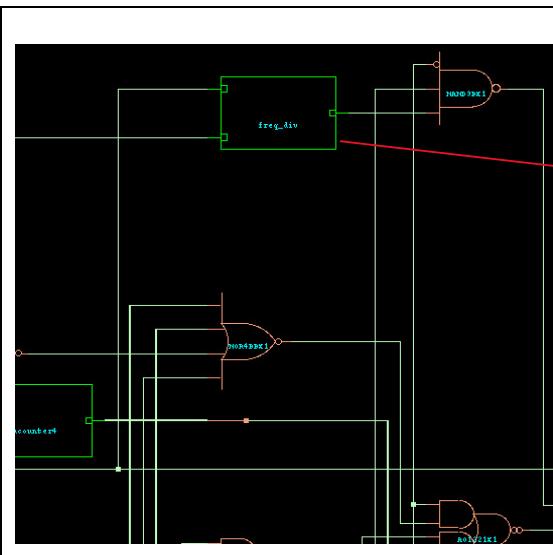
module Rcounter4(clk, rst, out1);
    input clk, rst;
    output [3:0] out1;
    wire clk, rst;
    wire [3:0] out1;
    wire n_0, n_1, n_2, n_3;
    DFFQX1 \out1_reg[3] (.CK (clk), .D (n_3), .Q (out1[3]));
    NOR2BX1 g4(.AN (out1[2]), .B (rst), .Y (n_3));
    DFFQX1 \out1_reg[2] (.CK (clk), .D (n_2), .Q (out1[2]));
    NOR2BX1 g6(.AN (out1[1]), .B (rst), .Y (n_2));
    DFFQX1 \out1_reg[1] (.CK (clk), .D (n_1), .Q (out1[1]));
    NOR2BX1 g8(.AN (out1[0]), .B (rst), .Y (n_1));
    DFFQX1 \out1_reg[0] (.CK (clk), .D (n_0), .Q (out1[0]));
    OR2X1 g9(.A (rst), .B (out1[3]), .Y (n_0));
endmodule

```

NETLIST

Module Rcounter4 is mapped to perform 4 bit ring counter in the netlist using 4 DFF, 3 NOR and 1 OR cell. Pin connections are shown in the schematic as well as it can be observed in the netlist generated.

- **RTL MODULE: freq_divider**



```

//-----Frequency Divider-----
module freq_div (
    input clk,
    input rst,
    output out3
);
    reg [3:0]temp;
    always @ (posedge clk)
    begin
        if(rst)
            temp <=4'b0000;
        else
            temp <= temp + 1;
    end
    assign out3=temp[2];
endmodule

```

RTL

```

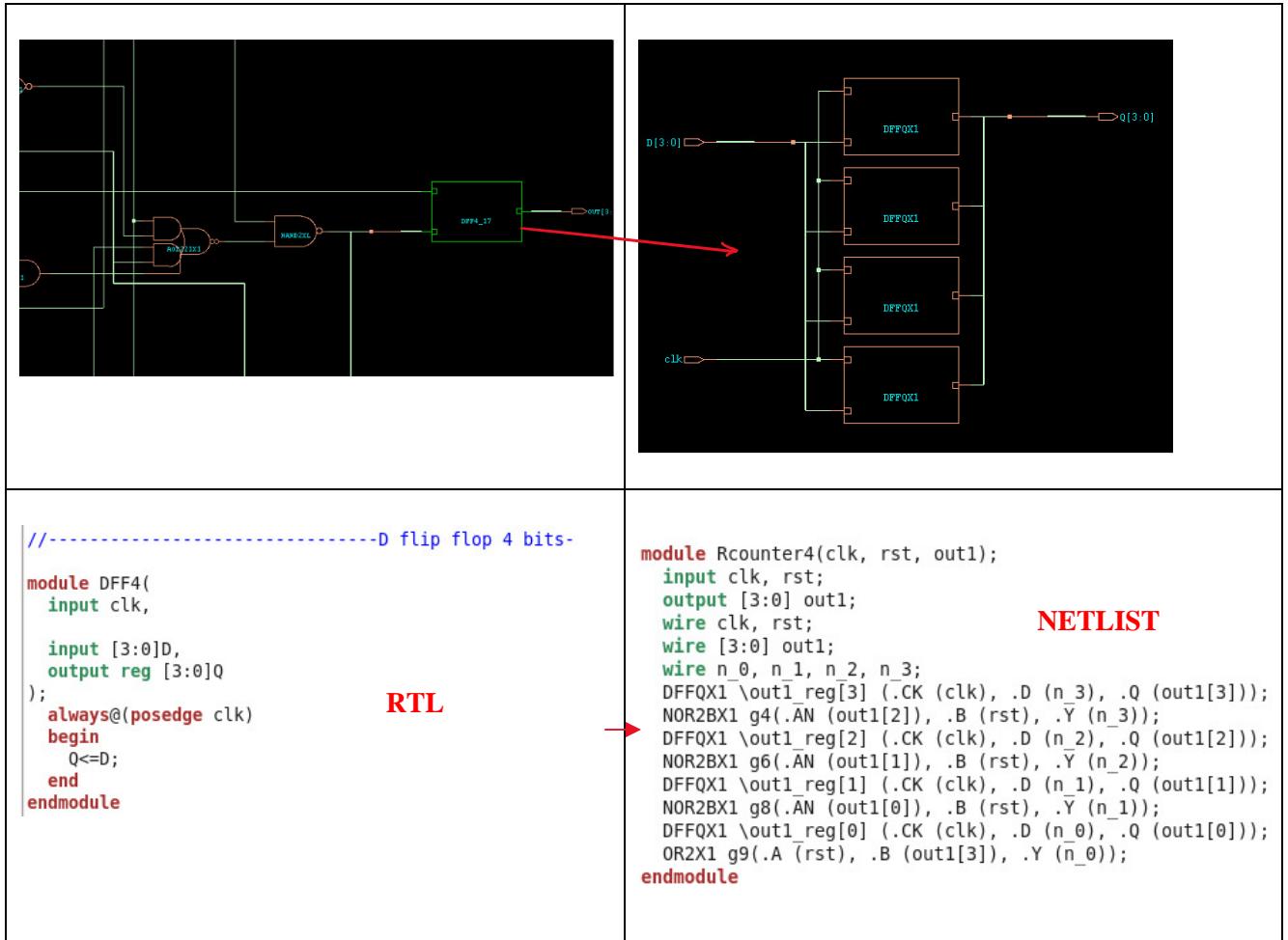
module freq_div(clk, rst, out3);
    input clk, rst;
    output out3;
    wire clk, rst;
    wire out3;
    wire [3:0] temp;
    wire n_0, n_1, n_2, n_3, n_4, n_5;
    DFFQX1 \temp_reg[2] (.CK (clk), .D (n_5), .Q (out3));
    NOR2XL g56(.A (rst), .B (n_4), .Y (n_5));
    DFFQX1 \temp_reg[1] (.CK (clk), .D (n_3), .Q (temp[1]));
    XNOR2X1 g58(.A (out3), .B (n_1), .Y (n_4));
    NOR2BX1 g59(.AN (n_2), .B (rst), .Y (n_3));
    ADDHX1 g60(.A (temp[1]), .B (temp[0]), .CO (n_1), .S (n_2));
    DFFQX1 \temp_reg[0] (.CK (clk), .D (n_0), .Q (temp[0]));
    NOR2XL g62(.A (rst), .B (temp[0]), .Y (n_0));
endmodule

```

NETLIST

Freq_divider module is mapped to perform frequency divider by 8 circuit. The netlist contains 3 DFFs, 3 NOR cells, 1 XNOR and 1 adder to get the functionality of 8-bit upcounter.

- RTL MODULE: DFF4



Similar to DFF8, DFF4 is mapped to 4 DFF cells in the netlist and schematic as shown.

STEP – 4

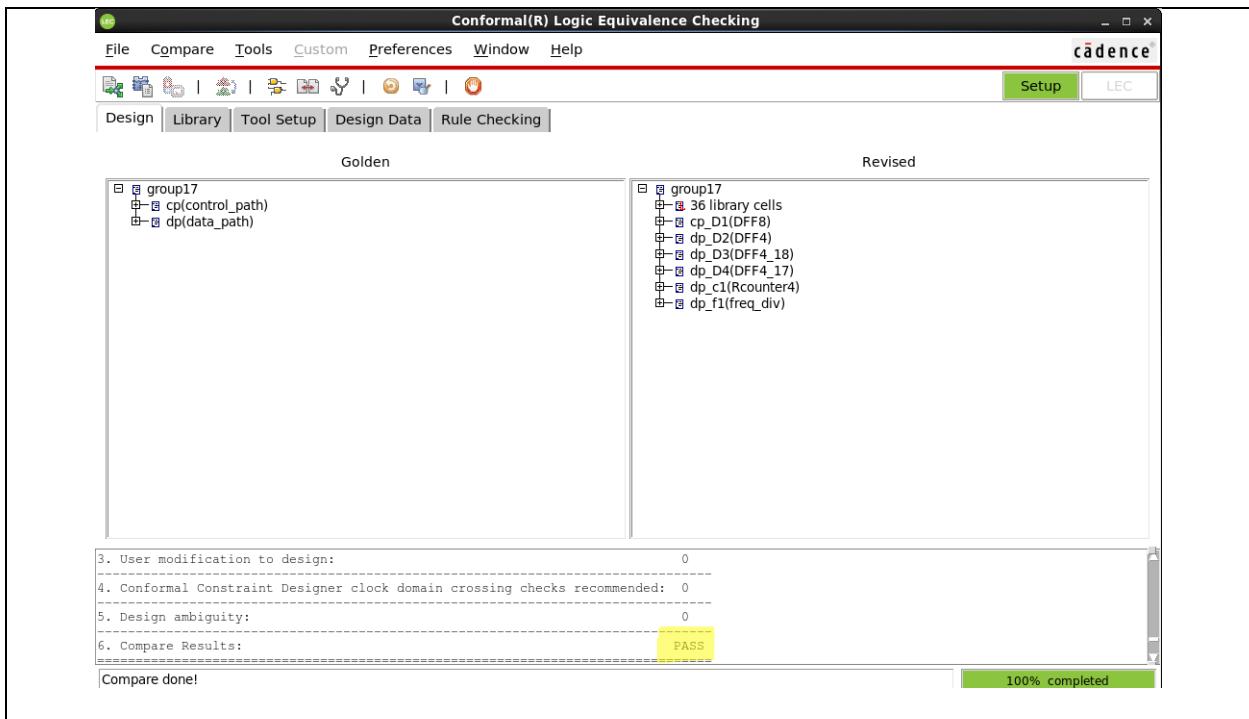
FORMAL EQUIVALENCE CHECKING

TOOL USED: Cadence Conformal LEC

Formal Equivalence Checking is done to verify and compare if the golden RTL and synthesised netlist is equivalent or not. We have performed checking for all the three cases and achieved PASS result for all the cases which means there are no equivalence violations in the design. Results are shown below:

CASE-1: MINIMUM AREA

Conformal LEC Report



Report

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	PASS

```

Mapped points: SYSTEM class
=====
  Mapped points    PI    PO    DFF    Total
  -----
  Golden          18     4     27     49
  Revised         18     4     27     49
=====

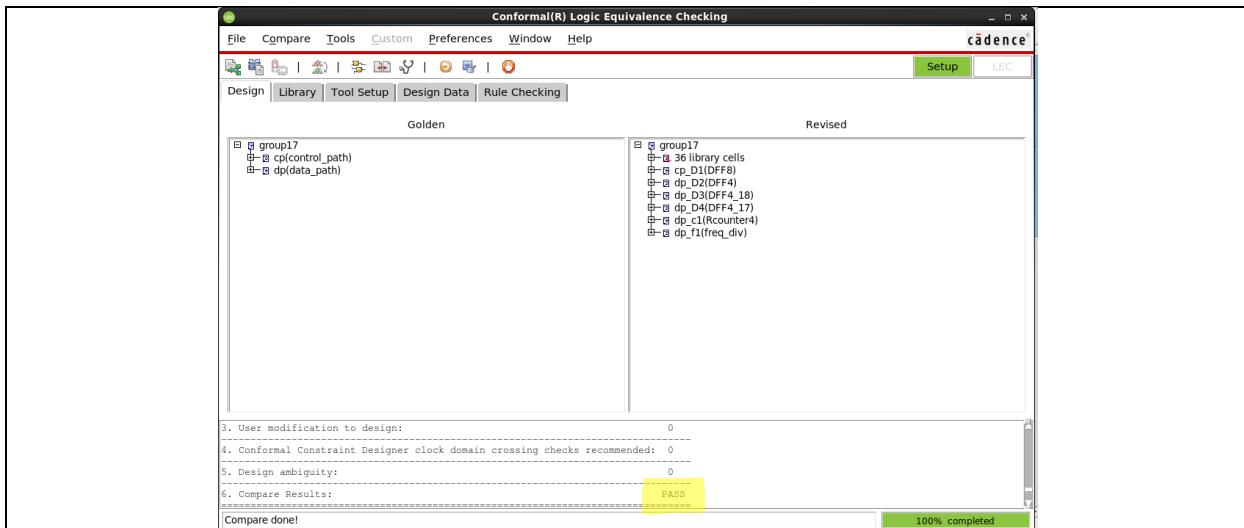
Unmapped points:
=====
Golden:
=====
  Unmapped points    DFF    Total
  -----
  Unreachable        1      1
  -----
  0
// Command: add_compared_points -all
// 31 compared points added to compare list
0
// Command: compare
=====
  Compared points    PO    DFF    Total
  -----
  Equivalent         4     27     31
  -----

```

We can observe that total 49 points are mapped from RTL to netlist and 31 equivalent points are compared and we are getting PASS result.

CASE-2: BEST TIMING CONSTRAINT

Conformal LEC Report



Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	PASS

```

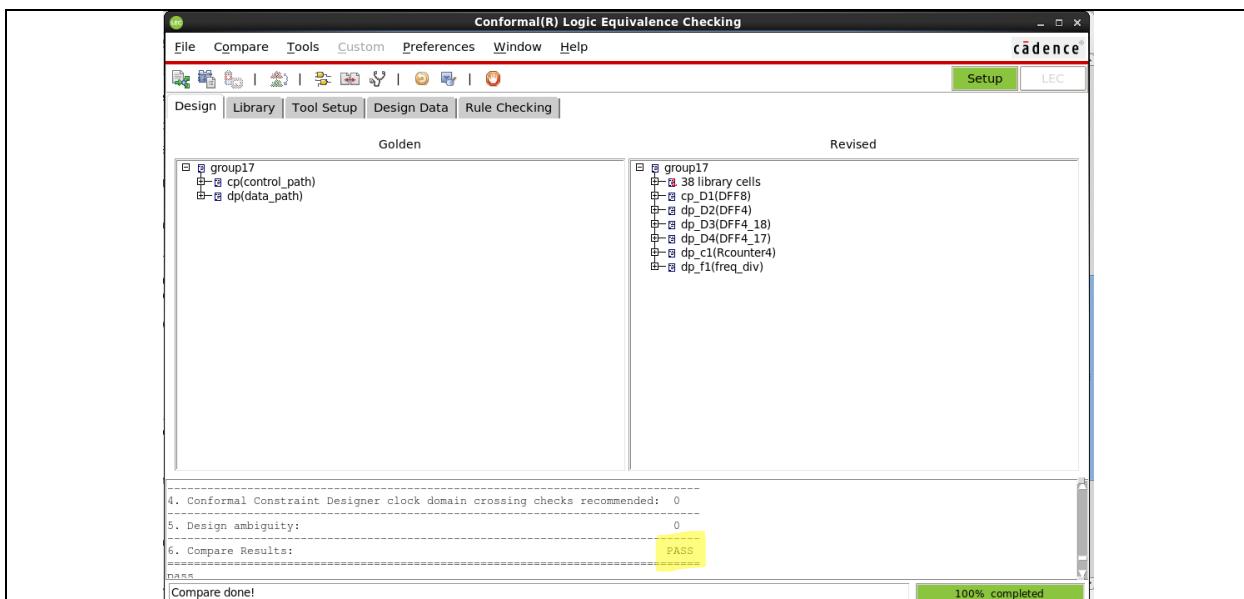
=====
      Mapped points: SYSTEM class
=====
      Mapped points    PI    PO    DFF   Total
      -----
      Golden          18     4    27    49
      Revised         18     4    27    49
      -----
      Unmapped points:
      -----
      Golden:
      -----
      Unmapped points    DFF   Total
      -----
      Unreachable        1     1
      -----
      0
      // Command: add_compared_points -all
      // 31 compared points added to compare list
      0
      // Command: compare
      -----
      Compared points    PO    DFF   Total
      -----
      Equivalent         4     27    31
      -----

```

We can observe that total 49 points are mapped from RTL to netlist and 31 equivalent points are compared and we are getting PASS result.

CASE-3: COMPROMISED CASE

Conformal LEC Report



===== Verification Report =====	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	PASS

===== Mapped points: SYSTEM class =====				
Mapped points	PI	P0	DFF	Total
Golden	18	4	27	49
Revised	18	4	27	49

===== Unmapped points: =====				
Golden:				
Unmapped points	DFF	Total		
Unreachable	1	1		

===== 0 // Command: add_compared_points -all // 31 compared points added to compare list 0 // Command: compare =====				
Compared points	P0	DFF	Total	
Equivalent	4	27	31	

We can observe that total 49 points are mapped from RTL to netlist and 31 equivalent points are compared and we are getting PASS result.

BAD-NETLIST LEC

Various experiments were performed by making some changes in the netlist to analyse the results and study the failures. We have performed total 7 experiments shown below:

1. Experiment – 1

A 4 bit input [3:0] D is removed from the module named DFF4.

```
module DFF4(clk, Q); // D input removed from here
  input clk;
  //input [3:0] D;
  output [3:0] Q;
  wire clk;
  wire [3:0] D;
  wire [3:0] Q;
  DFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .Q (Q[3]));
  DFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .Q (Q[2]));
  DFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .Q (Q[0]));
  DFFQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .Q (Q[1]));
endmodule

module DFF4_18(clk, D, Q);
  input clk;
  input [3:0] D;
  output [3:0] Q;
  wire clk;
  wire [3:0] D;
  wire [3:0] Q;
  DFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .Q (Q[3]));
  DFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .Q (Q[2]));
  DFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .Q (Q[0]));
  DFFQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .Q (Q[1]));
endmodule
```

Figure – Changed netlist

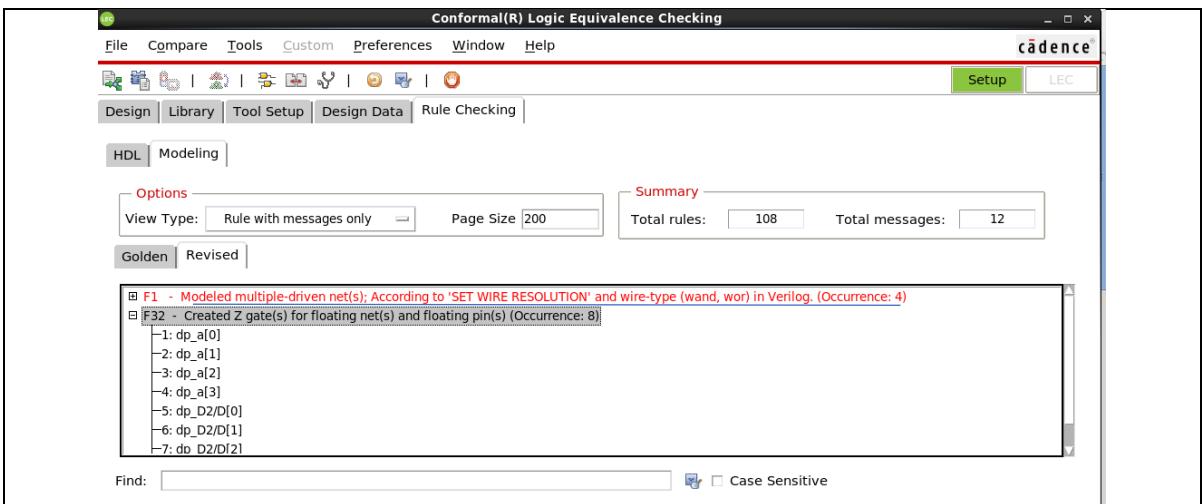


Figure – Error Report

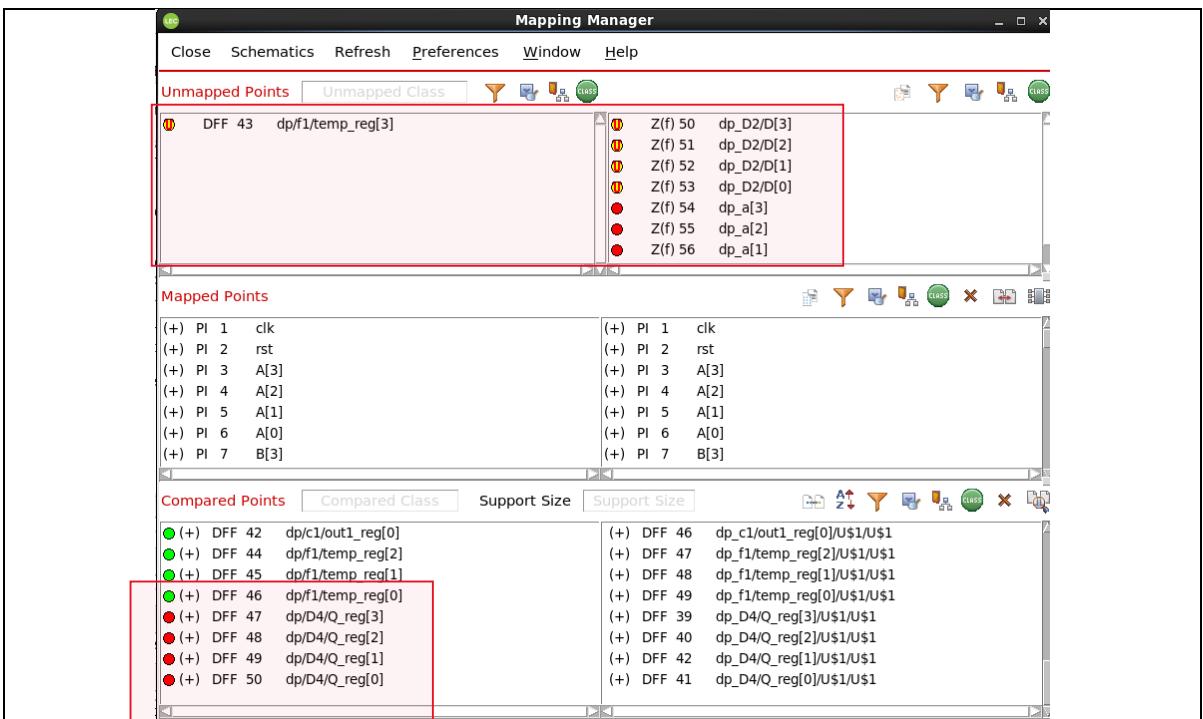


Figure – Unmapped, mapped and Compared points

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

Figure – Verification Report

2. Experiment – 2

Here, name of the output port ‘OUT’ is replaced with name ‘OUTPUT’.

```

module group17(clk, rst, A, B, C, OUTPUT); // out changed to output
  input clk, rst;
  input [3:0] A, B;
  input [7:0] C;
  output [3:0] OUTPUT;
  wire clk, rst;
  wire [3:0] A, B;
  wire [7:0] C;
  wire [3:0] OUT;
  wire [7:0] cp_c;
  wire [3:0] dp_a;
  wire [3:0] dp_b;
  wire [3:0] dp_out1;
  wire dp_out3, n_0, n_1, n_2, n_3, n_4, n_5, n_6;
  wire n_7, n_8, n_9, n_10, n_11, n_12, n_13, n_14;
  wire n_15, n_16, n_17, n_18, n_19, n_20, n_21, n_22;
  wire n_23, n_24, n_25, n_26, n_27, n_28, n_29, n_30;
  wire n_31, n_32, n_33, n_34, n_35, n_36, n_37;
  DFF8 cp_D1(clk, C, cp_c);
  DFF4 dp_D2(clk, A, dp_a);
  DFF4 18 dp_D3(clk, B, dp_b);
  DFF4 17 dp_D4(clk, {n_37, n_36, n_35, n_34}, OUT);
  RCounter4 dp_c1(clk, rst, dp_out1);
  freq_div dp_f1(clk, rst, dp_out3);
  OA121XL g964(.A0(n_32), .A1(n_5), .B0(n_31), .C0(n_33), .Y(n_34));
  OA121XL g965(.A0(n_6), .A1(n_32), .B0(n_26), .Y(n_37));
  OA122XL g966(.A0(dp_out3), .A1(n_29), .B0(dp_out1[0]), .B1(n_21), .C0(n_28), .C1(n_30), .Y(n_33));

```

Figure – Changed netlist

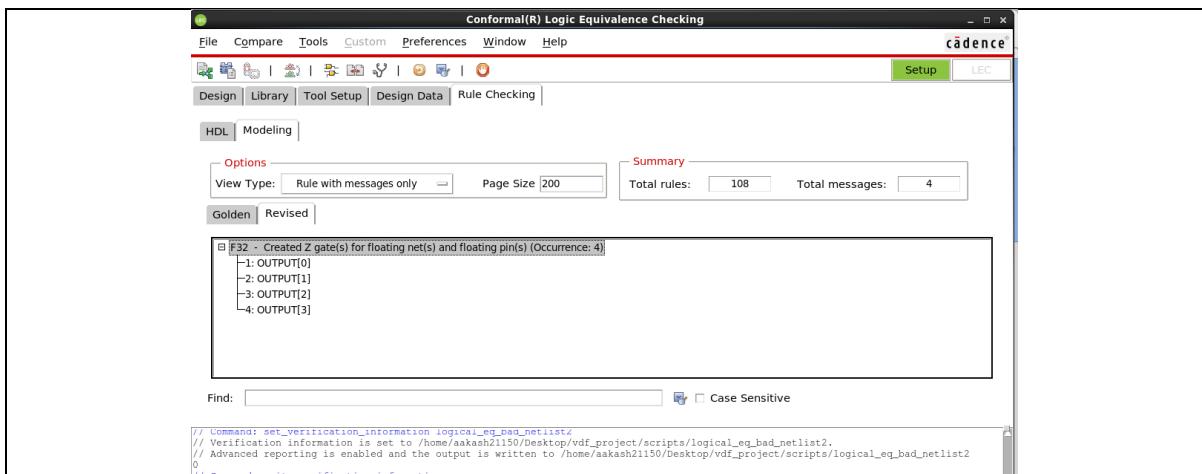


Figure – Error Report

We are getting 4 floating points or unmapped point. Due to changed name of the port, tool is not able to detect the output port with this name.

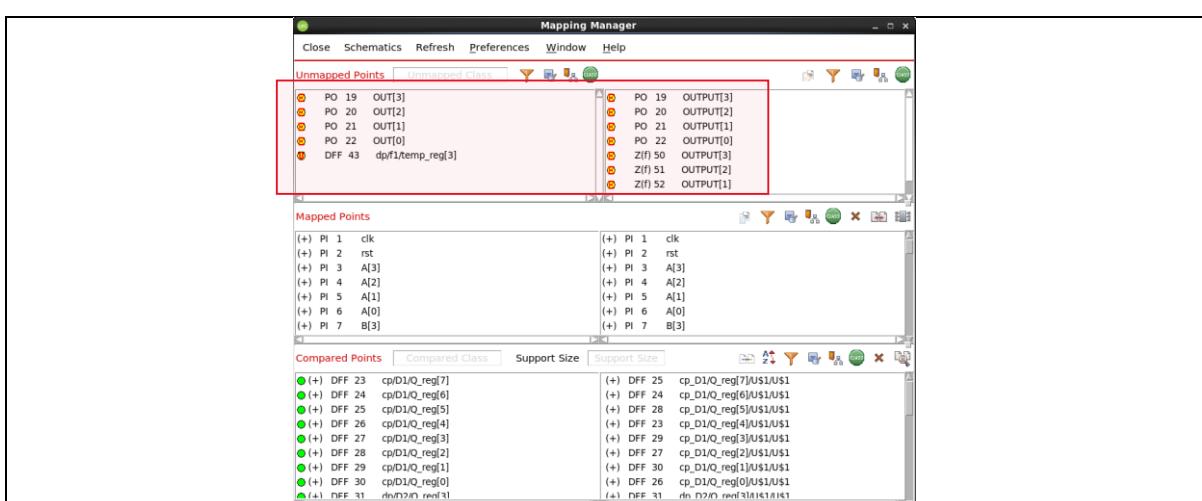


Figure – Unmapped, mapped and Compared points

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification: All primary outputs are mapped:	1 no
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity: Revised design has abnormal ratio of unreachable gates: yes Ratio of revised unreachable gates:	1 63%
6. Compare Results:	FAIL:INCOMPLETE

Figure – Verification Report

3. Experiment – 3

Here, we have given wrong net to the pin A shown in the commented netlist. Instead of out3 we gave it as ‘n_2’ (instantiating with wrong net) in freq_divider module..

```
module freq_div(clk, rst, out3);
    input clk, rst;
    output out3;
    wire clk, rst;
    wire out3;
    wire [3:0] temp;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6;
    DFFQX1 \temp_reg[2] (.CK (clk), .D (n_6), .Q (out3));
    NOR2XL g56(.A (rst), .B (n_5), .Y (n_6));
    DFFQX1 \temp_reg[1] (.CK (clk), .D (n_3), .Q (temp[1]));
    AOI21XL g58(.A0 (out3), .A1 (n_1), .B0 (n_4), .Y (n_5));
    NOR2XL g59(.A (n_2), .B (n_1), .Y (n_4)); // giving n_2 instead of out 3
    NOR2XL g60(.A (rst), .B (n_2), .Y (n_3));
    DFFQX1 \temp_reg[0] (.CK (clk), .D (n_0), .Q (temp[0]));
    OAI21XL g62(.A0 (temp[1]), .A1 (temp[0]), .B0 (n_1), .Y (n_2));
    NAND2XL g63(.A (temp[0]), .B (temp[1]), .Y (n_1));
    NOR2XL g64(.A (temp[0]), .B (rst), .Y (n_0));
endmodule
```

Figure – Changed netlist

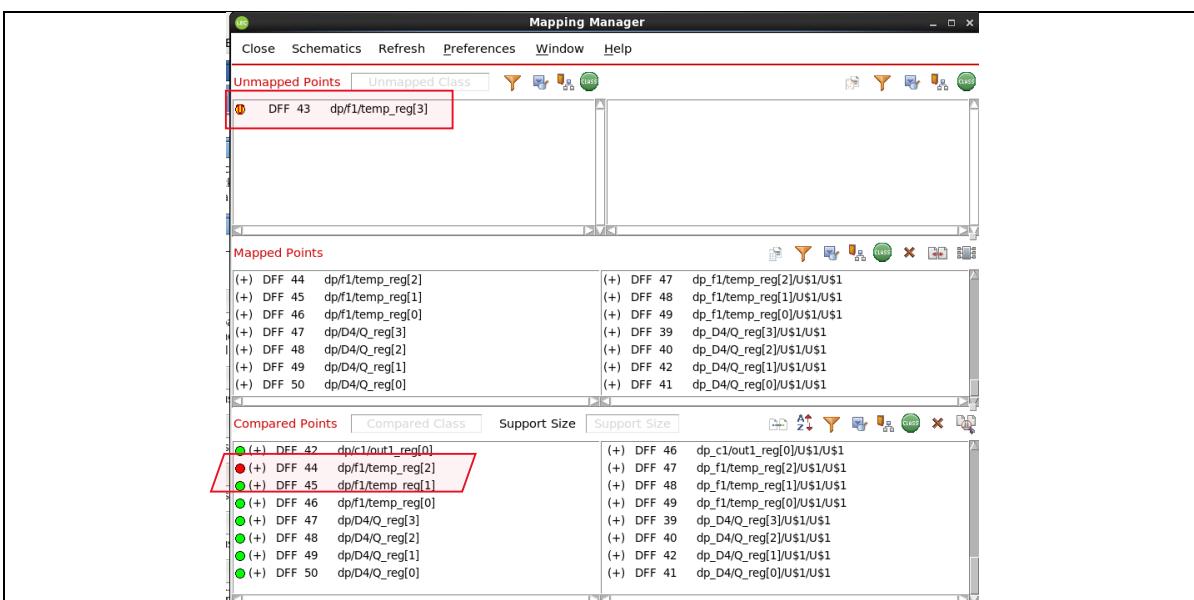


Figure – Unmapped, mapped and Compared points

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

Figure – Verification Report

4. Experiment – 4

In Rcounter4, we changed the combinational logic i.e., we replaced the NOR cell with the NAND cell.

```

module Rcounter4(clk, rst, out1);
    input clk;
    output [3:0] out1;
    wire clk, rst;
    wire [3:0] out1;
    wire n_0, n_1, n_2, n_3;
    DFFQX1 \out1_reg[3] (.CK (clk), .D (n_3), .Q (out1[3]));
    NAND2BX1 g4(.AN (out1[2]), .B (rst), .Y (n_3));// NAND2 instead of NOR2
    DFFQX1 \out1_reg[2] (.CK (clk), .D (n_2), .Q (out1[2]));
    NOR2BX1 g6(.AN (out1[1]), .B (rst), .Y (n_2));
    DFFQX1 \out1_reg[1] (.CK (clk), .D (n_1), .Q (out1[1]));
    NOR2BX1 g8(.AN (out1[0]), .B (rst), .Y (n_1));
    DFFQX1 \out1_reg[0] (.CK (clk), .D (n_0), .Q (out1[0]));
    OR2X1 g9(.A (out1[3]), .B (rst), .Y (n_0));
endmodule

```

Figure – Changed netlist

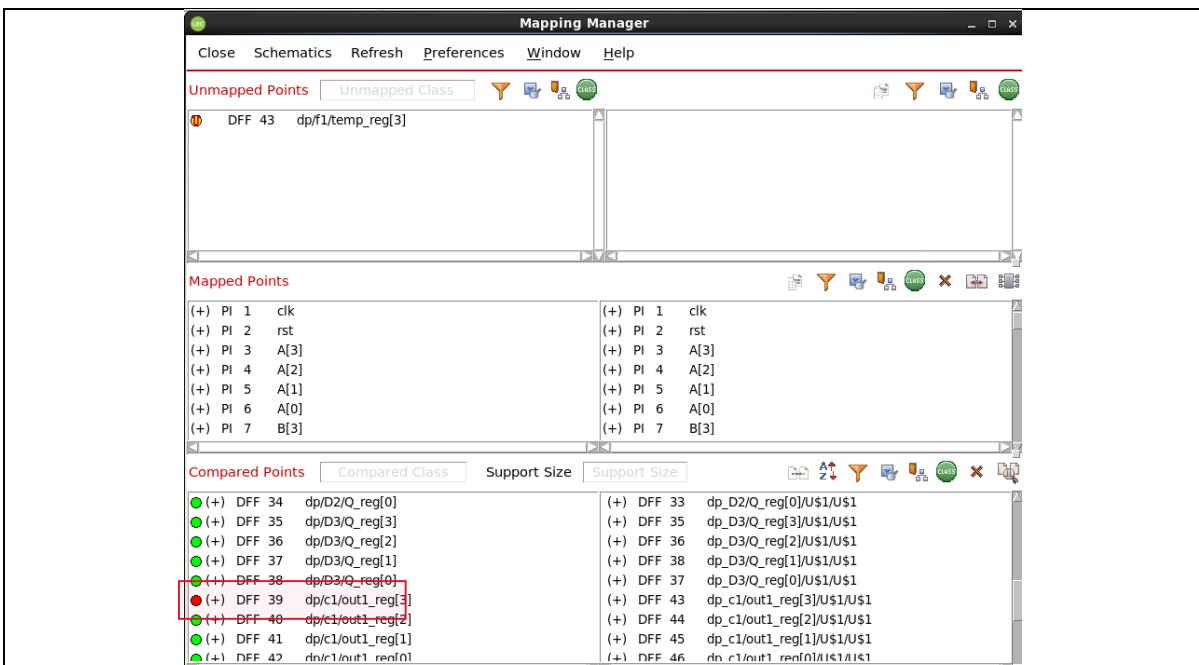


Figure – Unmapped, mapped and Compared points

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

Figure – Verification Report

5. Experiment – 5

Here, while instantiating DFFX1 in module DFF8 the ports clk and D are interchanged i.e, kept it as D[4] and clk respectively.

```
module DFF8(clk, D, Q);
  input clk;
  input [7:0] D;
  output [7:0] Q;
  wire clk;
  wire [7:0] D;
  wire [7:0] Q;
  DFFQX1 \Q_reg[4] (.CK (D[4]), .D (clk), .Q (Q[4])); // D[4] and clk interchange while
  DFFQX1 \Q_reg[6] (.CK (clk), .D (D[6]), .Q (Q[6]));
  DFFQX1 \Q_reg[7] (.CK (clk), .D (D[7]), .Q (Q[7]));
  DFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .Q (Q[0]));
  DFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .Q (Q[2]));
  DFFQX1 \Q_reg[5] (.CK (clk), .D (D[5]), .Q (Q[5]));
  DFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .Q (Q[3]));
  DFFQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .Q (Q[1]));
endmodule
```

Figure – Changed netlist

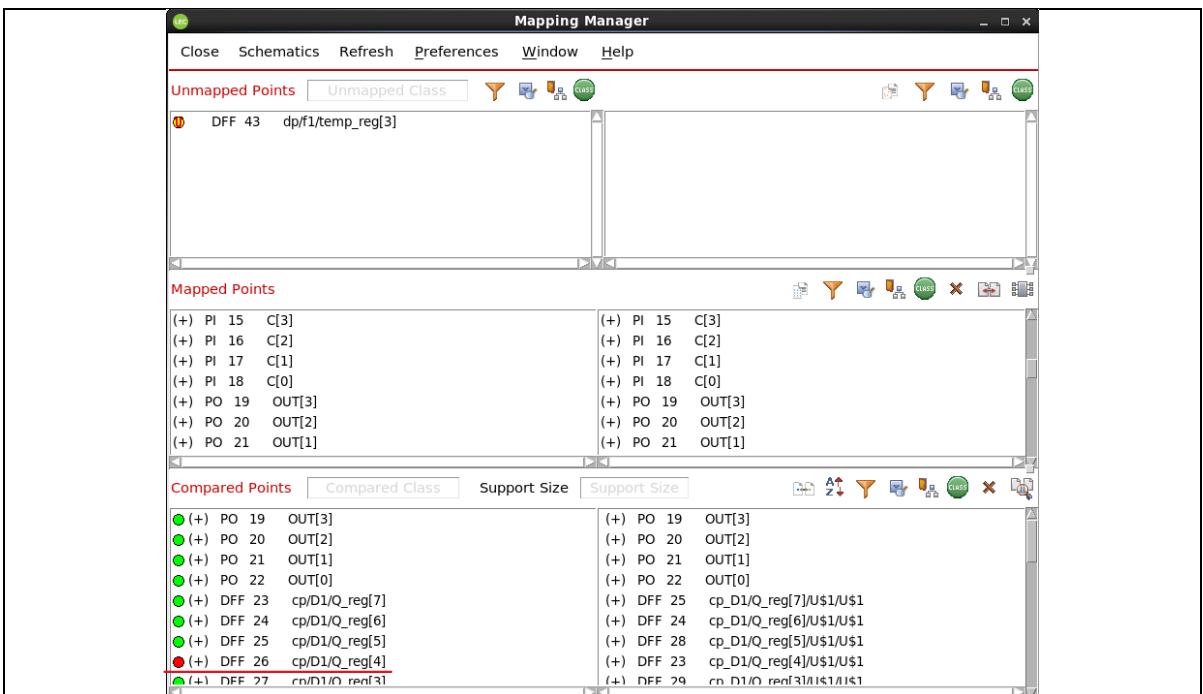


Figure – Unmapped, mapped and Compared points

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended: 1 Multiple clocks in the design:	yes
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

Figure – Verification Report

6. Experiment – 6

In this experiment, we deleted one cell of inverter. Inverter INX1 is deleted.

```

NOR2XL g971(.A (n_22), .B (n_21), .Y (n_30));
CLKINVX1 g972(.A (n_27), .Y (n_29));
OAI211X1 g973(.A0 (cp_c[6]), .A1 (n_16), .B0 (cp_c[7]), .C0 (n_28),
.Y (n_27));
AOI21X1 g974(.A0 (cp_c[7]), .A1 (n_19), .B0 (n_18), .Y (n_28));
NAND2XL g975(.A (dp_out1[3]), .B (n_21), .Y (n_26));
NAND2XL g976(.A (dp_out1[2]), .B (n_21), .Y (n_25));
NAND2XL g977(.A (dp_out1[1]), .B (n_21), .Y (n_24));
NOR3XL g978(.A (dp_b[0]), .B (n_8), .C (n_21), .Y (n_23));
OAI221X1 g979(.A0 (dp_a[3]), .A1 (n_0), .B0 (dp_a[1]), .B1 (dp_b[1]),
.C0 (dp_b[0]), .Y (n_22));
OAI2BB1XL1 g980(.A0N (n_1), .AIN (n_9), .B0 (cp_c[6]), .Y (n_20));
OAI21X1 g981(.A0 (cp_c[7]), .A1 (n_13), .B0 (n_15), .Y (n_21));
INVXL g982(.A (n_17), .Y (n_19));
AOI211X1 g983(.A0 (cp_c[3]), .A1 (n_2), .B0 (n_12), .C0 (n_14), .Y
(n_18));
AOI211X1 g984(.A0 (cp_c[4]), .A1 (n_11), .B0 (cp_c[6]), .C0
(cp_c[5]), .Y (n_17));
NOR2XL g985(.A (n_1), .B (n_10), .Y (n_16));
// INVXL g986(.A (n_14), .Y (n_15)); //one inverter deleted from the netlist
AOI211X1 g987(.A0 (cp_c[3]), .A1 (n_3), .B0 (cp_c[7]), .C0 (cp_c[5]),
.Y (n_14));
INVXL g988(.A (n_12), .Y (n_13));
INVXL g989(.A (n_10), .Y (n_11));
NAND4XL g990(.A (cp_c[5]), .B (cp_c[2]), .C (cp_c[3]), .D (cp_c[1]),
.Y (n_9));
AOI22XL1 g991(.A0 (dp_a[0]), .A1 (n_0), .B0 (dp_a[2]), .B1 (dp_b[1]),
.Y (n_8));
OAI21X1 g992(.A0 (cp_c[5]), .A1 (cp_c[4]), .B0 (cp_c[6]), .Y (n_12));
NOR4XL g993(.A (cp_c[0]), .B (cp_c[3]), .C (cp_c[1]), .D (cp_c[2]),
.Y (n_10));
XNOR2XL g994(.A (dp_a[2]), .B (dp_b[2]), .Y (n_7));
XNOR2XL g995(.A (dp_a[3]), .B (dp_b[3]), .Y (n_6));

```

Figure – Changed netlist

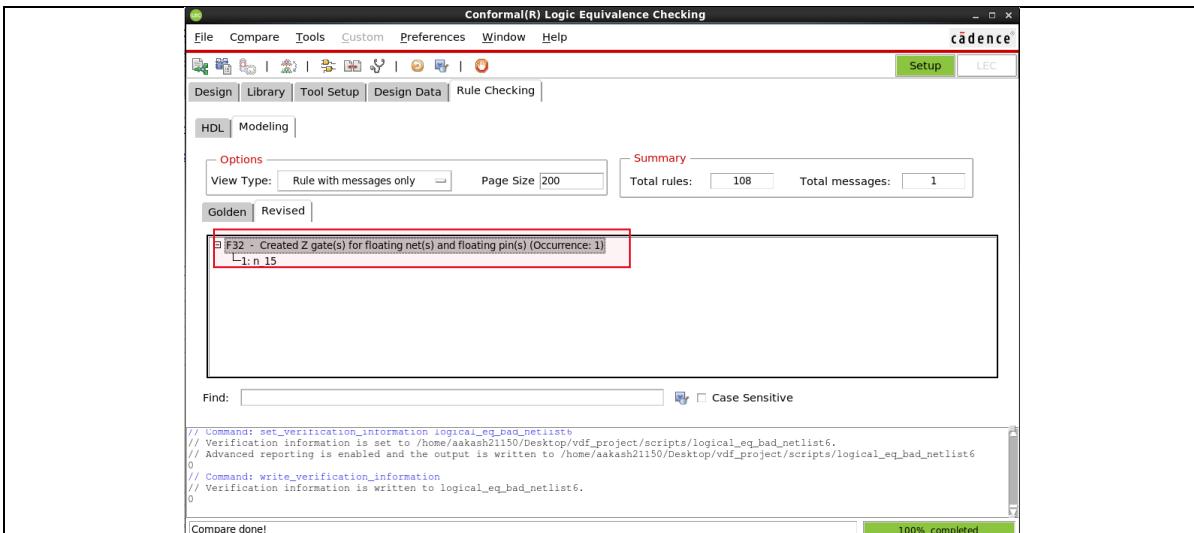


Figure – Error Report

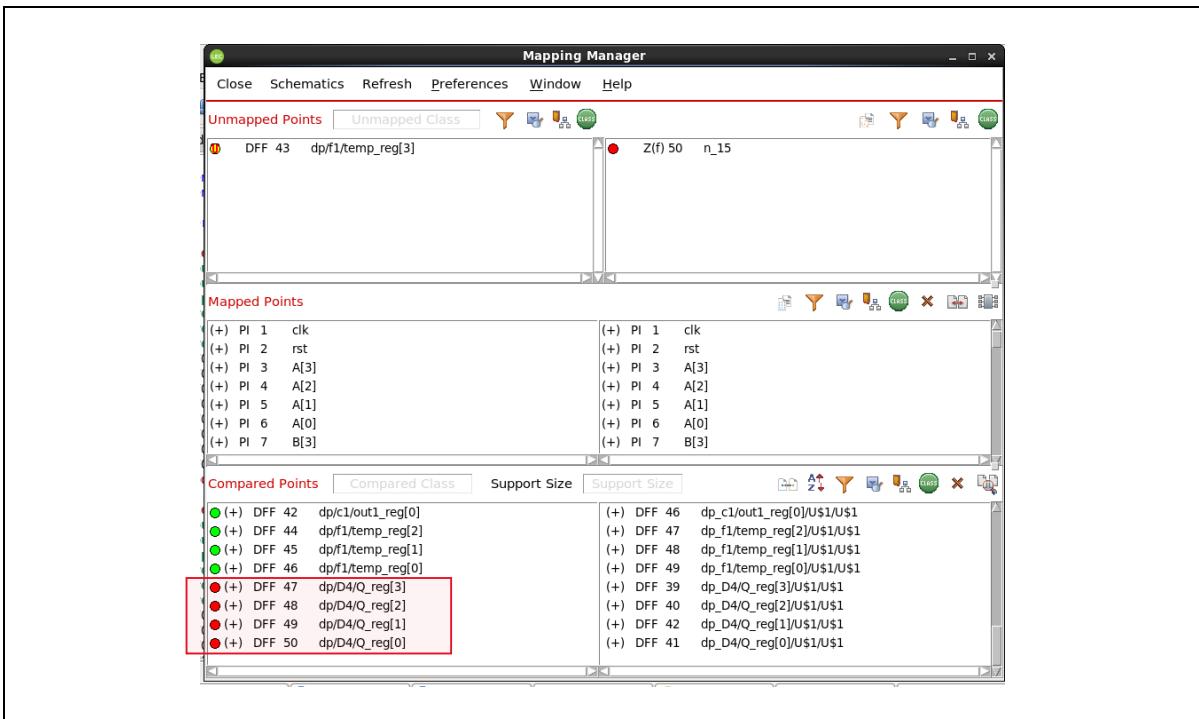


Figure – Unmapped, mapped and Compared points

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

Figure – Verification Report

7. Experiment – 7

Here, output is made of 8 bit forcefully and then a newly named wire of 8 bit is formed to provide it an arrangement while instantiating Rcounter4.

```
module Rcounter4(clk, rst, out1); // output is made of 8 bits forcefully and corresponding change is also done in group17 where instantiating
  input clk, rst;
  output [7:0] out1;
  wire clk, rst;
  wire [7:0] out1;
  wire n_0, n_1, n_2, n_3;
  DFFQX1 \out1_reg[3] (.CK (clk), .D (n_3), .Q (out1[3]));
  NOR2BX1 g4(.AN (out1[2]), .B (rst), .Y (n_3));
  DFFQX1 \out1_reg[2] (.CK (clk), .D (n_2), .Q (out1[2]));
  NOR2BX1 g6(.AN (out1[1]), .B (rst), .Y (n_2));
  DFFQX1 \out1_reg[1] (.CK (clk), .D (n_1), .Q (out1[1]));
  NOR2BX1 g8(.AN (out1[0]), .B (rst), .Y (n_1));
  DFFQX1 \out1_reg[0] (.CK (clk), .D (n_0), .Q (out1[0]));
  OR2X1 g9(.A (out1[3]), .B (rst), .Y (n_0));
endmodule
```

```

wire clk, rst;
wire [3:0] A, B;
wire [7:0] C;
wire [3:0] OUT;
wire [7:0] cp_c;
wire [3:0] dp_a;
wire [3:0] dp_b;
wire [3:0] dp_out1;
wire [7:0] newly_formed_wire; // newly formed wire
wire dp_out3, n_0, n_1, n_2, n_3, n_4, n_5, n_6;
wire n_7, n_8, n_9, n_10, n_11, n_12, n_13, n_14;
wire n_15, n_16, n_17, n_18, n_19, n_20, n_21, n_22;
wire n_23, n_24, n_25, n_26, n_27, n_28, n_29, n_30;
wire n_31, n_32, n_33, n_34, n_35, n_36, n_37;
DFF8 cp_D1(clk, C, cp_c);
DFF4 dp_D2(clk, A, dp_a);
DFF4_18 dp_D3(clk, B, dp_b);
DFF4_17 dp_D4(clk, {n_37, n_36, n_35, n_34}, OUT);
RCounter4 dp_c1(clk, rst, newly_formed_wire); // newly formed wire is provided here
freq_div dp f1(clk, rst, dp_out3);
OAI211XL g964(.A0 (n_32), .A1 (n_5), .B0 (n_31), .C0 (n_33), .Y
(n_34));
OAI21X1 g965(.A0 (n_6), .A1 (n_32), .B0 (n_26), .Y (n_37));
AOI222XL g966(.A0 (dp_out3), .A1 (n_29), .B0 (dp_out1[0]), .B1
(n_21), .C0 (n_28), .C1 (n_30), .Y (n_33));
OAI21X1 g967(.A0 (n_7), .A1 (n_32), .B0 (n_25), .Y (n_36));
OAI21X1 g968(.A0 (n_4), .A1 (n_32), .B0 (n_24), .Y (n_35));
OR2X1 g969(.A (n_29), .B (n_28), .Y (n_32));
NAND2XL g970(.A (n_23), .B (n_28), .Y (n_31));
NOR2XL g971(.A (n_22), .B (n_21), .Y (n_30));
CLKINVX1 g972(.A (n_27), .Y (n_29));
OAI211XL g973(.A0 (cp_c[6]), .A1 (n_16), .B0 (cp_c[7]), .C0 (n_20),

```

Figure – Changed netlist

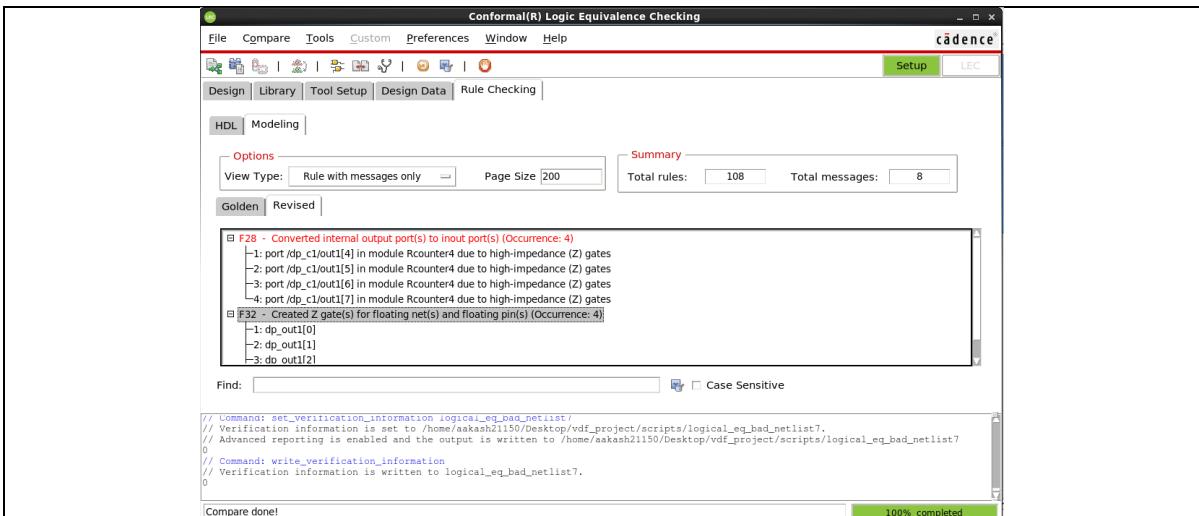


Figure – Error Report

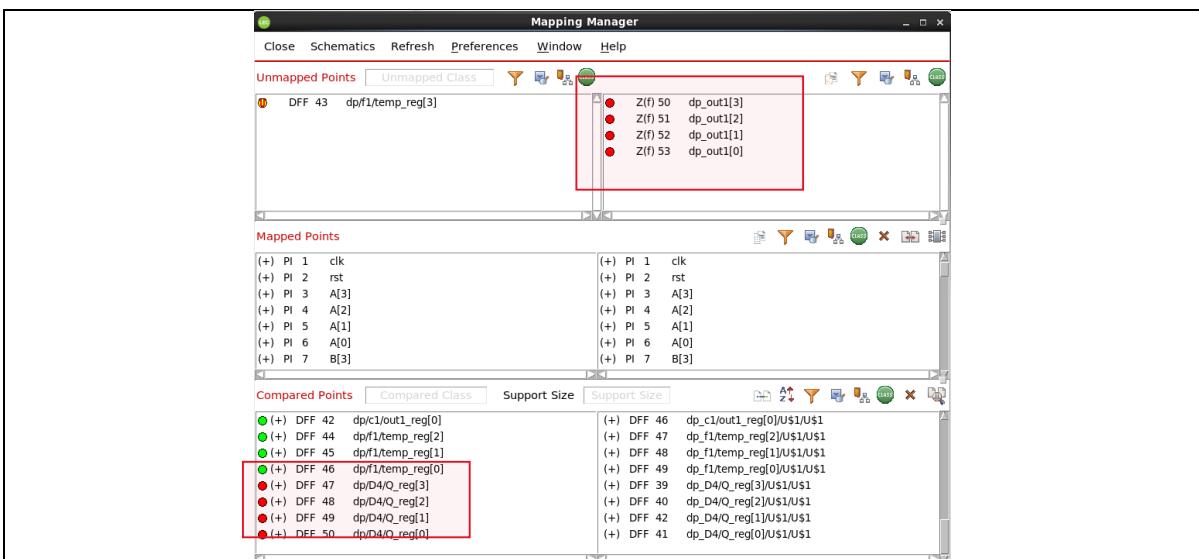


Figure – Unmapped, mapped and Compared points

Verification Report	
Category	Count
1. Non-standard modeling options used:	0
2. Incomplete verification:	0
3. User modification to design:	0
4. Conformal Constraint Designer clock domain crossing checks recommended:	0
5. Design ambiguity:	0
6. Compare Results:	FAIL:NONEQ

Figure – Verification Report

STEP – 5

STATIC TIMING ANALYSIS

STA

STA is a technique to measure whether the targeted design is following the timing constraints or not, in order to perform STA there is no need of external inputs and also the design need not to be functionally correct. The tool uses the routed netlist to perform To perform STA we have used the tool cadence tempus which is an industry standard tool. Static timing analysis' major purpose is to ensure that, despite these probable fluctuations, all signals arrive neither too early nor too late, ensuring adequate circuit operation. STA can detect other issues like as defects, sluggish routes, and clock skew because it can validate every path.

Key terminologies used along with explanation:

- **Data Arrival Time (AT)**

This is the time required for data to travel through data path.

- **Data Required Time (RT)**

This is the time taken for the clock to traverse through clock path.

- **Setup and hold slack:**

Defined as the difference between data required time and data arrival time. Slack is basically the margins to avoid violations, that is more the slack more relaxed are the constraints and vice versa.

$$\text{setup slack} = \text{Data Required Time} - \text{Data Arrival Time}$$

$$\text{hold slack} = \text{Data Arrival Time} - \text{Data Required Time}$$

- **GBA and PBA:**

GBA stands for the graph-based analysis and PBA stands for the path-based analysis, basically these two are the methods to perform STA. GBA is not the 100% correct method to perform STA as for the sake of less complexity it deals with the worst path delay and the worst slew irrespective of from which paths, they are coming from hence sometimes it may consider delay and slew from different paths. whereas is the accurate method to perform STA as it considers slew and delay on the basis of path and strictly follow the path-based dependency and hence we can say GBA provides the relaxed constraints comparatively to the PBA and hence GBA is widely used in order to save resources and PBA is used in timing critical applications where accuracy is more important. slack obtained in case of PBA is always greater or equal to slack obtained in case of PBA.

How we proceed:

1. We have made 3 different constraint files corresponding to the minimum area case, best timing case and the intermediate compromised case and performed the STA for the same.
2. In addition to above step we have run STA for all the netlist above using the constraint file of the intermediate compromised case.
3. For step 1 and 2 STA is done for both the cases that is without wireload model and with wireload model. Wireload model used is shown below.
4. Hold and setup slack for all the above cases are noted and analysed.

WIRELOAD MODEL USED:

```
/* ----- *
 * Design: Wired Load Model *
 * -----*/
wire_load("tsmc18_wl10") {
    resistance : 8.5e-8;
    capacitance : 1.5e-4;
    area : 0.7;
    slope : 66.667;
    fanout_length (1,66.667);
}
```

```
/* -----
 * Design : Wired Load Model *
 * -----*/
wire_load("tsmc18_wl10") {
    resistance : 8.5e-8;
    capacitance : 1.5e-4;
    area : 0.7;
    slope : 66.667;
    fanout_length (1,66.667);
}
```

I. STA of the netlists with its own constraint file

Case 1: Minimum Area and Relaxed Timing Constraint

	Without wireload model	With wireload model																																																																																																																																																																																																																																																	
HOLD CHECK	<pre> Path 1: MET Hold Check with Pin cp_D1/Q_reg[4]/CK Endpoint: cp_D1/Q_reg[4]/D (v) checked with leading edge of 'clk' Beginpoint: C[4] (v) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.029 + Phase Shift 0.000 + Uncertainty 0.020 = Required Time 0.049 Arrival Time 0.110 Slack Time 0.061 Clock Rise Edge 0.000 + Input Delay 0.110 = Beginpoint Arrival Time 0.110 Pin Cell Delay Slew Required Arrival Edge Wire Wireload Time Time Load Model -----</pre> <table border="1"> <tr><td>C[4]</td><td>-</td><td>0.060</td><td>0.049</td><td>0.110</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>D</td><td>DFFQX1</td><td>0.000</td><td>0.060</td><td>0.049</td><td>0.110</td><td>v</td><td>-</td></tr> </table>	C[4]	-	0.060	0.049	0.110	v	0.000	Wireload model(.lib None Generated)	D	DFFQX1	0.000	0.060	0.049	0.110	v	-	<pre> Path 1: MET Hold Check with Pin cp_D1/Q_reg[4]/CK Endpoint: cp_D1/Q_reg[4]/D (v) checked with leading edge of 'clk' Beginpoint: C[4] (v) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.029 + Phase Shift 0.000 + Uncertainty 0.020 = Required Time 0.049 Arrival Time 0.110 Slack Time 0.061 Clock Rise Edge 0.000 + Input Delay 0.110 = Beginpoint Arrival Time 0.110 Pin Cell Delay Slew Required Arrival Edge Wire Wireload Time Time Load Model -----</pre> <table border="1"> <tr><td>C[4]</td><td>-</td><td>0.060</td><td>0.049</td><td>0.110</td><td>v</td><td>0.010</td><td>Wireload model(.lib tsmc18_wl10 slow)</td></tr> <tr><td>D</td><td>DFFQX1</td><td>0.000</td><td>0.060</td><td>0.049</td><td>0.110</td><td>v</td><td>-</td></tr> </table>	C[4]	-	0.060	0.049	0.110	v	0.010	Wireload model(.lib tsmc18_wl10 slow)	D	DFFQX1	0.000	0.060	0.049	0.110	v	-																																																																																																																																																																																																																	
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	<i>Slack Time: 0.061</i>	<i>Slack Time: 0.061</i>																																																																																																																																																																																																																																																	
SETUP CHECK	<pre> Path 1: MET Setup Check with Pin dp_D4/Q_reg[0]/CK Endpoint: dp_D4/Q_reg[0]/D (^) checked with leading edge of 'clk' Beginpoint: cp_D1/Q_reg[2]/D (v) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 - Setup 0.177 + Phase Shift 15.000 - Uncertainty 0.020 = Required Time 14.803 - Arrival Time 1.479 = Slack Time 13.323 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000 Pin Cell Delay Slew Required Arrival Edge Wire Wireload Time Time Load Model -----</pre> <table border="1"> <tr><td>CK</td><td>-</td><td>0.003</td><td>13.323</td><td>0.000</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Q</td><td>DFFQX1</td><td>0.328</td><td>0.057</td><td>13.652</td><td>0.328</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>NOR2XL</td><td>0.158</td><td>0.184</td><td>13.810</td><td>0.456</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>INVX1</td><td>0.054</td><td>0.067</td><td>13.864</td><td>0.546</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>AOI31X1</td><td>0.133</td><td>0.154</td><td>13.997</td><td>0.674</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>NOR2XL</td><td>0.871</td><td>0.876</td><td>14.068</td><td>0.744</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>AOI21X1</td><td>0.093</td><td>0.092</td><td>14.161</td><td>0.838</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>AOI32X1</td><td>0.151</td><td>0.312</td><td>14.312</td><td>0.988</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>NOR2BX1</td><td>0.190</td><td>0.193</td><td>14.511</td><td>1.188</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>AOI32X1</td><td>0.097</td><td>0.174</td><td>14.608</td><td>1.285</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>AOI31X1</td><td>0.879</td><td>0.174</td><td>14.688</td><td>1.364</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>AOI21X1</td><td>0.859</td><td>0.896</td><td>14.746</td><td>1.423</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>AOI2BBX1</td><td>0.056</td><td>0.052</td><td>14.803</td><td>1.479</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>D</td><td>DFFQX1</td><td>0.000</td><td>0.052</td><td>14.803</td><td>1.479</td><td>^</td><td>-</td><td>-</td></tr> </table>	CK	-	0.003	13.323	0.000	^	0.000	Wireload model(.lib None Generated)	Q	DFFQX1	0.328	0.057	13.652	0.328	v	0.000	Wireload model(.lib None Generated)	Y	NOR2XL	0.158	0.184	13.810	0.456	^	0.000	Wireload model(.lib None Generated)	Y	INVX1	0.054	0.067	13.864	0.546	v	0.000	Wireload model(.lib None Generated)	Y	AOI31X1	0.133	0.154	13.997	0.674	^	0.000	Wireload model(.lib None Generated)	Y	NOR2XL	0.871	0.876	14.068	0.744	v	0.000	Wireload model(.lib None Generated)	Y	AOI21X1	0.093	0.092	14.161	0.838	^	0.000	Wireload model(.lib None Generated)	Y	AOI32X1	0.151	0.312	14.312	0.988	v	0.000	Wireload model(.lib None Generated)	Y	NOR2BX1	0.190	0.193	14.511	1.188	^	0.000	Wireload model(.lib None Generated)	Y	AOI32X1	0.097	0.174	14.608	1.285	v	0.000	Wireload model(.lib None Generated)	Y	AOI31X1	0.879	0.174	14.688	1.364	^	0.000	Wireload model(.lib None Generated)	Y	AOI21X1	0.859	0.896	14.746	1.423	v	0.000	Wireload model(.lib None Generated)	Y	AOI2BBX1	0.056	0.052	14.803	1.479	^	0.000	Wireload model(.lib None Generated)	D	DFFQX1	0.000	0.052	14.803	1.479	^	-	-	<pre> Path 1: MET Setup Check with Pin dp_D4/Q_reg[0]/CK Endpoint: dp_D4/Q_reg[0]/D (^) checked with leading edge of 'clk' Beginpoint: cp_D1/Q_reg[3]/D (^) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 - 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Case 2: Synthesis for Tight Timing Constraint, Slight -ve Slack

	Without wireload model	With wireload model																																																																						
HOLD CHECK	<pre> Path 1: MET Hold Check with Pin dp_f1/temp_reg[0]/CK Endpoint: dp_f1/temp_reg[0]/D (v) checked with leading edge of 'clk' Beginpoint: dp_f1/temp_reg[0]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.021 + Phase Shift 0.000 + Uncertainty 0.200 = Required Time 0.221 Arrival Time 0.329 Slack Time 0.107 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000 Pin Cell Delay Slew Required Arrival Edge Wire Wireload Time Time Load Model -----</pre> <table border="1"> <tr><td>CK</td><td>-</td><td>0.003</td><td>-0.107</td><td>0.000</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Q</td><td>DFFQX1</td><td>0.280</td><td>0.065</td><td>0.173</td><td>0.280</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>Y</td><td>NOR2XL</td><td>0.048</td><td>0.044</td><td>0.221</td><td>0.329</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td></tr> <tr><td>D</td><td>DFFQX1</td><td>0.000</td><td>0.044</td><td>0.221</td><td>0.329</td><td>v</td><td>-</td><td>-</td></tr> </table>	CK	-	0.003	-0.107	0.000	^	0.000	Wireload model(.lib None Generated)	Q	DFFQX1	0.280	0.065	0.173	0.280	^	0.000	Wireload model(.lib None Generated)	Y	NOR2XL	0.048	0.044	0.221	0.329	v	0.000	Wireload model(.lib None Generated)	D	DFFQX1	0.000	0.044	0.221	0.329	v	-	-	<pre> Path 1: MET Hold Check with Pin dp_c1/out1_reg[3]/CK Endpoint: dp_c1/out1_reg[3]/D (v) checked with leading edge of 'clk' Beginpoint: dp_c1/out1_reg[2]/D (v) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.042 + Phase Shift 0.000 + Uncertainty 0.200 = Required Time 0.242 Arrival Time 0.608 Slack Time 0.366 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000 Pin Cell Delay Slew Required Arrival Edge Wire Wireload Time Time Load Model -----</pre> <table border="1"> <tr><td>CK</td><td>-</td><td>0.003</td><td>-0.366</td><td>0.000</td><td>^</td><td>0.270</td><td>Wireload model(.lib tsmc18_wl10 slow)</td></tr> <tr><td>Q</td><td>DFFQX1</td><td>0.424</td><td>0.178</td><td>0.059</td><td>0.424</td><td>v</td><td>0.020</td><td>Wireload model(.lib tsmc18_wl10 slow)</td></tr> <tr><td>Y</td><td>NOR2BX1</td><td>0.184</td><td>0.105</td><td>0.242</td><td>0.608</td><td>v</td><td>0.010</td><td>Wireload model(.lib tsmc18_wl10 slow)</td></tr> <tr><td>D</td><td>DFFQX1</td><td>0.000</td><td>0.105</td><td>0.242</td><td>0.608</td><td>v</td><td>-</td><td>-</td></tr> </table>	CK	-	0.003	-0.366	0.000	^	0.270	Wireload model(.lib tsmc18_wl10 slow)	Q	DFFQX1	0.424	0.178	0.059	0.424	v	0.020	Wireload model(.lib tsmc18_wl10 slow)	Y	NOR2BX1	0.184	0.105	0.242	0.608	v	0.010	Wireload model(.lib tsmc18_wl10 slow)	D	DFFQX1	0.000	0.105	0.242	0.608	v	-	-
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SETUP CHECK

```

Path 1: MET Late External Delay Assertion
Endpoint: OUT[3] (v) checked with leading edge of 'clk'
Beginpoint: dp_04/0_reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- External Delay 3.000
+ Phase Shift 4.927
- Uncertainty 1.000
= Required Time 0.927
- Arrival Time 0.735
= Slack Time 0.192
    Clock Rise Edge 0.000
        + Clock Network Latency (Prop) 0.000
        = Beginpoint Arrival Time 0.000
    Pin Cell Delay Slew Required Arrival Edge Wire Wireload
    Time Time Load Model
    -----
    CK - 0.003 0.192 0.000 ^ 0.000 Wireload model(.lib None Generated)
    Q DFFX2 0.360 0.079 0.560 0.360 v 0.000 Wireload model(.lib None Generated)
    Y BUFX20 0.367 0.364 0.927 0.735 v 0.000 Wireload model(.lib None Generated)
    OUT[3] - 0.000 0.364 0.927 0.735 v
  
```

```

Path 1: VIOLATED Setup Check with Pin dp_04/0_reg[0]/CK
Endpoint: dp_04/0_reg[0]/D (^) checked with leading edge of 'clk'
Beginpoint: cp_D1/0_reg[3]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- Setup 0.200
+ Phase Shift 4.927
- Uncertainty 1.000
= Required Time 3.727
- Arrival Time 4.213
= Slack Time -0.487
    Clock Rise Edge 0.000
        + Clock Network Latency (Prop) 0.000
        = Beginpoint Arrival Time 0.000
    Pin Cell Delay Slew Required Arrival Edge Wire Wireload
    Time Time Load Model
    -----
    CK - 0.003 -0.487 0.000 ^ 0.270 Wireload model(.lib tsmc18_wl10_slow)
    Q DFFX1L 0.465 0.317 -0.022 0.465 ^ 0.330 Wireload model(.lib tsmc18_wl10_slow)
    Y NAND2XL 0.462 0.311 0.000 0.467 v 0.020 Wireload model(.lib tsmc18_wl10_slow)
    Y OAIZ1X1L 0.320 0.311 0.780 1.267 v 0.010 Wireload model(.lib tsmc18_wl10_slow)
    Y OAIZ2X1L 0.628 0.889 1.408 1.894 v 0.050 Wireload model(.lib tsmc18_wl10_slow)
    Y INVXL 0.385 0.370 1.793 2.288 ^ 0.010 Wireload model(.lib tsmc18_wl10_slow)
    Y AOI32X1L 0.448 0.827 2.241 2.727 v 0.030 Wireload model(.lib tsmc18_wl10_slow)
    Y NAND2X1 0.600 0.699 2.038 3.415 v 0.040 Wireload model(.lib tsmc18_wl10_slow)
    Y OAIZ1X1 0.325 0.316 0.293 0.360 v 0.010 Wireload model(.lib tsmc18_wl10_slow)
    Y OAIZ3X1L 0.168 0.371 3.461 3.948 v 0.010 Wireload model(.lib tsmc18_wl10_slow)
    Y OAIBB1XL 0.265 0.241 3.727 4.213 ^ 0.010 Wireload model(.lib tsmc18_wl10_slow)
    D DFFX2 0.000 0.241 3.727 4.213 ^ -
  
```

Slack Time: 0.192

Slack Time: -0.487

Case 3: Synthesis for Intermediate Timing Constraint, Intermediate Slack

Without wireload model

HOLD CHECK

```

Path 1: MET Hold Check with Pin dp_f1/temp_reg[0]/CK
Endpoint: dp_f1/temp_reg[0]/D (v) checked with leading edge of 'clk'
Beginpoint: dp_f1/temp_reg[0]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
+ Hold 0.042
+ Phase Shift 0.000
+ Uncertainty 0.200
= Required Time 0.242
Arrival Time 0.325
Slack Time 0.083
    Clock Rise Edge 0.000
        + Clock Network Latency (Prop) 0.000
        = Beginpoint Arrival Time 0.000
    Pin Cell Delay Slew Required Arrival Edge Wire Wireload
    Time Time Load Model
    -----
    CK - 0.003 -0.083 0.000 ^ 0.000 Wireload model(.lib None Generated)
    Q DFFQX1 0.281 0.066 0.198 0.281 v 0.000 Wireload model(.lib None Generated)
    Y NOR2XL 0.044 0.049 0.242 0.325 v 0.000 Wireload model(.lib None generated)
    D DFFQX1 0.000 0.049 0.242 0.325 v
  
```

With wireload model

```

Path 1: MET Hold Check with Pin dp_c1/out1_reg[3]/CK
Endpoint: dp_c1/out1_reg[3]/D (v) checked with leading edge of 'clk'
Beginpoint: dp_c1/out1_reg[2]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
+ Hold 0.042
+ Phase Shift 0.000
+ Uncertainty 0.200
= Required Time 0.242
Arrival Time 0.689
Slack Time 0.366
    Clock Rise Edge 0.000
        + Clock Network Latency (Prop) 0.000
        = Beginpoint Arrival Time 0.000
    Pin Cell Delay Slew Required Arrival Edge Wire Wireload
    Time Time Load Model
    -----
    CK - 0.003 -0.366 0.000 ^ 0.270 Wireload model(.lib tsmc18_wl10 slow)
    Q DFFQX1L 0.425 0.178 0.059 0.425 v 0.020 Wireload model(.lib tsmc18_wl10 slow)
    Y NOR2BX1 0.184 0.105 0.242 0.689 v 0.010 Wireload model(.lib tsmc18_wl10 slow)
    D DFFQX1 0.000 0.105 0.242 0.689 v -
  
```

Slack Time: 0.083

Slack Time: 0.366

SETUP CHECK

```

Path 1: MET Late External Delay Assertion
Endpoint: OUT[3] (^) checked with leading edge of 'clk'
Beginpoint: dp_04/0_reg[3]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- External Delay 3.000
+ Phase Shift 11.000
- Uncertainty 1.000
= Required Time 7.000
- Arrival Time 1.056
= Slack Time 5.944
    Clock Rise Edge 0.000
        + Clock Network Latency (Prop) 0.000
        = Beginpoint Arrival Time 0.000
    Pin Cell Delay Slew Required Arrival Edge Wire Wireload
    Time Time Load Model
    -----
    CK - 0.003 5.944 0.000 ^ 0.000 Wireload model(.lib None Generated)
    Q DFFHQX8 1.056 1.024 7.000 1.056 ^ 0.000 Wireload model(.lib None Generated)
    OUT[3] - 0.000 1.024 7.000 1.056 ^ -
  
```

```

Path 1: MET Setup Check with Pin dp_04/0_reg[0]/CK
Endpoint: dp_04/0_reg[0]/D (^) checked with leading edge of 'clk'
Beginpoint: cp_D1/0_reg[3]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- Setup 0.179
+ Phase Shift 11.000
- Uncertainty 1.000
= Required Time 9.822
- Arrival Time 4.628
= Slack Time 5.292
    Clock Rise Edge 0.000
        + Clock Network Latency (Prop) 0.000
        = Beginpoint Arrival Time 0.000
    Pin Cell Delay Slew Required Arrival Edge Wire Wireload
    Time Time Load Model
    -----
    CK - 0.003 5.292 0.000 ^ 0.270 Wireload model(.lib tsmc18_wl10 slow)
    Q DFFQX1L 0.465 0.319 5.668 0.465 ^ 0.030 Wireload model(.lib tsmc18_wl10 slow)
    Y NAND2XL 0.483 0.597 6.150 0.948 v 0.020 Wireload model(.lib tsmc18_wl10 slow)
    Y OAIZ1X1L 0.320 0.311 6.470 1.268 ^ 0.010 Wireload model(.lib tsmc18_wl10 slow)
    Y OAIZ2X1L 0.635 0.815 7.105 1.903 v 0.050 Wireload model(.lib tsmc18_wl10 slow)
    Y INVXL 0.388 0.373 7.494 2.292 ^ 0.010 Wireload model(.lib tsmc18_wl10 slow)
    Y AOI32X1L 0.567 1.087 8.061 2.859 v 0.040 Wireload model(.lib tsmc18_wl10 slow)
    Y NOR2BX1L 0.855 0.824 8.916 3.714 ^ 0.040 Wireload model(.lib tsmc18_wl10 slow)
    Y AOI32X1 0.313 0.444 9.229 4.027 v 0.010 Wireload model(.lib tsmc18_wl10 slow)
    Y INVXL 0.223 0.344 9.290 4.477 v 0.010 Wireload model(.lib tsmc18_wl10 slow)
    Y AOI21X1L 0.114 0.337 9.623 4.421 v 0.010 Wireload model(.lib tsmc18_wl10 slow)
    Y OAIBB1X1L 0.198 0.187 9.822 4.620 ^ 0.010 Wireload model(.lib tsmc18_wl10 slow)
    D DFFHQX8 0.000 0.187 9.822 4.620 ^ -
  
```

Slack Time: 5.944

Slack Time: 5.202

II. STA of the netlists with compromised constraint file

Case 1: Minimum Area

	Without wireload model	With wireload model																																																																																																																								
HOLD CHECK	<pre>Path 1: MET Hold Check with Pin dp_f1/temp_reg[0]/CK Endpoint: dp_f1/temp_reg[0]/D (v) checked with leading edge of 'clk' Beginpoint: dp_f1/temp_reg[0]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.042 + Phase Shift 0.000 + Uncertainty 0.200 = Required Time 0.242 Arrival Time 0.325 Slack Time 0.083 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000</pre> <table border="1"> <thead> <tr> <th>Pin</th><th>Cell</th><th>Delay</th><th>Slew</th><th>Required</th><th>Arrival</th><th>Edge</th><th>Wire</th><th>Wireload</th><th>Model</th></tr> <tr> <th></th><th></th><th>Time</th><th></th><th>Time</th><th></th><th></th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>CK</td><td>-</td><td>-</td><td>0.003</td><td>-0.083</td><td>0.000</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td><td></td></tr> <tr> <td>Q</td><td>DFFQX1</td><td>0.201</td><td>0.066</td><td>0.198</td><td>0.281</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td><td></td></tr> <tr> <td>Y</td><td>NOR2XL</td><td>0.044</td><td>0.040</td><td>0.242</td><td>0.325</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td><td></td></tr> <tr> <td>D</td><td>DFFQX1</td><td>0.000</td><td>0.040</td><td>0.242</td><td>0.325</td><td>v</td><td>-</td><td>-</td><td></td></tr> </tbody> </table>	Pin	Cell	Delay	Slew	Required	Arrival	Edge	Wire	Wireload	Model			Time		Time						CK	-	-	0.003	-0.083	0.000	^	0.000	Wireload model(.lib None Generated)		Q	DFFQX1	0.201	0.066	0.198	0.281	^	0.000	Wireload model(.lib None Generated)		Y	NOR2XL	0.044	0.040	0.242	0.325	v	0.000	Wireload model(.lib None Generated)		D	DFFQX1	0.000	0.040	0.242	0.325	v	-	-		<pre>Path 1: MET Hold Check with Pin dp_c1/out1_reg[3]/CK Endpoint: dp_c1/out1_reg[3]/D (v) checked with leading edge of 'clk' Beginpoint: dp_c1/out1_reg[2]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.042 + Phase Shift 0.000 + Uncertainty 0.200 = Required Time 0.242 Arrival Time 0.309 Slack Time 0.306 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000</pre> <table border="1"> <thead> <tr> <th>Pin</th><th>Cell</th><th>Delay</th><th>Slew</th><th>Required</th><th>Arrival</th><th>Edge</th><th>Wire</th><th>Wireload</th><th>Model</th></tr> <tr> <th></th><th></th><th>Time</th><th></th><th>Time</th><th></th><th></th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>CK</td><td>-</td><td>-</td><td>0.003</td><td>-0.366</td><td>0.000</td><td>^</td><td>0.270</td><td>Wireload model(.lib tsmc18_wl10 slow)</td><td></td></tr> <tr> <td>Q</td><td>DFFQX1</td><td>0.425</td><td>0.179</td><td>0.179</td><td>0.059</td><td>v</td><td>0.425</td><td>v</td><td>0.020</td></tr> <tr> <td>Y</td><td>NOR2BX1</td><td>0.184</td><td>0.105</td><td>0.242</td><td>0.609</td><td>v</td><td>0.010</td><td>Wireload model(.lib tsmc18_wl10 slow)</td><td></td></tr> <tr> <td>D</td><td>DFFQX1</td><td>0.000</td><td>0.105</td><td>0.242</td><td>0.609</td><td>v</td><td>-</td><td>-</td><td></td></tr> </tbody> </table>	Pin	Cell	Delay	Slew	Required	Arrival	Edge	Wire	Wireload	Model			Time		Time						CK	-	-	0.003	-0.366	0.000	^	0.270	Wireload model(.lib tsmc18_wl10 slow)		Q	DFFQX1	0.425	0.179	0.179	0.059	v	0.425	v	0.020	Y	NOR2BX1	0.184	0.105	0.242	0.609	v	0.010	Wireload model(.lib tsmc18_wl10 slow)		D	DFFQX1	0.000	0.105	0.242	0.609	v	-	-	
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	Slack Time: 0.963	Slack Time: 0.963																																																																																																																								

Case 2: Tight Timing Constraint

	Without wireload model	With wireload model																																																																																																																								
HOLD CHECK	<pre>Path 1: MET Hold Check with Pin dp_f1/temp_reg[0]/CK Endpoint: dp_f1/temp_reg[0]/D (v) checked with leading edge of 'clk' Beginpoint: dp_f1/temp_reg[0]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.021 + Phase Shift 0.000 + Uncertainty 0.200 = Required Time 0.221 Arrival Time 0.329 Slack Time 0.107 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000</pre> <table border="1"> <thead> <tr> <th>Pin</th><th>Cell</th><th>Delay</th><th>Slew</th><th>Required</th><th>Arrival</th><th>Edge</th><th>Wire</th><th>Wireload</th><th>Model</th></tr> <tr> <th></th><th></th><th>Time</th><th></th><th>Time</th><th></th><th></th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>CK</td><td>-</td><td>-</td><td>0.003</td><td>-0.107</td><td>0.000</td><td>^</td><td>0.000</td><td>Wireload model(.lib None Generated)</td><td></td></tr> <tr> <td>Q</td><td>DFFQX1</td><td>0.280</td><td>0.065</td><td>0.173</td><td>0.280</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td><td></td></tr> <tr> <td>Y</td><td>NOR2XL</td><td>0.048</td><td>0.044</td><td>0.221</td><td>0.329</td><td>v</td><td>0.000</td><td>Wireload model(.lib None Generated)</td><td></td></tr> <tr> <td>D</td><td>DFFQX1</td><td>0.000</td><td>0.044</td><td>0.221</td><td>0.329</td><td>v</td><td>-</td><td>-</td><td></td></tr> </tbody> </table>	Pin	Cell	Delay	Slew	Required	Arrival	Edge	Wire	Wireload	Model			Time		Time						CK	-	-	0.003	-0.107	0.000	^	0.000	Wireload model(.lib None Generated)		Q	DFFQX1	0.280	0.065	0.173	0.280	v	0.000	Wireload model(.lib None Generated)		Y	NOR2XL	0.048	0.044	0.221	0.329	v	0.000	Wireload model(.lib None Generated)		D	DFFQX1	0.000	0.044	0.221	0.329	v	-	-		<pre>Path 1: MET Hold Check with Pin dp_c1/out1_reg[3]/CK Endpoint: dp_c1/out1_reg[3]/D (v) checked with leading edge of 'clk' Beginpoint: dp_c1/out1_reg[2]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} Other End Arrival Time 0.000 + Hold 0.042 + Phase Shift 0.000 + Uncertainty 0.200 = Required Time 0.242 Arrival Time 0.595 Slack Time 0.306 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000</pre> <table border="1"> <thead> <tr> <th>Pin</th><th>Cell</th><th>Delay</th><th>Slew</th><th>Required</th><th>Arrival</th><th>Edge</th><th>Wire</th><th>Wireload</th><th>Model</th></tr> <tr> <th></th><th></th><th>Time</th><th></th><th>Time</th><th></th><th></th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>CK</td><td>-</td><td>-</td><td>0.003</td><td>-0.366</td><td>0.000</td><td>^</td><td>0.270</td><td>Wireload model(.lib tsmc18_wl10 slow)</td><td></td></tr> <tr> <td>Q</td><td>DFFQX1</td><td>0.424</td><td>0.178</td><td>0.059</td><td>0.424</td><td>v</td><td>0.424</td><td>v</td><td>0.020</td></tr> <tr> <td>Y</td><td>NOR2BX1</td><td>0.184</td><td>0.105</td><td>0.242</td><td>0.608</td><td>v</td><td>0.010</td><td>Wireload model(.lib tsmc18_wl10 slow)</td><td></td></tr> <tr> <td>D</td><td>DFFQX1</td><td>0.000</td><td>0.105</td><td>0.242</td><td>0.608</td><td>v</td><td>-</td><td>-</td><td></td></tr> </tbody> </table>	Pin	Cell	Delay	Slew	Required	Arrival	Edge	Wire	Wireload	Model			Time		Time						CK	-	-	0.003	-0.366	0.000	^	0.270	Wireload model(.lib tsmc18_wl10 slow)		Q	DFFQX1	0.424	0.178	0.059	0.424	v	0.424	v	0.020	Y	NOR2BX1	0.184	0.105	0.242	0.608	v	0.010	Wireload model(.lib tsmc18_wl10 slow)		D	DFFQX1	0.000	0.105	0.242	0.608	v	-	-	
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CK	-	-	0.003	-0.366	0.000	^	0.270	Wireload model(.lib tsmc18_wl10 slow)																																																																																																																		
Q	DFFQX1	0.424	0.178	0.059	0.424	v	0.424	v	0.020																																																																																																																	
Y	NOR2BX1	0.184	0.105	0.242	0.608	v	0.010	Wireload model(.lib tsmc18_wl10 slow)																																																																																																																		
D	DFFQX1	0.000	0.105	0.242	0.608	v	-	-																																																																																																																		
	Slack Time: 0.107	Slack Time: 0.366																																																																																																																								

SETUP CHECK

```

Path 1: MET Late External Delay Assertion
Endpoint: OUT[3] (v) checked with leading edge of 'clk'
Beginpoint: dp D4/Q.reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- External Delay 3.000
+ Phase Shift 11.000
- Uncertainty 1.000
= Required Time 7.000
- Arrival Time 6.735
= Slack Time 0.265
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.000
    = Beginpoint Arrival Time 0.000
-----Pin Cell Delay Slew Required Arrival Edge Wire Wireload
Time Time Load Model
-----CK - 0.003 6.265 0.000 ^ 0.000 Wireload model(.lib None Generated)
Q DFFX2 0.368 0.079 6.633 0.368 v 0.000 Wireload model(.lib None Generated)
Y BUFX20 0.367 0.364 7.000 0.735 v 0.000 Wireload model(.lib None Generated)
OUT[3] - 0.000 0.364 7.000 0.735 v -
-----
```

```

Path 1: MET Setup Check with Pin dp D4/Q.reg[0]/CK
Endpoint: dp D4/Q.reg[0]/D (^) checked with leading edge of 'clk'
Beginpoint: cp D1/Q.reg[3]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- Setup 0.200
+ Phase Shift 11.000
- Uncertainty 1.000
= Required Time 9.800
- Arrival Time 4.213
= Slack Time 5.586
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.000
    = Beginpoint Arrival Time 0.000
-----Pin Cell Delay Slew Required Arrival Edge Wire Wireload
Time Time Load Model
-----CK - - 0.003 5.586 0.000 ^ 0.270 Wireload model(.lib tsmc18_w110 slow)
Q DFFQX1 0.465 0.317 6.051 0.465 v 0.030 Wireload model(.lib tsmc18_w110 slow)
Y NAND2XL 0.482 0.597 6.454 0.947 v 0.020 Wireload model(.lib tsmc18_w110 slow)
Y AO121X1 0.391 0.311 6.893 1.077 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO121X1 0.628 0.804 4.491 1.894 v 0.050 Wireload model(.lib tsmc18_w110 slow)
Y INVX1 0.385 0.370 7.866 2.280 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO132X1 0.448 0.827 8.314 2.727 v 0.030 Wireload model(.lib tsmc18_w110 slow)
Y NAND2BX1 0.687 0.696 9.001 3.415 v 0.040 Wireload model(.lib tsmc18_w110 slow)
Y AO132X1 0.365 0.516 9.366 3.780 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO131X1 0.168 0.371 9.534 3.948 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO12B81XL 0.265 0.241 9.880 4.213 v 0.010 Wireload model(.lib tsmc18_w110 slow)
D DFFX2 0.000 0.241 9.880 4.213 v -
-----
```

Slack Time: 0.265

Slack Time: 5.586

Case 3: Intermediate Timing Constraint

Without wireload model

HOLD CHECK

```

Path 1: MET Hold Check with Pin dp_f1/temp_reg[0]/CK
Endpoint: dp_f1/temp_reg[0]/D (v) checked with leading edge of 'clk'
Beginpoint: dp_f1/temp_reg[0]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
+ Hold 0.042
+ Phase Shift 0.000
+ Uncertainty 0.200
= Required Time 0.242
Arrival Time 0.325
Slack Time 0.083
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.000
    = Beginpoint Arrival Time 0.000
-----Pin Cell Delay Slew Required Arrival Edge Wire Wireload
Time Time Load Model
-----CK - 0.003 -0.083 0.000 ^ 0.000 Wireload model(.lib None Generated)
Q DFFOX1 0.281 0.066 0.198 0.281 v 0.000 Wireload model(.lib None Generated)
Y NOR2XL 0.044 0.046 0.242 0.325 v 0.000 Wireload model(.lib None Generated)
D DFFOX1 0.000 0.046 0.242 0.325 v -
-----
```

With wireload model

```

Path 1: MET Hold Check with Pin dp_c1/out1_reg[3]/CK
Endpoint: dp_c1/out1_reg[3]/D (v) checked with leading edge of 'clk'
Beginpoint: dp_c1/out1_reg[2]/Q (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
+ Hold 0.042
+ Phase Shift 0.000
+ Uncertainty 0.200
= Required Time 0.242
Arrival Time 0.609
Slack Time 0.366
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.000
    = Beginpoint Arrival Time 0.000
-----Pin Cell Delay Slew Required Arrival Edge Wire Wireload
Time Time Load Model
-----CK - - 0.003 -0.366 0.000 ^ 0.270 Wireload model(.lib tsmc18_w110 slow)
Q DFFQX1 0.425 0.178 0.059 0.425 v 0.020 Wireload model(.lib tsmc18_w110 slow)
Y NOR2BX1 0.184 0.105 0.242 0.609 v 0.010 Wireload model(.lib tsmc18_w110 slow)
D DFFQX1 0.000 0.105 0.242 0.609 v -
-----
```

Slack Time: 0.083

Slack Time: 0.366

SETUP CHECK

```

Path 1: MET Late External Delay Assertion
Endpoint: OUT[3] (^) checked with leading edge of 'clk'
Beginpoint: dp D4/Q.reg[3]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- External Delay 3.000
+ Phase Shift 11.000
- Uncertainty 1.000
= Required Time 2.000
- Arrival Time 1.056
= Slack Time 3.944
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.000
    = Beginpoint Arrival Time 0.000
-----Pin Cell Delay Slew Required Arrival Edge Wire Wireload
Time Time Load Model
-----CK - 0.003 5.940 0.100 ^ 0.000 Wireload model(.lib None Generated)
Q DFFHDX8 1.056 1.000 0.000 1.056 ^ 0.000 Wireload model(.lib None Generated)
OUT[3] - 0.000 1.024 7.000 1.056 -
-----
```

```

Path 1: MET Setup Check with Pin dp D4/Q.reg[0]/CK
Endpoint: dp D4/Q.reg[0]/D (^) checked with leading edge of 'clk'
Beginpoint: cp D1/Q.reg[3]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.000
- Setup 0.178
+ Phase Shift 11.000
- Uncertainty 1.000
= Required Time 9.822
- Arrival Time 4.620
= Slack Time 5.200
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.000
    = Beginpoint Arrival Time 0.000
-----Pin Cell Delay Slew Required Arrival Edge Wire Wireload
Time Time Load Model
-----CK - - 0.003 5.200 0.000 ^ 0.270 Wireload model(.lib tsmc18_w110 slow)
Q DFFQX1 0.465 0.319 5.668 0.465 v 0.030 Wireload model(.lib tsmc18_w110 slow)
Y NAND2XL 0.483 0.597 6.159 0.948 v 0.020 Wireload model(.lib tsmc18_w110 slow)
Y AO121X1 0.329 0.311 6.470 1.268 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO121X1 0.625 0.804 4.505 1.589 v 0.050 Wireload model(.lib tsmc18_w110 slow)
Y INVX1 0.388 0.373 7.494 2.292 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO132X1 0.567 1.087 8.861 2.859 v 0.040 Wireload model(.lib tsmc18_w110 slow)
Y NOR2BX1 0.855 0.824 8.916 3.714 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO132X1 0.313 0.444 9.229 4.027 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO131X1 0.223 0.495 9.459 4.247 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO131X1 0.414 0.357 9.623 4.421 v 0.010 Wireload model(.lib tsmc18_w110 slow)
Y AO12B81XL 0.198 0.197 9.622 4.620 v 0.010 Wireload model(.lib tsmc18_w110 slow)
D DFFHDX8 0.000 0.187 9.822 4.620 v -
-----
```

Slack Time: 3.944

Slack Time: 5.202

COMPARISON AND ANALYSIS OF ALL CASES

CASE	SETUP		HOLD	
	Without Wireload model	With wireload model	Without Wireload model	With wireload model
Minimum Area	13.323	10.584	0.061	0.061
Best Timing	0.192	-0.487	0.107	0.366
Compromised	5.944	5.202	0.083	0.366
Minimum Area Compromised constraint	0.963	0.963	0.083	0.366
Best timing Compromised constraint	6.265	5.586	0.107	0.366
Compromised Compromised constraint	5.944	5.202	0.083	0.366

OBSERVATIONS AND EXPLANATION:

1. In all the cases the setup slack is degraded after using the wireload model and hold slack is improved after using the wireload model.
EXPLANATION: As after using the wireload model the RC delays are now taken in consideration and hence total delay is now became the arc delay plus the wire delay and hence the setup slack became worse and hold slack improves as expected.
2. The minimum slack is for the best_timing with tight constraints((setup slack of 0.192 and hold slack of 0.107) and the worst slack is for the min_area for the relaxed constraints(setup slack of 13.323 and hold slack of 0.061)).
3. For the best_timing case with the tighter constraints after the implementation of the wireload model the setup slack degraded and gets violated because we already kept it very tightly (violated at -1ps) without wireload model at the time of synthesis and its violation was expected after the wireload model implementation.
4. As expected for all the cases the min_are netlist has the best slack, best_timing netlist has the worst slack and the compromised netlist has the intermediated slack and vice versa for the area.

5. EFFECT OF APPLYING INTERMEDIATE CONSTRAINTS TO ALL THREE NETLISTS:

- > In hold check not much change is observed as we were primarily changing the time period which has no effect on hold slack and hence the only significant reason in the change of the hold slack is the wireload model.
- > Compromised case has the timing slack between the other two cases and as expected the slack corresponding to min_area netlist worsens and got to the edge of violation whereas the slack for best timing case improves significantly and the slacks for the compromised case remained the same as the same constraints were used previously. This is because for min_area case constraints are now relatively tighter and for best_timing case constraints are now relatively relaxed

STEP – 6

TEST INSERTION

TIMING AND AREA REPORT FOR ALL THREE CASES

Case 1: Minimum Area

	Without scan-cell inserted netlist	With scan-cell inserted netlist																																																																																																																																																																																																																																																																																																																																																																																																																																																		
AREA REPORT	<pre>===== Generated by: Genus(TM) Synthesis Solution 19.13-s073_1 Generated on: Apr 06 2022 02:37:24 pm Module: group17 Technology library: slow Operating conditions: slow (balanced_tree) Wireload mode: enclosed Area mode: timing library =====</pre> <table border="1"> <thead> <tr> <th>Instance</th><th>Module</th><th>Cell Count</th><th>Cell Area</th><th>Net Area</th><th>Total Area</th><th>Wireload</th></tr> </thead> <tbody> <tr> <td>group17</td><td></td><td>68</td><td>666.072</td><td>6533.366</td><td>7199.438</td><td>tsmc18_wl10 (F)</td></tr> <tr> <td>dp_f1</td><td>freq_div</td><td>8</td><td>78.718</td><td>420.002</td><td>498.720</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_c1</td><td>Rcounter4</td><td>8</td><td>81.745</td><td>186.668</td><td>268.413</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>cp_D1</td><td>DFF8</td><td>8</td><td>127.159</td><td>0.000</td><td>127.159</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_D4</td><td>DFF4_17</td><td>4</td><td>63.580</td><td>0.000</td><td>63.580</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_D3</td><td>DFF4_18</td><td>4</td><td>63.580</td><td>0.000</td><td>63.580</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_D2</td><td>DFF4</td><td>4</td><td>63.580</td><td>0.000</td><td>63.580</td><td>tsmc18_wl10 (D)</td></tr> </tbody> </table> <p>(D) = wireload is default in technology library (F) = wireload was set using 'force_wireload'</p>	Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload	group17		68	666.072	6533.366	7199.438	tsmc18_wl10 (F)	dp_f1	freq_div	8	78.718	420.002	498.720	tsmc18_wl10 (D)	dp_c1	Rcounter4	8	81.745	186.668	268.413	tsmc18_wl10 (D)	cp_D1	DFF8	8	127.159	0.000	127.159	tsmc18_wl10 (D)	dp_D4	DFF4_17	4	63.580	0.000	63.580	tsmc18_wl10 (D)	dp_D3	DFF4_18	4	63.580	0.000	63.580	tsmc18_wl10 (D)	dp_D2	DFF4	4	63.580	0.000	63.580	tsmc18_wl10 (D)	<pre>===== Generated by: Genus(TM) Synthesis Solution 19.13-s073_1 Generated on: Apr 08 2022 05:08:56 pm Module: group17 Technology library: slow Operating conditions: slow (balanced_tree) Wireload mode: enclosed Area mode: timing library =====</pre> <table border="1"> <thead> <tr> <th>Instance</th><th>Module</th><th>Cell Count</th><th>Cell Area</th><th>Net Area</th><th>Total Area</th><th>Wireload</th></tr> </thead> <tbody> <tr> <td>group17</td><td></td><td>66</td><td>784.905</td><td>8866.711</td><td>9651.616</td><td>tsmc18_wl10 (F)</td></tr> <tr> <td>dp_f1</td><td>freq_div</td><td>8</td><td>92.342</td><td>513.336</td><td>605.678</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_c1</td><td>Rcounter4</td><td>8</td><td>99.911</td><td>186.668</td><td>286.578</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>cp_D1</td><td>DFF8</td><td>8</td><td>163.490</td><td>0.000</td><td>163.490</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_D4</td><td>DFF4_17</td><td>4</td><td>81.745</td><td>0.000</td><td>81.745</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_D3</td><td>DFF4_18</td><td>4</td><td>81.745</td><td>0.000</td><td>81.745</td><td>tsmc18_wl10 (D)</td></tr> <tr> <td>dp_D2</td><td>DFF4</td><td>4</td><td>81.745</td><td>0.000</td><td>81.745</td><td>tsmc18_wl10 (D)</td></tr> </tbody> </table> <p>(D) = wireload is default in technology library (F) = wireload was set using 'force_wireload'</p>	Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload	group17		66	784.905	8866.711	9651.616	tsmc18_wl10 (F)	dp_f1	freq_div	8	92.342	513.336	605.678	tsmc18_wl10 (D)	dp_c1	Rcounter4	8	99.911	186.668	286.578	tsmc18_wl10 (D)	cp_D1	DFF8	8	163.490	0.000	163.490	tsmc18_wl10 (D)	dp_D4	DFF4_17	4	81.745	0.000	81.745	tsmc18_wl10 (D)	dp_D3	DFF4_18	4	81.745	0.000	81.745	tsmc18_wl10 (D)	dp_D2	DFF4	4	81.745	0.000	81.745	tsmc18_wl10 (D)																																																																																																																																																																																																																																																																																																																																		
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TIMING REPORT	<pre>===== Generated by: Genus(TM) Synthesis Solution 19.13-s073_1 Generated on: Apr 06 2022 02:37:24 pm Module: group17 Technology library: slow Operating conditions: slow (balanced_tree) Wireload mode: enclosed Area mode: timing library =====</pre> <table border="1"> <thead> <tr> <th>Pin</th><th>Type</th><th>Fanout</th><th>Load</th><th>Slew</th><th>Delay</th><th>Arrival</th></tr> <tr> <th></th><th></th><th>(ff)</th><th>(ps)</th><th>(ps)</th><th>(ps)</th><th></th></tr> </thead> <tbody> <tr> <td>(clock clk)</td><td>launch</td><td></td><td></td><td></td><td>0</td><td>R</td></tr> <tr> <td>cp_D1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td> Q_reg[4]/CK</td><td></td><td></td><td>30</td><td></td><td>0</td><td>R</td></tr> <tr> <td> Q_reg[4]/Q</td><td>DFFQX1</td><td>3</td><td>37.4</td><td>274</td><td>+483</td><td>483 F</td></tr> <tr> <td>cp_D1/Q[4]</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td>g866/A</td><td></td><td></td><td></td><td>+0</td><td>483</td><td></td></tr> <tr> <td>g866/Y</td><td>AND2X1</td><td>2</td><td>24.4</td><td>185</td><td>+270</td><td>753 F</td></tr> <tr> <td>g857/A1</td><td></td><td></td><td></td><td>+0</td><td>753</td><td></td></tr> <tr> <td>g857/Y</td><td>A021X1</td><td>1</td><td>12.8</td><td>133</td><td>+244</td><td>998 F</td></tr> <tr> <td>g851/A1</td><td></td><td></td><td></td><td>+0</td><td>998</td><td></td></tr> <tr> <td>g851/Y</td><td>AOI21X1</td><td>5</td><td>60.2</td><td>979</td><td>+723</td><td>1721 R</td></tr> <tr> <td>g845/A0</td><td></td><td></td><td></td><td>+0</td><td>1721</td><td></td></tr> <tr> <td>g845/Y</td><td>OAI22X1</td><td>4</td><td>47.7</td><td>722</td><td>+696</td><td>2417 F</td></tr> <tr> <td>g844/B</td><td></td><td></td><td></td><td>+0</td><td>2417</td><td></td></tr> <tr> <td>g844/Y</td><td>AND2X1</td><td>4</td><td>46.4</td><td>338</td><td>+433</td><td>2850 F</td></tr> <tr> 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<td></td><td>uncertainty</td><td></td><td></td><td>-20</td><td>4980</td><td>R</td></tr> <tr> <td>Cost Group : 'clk' (path_group 'clk')</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td>Timing slack : 1083ps</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td>Start-point : cp_D1/Q_reg[4]/CK</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td>End-point : dp_D4/Q_reg[0]/D</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> </tbody> </table>	Pin	Type	Fanout	Load	Slew	Delay	Arrival			(ff)	(ps)	(ps)	(ps)		(clock clk)	launch				0	R	cp_D1							Q_reg[4]/CK			30		0	R	Q_reg[4]/Q	DFFQX1	3	37.4	274	+483	483 F	cp_D1/Q[4]							g866/A				+0	483		g866/Y	AND2X1	2	24.4	185	+270	753 F	g857/A1				+0	753		g857/Y	A021X1	1	12.8	133	+244	998 F	g851/A1				+0	998		g851/Y	AOI21X1	5	60.2	979	+723	1721 R	g845/A0				+0	1721		g845/Y	OAI22X1	4	47.7	722	+696	2417 F	g844/B				+0	2417		g844/Y	AND2X1	4	46.4	338	+433	2850 F	g842/B1				+0	2850		g842/Y	A022X1	1	12.8	145	+292	3141 F	g838/Q0				+0	3141		g838/Y	A0I221X1	1	11.7	446	+293	3435 R	g837/B				+0	3435		g837/Y	NAND2XL	1	11.6	351	+316	3750 F	dp_D4/D[0]							Q_reg[0]/D <<<	DFFQX1			+0	3750		Q_reg[0]/CK				30	+146	3897 R	(clock clk)	capture				5000	R		uncertainty			-20	4980	R	Cost Group : 'clk' (path_group 'clk')							Timing slack : 1083ps							Start-point : cp_D1/Q_reg[4]/CK							End-point : dp_D4/Q_reg[0]/D							<pre>===== Generated by: Genus(TM) Synthesis Solution 19.13-s073_1 Generated on: Apr 08 2022 05:08:56 pm Module: group17 Technology library: slow Operating conditions: slow (balanced_tree) Wireload mode: enclosed Area mode: timing library =====</pre> <table border="1"> <thead> <tr> <th>Pin</th><th>Type</th><th>Fanout</th><th>Load</th><th>Slew</th><th>Delay</th><th>Arrival</th></tr> <tr> <th></th><th></th><th>(ff)</th><th>(ps)</th><th>(ps)</th><th>(ps)</th><th></th></tr> </thead> <tbody> <tr> <td>(clock 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Case 2: Tight Timing Constraint

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Case 3: Intermediate Timing Constraint

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QoR SUMMARY

CASE	Without scan cell inserted			With scan cell inserted		
	Area (um ²)	Slack (ps)	No. of cells	Area (um ²)	Slack (ps)	No. of cells
Minimum Area	6533.366	1083	68	9651.616	11297	66
Best Timing	7373.264	-48	71	9563.346	-33	65
Compromised	8602.054	2	82	9590.829	5444	65

OBSERVATIONS

- In all the three cases the timing slack degrades after the scan chain insertion, see the timing report attached.
- In all the three cases the AREA degrades after the scan chain insertion, see the area report attached.

3. Overall the min_area case has the lowest area and the worst slack with and without inserted scan chain.
4. Overall the min_area case has the lowest area and the worst slack with and without inserted scan chain.
5. Overall the best_timing case has the highest area and the best slack with and without inserted scan chain.
6. The compromised case has the intermediate area and slack of the above two.

EXPLANATION

Scanning designs is a quick and easy way to improve testability. However, depending on the stitching order of the scan chain affects size and performance. It can be seen that slack has been reduced in all the cases, that is, the min area case, best timing case, and the compromised case, due to the addition of the scan chain. This is because the AT, in this case, has been increased due to the increase in delays. And this increase in the AT is due to the bigger sizes of the newly inserted scan cells in place of the DFFs .and also, after insertion of these scan cells, the area is also increased, which can be seen in the cell report attached due to the same reason of the bigger sizes of these scan cells.

So, as a result, we can say the scan cells apply both timing and area penalty, but still, these are very critical to use in the design as these cells increase the controllability and observability of the design; that is how easily we can change the values at the internal nodes by applying the test vectors at the input nodes and how easily we can observe the corresponding change at the output nodes, that's why test insertion is the crucial step, and despite the penalty, we always promote this in our design flow.

ELEMENTS ADDED AND THEIR USAGE:

Following the addition of scan chains, all of the DFFQXL cells in the netlist were replaced by SDFFQX1 cells, and the scan cells were combined to form a scan chain. A clock port, a scan enable pin, and a scan pin comprise these scan cells.

The input pin is connected to the D pin, as shown in the diagram.

There is also a test mode port, which, along with the SE pin, determines the design's mode of operation. The table below depicts the various modes of the design. The D pin is connected to n.

FUNCTIONING OF A SCAN CHAIN

There are three stages of scan chain operation –

Step 1: Scan In

Objective - test patterns are loaded keeping the design in test timing mode

In this case, (scan enable) SE = 1 and all of the Flip Flops accept SI as inputs. The scan chain is active, and the test pattern generated by ATPG can be shifted to the Q pin of the flip flops in N clock cycles.

Step 2: Capture

Objective - Design is kept in functional timing mode and test pattern response is captured

After N clock cycles, SE -->0, and the D pin inputs of all the Flip Flops are latched to the Q pin. We also use the primary inputs, and if there is a fault, the value at Q pin will be corrupted.

Step 3: Scan Out

Objective – Design is brought back in test timing mode and test pattern response is unloaded (at times, this operation simultaneously initiates the injection of next test pattern via Scan In)

Now that the output at SO pin has been observed, the design runs through another N clock cycle, and the new pattern can be entered into the chain at the same time.

NETLIST BEFORE AND AFTER SCAIN INSERTION

NETLIST BEFORE SCAN INSERTION	NETLIST AFTER SCAN INSERTION
<pre>// Generated by Cadence Genus(TM) Synthesis Solution 19.13-s073_1 // Generated on: Apr 6 2022 14:38:24 IST (Apr 6 2022 09:08:24 UTC) // Verification Directory fv/group17 module DFF8(clk, D, Q); input clk; input [7:0] D; output [7:0] Q; wire clk; wire [7:0] D; wire [7:0] Q; DFFQX4 \Q_reg[4] (.CK (clk), .D (D[4]), .Q (Q[4])); DFFQX4 \Q_reg[6] (.CK (clk), .D (D[6]), .Q (Q[6])); DFFQX4 \Q_reg[7] (.CK (clk), .D (D[7]), .Q (Q[7])); DFFQX4 \Q_reg[0] (.CK (clk), .D (D[0]), .Q (Q[0])); DFFHQX8 \Q_reg[2] (.CK (clk), .D (D[2]), .Q (Q[2])); DFFHQX8 \Q_reg[5] (.CK (clk), .D (D[5]), .Q (Q[5])); DFFHQX8 \Q_reg[3] (.CK (clk), .D (D[3]), .Q (Q[3])); DFFHQX8 \Q_reg[1] (.CK (clk), .D (D[1]), .Q (Q[1])); endmodule module DFF4(clk, D, Q); input clk; input [3:0] D; output [3:0] Q; wire clk; wire [3:0] D; wire [3:0] Q; DFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .Q (Q[3])); DFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .Q (Q[2])); DFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .Q (Q[0])); DFFQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .Q (Q[1])); endmodule module DFF4_18(clk, D, Q); input clk;</pre>	<pre>// Generated by Cadence Genus(TM) Synthesis Solution 19.13-s073_1 // Generated on: Apr 8 2022 17:08:00 IST (Apr 8 2022 11:38:00 UTC) // Verification Directory fv/group17 module DFF8(clk, D, Q, DFT_sdi, DFT_sen); input clk, DFT_sdi, DFT_sen; input [7:0] D; output [7:0] Q; wire clk, DFT_sdi, DFT_sen; wire [7:0] D; wire [7:0] Q; SDFFQX1 \Q_reg[4] (.CK (clk), .D (D[4]), .SI (Q[3]), .SE (DFT_sen), .Q (Q[4])); SDFFQX1 \Q_reg[6] (.CK (clk), .D (D[6]), .SI (Q[5]), .SE (DFT_sen), .Q (Q[6])); SDFFQX1 \Q_reg[7] (.CK (clk), .D (D[7]), .SI (Q[6]), .SE (DFT_sen), .Q (Q[7])); SDFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .SI (DFT_sdi), .SE (DFT_sen), .Q (Q[0])); SDFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .SI (Q[1]), .SE (DFT_sen), .Q (Q[2])); SDFFQX1 \Q_reg[5] (.CK (clk), .D (D[5]), .SI (Q[4]), .SE (DFT_sen), .Q (Q[5])); SDFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .SI (Q[2]), .SE (DFT_sen), .Q (Q[3])); SDFFQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .SI (Q[0]), .SE (DFT_sen), .Q (Q[1])); endmodule module DFF4(clk, D, Q, DFT_sdi, DFT_sen); input clk, DFT_sdi, DFT_sen; input [3:0] D; output [3:0] Q; wire clk, DFT_sdi, DFT_sen; wire [3:0] D; wire [3:0] Q;</pre>

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input [3:0] D;
output [3:0] Q;
wire clk;
wire [3:0] D;
wire [3:0] Q;
DFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .Q (Q[3]));
DFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .Q (Q[2]));
DFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .Q (Q[0]));
DFFQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .Q (Q[1]));
endmodule

module DFF4_17(clk, D, Q);
input clk;
input [3:0] D;
output [3:0] Q;
wire clk;
wire [3:0] D;
wire [3:0] Q;
DFFHQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .Q (Q[3]));
DFFHQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .Q (Q[2]));
DFFRHQX4 \Q_reg[0] (.RN (1'b1), .CK (clk), .D (D[0]), .Q (Q[0]));
DFFHQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .Q (Q[1]));
endmodule

module Rcounter4(clk, rst, out1);
input clk, rst;
output [3:0] out1;
wire clk, rst;
wire [3:0] out1;
wire n_0, n_1, n_2, n_3;
DFFQX1 \out1_reg[3] (.CK (clk), .D (n_3), .Q (out1[3]));
NOR2BX1 g4(.AN (out1[2]), .B (rst), .Y (n_3));
DFFQX1 \out1_reg[2] (.CK (clk), .D (n_2), .Q (out1[2]));
NOR2BX1 g6(.AN (out1[1]), .B (rst), .Y (n_2));
DFFQX1 \out1_reg[1] (.CK (clk), .D (n_1), .Q (out1[1]));
NOR2BX1 g8(.AN (out1[0]), .B (rst), .Y (n_1));
DFFQX1 \out1_reg[0] (.CK (clk), .D (n_0), .Q (out1[0]));
OR2XL g9(.A (out1[3]), .B (rst), .Y (n_0));
endmodule

module freq_div(clk, rst, out3);
input clk, rst;
output out3;
wire clk, rst;
wire out3;
wire [3:0] temp;
wire n_0, n_1, n_2, n_3, n_4, n_5;
DFFQX1 \temp_reg[2] (.CK (clk), .D (n_5), .Q (out3));
NOR2BX1 g56(.A (rst), .B (n_4), .Y (n_5));
DFFQX1 \temp_reg[1] (.CK (clk), .D (n_3), .Q (temp[1]));
XNOR2BX1 g58(.A (out3), .B (n_1), .Y (n_4));
NOR2BX1 g59(.AN (n_2), .B (rst), .Y (n_3));
ADDHX1 g60(.A (temp[1]), .B (temp[0]), .CO (n_1), .S (n_2));
DFFQX1 \temp_reg[0] (.CK (clk), .D (n_0), .Q (temp[0]));
NOR2XL g62(.A (temp[0]), .B (rst), .Y (n_0));
endmodule

module group17(clk, rst, A, B, C, OUT);
input clk, rst;
input [3:0] A, B;
input [7:0] C;
output [3:0] OUT;
wire clk, rst;
wire [3:0] A, B;
wire [7:0] C;
wire [3:0] OUT;
wire [7:0] cp_c;
wire [3:0] dp_a;
wire [3:0] dp_b;
wire [3:0] dp_out1;
wire dp_out3, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
wire n_16, n_17, n_18, n_19, n_20, n_21, n_22, n_23;
wire n_24, n_25, n_26, n_28, n_29, n_30, n_31, n_32;
wire n_33, n_34, n_35, n_36, n_40, n_41, n_42, n_43;
wire n_44, n_45, n_46, n_47, n_48, n_72, n_73;
DFF8 cp_D1(clk, C, cp_c);
DFF4 dp_D2(clk, A, dp_a);
DFF4_18 dp_D3(clk, B, dp_b);
DFF4_17 dp_D4(clk, {n_48, n_47, n_46, n_45}, OUT);
Rcounter4 dp_c1(clk, rst, dp_out1);
freq_div dp_f1(clk, rst, dp_out3);
OAI211X4 g2213(A0 (n_72), .A1 (n_42), .B0 (n_44), .C0 (n_43), .Y

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SDFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .SI (Q[2]), .SE (DFT_sen),
.Q (Q[3]));
SDFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .SI (Q[1]), .SE (DFT_sen),
.Q (Q[2]));
SDFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .SI (Q[0]), .SE (DFT_sen),
.Q (Q[1]));
endmodule

module DFF4_18(clk, D, Q, DFT_sdi, DFT_sen, DFT_sdi_1);
input clk, DFT_sdi, DFT_sen, DFT_sdi_1;
input [3:0] D;
output [3:0] Q;
wire clk, DFT_sdi, DFT_sen, DFT_sdi_1;
wire [3:0] D;
wire [3:0] Q;
SDFFQX1 \Q_reg[3] (.CK (clk), .D (D[3]), .SI (Q[2]), .SE (DFT_sen),
.Q (Q[3]));
SDFFQX1 \Q_reg[2] (.CK (clk), .D (D[2]), .SI (DFT_sdi_1), .SE
(DFT_sen), .Q (Q[2]));
SDFFQX1 \Q_reg[0] (.CK (clk), .D (D[0]), .SI (DFT_sdi), .SE
(DFT_sen), .Q (Q[0]));
SDFFQX1 \Q_reg[1] (.CK (clk), .D (D[1]), .SI (Q[0]), .SE (DFT_sen),
.Q (Q[1]));
endmodule

module DFF4_17(clk, D, Q, DFT_sdi, DFT_sen);
input clk, DFT_sdi, DFT_sen;
input [3:0] D;
output [3:0] Q;
wire clk, DFT_sdi, DFT_sen;
wire [3:0] D;
wire [3:0] Q;
SDFFFHQX8 \Q_reg[3] (.CK (clk), .D (D[3]), .SI (Q[2]), .SE (DFT_sen),
.Q (Q[3]));
SDFFFHQX8 \Q_reg[2] (.CK (clk), .D (D[2]), .SI (Q[1]), .SE (DFT_sen),
.Q (Q[2]));
SDFFFHQX8 \Q_reg[0] (.CK (clk), .D (D[0]), .SI (DFT_sdi), .SE
(DFT_sen), .Q (Q[0]));
SDFFFHQX8 \Q_reg[1] (.CK (clk), .D (D[1]), .SI (Q[0]), .SE (DFT_sen),
.Q (Q[1]));
endmodule

module DFF4_17(clk, D, Q, DFT_sdi, DFT_sen);
input clk, DFT_sdi, DFT_sen;
input [3:0] D;
output [3:0] Q;
wire clk, DFT_sdi, DFT_sen;
wire [3:0] D;
wire [3:0] Q;
SDFFFHQX8 \Q_reg[3] (.CK (clk), .D (D[3]), .SI (Q[2]), .SE (DFT_sen),
.Q (Q[3]));
SDFFFHQX8 \Q_reg[2] (.CK (clk), .D (D[2]), .SI (Q[1]), .SE (DFT_sen),
.Q (Q[2]));
SDFFFHQX8 \Q_reg[0] (.CK (clk), .D (D[0]), .SI (DFT_sdi), .SE
(DFT_sen), .Q (Q[0]));
SDFFFHQX8 \Q_reg[1] (.CK (clk), .D (D[1]), .SI (Q[0]), .SE (DFT_sen),
.Q (Q[1]));
endmodule

module Rcounter4(clk, rst, out1, DFT_sdi, DFT_sen);
input clk, rst, DFT_sdi, DFT_sen;
output [3:0] out1;
wire clk, rst, DFT_sdi, DFT_sen;
wire [3:0] out1;
wire n_4, n_5, n_6, n_7;
SDFFQX1 \out1_reg[3] (.CK (clk), .D (n_7), .SI (out1[2]), .SE
(DFT_sen), .Q (out1[3]));
NOR2BX1 g38(.AN (out1[2]), .B (rst), .Y (n_7));
SDFFQX1 \out1_reg[2] (.CK (clk), .D (n_6), .SI (out1[1]), .SE
(DFT_sen), .Q (out1[2]));
SDFFQX1 \out1_reg[1] (.CK (clk), .D (n_5), .SI (out1[0]), .SE
(DFT_sen), .Q (out1[1]));
NOR2BX1 g40(.AN (out1[1]), .B (rst), .Y (n_6));
SDFFQX1 \out1_reg[0] (.CK (clk), .D (n_5), .SI (out1[0]), .SE
(DFT_sen), .Q (out1[1]));
endmodule

module freq_div(clk, rst, out3, DFT_sdi, DFT_sen);
input clk, rst, DFT_sdi, DFT_sen;
output out3;
wire clk, rst, DFT_sdi, DFT_sen;
wire out3;
wire [3:0] temp;
wire n_7, n_8, n_9, n_10, n_11, n_12;
SDFFQX1 \temp_reg[2] (.CK (clk), .D (n_12), .SI (temp[1]), .SE
(DFT_sen), .Q (out3));
NOR2XL g110(.A (rst), .B (n_11), .Y (n_12));
SDFFQX1 \temp_reg[1] (.CK (clk), .D (n_10), .SI (temp[0]), .SE
(DFT_sen), .Q (temp[1]));
XNOR2BX1 g112(.A (out3), .B (n_8), .Y (n_11));
NOR2BX1 g113(.AN (n_9), .B (rst), .Y (n_10));
ADDHX1 g114(.A (temp[1]), .B (temp[0]), .CO (n_8), .S (n_9));
SDFFQX1 \temp_reg[0] (.CK (clk), .D (n_7), .SI (DFT_sdi), .SE
(DFT_sen), .Q (temp[0]));
NOR2XL g116(.A (rst), .B (temp[0]), .Y (n_7));
endmodule

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(n_45));
NAND4X6 g2214(.A (n_73), .B (n_25), .C (n_30), .D (n_5), .Y (n_44));
OAI31X4 g2215(.A0 (n_17), .A1 (n_41), .A2 (n_72), .B0 (n_32), .Y
(n_46);
OAI31X4 g2216(.A0 (n_18), .A1 (n_41), .A2 (n_72), .B0 (n_35), .Y
(n_48));
OAI31X4 g2217(.A0 (n_15), .A1 (n_41), .A2 (n_72), .B0 (n_33), .Y
(n_47);
AOI22X4 g2218(.A0 (dp_out3), .A1 (n_41), .B0 (dp_out1[0]), .B1
(n_31), .Y (n_43));
NAND2X6 g2219(.A (n_16), .B (n_40), .Y (n_42));
CLKINVX8 g2220(.A (n_41), .Y (n_40));
CLKAND2X12 g2221(.A (n_36), .B (n_28), .Y (n_41));
NOR2X4 g2226(.A (n_9), .B (n_29), .Y (n_36));
NAND2X4 g2227(.A (dp_out1[3]), .B (n_31), .Y (n_35));
NAND3X6 g2229(.A (n_23), .B (n_21), .C (n_24), .Y (n_34));
NAND2X4 g2230(.A (dp_out1[2]), .B (n_31), .Y (n_33));
NAND2X4 g2231(.A (dp_out1[1]), .B (n_31), .Y (n_32));
CLKINVX6 g2232(.A (n_30), .Y (n_31));
AOI21X4 g2233(.A0 (n_14), .A1 (n_19), .B0 (n_11), .Y (n_29));
OAI21X4 g2234(.A0 (n_14), .A1 (n_1), .B0 (n_11), .Y (n_28));
AND2X6 g2235(.A (n_23), .B (n_22), .Y (n_30));
AOI21X4 g2237(.A0 (cp_c[4]), .A1 (n_4), .B0 (cp_c[5]), .Y (n_26));
NAND2X2 g2238(.A (n_21), .B (n_24), .Y (n_25));
NOR2X4 g2240(.A (n_11), .B (n_7), .Y (n_24));
AOI2BB1X2 g2241(.A0N (cp_c[7]), .A1N (cp_c[6]), .B0 (n_7), .Y
(n_22));
NAND2X4 g2242(.A (n_13), .B (n_20), .Y (n_23));
OAI21X4 g2244(.A0 (cp_c[2]), .A1 (cp_c[1]), .B0 (cp_c[3]), .Y (n_20));
OR2X4 g2245(.A (n_10), .B (n_14), .Y (n_21));
NAND4X6 g2246(.A (cp_c[1]), .B (cp_c[2]), .C (cp_c[3]), .D (cp_c[5]),
.Y (n_19));
NOR3X6 g2247(.A (cp_c[7]), .B (cp_c[4]), .C (cp_c[5]), .Y (n_7));
XNOR2X1 g2249(.A (dp_a[3]), .B (dp_b[3]), .Y (n_18));
XNOR2X1 g2250(.A (dp_a[1]), .B (dp_b[1]), .Y (n_17));
CLKXOR2X2 g2251(.A (dp_a[0]), .B (dp_b[0]), .Y (n_16));
XNOR2X1 g2252(.A (dp_a[2]), .B (dp_b[2]), .Y (n_15));
NOR2X4 g2256(.A (cp_c[7]), .B (cp_c[5]), .Y (n_13));
NAND2X8 g2258(.A (cp_c[4]), .B (cp_c[5]), .Y (n_14));
CLKINVX6 g2259(.A (cp_c[1]), .Y (n_12));
CLKINVX3 g2260(.A (cp_c[6]), .Y (n_11));
CLKINVX6 g2261(.A (cp_c[3]), .Y (n_10));
CLKINVX2 g2262(.A (cp_c[7]), .Y (n_9));
CLKINVX3 g2263(.A (cp_c[0]), .Y (n_8));
CLKINVX8 fopt(.A (cp_c[2]), .Y (n_6));
OR2X6 g2(.A (n_9), .B (n_26), .Y (n_5));
NAND4X4 g2272(.A (n_8), .B (n_6), .C (n_12), .D (n_10), .Y (n_4));
NOR2X6 g2273(.A (n_3), .B (n_2), .Y (n_1));
NAND2X4 g2274(.A (n_8), .B (n_6), .Y (n_3));
NAND2X6 g2275(.A (n_12), .B (n_10), .Y (n_2));
CLKAND2X6 g2278(.A (n_34), .B (n_5), .Y (n_72));
MX4X2 g2279(.A (dp_a[0]), .B (dp_a[2]), .C (dp_a[1]), .D (dp_a[3]),
.S0 (dp_b[1]), .S1 (dp_b[0]), .Y (n_73));
endmodule

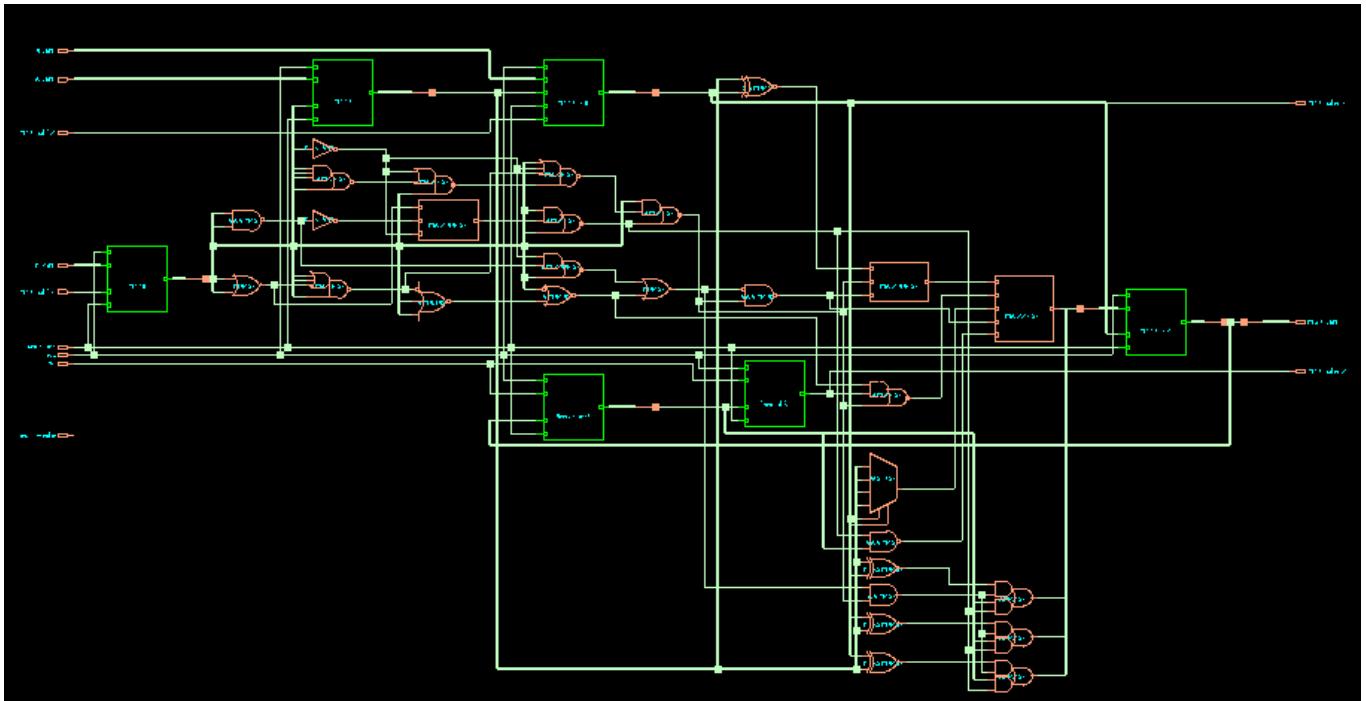
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module group17(clk, rst, A, B, C, OUT, scan_en, test_mode, DFT_sdi_1,
DFT_sdo_1, DFT_sdi_2, DFT_sdo_2);
input clk, rst, scan_en, test_mode, DFT_sdi_1, DFT_sdi_2;
input [3:0] A, B;
input [7:0] C;
output [3:0] OUT;
output DFT_sdo_1, DFT_sdo_2;
wire clk, rst, scan_en, test_mode, DFT_sdi_1, DFT_sdi_2;
wire [3:0] A, B;
wire [7:0] C;
wire [3:0] OUT;
wire DFT_sdo_1, DFT_sdo_2;
wire [7:0] cp_c;
wire [3:0] dp_a;
wire [3:0] dp_b;
wire [3:0] dp_out1;
wire n_31, n_32, n_33, n_34, n_35, n_36, n_37, n_38;
wire n_39, n_40, n_41, n_42, n_43, n_44, n_45, n_46;
wire n_47, n_48, n_49, n_54, n_55, n_56, n_57, n_58;
wire n_59, n_80, n_81, n_82, n_83;
DFF8 cp_D1(clk, C, cp_c, DFT_sdi_1, scan_en);
DFF4 dp_D2(clk, A, dp_a, cp_c[7], scan_en);
DFF4_18 dp_D3(clk, B, {dp_b[3:2], DFT_sdo_1, dp_b[0]}, dp_a[3],
scan_en, DFT_sdi_2);
DFF4_17 dp_D4(clk, {n_80, n_81, n_82, n_83}, OUT, dp_b[3], scan_en);
Rcounter4 dp_c1(clk, rst, dp_out1, OUT[3], scan_en);
freq_div dp_f1(clk, rst, DFT_sdo_2, dp_out1[3], scan_en);
OAI221X1 g893(.A0 (n_59), .A1 (n_56), .B0 (n_47), .B1 (n_58), .C0
(n_49), .Y (n_83));
AO22X1 g894(.A0 (n_36), .A1 (n_57), .B0 (dp_out1[2]), .B1 (n_45), .Y
(n_81));
AO22X1 g895(.A0 (n_37), .A1 (n_57), .B0 (dp_out1[3]), .B1 (n_45), .Y
(n_80));
AO22X1 g896(.A0 (n_35), .A1 (n_57), .B0 (dp_out1[1]), .B1 (n_45), .Y
(n_82));
OAI2BB1X1 g897(.A0N (n_38), .A1N (n_55), .B0 (n_58), .Y (n_59));
NAND2BX1 g898(.AN (n_54), .B (n_55), .Y (n_58));
AOI21X1 g899(.A0 (n_46), .A1 (DFT_sdo_2), .B0 (n_55), .Y (n_56));
AND2X1 g900(.A (n_54), .B (n_55), .Y (n_57));
AOI21X1 g901(.A0 (cp_c[7]), .A1 (n_48), .B0 (n_45), .Y (n_55));
NAND2XL g902(.A (n_45), .B (dp_out1[0]), .Y (n_49));
OR2X1 g903(.A (n_39), .B (n_46), .Y (n_54));
OAI31X1 g904(.A0 (cp_c[6]), .A1 (n_31), .A2 (n_42), .B0 (n_44), .Y
(n_48));
MX4X1 g905(.A (dp_a[0]), .B (dp_a[1]), .C (dp_a[2]), .D (dp_a[3]),
.S0 (dp_b[0]), .S1 (DFT_sdo_1), .Y (n_47));
NOR2BX1 g906(.AN (cp_c[7]), .B (n_43), .Y (n_46));
OAI21X1 g907(.A0 (n_31), .A1 (n_41), .B0 (cp_c[6]), .Y (n_44));
AOI21X1 g908(.A0 (cp_c[6]), .A1 (n_40), .B0 (cp_c[7]), .Y (n_45));
NOR3BX1 g909(.AN (n_42), .B (cp_c[6]), .C (cp_c[5]), .Y (n_43));
AOI31X1 g910(.A0 (cp_c[1]), .A1 (cp_c[2]), .A2 (cp_c[3]), .B0
(cp_c[4]), .Y (n_41));
OAI31X1 g911(.A0 (cp_c[0]), .A1 (cp_c[3]), .A2 (n_32), .B0 (cp_c[4]),
.Y (n_42));
OAI2BB1X1 g912(.A0N (n_32), .A1N (n_34), .B0 (n_31), .Y (n_40));
AOI2BB1X1 g913(.A0N (n_31), .A1N (n_33), .B0 (cp_c[7]), .Y (n_39));
XNOR2X1 g914(.A (dp_a[0]), .B (dp_b[0]), .Y (n_38));
CLKXOR2X1 g915(.A (dp_b[3]), .B (dp_a[3]), .Y (n_37));
CLKXOR2X1 g916(.A (dp_b[2]), .B (dp_a[2]), .Y (n_36));
CLKXOR2X1 g917(.A (dp_a[1]), .B (DFT_sdo_1), .Y (n_35));
CLKINVX1 g918(.A (n_33), .Y (n_34));
NAND2XL g919(.A (cp_c[4]), .B (cp_c[3]), .Y (n_33));
OR2X1 g920(.A (cp_c[2]), .B (cp_c[1]), .Y (n_32));
CLKINVX1 g921(.A (cp_c[5]), .Y (n_31));
endmodule

```

NETLIST MAPPING AFTER SCAN CHAIN INSERTION



RTL	NETLIST	SCHEMATIC
<p>DFF8 Module</p> <pre>//----- module DFF8(input clk, input [7:0]D, output reg [7:0]Q); always@(posedge clk) begin Q<=D; end endmodule</pre>	<pre>module DFF8(clk, D, Q, DFT_sdi, DFT_sen); input clk, DFT_sdi, DFT_sen; input [7:0] D; output [7:0] Q; wire CLK_DFT_sdi, DFT_sen; wire [7:0] Q; wire [7:0] Q; SDFHDX4 _Q reg[4] (.CK (clk), .D (D[4]), .SI (Q[3]), .SE (DFT_sen), .Q (Q[4])); SDFHDX8 _Q reg[6] (.CK (clk), .D (D[6]), .SI (Q[5]), .SE (DFT_sen), .Q (Q[6])); SDFHDX4 _Q reg[7] (.CK (clk), .D (D[7]), .SI (Q[6]), .SE (DFT_sen), .Q (Q[7])); SDFHDX4 _Q reg[8] (.CK (clk), .D (D[8]), .SI (DFT_sdi), .SE (DFT_sen), .Q (Q[8])); SDFHDX8 _Q reg[2] (.CK (clk), .D (D[2]), .SI (Q[1]), .SE (DFT_sen), .Q (Q[2])); SDFHDX8 _Q reg[5] (.CK (clk), .D (D[5]), .SI (Q[4]), .SE (DFT_sen), .Q (Q[5])); SDFHDX8 _Q reg[3] (.CK (clk), .D (D[3]), .SI (Q[2]), .SE (DFT_sen), .Q (Q[3])); SDFHDX8 _Q reg[1] (.CK (clk), .D (D[1]), .SI (Q[0]), .SE (DFT_sen), .Q (Q[1])); endmodule</pre>	
<p>Rcounter4 Module</p> <pre>//-----Ring counter----- module Rcounter4(clk, rst, out1, DFT_sdi, DFT_sen); input clk, input rst, output reg [3:0]out1; wire CLK_DFT_sdi, DFT_sen; output [3:0] out1; wire CLK_rst, DFT_sdi, DFT_sen; wire [3:0] out1; wire n_4, n_5, n_6, n_7; SDFHDX2 \out1 reg[3] (.CK (clk), .D (n_7), .SI (out1[2]), .SE (DFT_sen), .Q (out1[3])); NOR2BX1 g38(.AN (out1[2]), .B (rst), .Y (n_7)); SDFHDX2 \out1 reg[2] (.CK (clk), .D (n_6), .SI (out1[1]), .SE (DFT_sen), .Q (out1[2])); NOR2BX1 g40(.AN (out1[1]), .B (rst), .Y (n_6)); SDFHDX2 \out1 reg[1] (.CK (clk), .D (n_5), .SI (out1[0]), .SE (DFT_sen), .Q (out1[1])); NOR2BX1 g41(.AN (out1[0]), .B (rst), .Y (n_5)); SDFHDX2 \out1 reg[0] (.CK (clk), .D (n_4), .SI (DFT_sdi), .SE (DFT_sen), .Q (out1[0])); OR2X1 g19(.A (out1[3]), .B (rst), .Y (n_4)); endmodule</pre>		

Freq_divider Module <pre>//-----Frequency Divider----- module freq_div (input clk, input rst, output out3); reg [3:0]temp; always @ (posedge clk) begin if(rst) temp <= 4'b0000; else temp <= temp + 1; end assign out3=temp[2]; endmodule</pre>	<pre>module freq_div(clk, rst, out3, DFT_sdi, DFT_sen); input clk, rst, DFT_sdi, DFT_sen; output out3; wire clk, rst, DFT_sdi, DFT_sen; wire out3; wire [3:0] temp; wire n_0, n_8, n_9, n_10, n_11, n_12; SDFFFTRX1 temp1(.temp1(.temp[1]), .D(n_12), .RN(n_9), .SI(DFT_sen), .SE(DFT_sen)); NOR2XL g11(A(rst), .B(n_11), .Y(n_12)); SDFFFTRX1 temp2(.temp2(.temp[1]), .D(n_10), .RN(n_9), .SI(DFT_sen), .SE(DFT_sen)); NOR2XL g12(A(rst), .B(n_9), .Y(n_11)); SDFFFTRX1 temp3(.temp3(.temp[1]), .D(n_8), .RN(n_9), .SI(DFT_sdi), .SE(DFT_sen)); NOR2XL g13(A(rst), .B(n_8), .Y(n_9)); AND2XL g14(.A(temp1), .B(temp2), .Y(n_10)); NAND2XL g15(.A(temp2), .B(temp3), .Y(n_9)); NOR2XL g16(.A(temp3), .B(rst), .Y(n_8)); NOR2XL g17(.A(temp3), .B(rst), .Y(n_8)); endmodule</pre>	
DFF4 Module <pre>//-----D flip flop 4 bits- module DF4(input clk, input [3:0]D, output reg [3:0]); always@(posedge clk) begin D<=D; end endmodule</pre>	<pre>module DFF4_17(clk, D, Q, DFT_sdi, DFT_sen); input clk, DFT_sdi, DFT_sen; input [3:0] D; output [3:0] Q; wire clk, DFT_sdi, DFT_sen; wire [3:0] D; wire [3:0] Q; SDFFFOX4 Q_reg3(.CK(clk), .D(D[3]), .SI(0[2]), .SE(DFT_sen), .O(0[1])); SDFFFOX4 Q_reg2(.CK(clk), .D(D[2]), .SI(0[1]), .SE(DFT_sen), .O(0[2])); SDFFFOX8 Q_reg0(.CK(clk), .D(D[0]), .SI(DFT_sdi), .SE(DFT_sen), .O(0[0])); SDFFFOX4 Q_reg1(.CK(clk), .D(D[1]), .SI(0[0]), .SE(DFT_sen), .O(0[1])); endmodule</pre>	

Timing report of a same path in the original netlist and the scan-chain inserted netlist

Without Scan chain	With Scan chain																																																																																																																																									
<p>Endpoint: dp_D4/Q_reg[0]/D (^) checked with leading edge of 'clk' Beginpoint: cp_D1/Q_reg[2]/Q (^) triggered by leading edge of 'clk'</p> <p>Path Groups: {clk}</p> <table border="0"> <tr> <td>Other End Arrival Time</td> <td>0.000</td> </tr> <tr> <td>- Setup</td> <td>0.177</td> </tr> <tr> <td>+ Phase Shift</td> <td>15.000</td> </tr> <tr> <td>- Uncertainty</td> <td>0.020</td> </tr> <tr> <td>= Required Time</td> <td>14.883</td> </tr> <tr> <td>= Arrival Time</td> <td>1.479</td> </tr> <tr> <td>= Slack Time</td> <td>13.323</td> </tr> </table> <p>Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000</p> <table border="0"> <thead> <tr> <th>Pin</th> <th>Cell</th> <th>Delay</th> <th>Slew</th> <th>Required</th> <th>Arrival</th> <th>Edge</th> <th>Wire</th> <th>Wireload</th> </tr> <tr> <th></th> <th></th> <th>Time</th> <th></th> <th>Time</th> <th>Edge</th> <th></th> <th>Load</th> <th>Model</th> </tr> </thead> <tbody> <tr> <td>CK</td> <td>-</td> <td>-</td> <td>0.003</td> <td>13.323</td> <td>0.000</td> <td>^</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Q</td> <td>DFFQX1</td> <td>0.328</td> <td>0.057</td> <td>13.652</td> <td>0.328</td> <td>v</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>NOR2XL</td> <td>0.158</td> <td>0.184</td> <td>13.810</td> <td>0.486</td> <td>^</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>INVXL</td> <td>0.054</td> <td>0.067</td> <td>13.864</td> <td>0.540</td> <td>v</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>OA131X1</td> <td>0.133</td> <td>0.154</td> <td>13.997</td> <td>0.674</td> <td>^</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>NOR2XL</td> <td>0.071</td> <td>0.076</td> <td>14.068</td> <td>0.744</td> <td>v</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>OA121X1</td> <td>0.093</td> <td>0.092</td> <td>14.161</td> <td>0.838</td> <td>^</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>OA132X1</td> <td>0.151</td> <td>0.312</td> <td>14.312</td> <td>0.988</td> <td>v</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>NOR2BX1</td> <td>0.199</td> <td>0.192</td> <td>14.511</td> <td>1.188</td> <td>^</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>OA32X1</td> <td>0.097</td> <td>0.174</td> <td>14.608</td> <td>1.285</td> <td>v</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>OA131X1</td> <td>0.079</td> <td>0.174</td> <td>14.688</td> <td>1.364</td> <td>^</td> <td>0.000</td> <td>Wireload model(.lib None Generated)</td> </tr> <tr> <td>Y</td> <td>OA121X1</td> <td>0.059</td> td="0.096" style="text-align: right;">14.746</tr></tbody></table>	Other End Arrival Time	0.000	- Setup	0.177	+ Phase Shift	15.000	- Uncertainty	0.020	= Required Time	14.883	= Arrival Time	1.479	= Slack Time	13.323	Pin	Cell	Delay	Slew	Required	Arrival	Edge	Wire	Wireload			Time		Time	Edge		Load	Model	CK	-	-	0.003	13.323	0.000	^	0.000	Wireload model(.lib None Generated)	Q	DFFQX1	0.328	0.057	13.652	0.328	v	0.000	Wireload model(.lib None Generated)	Y	NOR2XL	0.158	0.184	13.810	0.486	^	0.000	Wireload model(.lib None Generated)	Y	INVXL	0.054	0.067	13.864	0.540	v	0.000	Wireload model(.lib None Generated)	Y	OA131X1	0.133	0.154	13.997	0.674	^	0.000	Wireload model(.lib None Generated)	Y	NOR2XL	0.071	0.076	14.068	0.744	v	0.000	Wireload model(.lib None Generated)	Y	OA121X1	0.093	0.092	14.161	0.838	^	0.000	Wireload model(.lib None Generated)	Y	OA132X1	0.151	0.312	14.312	0.988	v	0.000	Wireload model(.lib None Generated)	Y	NOR2BX1	0.199	0.192	14.511	1.188	^	0.000	Wireload model(.lib None Generated)	Y	OA32X1	0.097	0.174	14.608	1.285	v	0.000	Wireload model(.lib None Generated)	Y	OA131X1	0.079	0.174	14.688	1.364	^	0.000	Wireload model(.lib None Generated)	Y	OA121X1	0.059	1.423	v	0.000	Wireload model(.lib None Generated)
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Y	OA12BB1X1	0.056	0.852	14.803	1.479	^	0.000	Wireload model(.lib None Generated)																																																																																																																																		
D	DFFQX1	0.000	0.052	14.803	1.479	^	-	-																																																																																																																																		

 Endpoint: dp_D4/Q_reg[0]/D (^) checked with leading edge of 'clk' Beginpoint: cp_D1/Q_reg[2]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} | | | |------------------------|--------| | Other End Arrival Time | 0.000 | | - Setup | 0.261 | | + Phase Shift | 15.000 | | - Uncertainty | 0.020 | | = Required Time | 14.719 | | = Arrival Time | 3.443 | | = Slack Time | 11.275 | Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000 | Pin | Cell | Delay | Slew | Required | Arrival | Edge | |-----|------------|-------|-------|----------|---------|------| | | | Time | | Time | Edge | | | CK | - | - | 0.003 | 11.275 | 0.000 | ^ | | Q | SDFFFOX1 | 0.590 | 0.510 | 11.866 | 0.590 | ^ | | Y | AND2XL | 0.340 | 0.229 | 12.206 | 0.930 | ^ | | Y | AOI221X1 | 0.210 | 0.291 | 12.416 | 1.141 | v | | Y | AOI12BB1X1 | 0.491 | 0.480 | 12.907 | 1.632 | v | | Y | AOI21X1 | 0.573 | 0.634 | 13.481 | 2.205 | ^ | | Y | NAND2XL | 0.593 | 0.669 | 14.073 | 2.798 | v | | Y | CLKINVX1 | 0.347 | 0.335 | 14.421 | 3.145 | ^ | | Y | A022X1 | 0.298 | 0.160 | 14.719 | 3.443 | ^ | | D | SDFFFOX1 | 0.000 | 0.160 | 14.719 | 3.443 | ^ | |

With the scan chain for the same path the slack is reduced as due to the scan chain the arrival time (AT) is increased from 1.479 to 3.443 and also the required time (RT) is reduced from the 14.883 to 14.719 and as setup slack is slack = RT - AT hence the slack is degraded by an effective value of (3.443-1.479) + (14.883-14.719). slack is degraded by the 2.128 time units.

GROUP 17

Aakash Gupta

MT21150

Neeraj

MT21156

Prapti Makkar

MT21202

VDF PROJECT

PART 2

PROBLEM NUMBER - 7

If C=8'h00 TO 8'h59, 4-bit ring counter

C=8'h78 TO 8'h90, 4x1 Mux

C=8'hB1 TO 8'hED, frequency divider by 8

Else, bitwise A OR B

ANALYSIS

1. Ports overlap even after specified locations in the I/O file.

Explanation:

A chip's I/O ports should be kept as small as possible. As a result, costs are lowered. After the plan, it was discovered that some of the ports were being multiplexed. These ports can be used as input or output. This is because the tool assumes that the specified port will be utilized as an input or an output port at a time, rather than all simultaneously

2. After Placement, total power consumption is decreased.

Explanation:

After the Placement, it was expected that the power consumption would increase due to the addition of both components and interconnects RC parasitics, but as we had the sufficient slack hence tool may have resized the cells accordingly, and power consumption reduced

3. Total Area was coming out to be the same after the Placement.

Explanation:

Since there is no additional instance added hence the area remains the same.

4. Hold violations are fixed after the CTS(clock tree synthesis).

Explanation:

Because the clock is transmitted only after CTS (the actual clock tree is formed, clock buffers are inserted, and the clock tree hierarchy, clock skew, and insertion delay come into play, requiring timing analysis), hold violations are only corrected after CTS.

5. Area has increased after CTS.

Explanation:

As buffers and inverters are inserted additionally to fix the violations, the area gets increased.

6. Power consumption has increased after CTS.

Explanation:

As additional buffers and inverters are added after the CTS, these buffers will also consume some power, increasing the total power consumption.

7. Area and Slack are the same after CTS and Detailed Routing.

Explanation:

As enough optimization is done after CTS itself, there was no further scope of the optimization after the detailed routing and hence the area and slack are coming out to be the same.

8. Total power has increased after detailed routing.

Explanation:

As the internal power and switching power have grown without the addition of new cells, it can be assumed that some of the cells' sizes have been expanded to better timing restrictions as we had enough slack to do so, causing the switching and internal power to increase.

STEP 1

BEFORE PHYSICAL DESIGN

Before starting the physical design, we have done the logic synthesis part, including the synthesis, DFT, and STA; we have done these steps using the cadence tempus, cadence genus, and cadence conformal tools. Now we are proceeding toward our next step, physical design using the tool Cadence Innovus.

Comparison of Floorplanning done with core utilization of 0.5 and with 0.8 is done for all the timing, area and power is done.

1. TIMING ANALYSIS

A. Worst case hold slack

- Core Utilization of 0.5

```

Path 1: MET Late External Delay Assertion
Endpoint: OUT[0] (^) checked with leading edge of 'clk'
Beginpoint: dp_D4/Q_reg[0]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time      0.000
- External Delay            3.000
+ Phase Shift               11.000
- Uncertainty                1.000
= Required Time             7.000
- Arrival Time              1.072
= Slack Time                5.928
= Slack Time(original)      5.928
Clock Rise Edge           0.000
= Beginpoint Arrival Time  0.000
+-----+
| Load | Slew | Retime | Cell | Instance | Pin | Delay | Retime | Arrival | Required |
|      | Slew |        |       |          |     |       | Delay | Time   | Time    |
+-----+
| 0.047 | 0.003 | 0.003 |       |          | clk | 0.000 | 0.000 | 0.000 | 5.928 |
| 0.047 | 0.003 | 0.003 | SDFFHQX8 | dp_D4/Q_reg[0] | CK | 0.000 | 0.000 | 0.000 | 5.928 |
| 1.003 | 1.028 | 1.028 | SDFFHQX8 | dp_D4/Q_reg[0] | Q  | 1.072 | 1.072 | 1.072 | 7.000 |
| 1.003 | 1.028 | 1.028 | group17 |                 | OUT[0] | 0.000 | 0.000 | 1.072 | 7.000 |
+-----+

```

• Core Utilization of 0.8

```

Path 1: MET Late External Delay Assertion
Endpoint: OUT[0] (^) checked with leading edge of 'clk'
Beginpoint: dp_D4/Q_reg[0]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time      0.000
- External Delay            3.000
+ Phase Shift               11.000
- Uncertainty                1.000
= Required Time             7.000
- Arrival Time              1.072
= Slack Time                5.928
= Slack Time(original)      5.928
Clock Rise Edge             0.000
= Beginpoint Arrival Time   0.000
+
| Load | Slew | Retime | Cell | Instance | Pin | Delay | Retime | Arrival | Required |
|     |     | Slew |     |     |     |     | Delay | Delay | Time | Time |
+---+---+---+---+---+---+---+---+---+---+---+
| 0.047 | 0.003 | 0.003 |       |       | clk | 0.000 | 0.000 | 0.000 | 0.000 | 5.928 |
| 0.047 | 0.003 | 0.003 | SDFFHQX8 | dp_D4/Q_reg[0] | CK | 0.000 | 0.000 | 0.000 | 0.000 | 5.928 |
| 1.003 | 1.028 | 1.028 | SDFFHQX8 | dp_D4/Q_reg[0] | Q  | 1.072 | 1.072 | 1.072 | 1.072 | 7.000 |
| 1.003 | 1.028 | 1.028 | group17 |           | OUT[0] | 0.000 | 0.000 | 0.000 | 1.072 | 7.000 |
+

```

B. Worst case setup slack

- Core Utilization of 0.5

```

Path 1: VIOLATED Hold Check with Pin dp_D4/Q_reg[1]/CK
Endpoint: dp_D4/Q_reg[1]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of '@'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.079
+ Phase Shift 0.000
+ Uncertainty 0.002
= Required Time 0.001
Arrival Time 0.000
Slack Time -0.081
= Slack Time(original) -0.081
Clock Rise Edge 0.000
+ Input Delay 0.000
= Beginpoint Arrival Time 0.000
Timing Path:
+-----+
| Load | Slew | Retime | Cell | Instance | Pin | Delay | Retime | Arrival | Required |
|     |     |     |     |           |     |     |     |     |     |
+-----+
| 0.064 | 0.003 | 0.003 | SDFFHQX8 |          | scan_en | SE | 0.000 | 0.000 | 0.081 |
| 0.064 | 0.003 | 0.003 | SDFFHQX8 | dp_D4/Q_reg[1] |          |     | 0.000 | 0.000 | 0.081 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Load | Slew | Retime | Cell | Instance | Pin | Delay | Retime | Arrival | Required |
|     |     |     |     |           |     |     |     |     |     |
+-----+
| 0.047 | 0.003 | 0.003 | SDFFHQX8 |          | clk | CK | 0.000 | 0.000 | -0.081 |
| 0.047 | 0.003 | 0.003 | SDFFHQX8 | dp_D4/Q_reg[1] |          |     | 0.000 | 0.000 | -0.081 |
+-----+

```

- Core Utilization of 0.8

```

Path 1: VIOLATED Hold Check with Pin dp_D4/Q_reg[1]/CK
Endpoint: dp_D4/Q_reg[1]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of '@'
Path Groups: {clk}
Analysis View: view1
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.000
+ Hold 0.079
+ Phase Shift 0.000
+ Uncertainty 0.002
= Required Time 0.081
Arrival Time 0.000
Slack Time -0.081
= Slack Time(original) -0.081
Clock Rise Edge 0.000
+ Input Delay 0.000
= Beginpoint Arrival Time 0.000
Timing Path:
+-----+
| Load | Slew | Retime | Cell | Instance | Pin | Delay | Retime | Arrival | Required |
|     |     |     |     |           |     |     |     |     |     |
+-----+
| 0.064 | 0.003 | 0.003 | SDFFHQX8 |          | scan_en | SE | 0.000 | 0.000 | 0.081 |
| 0.064 | 0.003 | 0.003 | SDFFHQX8 | dp_D4/Q_reg[1] |          |     | 0.000 | 0.000 | 0.081 |
+-----+
Clock Rise Edge 0.000
= Beginpoint Arrival Time 0.000
Other End Path:
+-----+
| Load | Slew | Retime | Cell | Instance | Pin | Delay | Retime | Arrival | Required |
|     |     |     |     |           |     |     |     |     |     |
+-----+
| 0.047 | 0.003 | 0.003 | SDFFHQX8 |          | clk | CK | 0.000 | 0.000 | -0.081 |
| 0.047 | 0.003 | 0.003 | SDFFHQX8 | dp_D4/Q_reg[1] |          |     | 0.000 | 0.000 | -0.081 |
+-----+

```

The timing report of the setup PBA/GBA slack of the timing path is shown in the screenshot above. We have only examined the worst path between the two registers. The slew displays the signal's transition time from 20% to 80% of its highest value or vice versa. The slew value of the GBA path is displayed in the 'Slew' field in the above screenshot, while the slew values of the PBA path from source to destination are displayed in the 'Retime Slew' field. GBA is the pessimistic view considering the worst delay and worst slew in spite the fact that these both may be from the different paths, but the PBA considers the slew and the delay from the same path have to be considered actually.

The GBA and PBA slacks are the same in the figure shown for the worst-case setup slack worst path. Hence we are taking another path(not the worst path) for the explanation purpose to explain the GBA/PBA and the effect of the slew and load.

= uncertainty	1.000										
= Required Time	9.837										
- Arrival Time	1.415										
= Slack Time	8.422										
= Slack Time(original)	8.415										
Clock Rise Edge	0.000										
= Beginpoint Arrival Time	0.000										
Timing Path:											
Load	Slew	Retime	Cell	Instance	Pin	Delay	Retime	Arrival	Required		
	Slew					Delay	Delay	Time	Time		
0.047	0.003	0.003	SDFFQX1	cp_D1/Q_reg[2]	clk	0.000	0.000	0.000	8.422		
0.047	0.003	0.003	SDFFQX1	cp_D1/Q_reg[2]	Q	0.328	0.328	0.328	8.750		
0.006	0.068	0.068	OR2X1	g920	A	0.000	0.000	0.328	8.750		
0.005	0.065	0.065	OR2X1	g920	Y	0.162	0.162	0.490	8.912		
0.005	0.065	0.065	OAI31X1	g911	A2	0.000	0.000	0.490	8.912		
0.005	0.183	0.182	OAI31X1	g911	Y	0.153	0.153	0.643	9.065		
0.005	0.183	0.182	NOR3BX1	g909	AN	0.000	0.000	0.643	9.065		
0.003	0.124	0.122	NOR3BX1	g909	Y	0.198	0.198	0.841	9.263		
0.003	0.124	0.122	NOR2BX1	g906	B	0.000	0.000	0.841	9.263		
0.004	0.063	0.063	NOR2BX1	g906	Y	0.063	0.063	0.904	9.326		
0.004	0.063	0.063	OR2X1	g903	B	0.000	0.000	0.904	9.326		
0.004	0.059	0.059	OR2X1	g903	Y	0.145	0.145	1.049	9.471		
0.004	0.059	0.059	NAND2BX1	g898	AN	0.000	0.000	1.049	9.471		
0.005	0.122	0.099	NAND2BX1	g898	Y	0.149	0.149	1.198	9.620		
0.005	0.122	0.099	OAI2BB1X1	g897	B0	0.000	0.000	1.198	9.620		
0.003	0.061	0.055	OAI2BB1X1	g897	Y	0.070	0.064	1.263	9.685		
0.003	0.061	0.055	OAI221X1	g893	A0	0.000	0.000	1.263	9.685		
0.003	0.150	0.150	OAI221X1	g893	Y	0.153	0.152	1.415	9.837		
0.003	0.150	0.150	SDFFHQX8	dp_D4/Q_reg[0]	D	0.000	0.000	1.415	9.837		
<hr/>											
Clock Rise Edge											
A AAA											

As we can see from the above screenshot, the GBA and PBA slacks are different as the delays and slew here are considered from different paths in GBA and the same Paths in the case of PBA.

Effect of slew:

Slew is the time it takes for a signal to change from high to low or vice versa. Furthermore, we can see two slew columns in the timing report: retime slew and slew. The retime slew corresponds to the path's absolute slew (PBA), whereas the slew corresponds to an arc's greatest feasible slew (GBA). As a result, the retime slew value is never more than the GBA slew value.

Furthermore, an increase in the slew rate of the signals has a negative impact on the timing performance of a design. This is due to the fact that the slew time increases the cell's delay, and hence the arrival time increases, which leads to a decrease in the setup slack as $\text{setup slack} = \text{RT} - \text{AT}$.

Effect of load:

Load directly affects the slew value and, hence, affects the design's timing. As we can see from the above path report.

For Cell Instance- NAND2BXI	
Load (uF)	Slew at output pin (ns)
0.004	0.059
0.005	0.122

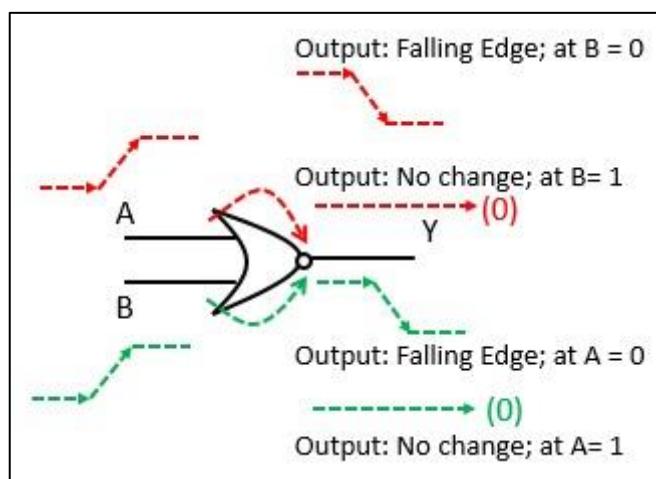
Hence we can clearly see that with the increase in load the value of the slew gets increased, and hence the setup slack decreased.

Effect of Unateness:

A positive unate timing arc occurs when the output signal rises (or does not change) with a rising transition on the input and falls (or does not change) with a falling transition on the input.

A negative unate timing arc occurs when the output signal falls (or shows no change) with a rising transition on the input and rises (or shows no change) with a falling transition on the input.

Therefore, the unateness of an arc is the significant factor that affects the timing performance of the design as unateness defines the slew, which defines the delays and hence the slacks changes.



2. AREA ANALYSIS

- **Core Utilization of 0.5**

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational
Flop	Latch	Clock Gate	Macro	Physical		
group17		65	817.452	0.000	4.541	218.744
594.167	0.000	0.000	0.000	0.000		
cp_D1	DFF8	8	163.490	0.000	0.000	0.000
163.490	0.000	0.000	0.000	0.000		
dp_D2	DFF4	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000		
dp_D3	DFF4_18	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000		
dp_D4	DFF4_17	4	124.132	0.000	0.000	0.000
124.132	0.000	0.000	0.000	0.000		
dp_c1	Rcounter4	8	99.911	0.000	0.000	18.166
81.745	0.000	0.000	0.000	0.000		
dp_f1	freq_div	8	92.342	0.000	0.000	31.033
61.309	0.000	0.000	0.000	0.000		

Design Status: In memory
Design Name: group17
Instances: 65
Hard Macros: 0
Std Cells: 65
Standard Cells in Netlist

Cell Type Instance Count Area (um^2)
OAI2BB1X1 2 10.5966
CLKXOR2X1 3 24.9777
OR2X1 3 13.6242
AOI2BB1X1 1 6.0552
AND2X1 1 4.5414
SDFFQX1 23 470.0349
XNOR2X1 2 16.6518
OAI21X1 1 4.5414
OAI221X1 1 7.5690
OAI31X1 2 12.1104
CLKINVX1 2 4.5414
NAND2BX1 1 4.5414
SDFFHQX8 4 124.1316
NAND2XL 2 6.0552
ADDHX1 1 12.1104
NOR2BX1 1 4.5414
AOI21X1 3 13.6242
NOR3BX1 1 6.0552
AOI31X1 1 6.0552
A022X1 3 22.7070
NOR2XL 2 6.0552
NOR2BXL 4 18.1656
MXI4X1 1 18.1656

Break up of area report after CTS

- **Core Utilization of 0.8**

Hinst Name	Module Name	Inst Count	Total Area
Buffer	Inverter	Combinational	Flop
Latch	Clock Gate	Macro	Physical
-	-	65	817.452
group17			
0.000	4.541	218.744	594.167
0.000	0.000	0.000	0.000
cp_D1	DFF8	8	163.490
0.000	0.000	0.000	163.490
0.000	0.000	0.000	0.000
dp_D2	DFF4	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D3	DFF4_18	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D4	DFF4_17	4	124.132
0.000	0.000	0.000	124.132
0.000	0.000	0.000	0.000
dp_c1	Rcounter4	8	99.911
0.000	0.000	18.166	81.745
0.000	0.000	0.000	0.000
dp_f1	freq_div	8	92.342
0.000	0.000	31.033	61.309
0.000	0.000	0.000	0.000

Total Area Report

Design Status: In memory				
Design Name: group17				
# Instances: 65				
# Hard Macros: 0				
# Std Cells: 65				

Standard Cells in Netlist				

Cell Type	Instance Count	Area (μm^2)		
OAI2BB1X1	2	10.5966		
CLKXOR2X1	3	24.9777		
OR2X1	3	13.6242		
AOI2BB1X1	1	6.0552		
AND2X1	1	4.5414		
SDFFHQX1	23	470.0349		
XNOR2X1	2	16.6518		
OAI21X1	1	4.5414		
OA1221X1	1	7.5690		
OAI31X1	2	12.1104		
CLKINVX1	2	4.5414		
NAND2BX1	1	4.5414		
SDFFHQX8	4	124.1316		
NAND2XL	2	6.0552		
ADDHX1	1	12.1104		
NOR2BX1	1	4.5414		
AOI21X1	3	13.6242		
NOR3BX1	1	6.0552		
OAI31X1	1	6.0552		
AO22X1	3	22.7070		
NOR2XL	2	6.0552		
NOR2BXL	4	18.1656		
MXI4X1	1	18.1656		

Break up of area report after CTS

As we are taking the same netlist generated after the scan insertion in the logic synthesis part of the project, in the scan insertion, the DFFs were replaced by the Scan chains hence the area was increased drastically. We will be using the cadence innovus area report to generate the area after the various steps. Before the placement, our area is coming out to be 817.452 μm^2 .for both 0.5 and 0.8 values of the core utilization factor.

3. POWER ANALYSIS

- Core Utilization of 0.5

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
dp_D4/Q_reg[2]	0.007275	0.03514	0.04275	0.0003386	SDFFHQX8
dp_D4/Q_reg[3]	0.007223	0.03462	0.04218	0.0003386	SDFFHQX8
dp_D4/Q_reg[1]	0.007098	0.03426	0.04169	0.0003386	SDFFHQX8
dp_D4/Q_reg[0]	0.006337	0.03031	0.03699	0.0003386	SDFFHQX8
dp_c1/out1_reg[0]	0.002721	0.00015	0.003007	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.002497	0.0001377	0.002771	0.0001363	SDFFQX1
dp_c1/out1_reg[2]	0.002377	0.0001237	0.002637	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.002214	0.000163	0.002513	0.0001363	SDFFQX1

dp_c1/out1_reg[3]	0.002247	0.0001086	0.002492	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.002211	0.0001146	0.002462	0.0001363	SDFFQX1
dp_f1/temp_reg[2]	0.002127	8.364e-05	0.002347	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001874	0.0001837	0.002194	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001877	0.0001708	0.002184	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001879	0.0001516	0.002166	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001879	0.00011	0.002125	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001858	0.0001272	0.002122	0.0001363	SDFFQX1
dp_D2/Q_reg[2]	0.001878	0.0001037	0.002118	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001878	0.0001022	0.002117	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001868	0.0001068	0.002112	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.001838	0.0001228	0.002097	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001878	7.775e-05	0.002092	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001877	7.63e-05	0.00209	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.001798	8.043e-05	0.002014	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.00173	6.882e-05	0.001935	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.00173	5.256e-05	0.001919	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001656	4.045e-05	0.001832	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001656	3.269e-05	0.001825	0.0001363	SDFFQX1
g893	0.0004773	0.0001194	0.0006099	1.314e-05	OAI221X1
dp_f1/g114	0.0004352	7.867e-05	0.0006094	9.553e-05	ADDHX1
g901	0.0003218	0.0002425	0.0005824	1.815e-05	AOI21X1
g896	0.0003459	8.827e-05	0.0004773	4.309e-05	AO22X1
g900	0.0002932	0.0001406	0.000461	2.717e-05	AND2X1
g894	0.0003329	8.45e-05	0.0004605	4.309e-05	AO22X1
dp_f1/g112	0.0003429	3.939e-05	0.0004528	7.055e-05	XNOR2X1
g905	0.0003071	5.043e-05	0.0004526	9.511e-05	MXI4X1
g895	0.0003205	8.095e-05	0.0004445	4.309e-05	AO22X1
g899	0.0003396	8.039e-05	0.0004381	1.815e-05	AOI21X1
g908	0.0002282	0.0001775	0.0004239	1.815e-05	AOI21X1
g897	0.0002873	8.716e-05	0.0003957	2.127e-05	OAI2BB1X1
g906	0.0002892	7.88e-05	0.000388	2.004e-05	NOR2BX1
g914	0.0002749	3.188e-05	0.0003774	7.055e-05	XNOR2X1
g917	0.0002731	2.982e-05	0.0003754	7.254e-05	CLKXOR2X1
g915	0.0002717	2.982e-05	0.0003741	7.254e-05	CLKXOR2X1
g916	0.0002707	2.981e-05	0.000373	7.254e-05	CLKXOR2X1
g909	0.0002729	3.316e-05	0.0003279	2.186e-05	NOR3BX1
g913	0.0002639	3.143e-05	0.0003268	3.144e-05	AOI2BB1X1
g903	0.0002093	7.36e-05	0.0003255	4.256e-05	OR2X1
g904	0.000233	6.578e-05	0.0003128	1.402e-05	OAI31X1
g898	0.0001578	0.0001041	0.0002969	3.499e-05	NAND2BX1
g910	0.0001928	4.758e-05	0.0002582	1.789e-05	AOI31X1
dp_c1/g19	0.0001778	3.053e-05	0.0002509	4.256e-05	OR2X1
dp_c1/g42	0.0001961	3.265e-05	0.0002454	1.662e-05	NOR2BXL
g921	8.435e-05	0.0001429	0.0002403	1.301e-05	CLKINVX1
g911	0.0001457	7.531e-05	0.000235	1.402e-05	OAI31X1
g907	0.0001618	5.343e-05	0.0002282	1.299e-05	OAI21X1
g920	0.0001249	5.562e-05	0.0002231	4.256e-05	OR2X1
dp_c1/g40	0.0001756	2.905e-05	0.0002213	1.662e-05	NOR2BXL
dp_f1/g113	0.0001725	2.877e-05	0.0002179	1.662e-05	NOR2BXL
g912	0.0001347	5.046e-05	0.0002064	2.127e-05	OAI2BB1X1
dp_c1/g38	0.0001546	2.545e-05	0.0001967	1.662e-05	NOR2BXL
dp_f1/g116	0.0001313	2.846e-05	0.0001721	1.236e-05	NOR2XL
dp_f1/g110	0.0001083	2.423e-05	0.0001449	1.236e-05	NOR2XL
g902	7.199e-05	5.244e-05	0.0001337	9.289e-06	NAND2XL
g919	5.364e-05	6.244e-05	0.0001254	9.289e-06	NAND2XL
g918	8.416e-05	2.405e-05	0.0001212	1.301e-05	CLKINVX1

Total (65 of 65) 0.0822 0.1394 0.2273 0.005735

Total Capacitance 4.29e-12 F

Power Density *** No Die Area ***

• Core Utilization of 0.8

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
dp_D4/Q_reg[2]	0.007275	0.03514	0.04275	0.0003386	SDFFHQX8
dp_D4/Q_reg[3]	0.007223	0.03462	0.04218	0.0003386	SDFFHQX8
dp_D4/Q_reg[1]	0.007098	0.03426	0.04169	0.0003386	SDFFHQX8
dp_D4/Q_reg[0]	0.006337	0.03031	0.03699	0.0003386	SDFFHQX8
dp_c1/out1_reg[0]	0.002721	0.00015	0.003007	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.002497	0.0001377	0.002771	0.0001363	SDFFQX1
dp_c1/out1_reg[2]	0.002377	0.0001237	0.002637	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.002214	0.000163	0.002513	0.0001363	SDFFQX1
dp_c1/out1_reg[3]	0.002247	0.0001086	0.002492	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.002211	0.0001146	0.002462	0.0001363	SDFFQX1
dp_f1/temp_reg[2]	0.002127	8.364e-05	0.002347	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001874	0.0001837	0.002194	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001877	0.0001708	0.002184	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001879	0.0001516	0.002166	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001879	0.00011	0.002125	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001858	0.0001272	0.002122	0.0001363	SDFFQX1
dp_D2/Q_reg[2]	0.001878	0.0001037	0.002118	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001878	0.0001022	0.002117	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001868	0.0001068	0.002112	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.001838	0.0001228	0.002097	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001878	7.775e-05	0.002092	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001877	7.63e-05	0.00209	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.001798	8.043e-05	0.002014	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.00173	6.882e-05	0.001935	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.00173	5.256e-05	0.001919	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001656	4.045e-05	0.001832	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001656	3.269e-05	0.001825	0.0001363	SDFFQX1
g893	0.0004773	0.0001194	0.0006099	1.314e-05	OAI221X1
dp_f1/g114	0.0004352	7.867e-05	0.0006094	9.553e-05	ADDHX1
g901	0.0003218	0.0002425	0.0005824	1.815e-05	AOI21X1
g896	0.0003459	8.827e-05	0.0004773	4.309e-05	AO22X1
g900	0.0002932	0.0001406	0.000461	2.717e-05	AND2X1
g894	0.0003329	8.45e-05	0.0004605	4.309e-05	AO22X1
dp_f1/g112	0.0003429	3.939e-05	0.0004528	7.055e-05	XNOR2X1
g905	0.0003071	5.043e-05	0.0004526	9.511e-05	MXI4X1
g895	0.0003205	8.095e-05	0.0004445	4.309e-05	AO22X1
g899	0.0003396	8.039e-05	0.0004381	1.815e-05	AOI21X1
g908	0.0002282	0.0001775	0.0004239	1.815e-05	AOI21X1
g897	0.0002873	8.716e-05	0.0003957	2.127e-05	OAI2BB1X1
g906	0.0002892	7.88e-05	0.000388	2.004e-05	NOR2BX1
g914	0.0002749	3.188e-05	0.0003774	7.055e-05	XNOR2X1
g917	0.0002731	2.982e-05	0.0003754	7.254e-05	CLKXOR2X1
g915	0.0002717	2.982e-05	0.0003741	7.254e-05	CLKXOR2X1
g916	0.0002707	2.981e-05	0.000373	7.254e-05	CLKXOR2X1
g909	0.0002729	3.316e-05	0.0003279	2.186e-05	NOR3BX1
g913	0.0002639	3.143e-05	0.0003268	3.144e-05	AOI2BB1X1
g903	0.0002093	7.36e-05	0.0003255	4.256e-05	OR2X1
g904	0.000233	6.578e-05	0.0003128	1.402e-05	OAI31X1
g898	0.0001578	0.0001041	0.0002969	3.499e-05	NAND2BX1
g910	0.0001928	4.758e-05	0.0002582	1.789e-05	OAI31X1
dp_c1/g19	0.0001778	3.053e-05	0.0002509	4.256e-05	OR2X1
dp_c1/g42	0.0001961	3.265e-05	0.0002454	1.662e-05	NOR2BXL
g921	8.435e-05	0.0001429	0.0002403	1.301e-05	CLKINVX1
g911	0.0001457	7.531e-05	0.000235	1.402e-05	OAI31X1
g907	0.0001618	5.343e-05	0.0002282	1.299e-05	OAI21X1
g920	0.0001249	5.562e-05	0.0002231	4.256e-05	OR2X1
dp_c1/g40	0.0001756	2.905e-05	0.0002213	1.662e-05	NOR2BXL
dp_f1/g113	0.0001725	2.877e-05	0.0002179	1.662e-05	NOR2BXL
g912	0.0001347	5.046e-05	0.0002064	2.127e-05	OAI2BB1X1
dp_c1/g38	0.0001546	2.545e-05	0.0001967	1.662e-05	NOR2BXL
dp_f1/g116	0.0001313	2.846e-05	0.0001721	1.236e-05	NOR2XL
dp_f1/g110	0.0001083	2.423e-05	0.0001449	1.236e-05	NOR2XL

g902	7.199e-05	5.244e-05	0.0001337	9.289e-06	NAND2XL
g919	5.364e-05	6.244e-05	0.0001254	9.289e-06	NAND2XL
g918	8.416e-05	2.405e-05	0.0001212	1.301e-05	CLKINVX1
<hr/>					
Total (65 of 65)	0.0822	0.1394	0.2273	0.005735	
Total Capacitance	4.29e-12 F				
Power Density	*** No Die Area ***				

Initially, we are getting the following values for different types of powers

Switching power: 0.1394mW

Total power: 0.2273mW

Leakage Power: 0.005735mW

Total Capacitance: 4.29×10^{-12} F

we will be using the cade innovus power report for the further steps to measure all these powers and will analyze accordingly.

STEP 2

AFTER PLACEMENT

During the placement step, we decide where to place the standard cells in our design and optimize it for timing violations.

Comparison of after placement with core utilization of 0.5 and with 0.8 is done for all the timing, area and power is done.

1. TIMING ANALYSIS

A. Worst case hold slack

Core Utilization – 0.5	Core Utilization – 0.8
<pre> ##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 12:33:05 2022 # Design: group17 # Command: report_timing -early -view {view1} -max_paths 100 >/reports/final_report/large_die_area/timing/hold_after_placement.txt ##### Path 1: VIOLATED Hold Check with Pin dp_D4/Q_reg[1]/CK Endpoint: dp_D4/Q_reg[1]/SE (v) checked with leading edge of 'clk' Beginpoint: scan_en (v) triggered by leading edge of '@' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.000 + Hold 0.079 + Phase Shift 0.000 + Uncertainty 0.002 = Required Time 0.081 Arrival Time 0.000 Slack Time -0.081 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 +-----+ Instance Arc Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+ scan_en v SE v SDFFHQX8 0.000 0.000 0.081 dp_D4/Q_reg[1] SE v SDFFHQX8 0.000 0.000 0.081 +-----+ </pre> <p style="text-align: center;"><i>Slack = -0.081</i></p>	<pre> ##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 10:32:16 2022 # Design: group17 # Command: report_timing -early -view {view1} -max_paths 100 >/reports/final_report/small_die_area/timing/hold_after_placement.txt ##### Path 1: VIOLATED Hold Check with Pin dp_D4/Q_reg[1]/CK Endpoint: dp_D4/Q_reg[1]/SE (v) checked with leading edge of 'clk' Beginpoint: scan_en (v) triggered by leading edge of '@' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.000 + Hold 0.079 + Phase Shift 0.000 + Uncertainty 0.002 = Required Time 0.081 Arrival Time 0.000 Slack Time -0.081 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 +-----+ Instance Arc Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+ scan_en v SE v SDFFHQX8 0.000 0.000 0.081 dp_D4/Q_reg[1] SE v SDFFHQX8 0.000 0.000 0.081 +-----+ </pre> <p style="text-align: center;"><i>Slack = -0.081</i></p>

Hold Slack(for both UF=0.5 and UF=0.8) : The Hold slack is calculated as AT-RT. The GBA path is considered from (Scan_en to dp D4/Q_reg[1]/SE), and it considers the minimum value among the slews while traversing, whereas PBA only considers the specified path whatever slew it may have .

So, in GBA, the worst slew results in the worst computation delay and higher RT or shorter AT, so slack (AT-RT) is less in GBA than in PBA. As shown in the figure above, the Slack is calculated as AT-RT = 0.000-0.081 = -0.081.

B. Worst case setup slack

Core Utilization – 0.5	Core Utilization – 0.8
<pre> ##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 12:33:06 2022 # Design: group17 # Command: report_timing -late -max_paths 100 >/reports/final_report/large_die_area/timing/setup_after_placement.txt ##### Path 1: MET Late External Delay Assertion Endpoint: OUT[0] (^) checked with leading edge of 'clk' Beginpoint: dp_D4/Q_reg[0]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.000 - External Delay 3.000 + Phase Shift 11.000 Uncertainty 1.000 = Required Time 7.000 - Arrival Time 1.072 = Slack Time 5.928 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000 +-----+ Instance Arc Cell Delay Arrival Required Time Time +-----+ dp_D4/Q_reg[0] CK ^ 0.000 5.928 dp_D4/Q_reg[0] CK ^ -> Q ^ SDFFHQX8 1.072 7.000 OUT[0] ^ 0.000 1.072 7.000 +-----+ </pre> <p style="color: blue;"><i>Slack = 5.928</i></p>	<pre> ##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 10:32:16 2022 # Design: group17 # Command: report_timing -late -max_paths 100 >/reports/final_report/small_die_area/timing/setup_after_placement.txt ##### Path 1: MET Late External Delay Assertion Endpoint: OUT[1] (^) checked with leading edge of 'clk' Beginpoint: dp_D4/Q_reg[1]/Q (^) triggered by leading edge of 'clk' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.000 - External Delay 3.000 + Phase Shift 11.000 Uncertainty 1.000 = Required Time 7.000 - Arrival Time 1.072 = Slack Time 5.928 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.000 = Beginpoint Arrival Time 0.000 +-----+ Instance Arc Cell Delay Arrival Required Time Time +-----+ dp_D4/Q_reg[1] CK ^ 0.000 5.928 dp_D4/Q_reg[1] CK ^ -> Q ^ SDFFHQX8 1.072 7.000 OUT[1] ^ 0.000 1.072 7.000 +-----+ </pre> <p style="color: blue;"><i>Slack = 5.928</i></p>

Setup slack(for both UF=0.5 and UF=0.8) : The setup slack is calculated as RT - AT. The GBA path is considered from (dp D4/Q_reg[0]/Q to OUT[0]), and it considers the maximum value among the slews while traversing, whereas PBA only considers the specified path whatever slew it may have . So, in GBA, the worst slew results in the worst computation delay and higher AT or shorter RT, so slack (RT-AT) is less in GBA than in PBA. As shown in the figure above, the cell-arc delay (which is a function of input slew and output load) is calculated, and AT is calculated at each arc. AT at an output pin equals cell-arc delay added to AT at an input pin.The slack is calculated as RT-AT=7.000-1.072=5.928.

Reason why Setup and Hold slacks are same:

The timing report for the worst path is shown in the screenshot above . Wire lengths are estimated in the same way that placement is, and appropriate wire loads are taken into account. Because RC delays of wires are computed between pins of two instances, but as we were considering the wireload model previously also hence the hold slacks and setup slacks are seems to be same in case of UF=0.5 and UF=0.8, because actual routing is still not done only estimation is done.

2. AREA ANALYSIS

- Core Utilization of 0.5

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational
Flop	Latch	Clock Gate	Macro	Physical		
group17		65	817.452	0.000	4.541	218.744
594.167	0.000	0.000	0.000	0.000	0.000	0.000
cp_D1	DFF8	8	163.490	0.000	0.000	0.000
163.490	0.000	0.000	0.000	0.000	0.000	0.000
dp_D2	DFF4	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000	0.000	0.000
dp_D3	DFF4_18	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000	0.000	0.000
dp_D4	DFF4_17	4	124.132	0.000	0.000	0.000
124.132	0.000	0.000	0.000	0.000	0.000	0.000
dp_c1	Rcounter4	8	99.911	0.000	0.000	18.166
81.745	0.000	0.000	0.000	0.000	0.000	0.000
dp_f1	freq_div	8	92.342	0.000	0.000	31.033
61.309	0.000	0.000	0.000	0.000	0.000	0.000

Design Status: Routed

Design Name: group17

Instances: 65

Hard Macros: 0

Std Cells: 65

Standard Cells in Netlist

Cell Type	Instance Count	Area (um^2)
OAI2BB1X1	2	10.5966
CLKXOR2X1	3	24.9777
OR2X1	3	13.6242
AOI2BB1X1	1	6.0552
AND2X1	1	4.5414
SDFFQX1	23	470.0349
XNOR2X1	2	16.6518
OAI21X1	1	4.5414
OAI221X1	1	7.5690
OAI31X1	2	12.1104
CLKINVX1	2	4.5414
NAND2BX1	1	4.5414
SDFFHQX8	4	124.1316
NAND2XL	2	6.0552
ADDHX1	1	12.1104
NOR2BX1	1	4.5414
AOI21X1	3	13.6242
NOR3BX1	1	6.0552
AOI31X1	1	6.0552
A022X1	3	22.7070
NOR2XL	2	6.0552
NOR2BXL	4	18.1656
MXI4X1	1	18.1656

• Core Utilization of 0.8

Hinst Name	Module Name	Inst Count	Total Area
Buffer	Inverter	Combinational	Flop
Latch	Clock Gate	Macro	Physical
-	-	-	-
group17		65	817.452
0.000	4.541	218.744	594.167
0.000	0.000	0.000	0.000
cp_D1	DFF8	8	163.490
0.000	0.000	0.000	163.490
0.000	0.000	0.000	0.000
dp_D2	DFF4	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D3	DFF4_18	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D4	DFF4_17	4	124.132
0.000	0.000	0.000	124.132
0.000	0.000	0.000	0.000
dp_c1	Rcounter4	8	99.911
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_f1	freq_div	8	92.342
0.000	0.000	31.033	61.309
0.000	0.000	0.000	0.000

Total Area Report

Design Status: Routed		
Design Name: group17		
# Instances: 65		
# Hard Macros: 0		
# Std Cells: 65		

Standard Cells in Netlist		

Cell Type	Instance Count	Area (um^2)
OAI2BB1X1	2	10.5966
CLKXOR2X1	3	24.9777
OR2X1	3	13.6242
AOI2BB1X1	1	6.0552
AND2X1	1	4.5414
SDFFQX1	23	470.0349
XNOR2X1	2	16.6518
OAI21X1	1	4.5414
OAI221X1	1	7.5690
OAI31X1	2	12.1104
CLKINVX1	2	4.5414
NAND2BX1	1	4.5414
SDFFHQX8	4	124.1316
NAND2XL	2	6.0552
ADDHX1	1	12.1104
NOR2BX1	1	4.5414
AOI21X1	3	13.6242
NOR3BX1	1	6.0552
AOI31X1	1	6.0552
A022X1	3	22.7070
NOR2XL	2	6.0552
NOR2BXL	4	18.1656
MXI4X1	1	18.1656

Break up of area report after CTS

The obtained area is the same before and after the placements.

As an example, consider the following:

1. **Global placement:** The circuit is simply divided into subcircuits repeatedly using algorithmic and mathematical methods. As a result, the number of cells/instances in the design remains constant which can be seen from the attached cell and the area report also, implying that the area of the design should also remain constant.

2. **Detailed placement** entails redistributing the cells so that the design's illegalities (overlap and occupancy of illegal sites in the core) can be removed. As a result, it is obvious that the area consumption will remain constant.

Total Area=817.452

As a result, the area should remain the same after the placement step.

And also the area is same in case of the UF=0.5 and UF=0.8.

3. POWER ANALYSIS

- **Core Utilization of 0.5**

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
dp_D4/Q_reg[2]	0.007323	0.03538	0.04305	0.0003386	SDFFHQX8
dp_D4/Q_reg[1]	0.007177	0.03457	0.04209	0.0003386	SDFFHQX8
dp_D4/Q_reg[0]	0.006891	0.03396	0.04119	0.0003386	SDFFHQX8
dp_D4/Q_reg[3]	0.00529	0.02339	0.02902	0.0003386	SDFFHQX8
dp_c1/out1_reg[2]	0.002586	0.0001317	0.002854	0.0001363	SDFFQX1
dp_c1/out1_reg[3]	0.002298	0.0001134	0.002548	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.002274	0.0001187	0.002529	0.0001363	SDFFQX1
dp_c1/out1_reg[0]	0.002271	0.000117	0.002524	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.002206	0.0001609	0.002503	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.002203	0.0001037	0.002443	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.002172	8.698e-05	0.002395	0.0001363	SDFFQX1
dp_f1/temp_reg[2]	0.002125	8.351e-05	0.002344	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001869	0.0001824	0.002187	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001876	0.0001708	0.002183	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001878	0.0001515	0.002166	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001878	0.00011	0.002125	0.0001363	SDFFQX1
dp_D2/Q_reg[2]	0.001878	0.0001037	0.002118	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001874	0.0001076	0.002118	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001878	0.0001022	0.002117	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001878	7.781e-05	0.002092	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001877	7.63e-05	0.00209	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.001858	8.784e-05	0.002082	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.001838	8.327e-05	0.002058	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001798	0.0001164	0.002051	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.00173	0.0001015	0.001968	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001656	4.204e-05	0.001834	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001656	4.045e-05	0.001832	0.0001363	SDFFQX1
dp_f1/g114	0.0004943	9.321e-05	0.0006831	9.553e-05	ADDHX1
g893	0.0004814	0.0001188	0.0006133	1.314e-05	OAI221X1
g901	0.0003202	0.0002414	0.0005797	1.815e-05	AOI21X1
g895	0.0003437	8.654e-05	0.0004733	4.309e-05	AO22X1
g894	0.000337	8.553e-05	0.0004656	4.309e-05	AO22X1
g915	0.0003543	3.856e-05	0.0004654	7.254e-05	CLKXOR2X1
g900	0.0002911	0.0001396	0.0004579	2.717e-05	AND2X1
g905	0.0003071	5.043e-05	0.0004526	9.511e-05	MXI4X1
dp_f1/g112	0.0003417	3.933e-05	0.0004515	7.055e-05	XNOR2X1
g896	0.0003199	8.08e-05	0.0004438	4.309e-05	AO22X1
g899	0.0003382	7.975e-05	0.0004361	1.815e-05	AOI21X1
g908	0.0002282	0.0001775	0.0004239	1.815e-05	AOI21X1
g897	0.000286	8.67e-05	0.000394	2.127e-05	OAI2BB1X1
g906	0.0002896	7.88e-05	0.0003884	2.004e-05	NOR2BX1
g914	0.0002747	3.186e-05	0.0003771	7.055e-05	XNOR2X1
g917	0.0002731	2.982e-05	0.0003754	7.254e-05	CLKXOR2X1
g916	0.0002707	2.981e-05	0.0003731	7.254e-05	CLKXOR2X1
g903	0.0002067	7.271e-05	0.000322	4.256e-05	OR2X1
g909	0.0002658	3.242e-05	0.0003201	2.186e-05	NOR3BX1
g913	0.0002566	3.067e-05	0.0003187	3.144e-05	AOI2BB1X1
g904	0.0002293	6.479e-05	0.0003081	1.402e-05	OAI31X1
g898	0.0001563	0.0001032	0.0002945	3.499e-05	NAND2BX1
dp_c1/g19	0.000184	3.16e-05	0.0002581	4.256e-05	OR2X1
g920	0.0001431	6.381e-05	0.0002495	4.256e-05	OR2X1
g910	0.0001842	4.509e-05	0.0002472	1.789e-05	AOI31X1
g921	8.494e-05	0.0001439	0.0002419	1.301e-05	CLKINVX1
dp_f1/g113	0.0001829	3.057e-05	0.0002301	1.662e-05	NOR2BX1
g907	0.0001593	5.267e-05	0.000225	1.299e-05	OAI21X1
g911	0.0001382	7.046e-05	0.0002227	1.402e-05	OAI31X1
g912	0.000134	5.076e-05	0.000206	2.127e-05	OAI2BB1X1

dp_c1/g38	0.0001621	2.659e-05	0.0002053	1.662e-05	NOR2BXL
dp_c1/g42	0.0001563	2.614e-05	0.0001991	1.662e-05	NOR2BXL
dp_f1/g116	0.0001274	2.767e-05	0.0001675	1.236e-05	NOR2XL
dp_c1/g40	0.0001289	2.119e-05	0.0001667	1.662e-05	NOR2BXL
dp_f1/g110	0.0001122	2.499e-05	0.0001495	1.236e-05	NOR2XL
g902	5.974e-05	4.365e-05	0.0001127	9.289e-06	NAND2XL
g919	4.659e-05	5.443e-05	0.0001103	9.289e-06	NAND2XL
g918	7.337e-05	2.097e-05	0.0001073	1.301e-05	CLKINVX1

Total (65 of 65) 0.08098 0.1323 0.219 0.005735

Total Capacitance 4.29e-12 F

Power Density *** No Die Area ***

- **Core Utilization of 0.8**

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
dp_D4/Q_reg[0]	0.00682	0.03347	0.04063	0.0003386	SDFFHQX8
dp_D4/Q_reg[3]	0.006708	0.03148	0.03853	0.0003386	SDFFHQX8
dp_D4/Q_reg[1]	0.006262	0.02885	0.03545	0.0003386	SDFFHQX8
dp_D4/Q_reg[2]	0.005286	0.02339	0.02901	0.0003386	SDFFHQX8
dp_f1/temp_reg[2]	0.002724	0.0001281	0.002988	0.0001363	SDFFQX1
dp_c1/out1_reg[3]	0.002506	0.0001239	0.002766	0.0001363	SDFFQX1
dp_c1/out1_reg[0]	0.002387	0.0001291	0.002652	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.002214	0.0001629	0.002514	0.0001363	SDFFQX1
dp_c1/out1_reg[2]	0.002254	0.0001116	0.002501	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.002217	0.0001369	0.00249	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.002244	0.00011	0.00249	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001878	0.0001515	0.002166	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001876	0.0001303	0.002143	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.001874	0.000129	0.002139	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001838	0.000162	0.002137	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001878	0.00011	0.002125	0.0001363	SDFFQX1
dp_D2/Q_reg[2]	0.001878	0.0001037	0.002118	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001878	0.0001022	0.002117	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.001868	8.907e-05	0.002094	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001878	7.781e-05	0.002092	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001877	7.63e-05	0.00209	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.001859	8.568e-05	0.00208	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001798	9.646e-05	0.002031	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001731	0.0001445	0.002011	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.00173	5.256e-05	0.001919	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001656	4.045e-05	0.001832	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001656	3.269e-05	0.001825	0.0001363	SDFFQX1
dp_f1/g112	0.0005262	6.03e-05	0.000657	7.055e-05	XNOR2X1
dp_f1/g114	0.0004465	8.191e-05	0.0006239	9.553e-05	ADDHX1
g893	0.0004445	0.0001103	0.0005679	1.314e-05	OAI221X1
g901	0.0002944	0.0002221	0.0005346	1.815e-05	AOI21X1
g905	0.0003071	5.043e-05	0.0004526	9.511e-05	MXI4X1
g895	0.0003169	8.04e-05	0.0004404	4.309e-05	AO22X1
g894	0.0003141	7.976e-05	0.000437	4.309e-05	AO22X1
g896	0.0003134	7.944e-05	0.0004359	4.309e-05	AO22X1
g900	0.0002727	0.0001308	0.0004307	2.717e-05	AND2X1
g899	0.000331	7.621e-05	0.0004254	1.815e-05	AOI21X1
g908	0.0002097	0.0001636	0.0003915	1.815e-05	AOI21X1
g914	0.0002747	3.186e-05	0.0003771	7.055e-05	XNOR2X1
g917	0.0002731	2.982e-05	0.0003754	7.254e-05	CLKXOR2X1
g915	0.0002717	2.982e-05	0.0003741	7.254e-05	CLKXOR2X1
g916	0.0002707	2.981e-05	0.000373	7.254e-05	CLKXOR2X1
g906	0.000275	7.474e-05	0.0003698	2.004e-05	NOR2BX1
g897	0.0002659	8.051e-05	0.0003677	2.127e-05	OAI2BB1X1
g913	0.0002541	3.021e-05	0.0003158	3.144e-05	AOI2BB1X1
g903	0.0001999	7.028e-05	0.0003127	4.256e-05	OR2X1
g909	0.0002515	3.024e-05	0.0003036	2.186e-05	NOR3BX1

g898	0.0001485	9.757e-05	0.000281	3.499e-05	NAND2BX1
g904	0.0002081	5.841e-05	0.0002806	1.402e-05	OAI31X1
g910	0.0002045	5.012e-05	0.0002725	1.789e-05	OAI31X1
dp_c1/g19	0.0001896	3.264e-05	0.0002648	4.256e-05	OR2X1
g920	0.0001462	6.517e-05	0.0002539	4.256e-05	OR2X1
g911	0.0001527	7.824e-05	0.000245	1.402e-05	OAI31X1
dp_f1/g113	0.0001737	2.902e-05	0.0002193	1.662e-05	NOR2BXL
g921	7.617e-05	0.0001291	0.0002182	1.301e-05	CLKINVX1
dp_c1/g42	0.000172	2.876e-05	0.0002174	1.662e-05	NOR2BXL
dp_f1/g110	0.0001628	3.648e-05	0.0002116	1.236e-05	NOR2XL
g912	0.0001368	4.99e-05	0.000208	2.127e-05	OAI2BB1X1
g907	0.0001443	4.664e-05	0.0002039	1.299e-05	OAI21X1
dp_c1/g38	0.0001436	2.381e-05	0.0001841	1.662e-05	NOR2BXL
dp_c1/g40	0.0001394	2.303e-05	0.0001791	1.662e-05	NOR2BXL
dp_f1/g116	0.0001299	2.818e-05	0.0001704	1.236e-05	NOR2XL
g919	5.569e-05	6.478e-05	0.0001298	9.289e-06	NAND2XL
g918	8.731e-05	2.495e-05	0.0001253	1.301e-05	CLKINVX1
g902	6.311e-05	4.602e-05	0.0001184	9.289e-06	NAND2XL

Total (65 of 65) 0.07942 0.1221 0.2073 0.005735

Total Capacitance 4.29e-12 F

Power Density *** No Die Area ***

Power is primarily decreased as the switching power of the instances increases. This is because the resistance and capacitances of the wire are taken into account during placement differs slightly from the assumed wired load model, implying that more power is consumed.

In **both of the UF cases**, power has been decreased. However, we can see that the decrease in power consumption is greater when UF is 0.5. This can be explained as follows: when the core UF is higher, wirelength should decrease (because less area is available for wires/path placement), and thus RC delays should decrease (because R and C are directly proportional to wire length) in comparison to the UF 0.5 case.

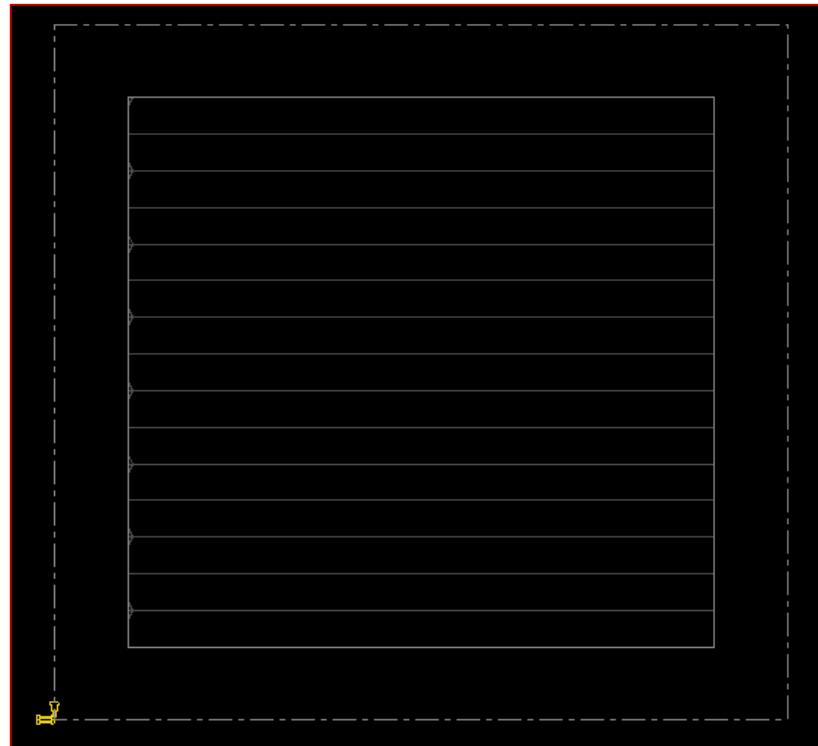
Total power=0.2273um².

4. SNAPSHOTS OF LAYOUT

- **Core Utilization of 0.5**
 - **After Floorplanning**

This stage specifies the die size and aspect ratio, as well as the area for the die to be assigned in the layout for physical design. A squarish chip is produced by keeping the aspect ratio close to one. In addition, the usage factors of 0.5 and 0.8 are indicated.

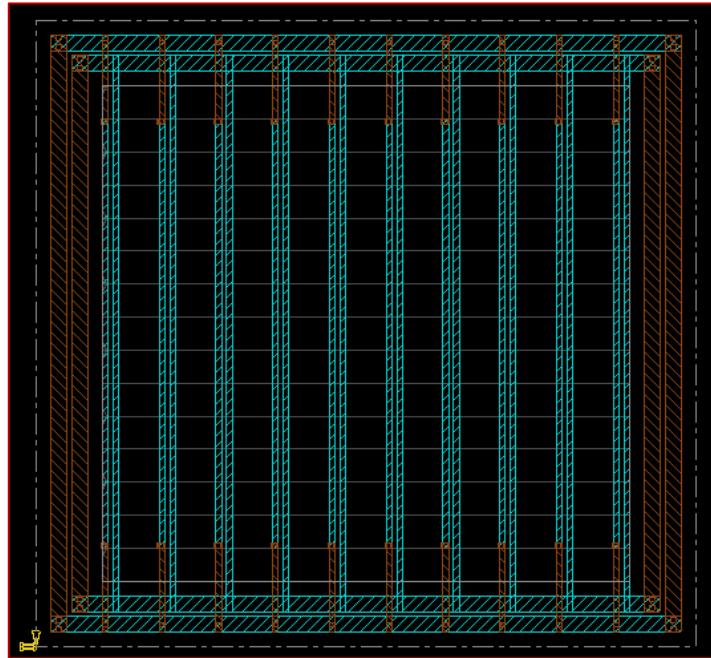
The conventional cell rows may be seen in the core area (hard line) below, while the dotted line accompanying accounts for the power rail margins and represents the entire chip area.



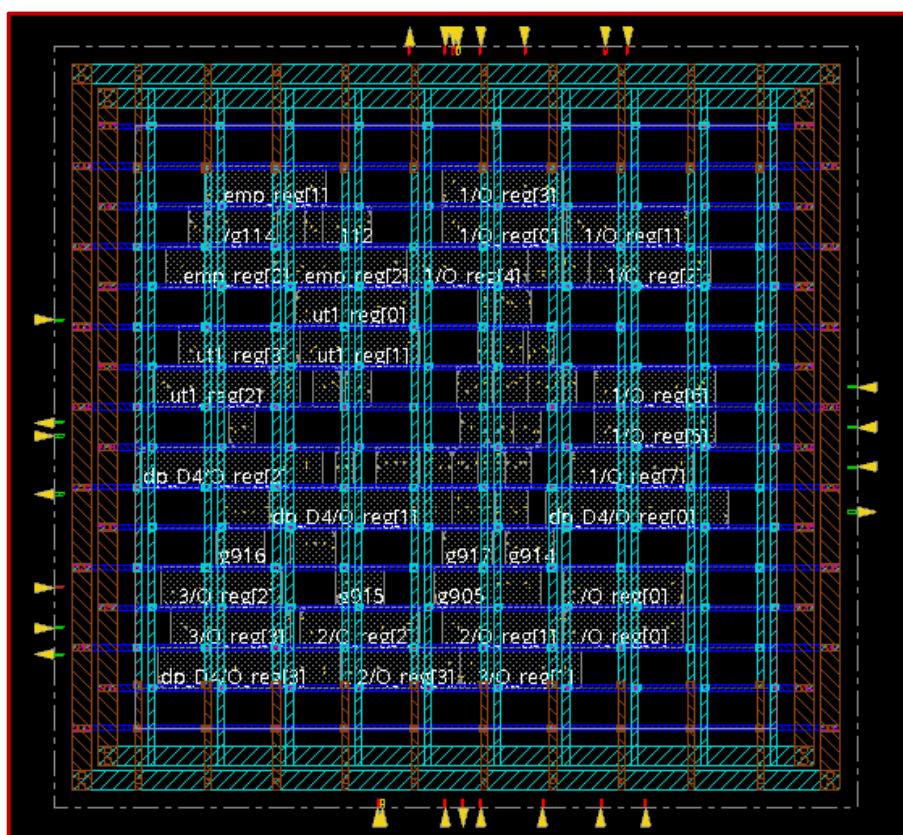
○ After Power Planning

The power distribution network has been built in this phase, which includes VDD and GND rails strapped in a mesh topology with a regularly spaced array. With vias at intersections, the power lines run horizontally and vertically in alternate levels.

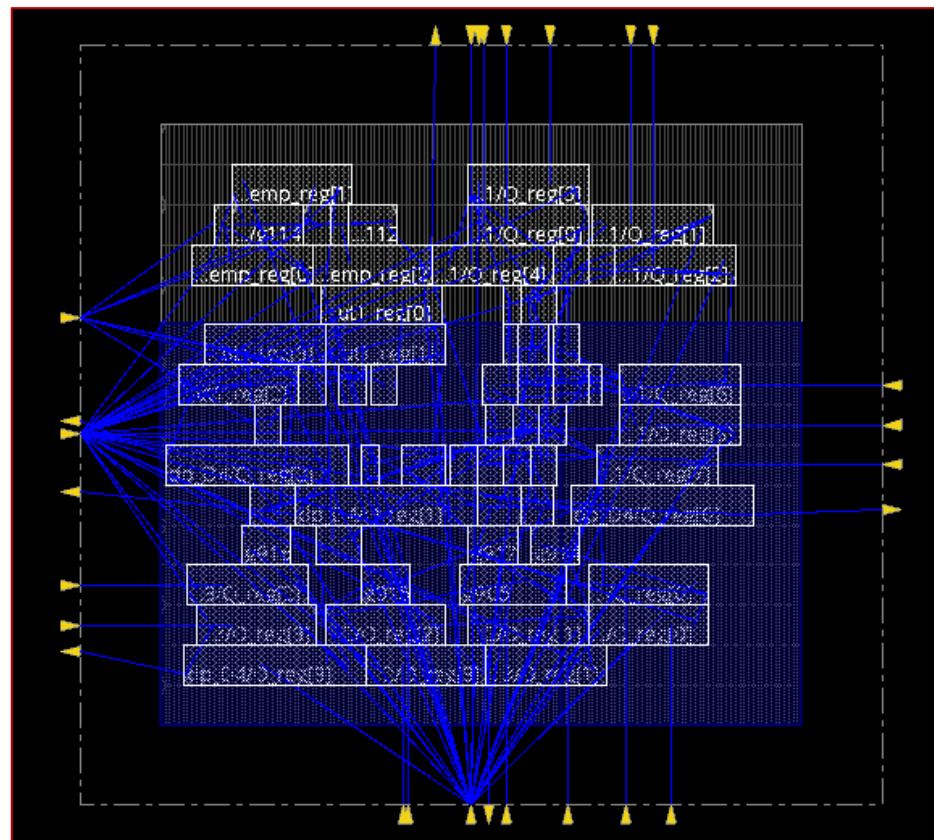
Metal 8 and Metal 9 layers were used to create the power rings that surround the core region. The M1 layer is used at the bottom of the horizontal straps to provide VDD and GND connections to standard cells. An M8 layer is used to create the vertical straps.



○ After Placement

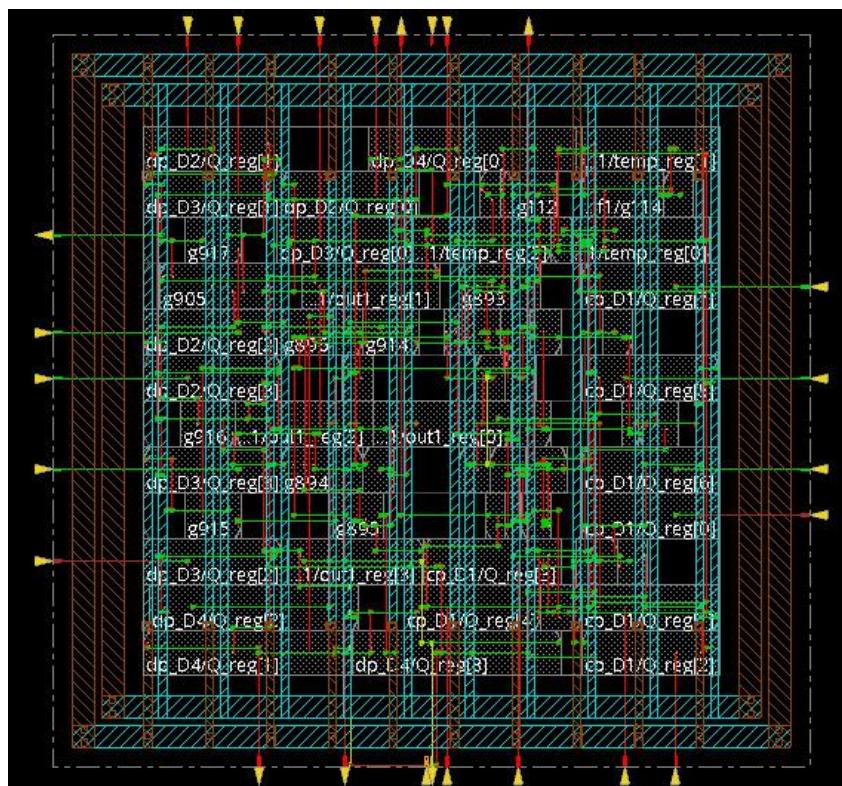


- After placement snapshot showing Fly Lines

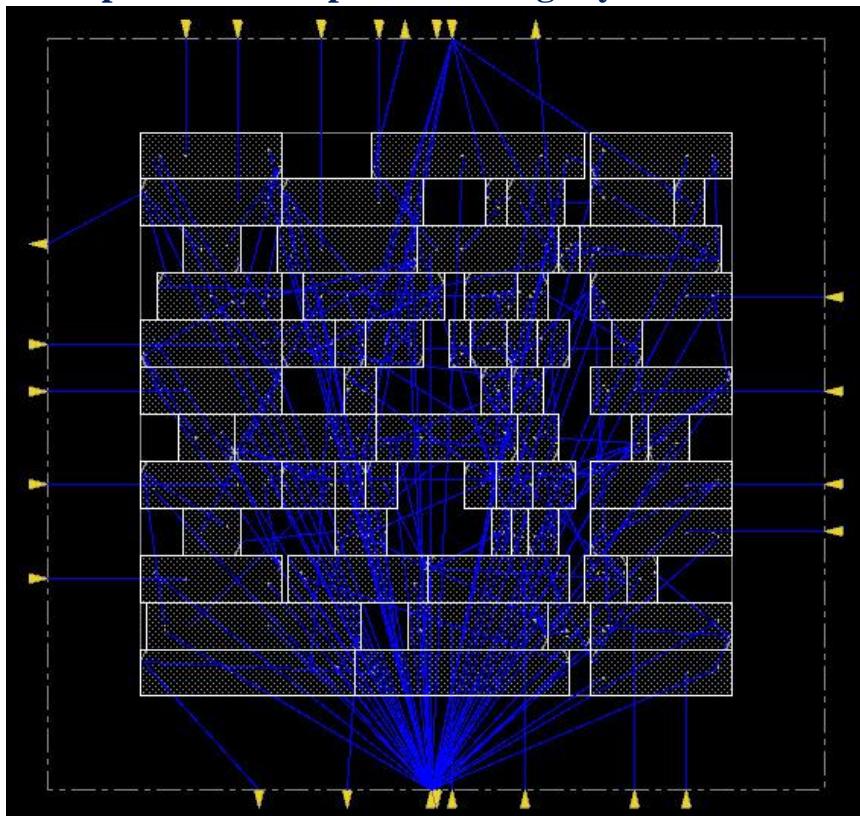


- Core Utilization of 0.8

- ### ○ After Placement



- After placement snapshot showing Fly Lines



STEP 3

AFTER CLOCK TREE SYNTHESIS

Clock Tree Synthesis is done to provide real clock in the layout from the source clock to other multiple registers by inserting interconnects and buffers. To drive the clock, a tree of clock buffers is constructed. The main goal is to set up a balanced clock network in order to reduce global clock skew.

Comparison of post CTS with core utilization of 0.5 and with 0.8 is done for all the timing, area and power is done.

1. TIMING ANALYSIS

A. Worst case hold slack

Core Utilization – 0.5	Core Utilization – 0.8
<pre>##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 12:34:17 2022 # Design: group17 # Command: report_timing -early -view {view1} -max_paths 100 >/reports/final_report/large_die_area/timing/hold_after_CTS.txt ##### Path 1: MET Hold Check with Pin cp_D1/Q_reg[0]/CK Endpoint: cp_D1/Q_reg[0]/SI (v) checked with leading edge of 'clk' Beginpoint: DFT_sdi_1 (v) triggered by leading edge of '@' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.001 + Hold -0.015 + Phase Shift 0.000 + Uncertainty 0.002 = Required Time -0.012 Arrival Time 0.000 Slack Time 0.012 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 + Instance Arc Cell Delay Arrival Required DFT_sdi_1 v SI v 0.000 0.000 -0.012 cp_D1/Q_reg[0] +-----+-----+-----+-----+-----+-----+</pre> <p style="text-align: center;">Slack = 0.012</p>	<pre>##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 10:33:18 2022 # Design: group17 # Command: report_timing -early -view {view1} -max_paths 100 >/reports/final_report/small_die_area/timing/hold_after_CTS.txt ##### Path 1: MET Hold Check with Pin dp_D3/Q_reg[2]/CK Endpoint: dp_D3/Q_reg[2]/SI (v) checked with leading edge of 'clk' Beginpoint: DFT_sdi_2 (v) triggered by leading edge of '@' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.001 + Hold -0.015 + Phase Shift 0.000 + Uncertainty 0.002 = Required Time -0.012 Arrival Time 0.000 Slack Time 0.012 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 + Instance Arc Cell Delay Arrival Required DFT_sdi_2 v SI v 0.000 0.000 -0.012 dp_D3/Q_reg[2] +-----+-----+-----+-----+-----+-----+</pre> <p style="text-align: center;">Slack = 0.012</p>

For core utilization of 0.5,

The worst path for hold slack is shown above. The beginning point is DFT_sdi_1 and the ending point is cp_D1/Q_reg[0]/SI which is a scan cell.

As compared to the post placement slacks, the worst slack for hold has been improved and violation has been removed after optimization by adding buffers in the path. After clock tree synthesis, slack can be degraded or some timing violations can occur due to actual routing of the clock. The worst case hold slack is coming out

to be 0.012 since, the required time is $RT = -0.012$ and the arrival time is 0 (there are no combinational elements in between this path). So, overall slack coming out to be is 0.012.

For core utilization of 0.8 and comparison with UF 0.5,

The slack is same as 0.012 of UF 0.5. Probably the reason is that the wirelength or buffers taken in such a way that slack is coming same. Since, our circuit is not that big, so there are very less changes in the slack by changing the value of UF.

B. Worst case setup slack

Core Utilization – 0.5	Core Utilization – 0.8
<pre>##### # Generated by: Cadence Innovus 20.10-p004.1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 12:34:18 2022 # Design: group17 # Command: report_timing -late -max_paths 100 > ./reports/final_report/large_die_area/timing/setup_after_CTS.txt ##### Path 1: MET Late External Delay Assertion Endpoint: OUT[0] (^.^) checked with leading edge of 'clk' Beginpoint: dp_D4/Q_reg[0]/Q (^.^) triggered by leading edge of 'clk' Path Groups: (1) Analysis View: view1 Other End Arrival Time 0.000 - External Delay 3.000 + Phase Shift 11.000 - Uncertainty 1.000 = Required Time 7.000 - Arrival Time 0.903 = Slack Time 6.097 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.001 = Beginpoint Arrival Time 0.001 +-----+ Instance Arc Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+ dp_D4/Q_reg[0] CK ^ SDFFFQX1 0.302 0.303 6.400 dp_D4/Q_reg[0] CK ^ -> Q ^ CLKBUFX12 0.599 0.892 6.990 dp_D4/FE_OFCC_OUT_0 A ^ -> Y ^ OUT[0] ^ 0.011 0.903 7.000 +-----+</pre> <p style="text-align: center;">Slack = 6.097</p>	<pre>##### # Generated by: Cadence Innovus 20.10-p004.1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 10:33:18 2022 # Design: group17 # Command: report_timing -late -max_paths 100 > ./reports/final_report/small_die_area/timing/setup_after_CTS.txt ##### Path 1: MET Late External Delay Assertion Endpoint: OUT[2] (^.^) checked with leading edge of 'clk' Beginpoint: dp_D4/Q_reg[2]/Q (^.^) triggered by leading edge of 'clk' Path Groups: (1) Analysis View: view1 Other End Arrival Time 0.000 - External Delay 3.000 + Phase Shift 11.000 - Uncertainty 1.000 = Required Time 7.000 - Arrival Time 0.914 = Slack Time 6.086 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.001 = Beginpoint Arrival Time 0.001 +-----+ Instance Arc Cell Delay Arrival Required -----+-----+-----+-----+-----+-----+ dp_D4/Q_reg[2] CK ^ SDFFFQX1 0.310 0.311 6.396 dp_D4/Q_reg[2] CK ^ -> Q ^ CLKBUFX12 0.599 0.901 6.987 dp_D4/FE_OFCC_OUT_2 A ^ -> Y ^ OUT[2] ^ 0.013 0.914 7.000 +-----+</pre> <p style="text-align: center;">Slack = 6.086</p>

For core utilization of 0.5,

The worst path for setup slack is shown above. The beginning point is $dp_D4/Q_reg[0]/Q$ (leading edge) and the ending point is $OUT[0]$ (leading edge).

As shown in the timing report, a clock buffer is added in the path after CTS which was not present before. Its delay also gets added to the path which increases the RT (Required Time) of the path. After addition of CLKBUFX12, the RT has increased from 6.400 to 6.990 and the AT has also increased significantly thus obtaining the slack ($RT - AT = 7 - 0.903 \Rightarrow 6.097$). Hence, the setup slack (slack = 6.097) has been increased from the post placement step (slack was 5.928). The GBA slack computes arrival time at the output, which is arrival time at the input pin added with cell arc delay, using the worst of all the slews present at input.

For core utilization of 0.8 and comparison with UF 0.5,

The slack is 6.086 as which is slightly less than as of UF 0.5. Probably the reason is that the wirelength is changed in case of UF 0.8 because the area for routing is limited hence, limiting the buffer size and wirelength causing increase in slack from the ‘post placement’ step. But a slight decrease from UF 0.5. Here, the beginning point is a flipflop dp_D4/Q_reg[2] (a scan cell) and the ending point is dp_D4/FE_OFC2_OUT2. A CLKBUFX12 is added in the clock CK to Q path which changes the AT and the RT. Thus, obtaining an increased slack ($7 - 0.914 = 6.086$) here. Since, our circuit is not that big, so there are very less changes in the slack by changing the value of UF.

2. AREA ANALYSIS

- Core Utilization of 0.5**

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational
Flop	Latch	Clock Gate	Macro	Physical		
group17		70	843.187	68.121	4.541	218.744
551.780	0.000	0.000	0.000	0.000		
cp_D1	DFF8	8	163.490	0.000	0.000	0.000
163.490	0.000	0.000	0.000	0.000		
dp_D2	DFF4	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000		
dp_D3	DFF4_18	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000		
dp_D4	DFF4_17	6	113.535	31.790	0.000	0.000
81.745	0.000	0.000	0.000	0.000		
dp_c1	Rcounter4	8	99.911	0.000	0.000	18.166
81.745	0.000	0.000	0.000	0.000		
dp_f1	freq_div	8	92.342	0.000	0.000	31.033
61.309	0.000	0.000	0.000	0.000		

# Instances: 70		
# Hard Macros: 0		
# Std Cells: 70		

Standard Cells in Netlist		

Cell Type	Instance Count	Area (um^2)
0AI2BB1X1	2	10.5966
CLKBUFX2	1	4.5414
CLKBUFX12	4	63.5796
CLKXOR2X1	3	24.9777
OR2X1	3	13.6242
AOI2BB1X1	1	6.0552
AND2X1	1	4.5414
SDFFQX1	27	551.7801
XNOR2X1	2	16.6518
OAI21X1	1	4.5414
OAI221X1	1	7.5690
OAI31X1	2	12.1104
CLKINVX1	2	4.5414
NAND2BX1	1	4.5414
NAND2XL	2	6.0552
ADDHX1	1	12.1104
NOR2BX1	1	4.5414
AOI21X1	3	13.6242
NOR3BX1	1	6.0552
AOI31X1	1	6.0552
A022X1	3	22.7070
NOR2XL	2	6.0552
NOR2BXL	4	18.1656
MXI4X1	1	18.1656

Breakup of area after CTS

```

Total area of Standard cells: 843.187 um^2
Total area of Standard cells(Subtracting Physical Cells): 843.187 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 1634.904 um^2
Total area of Chip: 2588.598 um^2
Effective Utilization: 5.1574e-01
Number of Cell Rows: 15

```

Total Area Report

After clock tree synthesis, the total area has been increased from 817.452 um² to 843.187 um². The reason behind that is, CTS introduces some buffers and delay instances in the design while routing the clock in order to reduce the overall clock skew (skew minimization). Because of the extra instances added in the design, the overall area has been increased.

The total area reported is 843.187 um² and total instances used are 70. Some of the instances that are added are DLY3X1, CLKBUFX12, etc.

- **Core Utilization of 0.8**

Hinst Name	Module Name	Inst Count	Total Area
Buffer	Inverter	Combinational	Flop
Latch	Clock Gate	Macro	Physical
-	-	-	-
group17		72	852.269
77.204	4.541	218.744	551.780
0.000	0.000	0.000	0.000
cp_D1	DFF8	8	163.490
0.000	0.000	0.000	163.490
0.000	0.000	0.000	0.000
dp_D2	DFF4	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D3	DFF4_18	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D4	DFF4_17	9	127.159
45.414	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_c1	Rcounter4	8	99.911
0.000	0.000	18.166	81.745
0.000	0.000	0.000	0.000
dp_f1	freq_div	8	92.342
0.000	0.000	31.033	61.309
0.000	0.000	0.000	0.000

Design Status: Routed
Design Name: group17
Instances: 72
Hard Macros: 0
Std Cells: 72

Standard Cells in Netlist

Cell Type Instance Count Area (um^2)
OAI2BB1X1 2 10.5966
CLKBUFX2 3 13.6242
CLKBUFX12 4 63.5796
CLKXOR2X1 3 24.9777
OR2X1 3 13.6242
AOI2BB1X1 1 6.0552
AND2X1 1 4.5414
SDFFQX1 27 551.7801
XNOR2X1 2 16.6518
OAI21X1 1 4.5414
OAI221X1 1 7.5690
OAI31X1 2 12.1104
CLKINVX1 2 4.5414
NAND2BX1 1 4.5414
NAND2XL 2 6.0552
ADDHX1 1 12.1104
NOR2BX1 1 4.5414
AOI21X1 3 13.6242
NOR3BX1 1 6.0552
AOI31X1 1 6.0552
A022X1 3 22.7070
NOR2XL 2 6.0552
NOR2BXL 4 18.1656
MXI4X1 1 18.1656

Break up of area report after CTS

```
Total area of Standard cells: 852.269 um^2
Total area of Standard cells(Subtracting Physical Cells): 852.269 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 1026.356 um^2
Total area of Chip: 1804.450 um^2
Effective Utilization: 8.3038e-01
Number of Cell Rows: 12
```

Total area report after CTS

After clock tree synthesis, the total area has been increased from 817.452 um² to 852.269 um². The reason behind that is, CTS introduces some buffers and delay instances in the design while routing the clock in order to reduce the overall clock skew (skew minimization). Because of the extra instances added in the design, the overall area has been increased.

The total area reported is 852.269 um² and total instances used are 72. Some of the instances that are added are DLY3X1, CLKBUFX12, etc.

Comparing area report for both UF,

Area has been increased in both the cases as compared to the post placement step but comparatively the area in case of UF = 0.8 is slightly more than UF 0.5. The probable reason can be due to more congested routing in case of 0.8 UF, extra two instances are required to improve the clock skew and to reduce the latency due to various effects like coupling in nets, etc. Therefore, to adjust latency and slews more cells are required which ends up increasing the total area.

3. POWER ANALYSIS

- Core Utilization of 0.5**

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
dp_D4/FE_OFC0_OUT_0	0.0007637	0.007406	0.00839	0.0002199	CLKBUFX12
dp_D4/FE_OFC1_OUT_1	0.0007636	0.007395	0.008379	0.0002199	CLKBUFX12
FE_OFC3_OUT_3	0.0007637	0.00739	0.008373	0.0002199	CLKBUFX12
FE_OFC2_OUT_2	0.0007637	0.007385	0.008369	0.0002199	CLKBUFX12
dp_D4/Q_reg[0]	0.001812	6.659e-05	0.002015	0.0001363	SDFFQX1
dp_D4/Q_reg[2]	0.001736	6.63e-05	0.001938	0.0001363	SDFFQX1
dp_D4/Q_reg[1]	0.001736	6.551e-05	0.001938	0.0001363	SDFFQX1
dp_D4/Q_reg[3]	0.001721	6.606e-05	0.001923	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001617	0.0001116	0.001864	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001617	0.0001044	0.001857	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001616	9.089e-05	0.001844	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.001616	8.071e-05	0.001833	0.0001363	SDFFQX1
dp_D2/Q_reg[2]	0.001617	7.864e-05	0.001832	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001617	7.549e-05	0.001828	0.0001363	SDFFQX1
dp_f1/temp_reg[2]	0.001627	6.46e-05	0.001828	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001616	7.268e-05	0.001825	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001617	6.83e-05	0.001821	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.001613	6.786e-05	0.001817	0.0001363	SDFFQX1
dp_c1/out1_reg[2]	0.001628	5.181e-05	0.001816	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001617	6.325e-05	0.001816	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.001631	4.773e-05	0.001815	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.001616	6.224e-05	0.001815	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.001627	4.69e-05	0.00181	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.001616	5.462e-05	0.001807	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001616	5.443e-05	0.001807	0.0001363	SDFFQX1
dp_c1/out1_reg[0]	0.001613	5.688e-05	0.001806	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001617	5.325e-05	0.001806	0.0001363	SDFFQX1
dp_c1/out1_reg[3]	0.001613	5.614e-05	0.001806	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.001613	5.466e-05	0.001804	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001617	4.126e-05	0.001794	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001617	3.643e-05	0.00179	0.0001363	SDFFQX1
dp_f1/g114	0.0002031	5.112e-05	0.0003498	9.553e-05	ADDHX1
g893	0.0002459	7.045e-05	0.0003295	1.314e-05	OAI221X1
FE_PHC0_scan_en	0.0001304	0.0001505	0.0003222	4.129e-05	CLKBUFX2
g901	0.0001645	0.0001387	0.0003214	1.815e-05	AOI21X1
g900	0.000149	0.00011	0.0002862	2.717e-05	AND2X1
g905	0.0001533	3.537e-05	0.0002837	9.511e-05	MXI4X1
g908	0.0001152	0.0001242	0.0002575	1.815e-05	AOI21X1
g895	0.0001668	4.289e-05	0.0002528	4.309e-05	AO22X1
g896	0.0001669	3.987e-05	0.0002499	4.309e-05	AO22X1
g894	0.000167	3.713e-05	0.0002473	4.309e-05	AO22X1
g917	0.0001362	2.522e-05	0.000234	7.254e-05	CLKXOR2X1
g899	0.0001665	4.413e-05	0.0002288	1.815e-05	AOI21X1
g916	0.0001366	1.888e-05	0.000228	7.254e-05	CLKXOR2X1
g914	0.0001375	1.927e-05	0.0002274	7.055e-05	XNOR2X1
dp_f1/g112	0.0001365	2.027e-05	0.0002273	7.055e-05	XNOR2X1
g915	0.0001367	1.59e-05	0.0002251	7.254e-05	CLKXOR2X1
g897	0.0001456	4.694e-05	0.0002138	2.127e-05	OAI2BB1X1

g906	0.0001454	4.794e-05	0.0002134	2.004e-05	NOR2BX1
g903	0.0001055	4.651e-05	0.0001946	4.256e-05	OR2X1
g913	0.0001343	2.02e-05	0.0001859	3.144e-05	AOI2BB1X1
g909	0.0001412	2.234e-05	0.0001854	2.186e-05	NOR3BX1
g898	8.011e-05	6.12e-05	0.0001763	3.499e-05	NAND2BX1
g904	0.0001195	4.181e-05	0.0001753	1.402e-05	OAI31X1
g920	7.466e-05	4.289e-05	0.0001601	4.256e-05	OR2X1
g910	0.0001034	3.051e-05	0.0001518	1.789e-05	AOI31X1
g911	8.005e-05	4.912e-05	0.0001432	1.402e-05	OAI31X1
dp_c1/g19	7.887e-05	1.892e-05	0.0001403	4.256e-05	OR2X1
g921	4.306e-05	8.342e-05	0.0001395	1.301e-05	CLKINVX1
g907	8.331e-05	3.035e-05	0.0001266	1.299e-05	OAI21X1
g912	6.931e-05	3.581e-05	0.0001264	2.127e-05	OAI2BB1X1
dp_f1/g113	8.545e-05	2.078e-05	0.0001229	1.662e-05	NOR2BXL
dp_c1/g38	7.502e-05	1.955e-05	0.0001112	1.662e-05	NOR2BXL
dp_c1/g40	7.506e-05	1.887e-05	0.0001105	1.662e-05	NOR2BXL
dp_c1/g42	7.52e-05	1.579e-05	0.0001076	1.662e-05	NOR2BXL
dp_f1/g110	7.079e-05	1.808e-05	0.0001012	1.236e-05	NOR2XL
dp_f1/g116	6.352e-05	1.581e-05	9.169e-05	1.236e-05	NOR2XL
g919	2.815e-05	3.884e-05	7.628e-05	9.289e-06	NAND2XL
g918	4.459e-05	1.493e-05	7.253e-05	1.301e-05	CLKINVX1
g902	2.886e-05	3.157e-05	6.972e-05	9.289e-06	NAND2XL

Total (70 of 70) 0.05174 0.03305 0.09064 0.005847

Total Capacitance 4.432e-12 F

Power Density *** No Die Area ***

The total power for UF 0.5 after CTS is 0.09064mW, which has been decreased as compared to post placement step. The reason is that the internal power has been drastically reduced to 0.05174mW because of optimization happens after CTS. The internal power consumption has been reduced by using and connecting the instances optimally with clock. Switching power has reduced slightly whereas the leakage power has been increased slightly due to a greater number of instances present in the design after CTS. The capacitance has increased as compared to the last step due to extra buffers and delay instances added.

- **Core Utilization of 0.8**

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OFC1_OUT_3	0.000764	0.007408	0.008392	0.0002199	CLKBUFX12
dp_D4/FE_OFC2_OUT_2	0.0007644	0.007397	0.008382	0.0002199	CLKBUFX12
dp_D4/FE_OFC0_OUT_1	0.0007645	0.007392	0.008376	0.0002199	CLKBUFX12
FE_OFC3_OUT_0	0.0007638	0.007392	0.008375	0.0002199	CLKBUFX12
dp_D4/Q_reg[0]	0.001811	6.794e-05	0.002015	0.0001363	SDFFQX1
dp_D4/Q_reg[1]	0.001735	7.697e-05	0.001948	0.0001363	SDFFQX1
dp_D4/Q_reg[3]	0.001735	7.017e-05	0.001941	0.0001363	SDFFQX1
dp_D4/Q_reg[2]	0.00172	7.658e-05	0.001932	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001617	0.0001162	0.001869	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001617	0.000115	0.001868	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001617	0.0001085	0.001862	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.001617	9.583e-05	0.001849	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001617	8.965e-05	0.001842	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001617	7.897e-05	0.001832	0.0001363	SDFFQX1
dp_f1/temp_reg[2]	0.001642	4.836e-05	0.001826	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.001613	7.54e-05	0.001825	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.001616	6.96e-05	0.001822	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001617	6.888e-05	0.001822	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001616	6.895e-05	0.001822	0.0001363	SDFFQX1

dp_D2/Q_reg[2]	0.001617	6.591e-05	0.001819	0.0001363	SDFFQX1
dp_c1/out1_reg[3]	0.001629	4.842e-05	0.001813	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.001627	4.859e-05	0.001812	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.001613	6.099e-05	0.001811	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001617	5.676e-05	0.00181	0.0001363	SDFFQX1
dp_c1/out1_reg[0]	0.001613	5.999e-05	0.001809	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.001617	5.419e-05	0.001807	0.0001363	SDFFQX1
dp_c1/out1_reg[2]	0.001613	5.506e-05	0.001805	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001616	4.878e-05	0.001801	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001617	4.775e-05	0.001801	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.001616	3.999e-05	0.001793	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001617	3.735e-05	0.00179	0.0001363	SDFFQX1
dp_f1/g114	0.0002035	4.671e-05	0.0003458	9.553e-05	ADDHX1
g901	0.0001652	0.000142	0.0003253	1.815e-05	AOI21X1
g893	0.0002457	6.052e-05	0.0003194	1.314e-05	OAI221X1
g900	0.0001493	0.0001271	0.0003035	2.717e-05	AND2X1
g905	0.0001528	4.707e-05	0.000295	9.511e-05	MXI4X1
g896	0.0001661	8.033e-05	0.0002895	4.309e-05	AO22X1
g894	0.0001665	6.01e-05	0.0002697	4.309e-05	AO22X1
g908	0.0001153	0.0001352	0.0002687	1.815e-05	AOI21X1
g895	0.0001675	3.505e-05	0.0002457	4.309e-05	AO22X1
dp_D4/FE_PHCO_scan_en	0.0001299	7.076e-05	0.000242	4.129e-05	CLKBUFX2
g917	0.0001361	2.456e-05	0.0002332	7.254e-05	CLKXOR2X1
g915	0.0001364	2.374e-05	0.0002327	7.254e-05	CLKXOR2X1
g916	0.0001362	2.112e-05	0.0002298	7.254e-05	CLKXOR2X1
g914	0.0001375	2.119e-05	0.0002292	7.055e-05	XNOR2X1
dp_f1/g112	0.0001362	2.242e-05	0.0002292	7.055e-05	XNOR2X1
g899	0.000167	4.245e-05	0.0002276	1.815e-05	AOI21X1
g897	0.0001458	5.39e-05	0.0002209	2.127e-05	OAI2BB1X1
g906	0.0001456	4.936e-05	0.000215	2.004e-05	NOR2BX1
dp_D4/FE_PHC2_scan_en	0.0001299	3.885e-05	0.00021	4.129e-05	CLKBUFX2
dp_D4/FE_PHC1_scan_en	0.0001299	3.664e-05	0.0002078	4.129e-05	CLKBUFX2
g903	0.0001056	4.387e-05	0.000192	4.256e-05	OR2X1
g913	0.0001345	2.247e-05	0.0001884	3.144e-05	AOI2BB1X1
g909	0.0001414	2.187e-05	0.0001852	2.186e-05	NOR3BX1
g904	0.0001198	4.691e-05	0.0001808	1.402e-05	OA131X1
g898	8.025e-05	5.906e-05	0.0001743	3.499e-05	NAND2BX1
g920	7.474e-05	4.807e-05	0.0001654	4.256e-05	OR2X1
g910	0.0001043	4.296e-05	0.0001651	1.789e-05	AOI31X1
g911	8.077e-05	5.731e-05	0.0001521	1.402e-05	OAI31X1
g921	4.309e-05	8.726e-05	0.0001434	1.301e-05	CLKINVX1
dp_c1/g19	7.891e-05	1.779e-05	0.0001393	4.256e-05	OR2X1
g907	8.352e-05	3.319e-05	0.0001297	1.299e-05	AOI21X1
dp_f1/g113	8.554e-05	1.825e-05	0.0001204	1.662e-05	NOR2BXL
g912	6.928e-05	2.928e-05	0.0001198	2.127e-05	OAI2BB1X1
dp_c1/g38	7.504e-05	1.97e-05	0.0001114	1.662e-05	NOR2BXL
dp_c1/g40	7.51e-05	1.94e-05	0.0001111	1.662e-05	NOR2BXL
dp_c1/g42	7.515e-05	1.735e-05	0.0001091	1.662e-05	NOR2BXL
dp_f1/g110	7.072e-05	2.152e-05	0.0001046	1.236e-05	NOR2XL
dp_f1/g116	6.356e-05	1.619e-05	9.211e-05	1.236e-05	NOR2XL
g919	2.832e-05	4.038e-05	7.799e-05	9.289e-06	NAND2XL
g918	4.491e-05	1.606e-05	7.399e-05	1.301e-05	CLKINVX1
g902	2.916e-05	2.749e-05	6.594e-05	9.289e-06	NAND2XL

Total (72 of 72) 0.052 0.03328 0.09121 0.005929

Total Capacitance 4.457e-12 F

Power Density *** No Die Area ***

The total power for UF 0.8 after CTS is 0.09121mW, which has been decreased as compared to post placement step. The reason is that the internal power has been drastically reduced to 0.052mW because of optimization happens after CTS. The internal power consumption has been reduced by using and connecting the instances optimally with clock. Switching power has reduced slightly whereas the leakage

power has been increased slightly due to a greater number of instances present in the design after CTS. The capacitance has also increased because of the extra instances added, there load will also come in the total load.

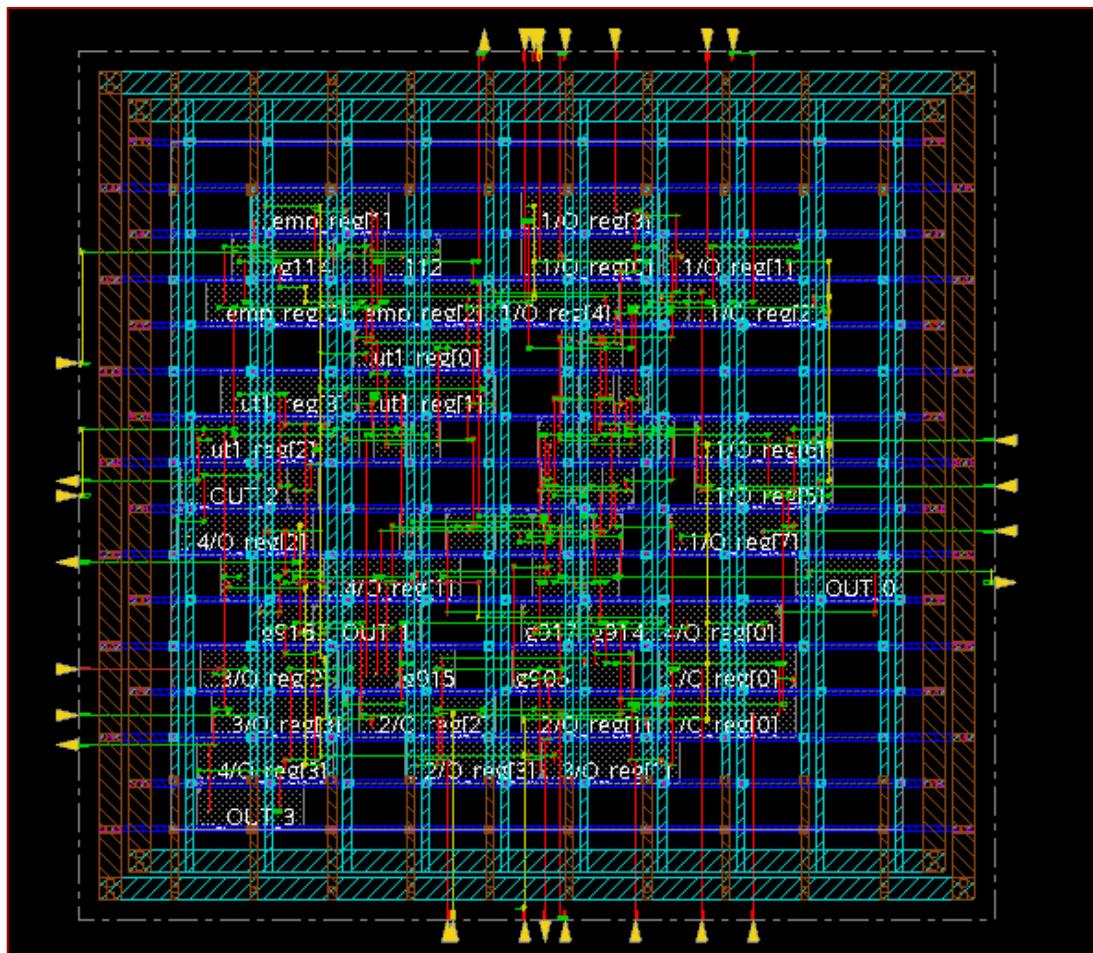
Comparing power report for both UF,

The power has reduced in both the cases due to optimization, but comparatively it has decreased more in case of UF 0.5 probably because of more optimized routing of clock and effective use of it reducing the internal power drastically. The total capacitive load has increased more in the case of UF 0.8 because of two more extra instances.

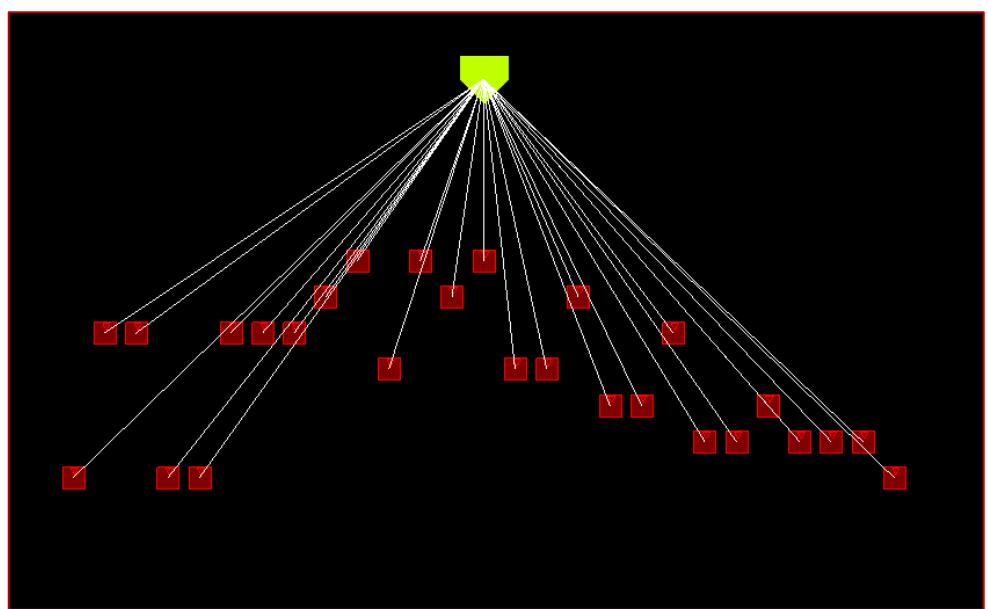
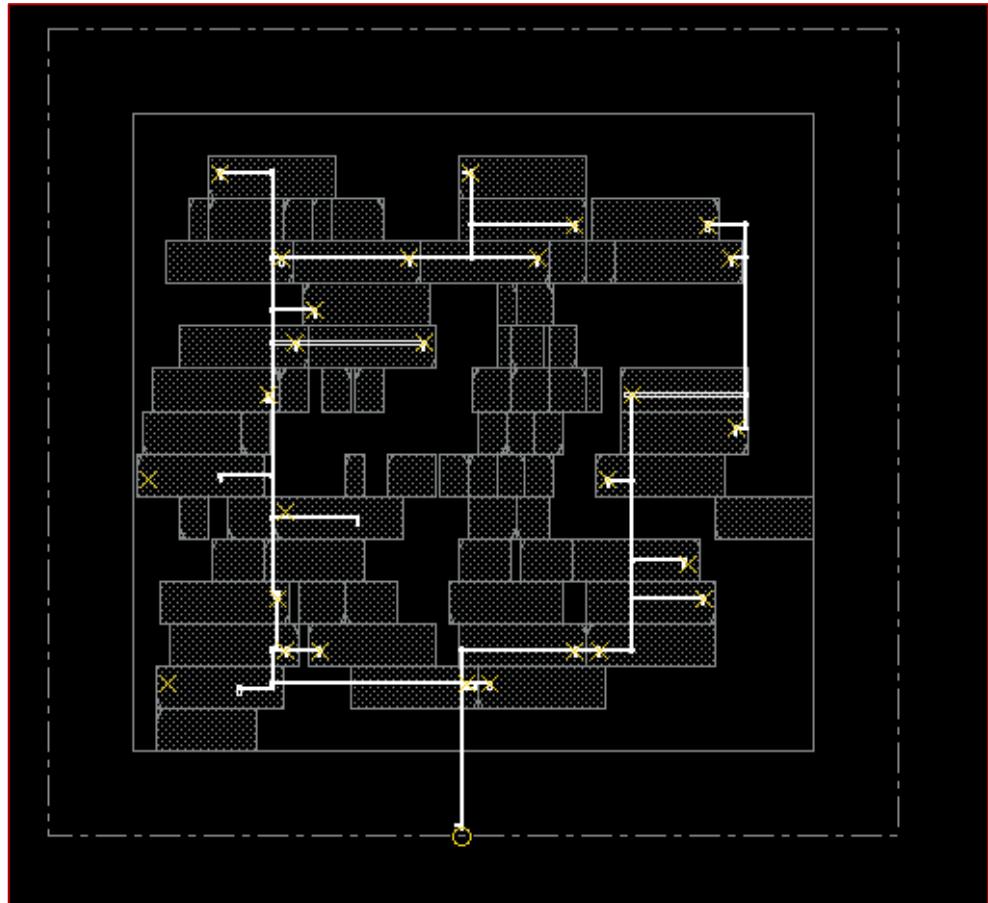
4. SNAPSHOTS OF LAYOUT

- Core Utilization of 0.5

○ After Clock Tree Synthesis



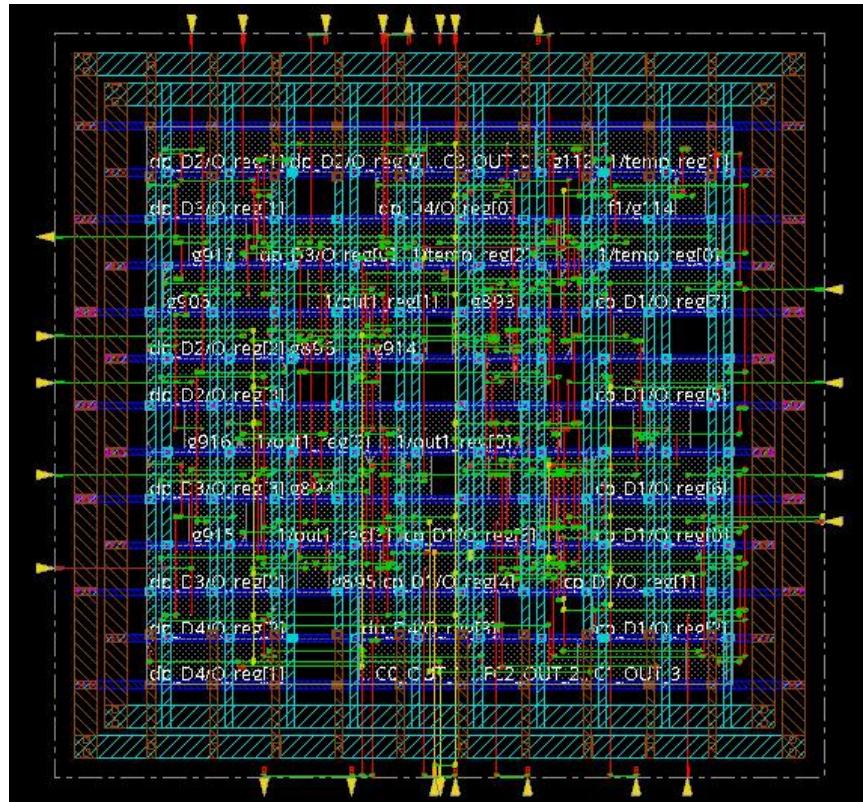
- Clock Tree network after CTS



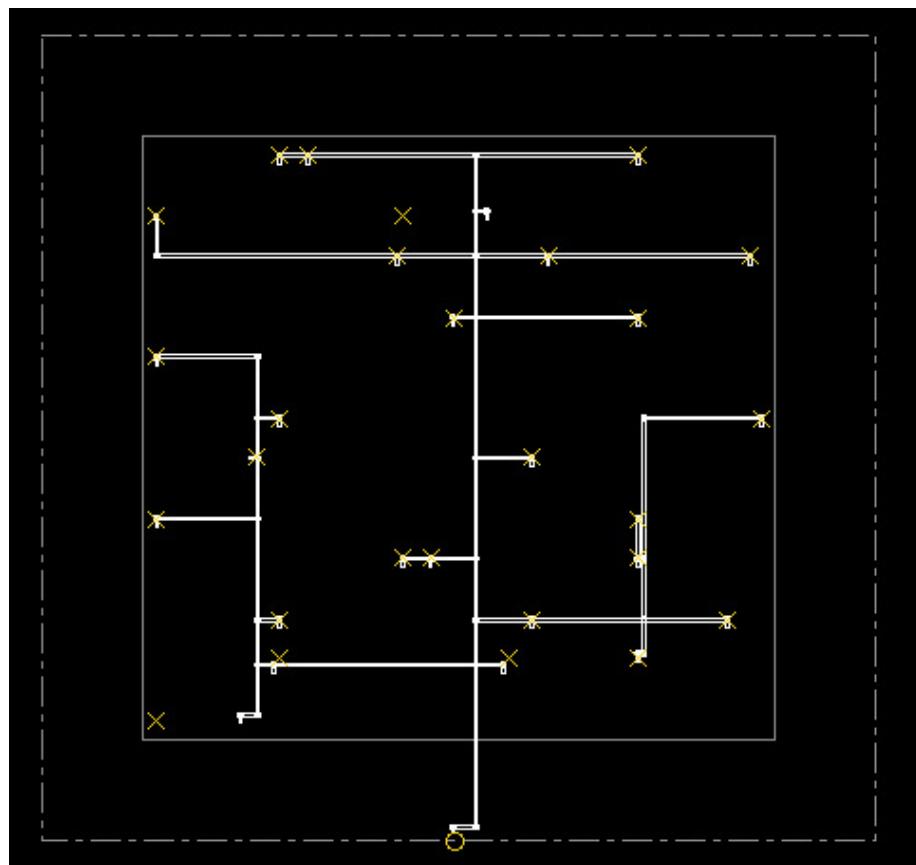
Clock Tree

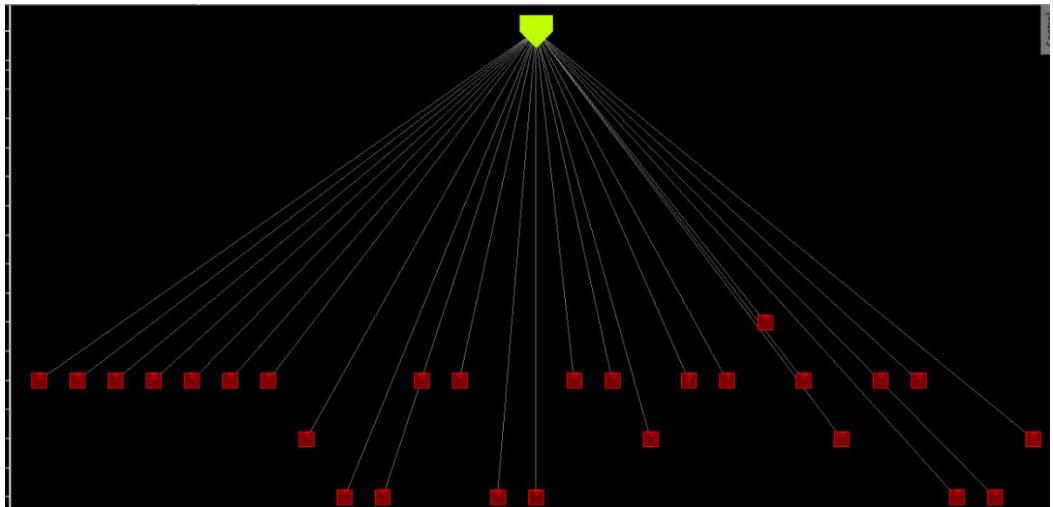
- **Core Utilization of 0.8**

- ### ○ After Clock Tree Synthesis



- ### ○ Clock Tree network after CTS





Clock Tree

STEP 4

AFTER DETAILED ROUTING

This phase involves routing the datapath signals, which is divided into two stages: global and detailed routing. The routing between two sites is chosen on a Gcell in global routing, whereas detailed routing is done by putting in the metal layers that are accessible, along with pertinent via connections.

Comparison of after detailed routing with core utilization of 0.5 and with 0.8 is done for all the timing, area and power is done.

1. TIMING ANALYSIS

A. Worst case hold slack

Core Utilization – 0.5	Core Utilization – 0.8
<pre> ##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 12:35:58 2022 # Design: group17 # Command: report_timing -early -view {view1} -max_paths 100 > ../reports/final_report/large_die_area/timing/hold_after_gds.txt ##### Path 1: MET Hold Check with Pin cp_D1/Q_reg[0]/CK Endpoint: cp_D1/Q_reg[0]/SI (v) checked with leading edge of 'clk' Beginpoint: DFT_sdi_1 (v) triggered by leading edge of '@' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.001 + Hold -0.015 + Phase Shift 0.000 + Uncertainty 0.002 = Required Time -0.012 Arrival Time 0.000 Slack Time 0.012 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 + Instance Arc Cell Delay Arrival Required Time Time -----+-----+-----+-----+-----+-----+ DFT_sdi_1 v SI v SDFFQX1 0.000 -0.012 cp_D1/Q_reg[0] 0.000 -0.012 +-----+-----+-----+-----+-----+-----+ </pre> <p style="text-align: center;">Slack = 0.012</p>	<pre> ##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 10:33:54 2022 # Design: group17 # Command: report_timing -early -view {view1} -max_paths 100 > ../reports/final_report/small_die_area/timing/hold_after_gds.txt ##### Path 1: MET Hold Check with Pin dp_D3/Q_reg[2]/SI (v) Endpoint: dp_D3/Q_reg[2]/SI (v) checked with leading edge of 'clk' Beginpoint: DFT_sdi_2 (v) triggered by leading edge of '@' Path Groups: {clk} Analysis View: view1 Other End Arrival Time 0.001 + Hold -0.015 + Phase Shift 0.000 + Uncertainty 0.002 = Required Time -0.012 Arrival Time 0.000 Slack Time 0.012 Clock Rise Edge 0.000 + Input Delay 0.000 = Beginpoint Arrival Time 0.000 + Instance Arc Cell Delay Arrival Required Time Time -----+-----+-----+-----+-----+-----+ DFT_sdi_2 v SI v SDFFQX1 0.000 -0.012 dp_D3/Q_reg[2] 0.000 -0.012 +-----+-----+-----+-----+-----+-----+ </pre> <p style="text-align: center;">Slack = 0.012</p>

For Utilisation Factor Of 0.5

As it can be seen from the above snapshot of the timing report for the path DFT_sdi_1 to cp_D1/Q_reg[0]/SI. The hold slack observed here is 0.012 ns = AT - RT = 0.000 - (- 0.012) ns.

For Utilisation Factor Of 0.8

As it can be seen from the above snapshot of the timing report for the path DFT_sdi_2 to dp_D3/Q_reg[2]/SI. The hold slack observed here is 0.012 ns = AT - RT = 0.000 - (- 0.012) ns.

Reason as to why hold slack remains same

Here as it can be seen that the hold slack after detailed routing remains to be exact same as it is in the post clock tree synthesis as our design is fully optimized in the post clock tree synthesis.

B. Worst case setup slack

Core Utilization – 0.5	Core Utilization – 0.8
<pre>##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 12:36:02 2022 # Design: group17 # Command: report_timing -late -max_paths 100 > ./reports/final_report/large_die_area/timing/setup_after_gds.txt ##### Path 1: MEI Late External Delay Assertion Endpoint: OUT[1] (^) checked with leading edge of 'clk' Beginpoint: dp_D4/Q_reg[1]/Q (^) triggered by leading edge of 'clk' Path 1: MEI Early External Delay Assertion Analysis View: View1 Other End Arrival Time 0.000 External Delay 3.000 + Phase Shift 11.000 - Uncertainty 1.000 = Required Time 7.000 - Arrival Time 0.904 = Slack Time 6.096 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.001 = Beginpoint Arrival Time 0.001 +-----+ Instance Arc Cell Delay Arrival Required Time Time Time +-----+ dp_D4/Q_reg[1] CK ^ SDFEQX1 0.001 6.097 dp_D4/Q_reg[1] CK ^ -> Q ^ SDFEQX1 0.303 6.400 dp_D4/FE_OFCl_OUT_1 A ^ -> Y ^ CLKBUX12 0.589 6.892 OUT[1] ^ 0.012 0.904 7.000 +-----+</pre> <p style="text-align: center;">Slack = 6.096</p>	<pre>##### # Generated by: Cadence Innovus 20.10-p004_1 # OS: Linux x86_64(Host ID edaserver4) # Generated on: Sat Apr 30 10:33:54 2022 # Design: group17 # Command: report_timing -late -max_paths 100 > ./reports/final_report/small_die_area/timing/setup_after_gds.txt ##### Path 1: MEI Late External Delay Assertion Endpoint: OUT[2] (^) checked with leading edge of 'clk' Beginpoint: dp_D4/Q_reg[2]/Q (^) triggered by leading edge of 'clk' Path 1: MEI Early External Delay Assertion Analysis View: View1 Other End Arrival Time 0.000 External Delay 3.000 + Phase Shift 11.000 - Uncertainty 1.000 = Required Time 7.000 - Arrival Time 0.913 = Slack Time 6.087 Clock Rise Edge 0.000 + Clock Network Latency (Prop) 0.001 = Beginpoint Arrival Time 0.001 +-----+ Instance Arc Cell Delay Arrival Required Time Time Time +-----+ dp_D4/Q_reg[2] CK ^ SDFEQX1 0.310 6.088 dp_D4/Q_reg[2] CK ^ -> Q ^ SDFEQX1 0.311 6.398 dp_D4/FE_OFc2_OUT_2 A ^ -> Y ^ CLKBUX12 0.592 6.983 OUT[2] ^ 0.010 0.913 7.000 +-----+</pre> <p style="text-align: center;">Slack = 6.087</p>

For Utilisation Factor Of 0.5

As it can be seen from the above snapshot of the timing report for the path dp_D4/Q_reg[1]/Q to OUT[1]. The setup slack observed here is 6.096 ns = RT - AT = 7.000 – 0.904 ns.

For Utilisation Factor Of 0.8

As it can be seen from the above snapshot of the timing report for the path dp_D4/Q_reg[2]/Q to OUT[2]. The setup slack observed here is 6.087 ns = RT - AT = 7.000 – 0.913 ns.

Reason as to why setup slack increases

A plan for each net that has to be routed is produced during routing. However, in detailed routing, the exact layout of each net is determined. Assigning additional metal tracks for tracking results in less wire congestion, improved routing, and hence improved slack. The AT also decreases due to the ease of routing.

Reason as to why setup slack increases with increase in UF from 0.5 to 0.8

With the increase in UF, the AT decreases, The total slack has decreased as delays have dropped owing to less standard cell congestion and RC delays have decreased with shorter wire lengths utilised for routing.

2. AREA ANALYSIS

- Core Utilization of 0.5

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational
Flop	Latch	Clock Gate	Macro	Physical		
group17		70	843.187	68.121	4.541	218.744
551.780	0.000	0.000	0.000	0.000	0.000	0.000
cp_D1	DFF8	8	163.490	0.000	0.000	0.000
163.490	0.000	0.000	0.000	0.000	0.000	0.000
dp_D2	DFF4	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000	0.000	0.000
dp_D3	DFF4_18	4	81.745	0.000	0.000	0.000
81.745	0.000	0.000	0.000	0.000	0.000	0.000
dp_D4	DFF4_17	6	113.535	31.790	0.000	0.000
81.745	0.000	0.000	0.000	0.000	0.000	0.000
dp_c1	Rcounter4	8	99.911	0.000	0.000	18.166
81.745	0.000	0.000	0.000	0.000	0.000	0.000
dp_f1	freq_div	8	92.342	0.000	0.000	31.033
61.309	0.000	0.000	0.000	0.000	0.000	

Design Status: Routed
Design Name: group17
Instances: 70
Hard Macros: 0
Std Cells: 70

Standard Cells in Netlist

Cell Type Instance Count Area (um^2)
OAI2BB1X1 2 10.5966
CLKBUFX2 1 4.5414
CLKBUFX12 4 63.5796
CLKXOR2X1 3 24.9777
OR2X1 3 13.6242
AOI2BB1X1 1 6.0552
AND2X1 1 4.5414
SDFFQX1 27 551.7801
XNOR2X1 2 16.6518
OAI21X1 1 4.5414
OAI221X1 1 7.5690
OAI31X1 2 12.1104
CLKINVX1 2 4.5414
NAND2BX1 1 4.5414
NAND2XL 2 6.0552
ADDHX1 1 12.1104
NOR2BX1 1 4.5414
AOI21X1 3 13.6242
NOR3BX1 1 6.0552
AOI31X1 1 6.0552
AO22X1 3 22.7070
NOR2XL 2 6.0552
NOR2BXL 4 18.1656
MXI4X1 1 18.1656

Break up of area report after CTS

As it can be seen from the above snapshot of the timing report. The area after detailed routing remains to be exact same as it is in the post clock tree synthesis i.e. 843.187 um^2 .

- Core Utilization of 0.8

Inst Name	Module Name	Inst Count	Total Area
Buffer	Inverter	Combinational	Flop
Latch	Clock Gate	Macro	Physical
<hr/>			
-	-	72	852.269
group17	-	-	-
77.204	4.541	218.744	551.780
0.000	0.000	0.000	0.000
cp_D1	DFF8	8	163.490
0.000	0.000	0.000	163.490
0.000	0.000	0.000	0.000
dp_D2	DFF4	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D3	DFF4_18	4	81.745
0.000	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_D4	DFF4_17	9	127.159
45.414	0.000	0.000	81.745
0.000	0.000	0.000	0.000
dp_c1	Rcounter4	8	99.911
0.000	0.000	18.166	81.745
0.000	0.000	0.000	0.000
dp_f1	freq_div	8	92.342
0.000	0.000	31.033	61.309
0.000	0.000	0.000	0.000

Total Area Report

Design Status: Routed
Design Name: group17
Instances: 72
Hard Macros: 0
Std Cells: 72
<hr/>
Standard Cells in Netlist
<hr/>
Cell Type Instance Count Area (um^2)
OA12BB1X1 2 10.5966
CLKBUFX2 3 13.6242
CLKBUFX12 4 63.5796
CLKXOR2X1 3 24.9777
OR2X1 3 13.6242
AOI2BB1X1 1 6.0552
AND2X1 1 4.5414
SDFFQX1 27 551.7801
XNOR2X1 2 16.6518
OAI21X1 1 4.5414
OAI221X1 1 7.5690
OAI31X1 2 12.1104
CLKINVX1 2 4.5414
NAND2BX1 1 4.5414
NAND2XL 2 6.0552
ADDHX1 1 12.1104
NOR2BX1 1 4.5414
AOI21X1 3 13.6242
NOR3BX1 1 6.0552
AOI31X1 1 6.0552
A022X1 3 22.7070
NOR2XL 2 6.0552
NOR2BXL 4 18.1656
MXI4X1 1 18.1656

Break up of area report after CTS

The area after detailed routing remains to be exact same as it is in the post clock tree synthesis i.e. 852.269 um².

Explanation

The obtained area after detailed routing remains to be exact same as it is in the post clock tree synthesis because In the design, no new instances have been introduced or changed. As a result, it's reasonable to assume that the area will remain unchanged.

3. POWER ANALYSIS

- **Core Utilization of 0.5**

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OF_C2_OUT_2	0.003819	0.03694	0.04098	0.0002199	CLKBUFX12
dp_D4/FE_OF_C1_OUT_1	0.003783	0.03663	0.04063	0.0002199	CLKBUFX12
dp_D4/FE_OF_C0_OUT_0	0.003675	0.03563	0.03952	0.0002199	CLKBUFX12
FE_OF_C3_OUT_3	0.002587	0.02503	0.02784	0.0002199	CLKBUFX12
dp_D4/Q_reg[2]	0.003098	0.0003326	0.003567	0.0001363	SDFFQX1
dp_D4/Q_reg[1]	0.003045	0.0003345	0.003516	0.0001363	SDFFQX1
dp_D4/Q_reg[0]	0.002933	0.0003214	0.003391	0.0001363	SDFFQX1
dp_c1/out1_reg[2]	0.002614	0.0001955	0.002946	0.0001363	SDFFQX1
dp_D4/Q_reg[3]	0.002395	0.0002238	0.002755	0.0001363	SDFFQX1
dp_c1/out1_reg[3]	0.002364	0.0001854	0.002686	0.0001363	SDFFQX1
dp_c1/out1_reg[0]	0.002335	0.0001909	0.002663	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.002343	0.000151	0.002631	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.00227	0.0002084	0.002615	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.002266	0.000159	0.002561	0.0001363	SDFFQX1
dp_f1/temp_reg[2]	0.002187	0.0001663	0.00249	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.002206	0.0001279	0.00247	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001909	0.0002385	0.002284	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001916	0.0002281	0.00228	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001917	0.0001932	0.002246	0.0001363	SDFFQX1
dp_D2/Q_reg[2]	0.001918	0.0001707	0.002225	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001917	0.000148	0.002202	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001914	0.0001478	0.002198	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001918	0.0001358	0.00219	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001917	0.0001164	0.00217	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001917	0.0001129	0.002166	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.0019	0.0001292	0.002165	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.001882	0.0001162	0.002135	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001847	0.0001494	0.002133	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.001781	0.0001481	0.002065	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001698	5.758e-05	0.001892	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001698	5.497e-05	0.00189	0.0001363	SDFFQX1
dp_f1/g114	0.0005229	0.0001312	0.0007496	9.553e-05	ADDHX1
g893	0.0005078	0.000156	0.0006769	1.314e-05	OAI221X1
g901	0.0003428	0.0002953	0.0006562	1.815e-05	AOI21X1
g900	0.0003093	0.0002529	0.0005895	2.717e-05	AND2X1
g908	0.0002406	0.0002918	0.0005506	1.815e-05	AOI21X1
g895	0.0003658	9.115e-05	0.0005	4.309e-05	AO22X1
g915	0.0003769	4.175e-05	0.0004911	7.254e-05	CLKXOR2X1
dp_f1/g112	0.0003611	5.928e-05	0.0004909	7.055e-05	XNOR2X1
g905	0.000322	7.042e-05	0.0004875	9.511e-05	MXI4X1
g894	0.0003591	8.442e-05	0.0004866	4.309e-05	AO22X1
g899	0.0003611	9.846e-05	0.0004777	1.815e-05	AOI21X1
g896	0.0003391	7.922e-05	0.0004615	4.309e-05	AO22X1
g906	0.0003054	0.000106	0.0004314	2.004e-05	NOR2BX1
g897	0.0003034	9.459e-05	0.0004193	2.127e-05	OAI2BB1X1
g917	0.0002857	5.744e-05	0.0004157	7.254e-05	CLKXOR2X1
g914	0.0002887	3.979e-05	0.0003991	7.055e-05	XNOR2X1
g916	0.0002853	3.961e-05	0.0003974	7.254e-05	CLKXOR2X1
g903	0.000218	9.75e-05	0.000358	4.256e-05	OR2X1
FE_PH_C0_scan_en	0.0001435	0.0001732	0.000358	4.129e-05	CLKBUFX2
g904	0.0002437	9.257e-05	0.0003503	1.402e-05	OAI31X1
g909	0.0002827	4.022e-05	0.0003448	2.186e-05	NOR3BX1
g913	0.0002727	4.03e-05	0.0003444	3.144e-05	AOI2BB1X1
g898	0.0001661	0.0001265	0.0003276	3.499e-05	NAND2BX1
g920	0.0001516	9.173e-05	0.0002859	4.256e-05	OR2X1
g921	9.006e-05	0.0001819	0.0002849	1.301e-05	CLKINVX1
dp_c1/g19	0.0001896	4.435e-05	0.0002765	4.256e-05	OR2X1
g910	0.0001981	5.961e-05	0.0002756	1.789e-05	AOI31X1

g911	0.0001492	0.0001034	0.0002666	1.402e-05	OAI31X1
g907	0.0001696	6.812e-05	0.0002507	1.299e-05	OAI21X1
dp_f1/g113	0.0001919	3.922e-05	0.0002477	1.662e-05	NOR2BXL
g912	0.0001425	7.928e-05	0.000243	2.127e-05	OAI2BB1X1
dp_c1/g38	0.0001697	4.076e-05	0.0002271	1.662e-05	NOR2BXL
dp_c1/g42	0.0001639	3.313e-05	0.0002136	1.662e-05	NOR2BXL
dp_c1/g40	0.0001356	3.115e-05	0.0001834	1.662e-05	NOR2BXL
dp_f1/g116	0.0001321	3.672e-05	0.0001812	1.236e-05	NOR2XL
dp_f1/g110	0.0001177	3.437e-05	0.0001644	1.236e-05	NOR2XL
g902	6.465e-05	6.633e-05	0.0001403	9.289e-06	NAND2XL
g919	5.094e-05	7.2e-05	0.0001322	9.289e-06	NAND2XL
g918	8.106e-05	2.86e-05	0.0001227	1.301e-05	CLKINVX1
<hr/>					
Total (70 of 70)	0.08137	0.1425	0.2298	0.005847	
Total Capacitance	4.445e-12 F				
Power Density	*** No Die Area ***				

As it can be seen from the above snapshot, the power obtained post clock tree synthesis is 0.09064 mW and the Capacitance obtained is 4.432×10^{-12} whereas the power obtained after detailed routing is 0.09065 mW and the Capacitance obtained is 4.445×10^{-12} .

Explanation

The total power and capacitance have been raised slightly. Because the routing engine has done few re-routings to remove the trial route violations, the RC delays of the paths may have risen in the detailed path routing step (in Post route). As a result, the change in resistance and capacitance levels must have resulted in an increase in total power.

- **Core Utilization of 0.8**

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
FE_OFC3_OUT_0	0.003705	0.03585	0.03977	0.0002199	CLKBUFX12
FE_OFC1_OUT_3	0.003491	0.03385	0.03756	0.0002199	CLKBUFX12
dp_D4/FE_OFC0_OUT_1	0.003203	0.03097	0.03439	0.0002199	CLKBUFX12
dp_D4/FE_OFC2_OUT_2	0.002609	0.02524	0.02807	0.0002199	CLKBUFX12
dp_D4/Q_reg[0]	0.002931	0.0003294	0.003397	0.0001363	SDFFQX1
dp_D4/Q_reg[3]	0.002909	0.0003197	0.003365	0.0001363	SDFFQX1
dp_D4/Q_reg[1]	0.00275	0.0003204	0.003207	0.0001363	SDFFQX1
dp_f1/temp_reg[2]	0.00279	0.000195	0.003121	0.0001363	SDFFQX1
dp_c1/out1_reg[3]	0.002562	0.0001713	0.00287	0.0001363	SDFFQX1
dp_c1/out1_reg[0]	0.002471	0.0002079	0.002816	0.0001363	SDFFQX1
dp_D4/Q_reg[2]	0.002398	0.0002614	0.002796	0.0001363	SDFFQX1
dp_c1/out1_reg[1]	0.00232	0.0002038	0.00266	0.0001363	SDFFQX1
dp_c1/out1_reg[2]	0.002332	0.0001722	0.00264	0.0001363	SDFFQX1
dp_f1/temp_reg[0]	0.002284	0.0002162	0.002636	0.0001363	SDFFQX1
dp_f1/temp_reg[1]	0.002287	0.0001472	0.002571	0.0001363	SDFFQX1
cp_D1/Q_reg[4]	0.001916	0.0002342	0.002287	0.0001363	SDFFQX1
cp_D1/Q_reg[7]	0.001883	0.0002332	0.002252	0.0001363	SDFFQX1
cp_D1/Q_reg[3]	0.001913	0.0001962	0.002246	0.0001363	SDFFQX1
dp_D3/Q_reg[0]	0.001917	0.0001903	0.002244	0.0001363	SDFFQX1
dp_D2/Q_reg[3]	0.001917	0.000169	0.002223	0.0001363	SDFFQX1
dp_D3/Q_reg[1]	0.001917	0.000142	0.002196	0.0001363	SDFFQX1

dp_D2/Q_reg[2]	0.001918	0.0001412	0.002195	0.0001363	SDFFQX1
cp_D1/Q_reg[2]	0.001909	0.0001372	0.002182	0.0001363	SDFFQX1
dp_D2/Q_reg[0]	0.001917	0.0001195	0.002173	0.0001363	SDFFQX1
dp_D2/Q_reg[1]	0.001917	0.0001035	0.002157	0.0001363	SDFFQX1
cp_D1/Q_reg[1]	0.001901	0.0001056	0.002142	0.0001363	SDFFQX1
cp_D1/Q_reg[5]	0.001848	0.0001287	0.002113	0.0001363	SDFFQX1
cp_D1/Q_reg[6]	0.001781	0.0001936	0.002111	0.0001363	SDFFQX1
dp_D3/Q_reg[3]	0.00178	7.004e-05	0.001987	0.0001363	SDFFQX1
cp_D1/Q_reg[0]	0.001698	6.402e-05	0.001899	0.0001363	SDFFQX1
dp_D3/Q_reg[2]	0.001698	5.194e-05	0.001886	0.0001363	SDFFQX1
dp_f1/g112	0.0005602	8.698e-05	0.0007177	7.055e-05	XNOR2X1
dp_f1/g114	0.0004743	9.715e-05	0.000667	9.553e-05	ADDHX1
g901	0.0003194	0.0002679	0.0006054	1.815e-05	AOI21X1
g893	0.0004748	0.0001107	0.0005985	1.314e-05	OAI221X1
g900	0.0002926	0.0002562	0.000576	2.717e-05	AND2X1
g896	0.0003325	0.0001454	0.0005209	4.309e-05	AO22X1
g908	0.0002252	0.000273	0.0005164	1.815e-05	AOI21X1
g905	0.0003208	9.95e-05	0.0005154	9.511e-05	MXI4X1
g894	0.0003342	0.0001173	0.0004945	4.309e-05	AO22X1
g899	0.0003566	8.948e-05	0.0004642	1.815e-05	AOI21X1
g895	0.0003386	6.733e-05	0.0004491	4.309e-05	AO22X1
g906	0.0002929	9.849e-05	0.0004114	2.004e-05	NOR2BX1
g915	0.0002856	5.133e-05	0.0004095	7.254e-05	CLKXOR2X1
g917	0.0002859	4.981e-05	0.0004082	7.254e-05	CLKXOR2X1
g897	0.0002855	9.82e-05	0.000405	2.127e-05	OAI2BB1X1
g914	0.0002885	4.507e-05	0.0004041	7.055e-05	XNOR2X1
g916	0.0002841	4.437e-05	0.000401	7.254e-05	CLKXOR2X1
g913	0.0002709	4.199e-05	0.0003444	3.144e-05	AOI2BB1X1
g903	0.000212	8.574e-05	0.0003403	4.256e-05	OR2X1
g909	0.0002703	4.033e-05	0.0003325	2.186e-05	NOR3BX1
g904	0.0002233	8.62e-05	0.0003235	1.402e-05	OAI31X1
g910	0.0002177	8.701e-05	0.0003226	1.789e-05	AOI31X1
g898	0.0001589	0.0001152	0.0003091	3.499e-05	NAND2BX1
g920	0.0001543	0.0001018	0.0002986	4.256e-05	OR2X1
g911	0.0001633	0.0001176	0.0002949	1.402e-05	OAI31X1
dp_c1/g19	0.0001978	4.371e-05	0.0002841	4.256e-05	OR2X1
g921	8.22e-05	0.0001665	0.0002617	1.301e-05	CLKINVX1
dp_D4/FE_PHCO_scan_en	0.0001429	7.72e-05	0.0002614	4.129e-05	CLKBUFX2
dp_f1/g110	0.0001726	5.569e-05	0.0002407	1.236e-05	NOR2XL
dp_c1/g42	0.0001819	3.692e-05	0.0002354	1.662e-05	NOR2BXL
dp_f1/g113	0.0001827	3.601e-05	0.0002353	1.662e-05	NOR2BXL
g907	0.0001564	5.868e-05	0.0002281	1.299e-05	AOI21X1
g912	0.0001457	5.995e-05	0.0002269	2.127e-05	OAI2BB1X1
dp_D4/FE_PHC2_scan_en	0.0001429	4.236e-05	0.0002265	4.129e-05	CLKBUFX2
dp_D4/FE_PHC1_scan_en	0.0001428	3.932e-05	0.0002235	4.129e-05	CLKBUFX2
dp_c1/g38	0.0001522	3.609e-05	0.000205	1.662e-05	NOR2BXL
dp_c1/g40	0.0001482	3.009e-05	0.0001949	1.662e-05	NOR2BXL
dp_f1/g116	0.0001351	3.619e-05	0.0001836	1.236e-05	NOR2XL
g919	5.922e-05	8.524e-05	0.0001537	9.289e-06	NAND2XL
g918	9.412e-05	3.231e-05	0.0001394	1.301e-05	CLKINVX1
g902	6.919e-05	5.987e-05	0.0001384	9.289e-06	NAND2XL

Total (72 of 72) 0.0805 0.1343 0.2207 0.005929

Total Capacitance 4.453e-12 F

Power Density *** No Die Area ***

As it can be seen from the above snapshot, the power obtained post clock tree synthesis is 0.09121 mW and the Capacitance obtained is 4.457×10^{-12} whereas the power obtained after detailed routing is 0.09117mW and the Capacitance obtained is 4.445×10^{-12} .

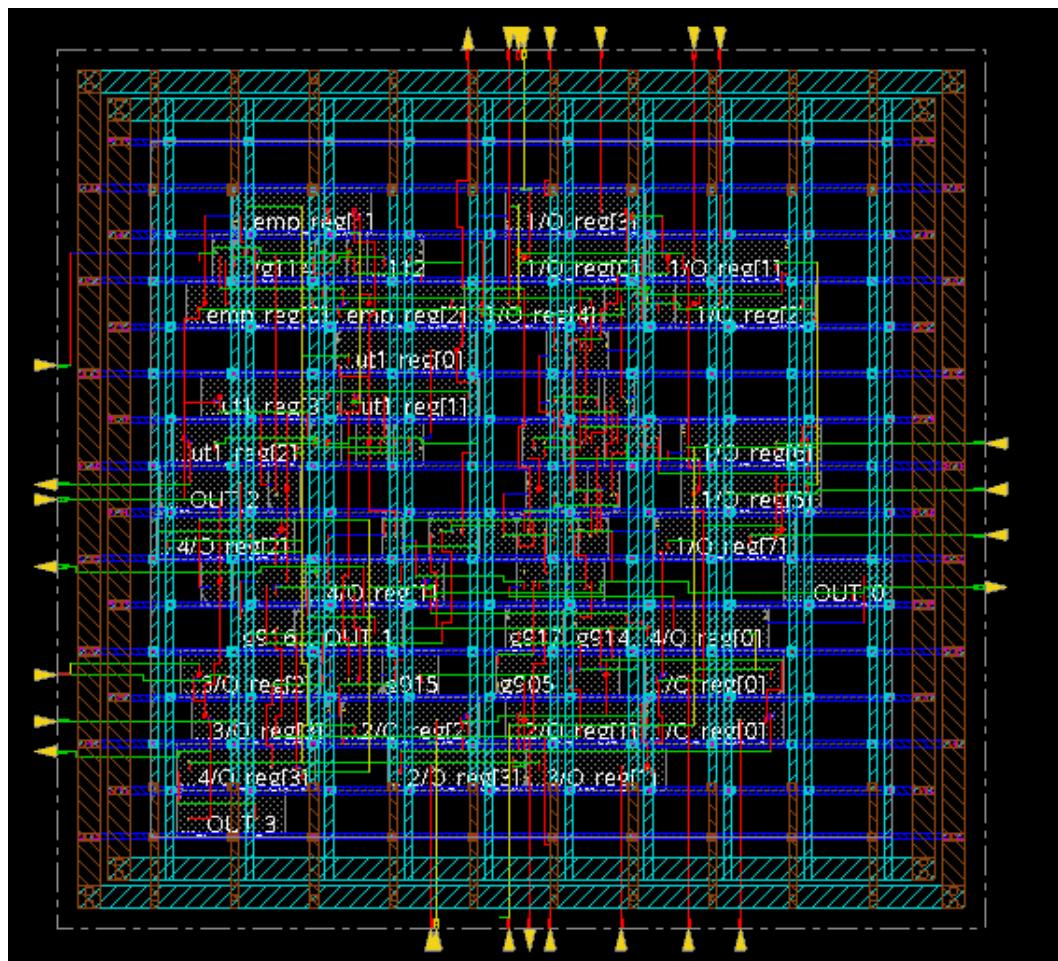
Explanation

Here, It can be seen that the power dissipation is nearly identical to what was reported in the post clock tree synthesis data. Furthermore, it has been lowered little in the post-route data. This behaviour is due to the fact that post route (particularly detailed routing) reduces power consumption.

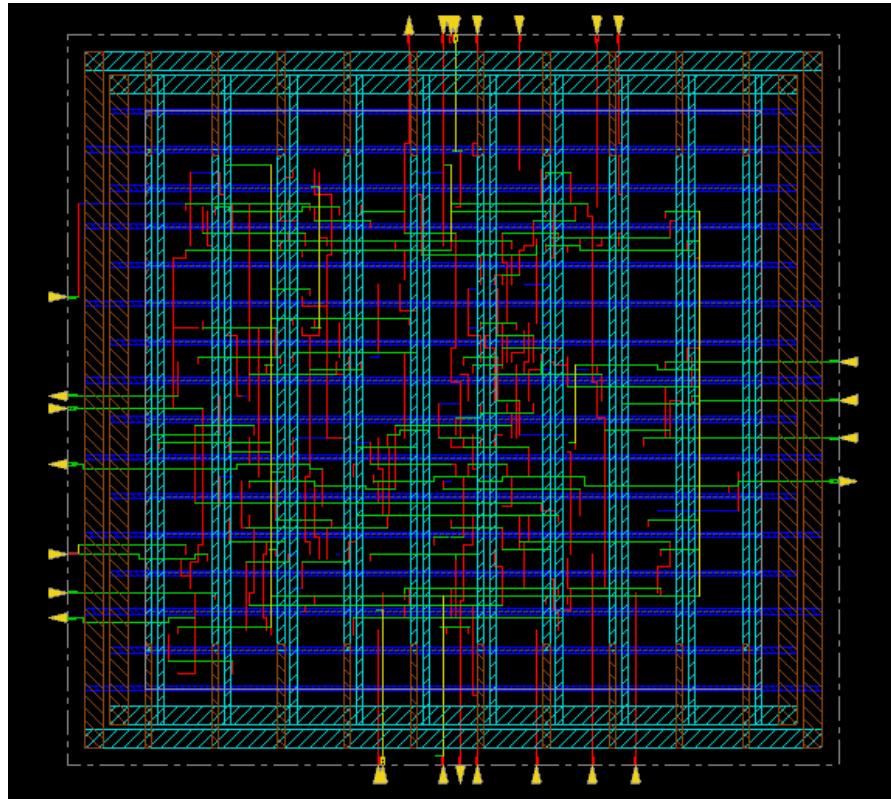
4. SNAPSHOTS OF LAYOUT

- **Core Utilization of 0.8**

- ### ○ Complete Layout after Detailed routing

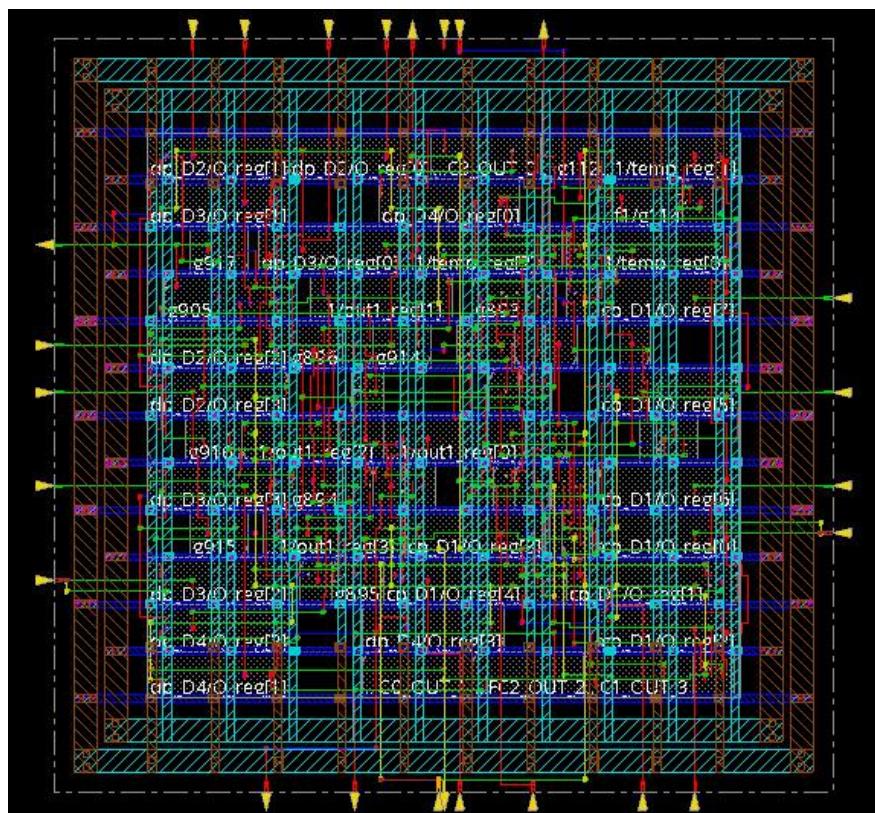


- Snapshot of layout of design and connectivity showing different metal layers



- Core Utilization of 0.5

- ### ○ Complete Layout after Detailed routing



- Snapshot of layout of design and connectivity showing different metal layers

