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THIRD SEMESTER

B.Tech (CSE)

MID TERM EXAMINATION **March-2023**

CO206 Computer Organization & Architecture

Time: 1:30 Hours **Max.Marks: 25**

Note: Attempt Any FIVE Questions
All questions carry equal marks
Assume suitable missing data, if any

Q1. Define Computer Organisation. Illustrate diagrammatically 4 bit Parallel Adder-Subtractor. **[5 Marks][CO1]**

Q2. Draw the hardware circuit for Logical shift, Arithmetic shift and Circular shift. State your design specification **[5 Marks][CO1]**

Q3. Compare the following

(a) Combinational Circuit with Sequential Circuit.
(b) Hardwired and Micro program control unit **[5 Marks][CO2]**

Q4. Explain Instruction cycle. Illustrate diagrammatically each instruction sub cycle with micro instructions. **[5 Marks][CO2]**

Q.5 Explain addressing mode. In a computer system, the memory is byte addressable. The word length is 4 bytes. An instruction is stored in one word. 24 bits are used to store the address part of the instruction. The value of the PC is 1200. The value of register R is 700. While executing the following two instructions: AC ← (PC+200) and AC← -(R)

What will be the effective address of each instruction respectively?

[5 Marks][CO3]

Q.6 Write short notes on **any two** of the following

a) Microprogram Sequencer
b) Zero Address Instruction
c) Second Pass Assembler

[5 Marks][CO3]

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