ALEXANDER KNAPEN

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OBJECTIVE

Second-year PhD student specializing in *quantum error correction* and *quantum-classical systems design* with demonstrated contributions to cryogenic predecoding and scalable cryogenic architectures, as well as extensive academic and industrial experience spanning the entire computing stack. Seeking internship opportunities to broaden my understanding of fault-tolerant quantum computing systems and architectures.

EDUCATION

- **University of Michigan, Ann Arbor** — *Aug. 2024 - Present*
  Ph.D. Computer Science and Engineering | Advisor: Dr. Gokul Ravi — Ann Arbor, MI
  - GPA: 4.00/4.00
  - Awards: Quantum Research Institute Presidential Graduate Fellowship
- **Delft University of Technology** — *Sep. 2022 - Jul. 2024*
  MSc. Computer Engineering — Delft, the Netherlands
  - Grade: 8.88/10 (4.00 U.S. equiv.), *Cum Laude (highest distinction)*
- **California Polytechnic State University, SLO** — *Sep. 2018 - Jun. 2024*
  B.S. Computer Engineering — San Luis Obispo, CA
  - GPA: 3.98/4.00, *Summa Cum Laude (highest distinction)*

Relevant Coursework: Hybrid Quantum-Classical Systems, Quantum Computer Architectures and Electronics, Fundamentals of Quantum Information, Computer Architecture, Advanced Computing Systems

PUBLICATIONS

* = AUTHORS CONTRIBUTED EQUALLY

[1] **Alexander Knapen***, Guanchen Tao*, Jacob Mack, Tomas Bruno, Mehdi Saligane, Dennis Sylvester, Qirui Zhang, Gokul Subramanian Ravi. "Pinball: A Cryogenic Predecoder for Surface Code Decoding Under Circuit-Level Noise." *To appear at the 2026 IEEE International Symposium on High-Performance Computer Architecture (HPCA'26)*.

[2] Folkert de Ronde*, **Alexander Knapen***, Stephan Wong, Sebastian Feld. "Parallelizing Program Execution on Distributed Quantum Systems via Compiler/Hardware Co-Design." *Under review at ACM Transactions on Quantum Computing*.

RESEARCH PROJECTS

- **Quantum-Classical Instruction Set Architecture Design** — *Sep. 2025 - Present*
  - Exploring extensions to the RISC-V instruction set to enable high performance in hybrid programs with interleaved quantum and classical instructions
  - Approaching the instruction set design from a systems perspective, considering both high-level quantum software requirements and design implications for low-level quantum hardware architectures and controllers
- **Predecoders for Generic CSS QEC Codes** — *Jun. 2025 - Present*
  - Developing a framework which can automatically generate a predecoder, a lightweight, classical pre-processing algorithm which can decode simple, common error patterns on qubits, for any CCS-type QEC code, including color codes and bivariate bicycle codes
  - Preliminary results demonstrate on-par logical error rates when incorporating the automated predecoder into a QEC hierarchy
- **Cryogenic Hardware for Quantum Error Correction Syndrome Compression** — *Jan. 2025 - Present*
  - Developing a novel, low-power hardware algorithm to compress syndromes in the cryogenic domain before transferring them for room-temperature decoding
  - Compresses syndromes up to 48.3× ($> 14,000\times$ when combined with predecoding) and delivers up to 25.74× energy savings
- **Cryogenic Hardware Predecoder for Surface Code Quantum Error Correction** — *Sep. 2024 - Nov. 2025*
  - Designed and implemented Pinball, a cryogenic predecoder for processing significant portions of syndrome data within the dilution refrigerator

- Reduced logical error rates by nearly 1,000,000× and syndrome transmission up to 34.72× relative to prior SOTA, while increasing energy savings up to 67.4× through application-architecture-hardware codesign

- **Hardware Control Architecture for Distributed Diamond Spin Qubits (MSc. Thesis)** *Nov. 2023 - Jul. 2024*
  - Translated a quantum instruction set architecture targeting qubits in diamond NV centers into a cryogenic microarchitectural specification and implementation in SystemVerilog
  - Accelerated quantum programs up to 56.2× and reduced instruction bandwidth by designing a room-temperature-to-4 K network control interface capable of SIMD execution
  - Achieved constant cryogenic waveform memory storage overhead by developing hardware blocks to dynamically generate microwave and RF signals for arbitrary single-qubit gates

Work Experience

- **NVIDIA** *Jun. 2022 - Aug. 2022*
  Host Architecture Intern Santa Clara, CA
  - Contributed to the design, implementation, and verification of the GPU/CPU interface microarchitecture for high-performance GPUs
  - Focused on C++ functional modeling of the GPU/host interface during early-stage boot-up of the GPU

- **Intel** *Jun. 2020 - Dec. 2020, Jun. 2021 - Dec. 2021*
  Firmware Development Intern Remote
  - Supported development and validation of novel firmware versioning control on datacenter SSDs
  - Implemented firmware APIs for deploying customer-specific features in the field, performing verification on live hardware

- **imec** *Aug. 2019 - Sep. 2019*
  Research Intern Leuven, Belgium
  - Designed several metric tools for DNA quality and alignment analysis in elprep, a high-performance tool for preparing sequence alignment/map files for variant calling

Skills

- **Programming Languages:** (Proficient) Python, SystemVerilog, C/C++; (Familiar) CUDA, Rust, MATLAB
- **Frameworks & Tools:** (Proficient) Stim, Git, Slurm, Linux, Latex; (Familiar) JAX, Vivado, Synopsys Design Toolchain, ModelSim, Cadence Genus

Teaching Experience

- **EECS 479: Introduction to Quantum Computing** *University of Michigan, Fall 2025*
  - Lead lab lectures for a class of 40+ students, host weekly office hours to provide additional help with course material, and prepare weekly course material alongside course staff
  - Course topics include single- and multi-qubit quantum system and circuit representations, phase kickback, quantum algorithms, error correction, and fault-tolerant quantum computation

- **CESE 4085: Modern Computer Architectures** *Delft University of Technology, Winter 2023-2024*
  - Presented project materials, assisted students with coursework during lab sessions, and evaluated project reports
  - Course topics included instruction set architectures, pipelining/superscalar/VLIW architectures, branch prediction/speculation, multiprocessing, and memory hierarchies

- **CESE 4025: Real-Time Systems** *Delft University of Technology, Fall 2023*
  - Redesigned the course's lab component, including developing project material and evaluation rubrics
  - Implemented projects from scratch in C++, prototyped initial PCBs, and prepared design files for manufacturing

- **Mathematics Tutor** *Freelance, Cal Poly, SLO, Fall 2023*
  - Worked as a mathematics tutor in the university's tutoring program, engaging one-on-one with Cal Poly students as well as younger students in the wider San Luis Obispo community
  - Subjects ranged from middle school arithmetic to trigonometry, multivariable calculus, and linear algebra

Honors and Awards

- **Quantum Research Institute Presidential Graduate Fellowship** *University of Michigan, 2024*
  - Awarded in recognition of outstanding academic qualifications, exceptional potential for scholarly success, and contributions to the wider academic and professional communities

- **2nd Place at MIT iQuHack 2022, QuTech QKD Challenge** *MIT iQuHACK, 2022*
  - Developed a real-time chat web server called Keytanglement, using Bell State encoding and dynamic circuit configuration to securely generate keys for encrypted communications
  - Presented the design with a live demo to members of iQuISE (MIT) and QuTech (TU Delft)

Volunteer and Leadership Experience

- **UMich CSE Graduate Student Secretary** *Aug. 2025 - Present*
  - Responsible for organizing and facilitating graduate student events and interfacing between department chairs and the student body
  - Committed to engaging with and fostering a welcoming and fulfilling department environment for graduate students