Alexander Knapen

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Committed Computer Engineer

Strong expertise in quantum computing and software-hardware co-design of cryogenic electronics for quantum error correction. Utilizes strong work ethic and critical thinking to solve diverse sets of multidisciplinary problems.
Quantum Computing | Quantum Error Correction | Cryogenic Hardware Design | Computer Architecture

Education

University of Michigan, Ph.D. Computer Science and Engineering August 2024 – Present
GPA: 4.0/4.0
Honors: Quantum Research Institute Presidential Graduate Fellowship

Delft University of Technology, M.S. Computer and Embedded Systems Engineering June 2024
GPA: 8.88/10.0 (Cum Laude, 4.0 U.S. GPA equivalent)

California Polytechnic State University, San Luis Obispo, B.S. Computer Engineering June 2022
GPA: 3.98/4.0 (Summa Cum Laude, President's List)

Relevant Coursework: Hybrid Quantum-Classical Systems, Quantum Computer Architectures and Electronics, Fundamentals of Quantum Information, Computer Hardware Architecture and Design, Advanced Computing Systems

Publications

Pinball: A Cryogenic Predecoder for Quantum Error Correction Under Circuit-Level Noise. [under submission] A. Knapen*, G.Tao*, J. Mack, T. Bruno, M. Saligane, D. Sylvester, Q. Zhang, G.S. Ravi.

Hardware-Software Co-Design for Parallel Execution of Arbitrary Quantum Algorithms on Distributed Systems. [under submission] F. De Ronde*, A. Knapen*, S. Wong, S. Feld.

Skills

- Python, SystemVerilog, C/C++, CUDA, Git, Stim, Vivado, Linux

Research Projects

Cryogenic Predecoding for Quantum Error Correction **August 2024 – Present**
- Designing novel algorithms and architectures for lightweight, low-power cryogenic quantum error correction predecoders with the goal of reducing 4 K-to-300 K syndrome decoding bandwidth

NV Center Quantum Controller Microarchitecture (Master's Thesis) **November 2023 – July 2024**
- Translated quantum ISA for arbitrary single-qubit gates in diamond NV-centers into an architectural specification and implementation in SystemVerilog, designing for ultra-low-power operation at 4 K.

Temperature Characterization of Digital Components (QuTech Research Internship) **Fall 2023**
- Implemented standard digital logic blocks (MUXs, adders, multipliers) in SystemVerilog, using Cadence and CoolSPICE for transistor-level simulations to characterize power, performance, and area from 300 K down to 4 K.

Industry Experience

Host Architecture Intern, NVIDIA: **June 2022 – August 2022**
- Contributed to the design, implementation, and verification of GPU/CPU interface microarchitecture for high-performance GPUs

Firmware Development Intern, Intel: **June 2021/22 – December 2021/22**
- Supported development and validation of novel firmware versioning control on datacenter SSDs
- Implemented an API for customer-specific features in firmware, performing verification on live hardware

Research Intern, Exascience Life Lab, imec: **Summer 2019**
- Designed several metric tools for DNA quality and alignment analysis in elprep, a high-performance tool for preparing sequence alignment/map files for variant calling