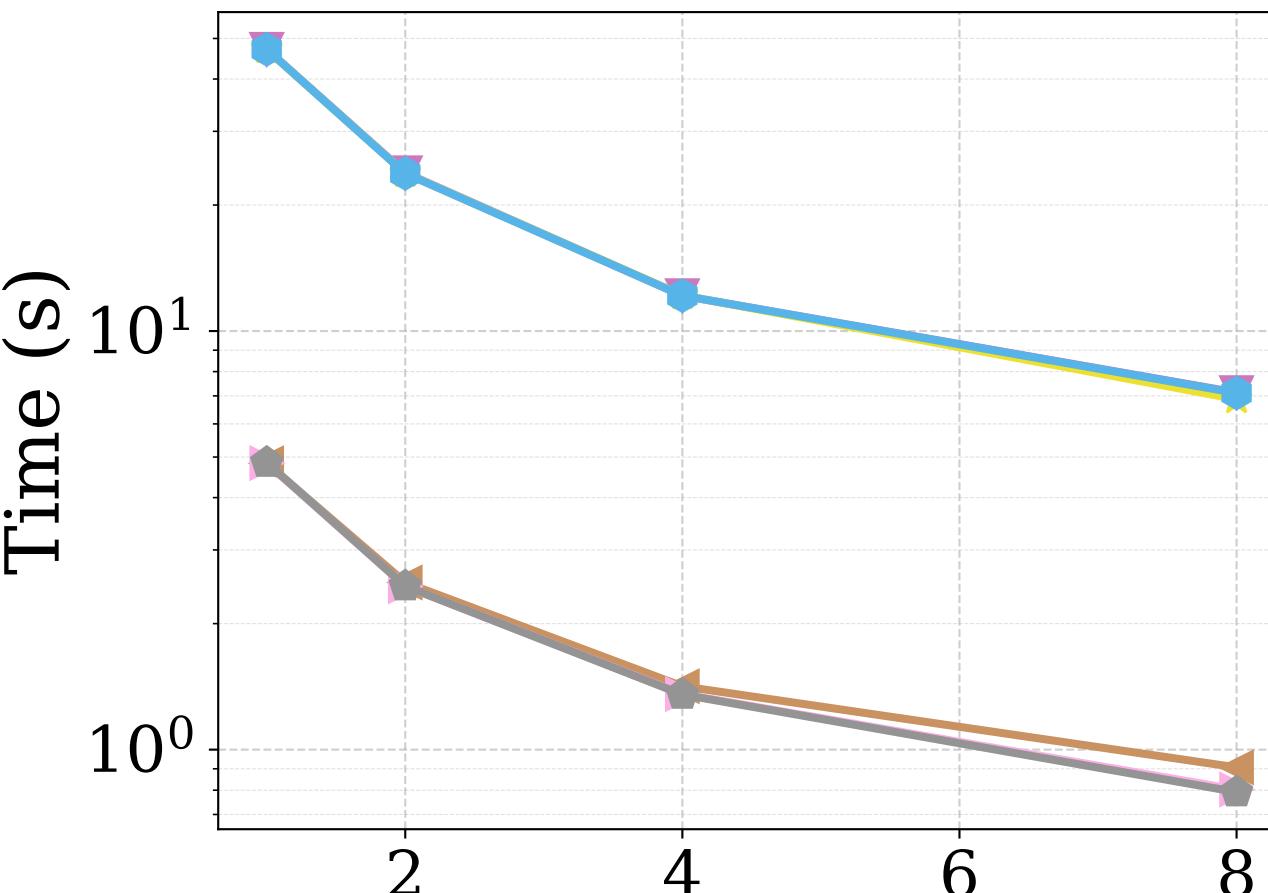
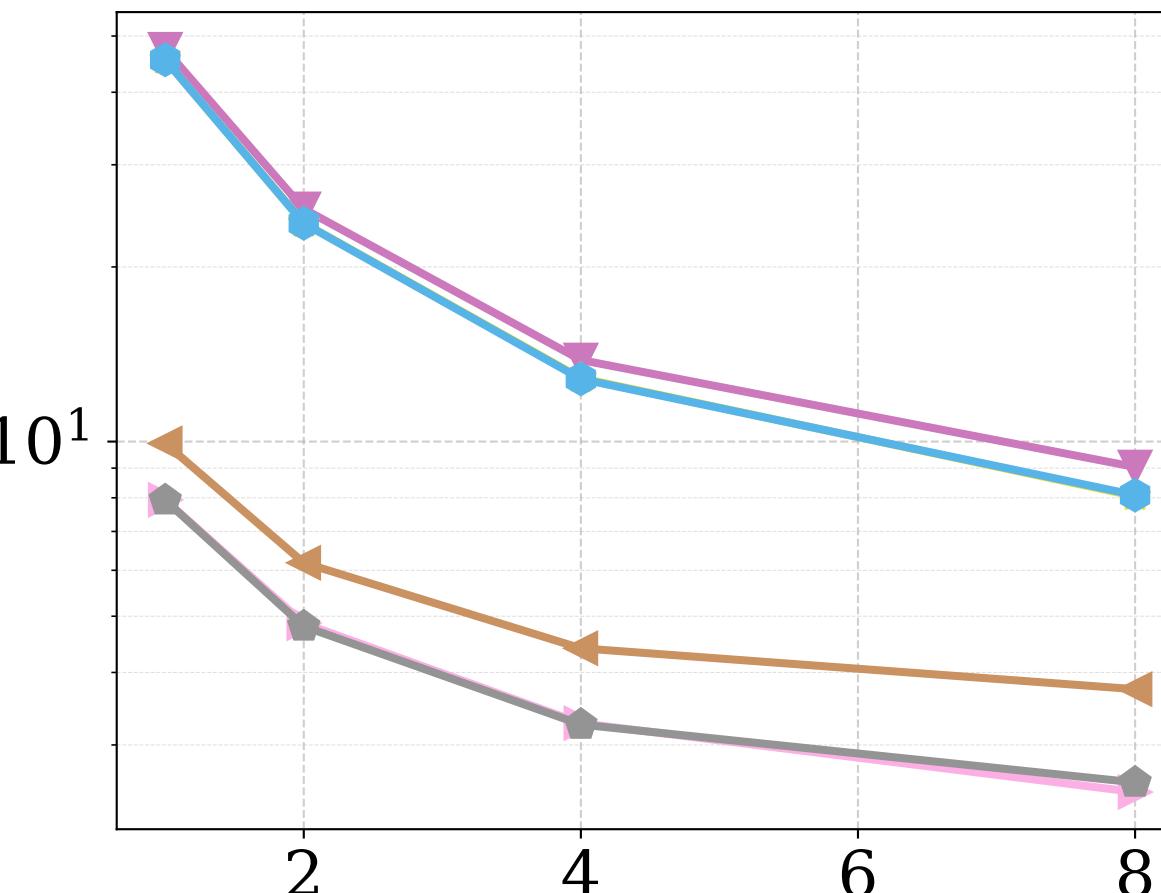


▼ CacheV2QPara → SIMDPara ★ CPara
— CacheV2SIMDQPara ◆ SIMDQPara ◆ QPara

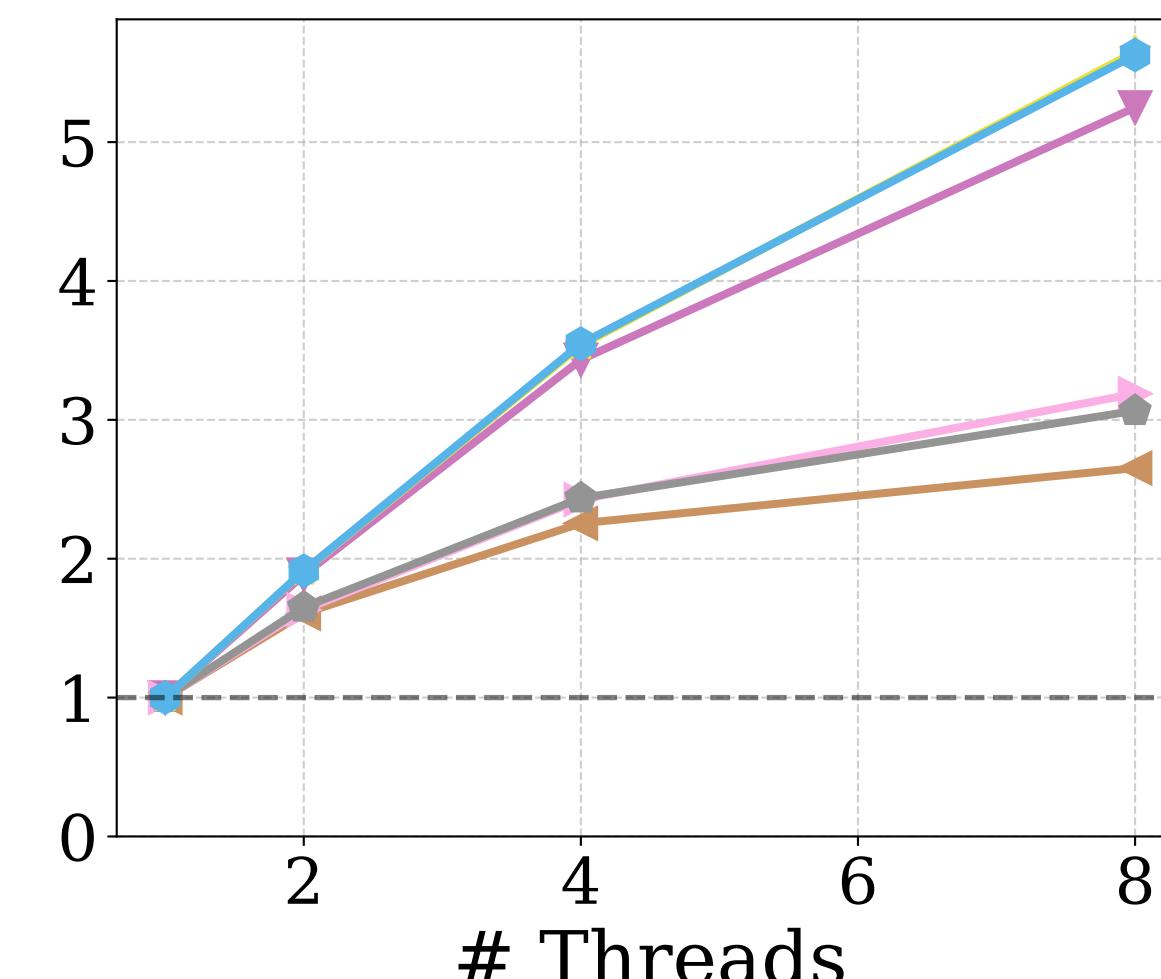
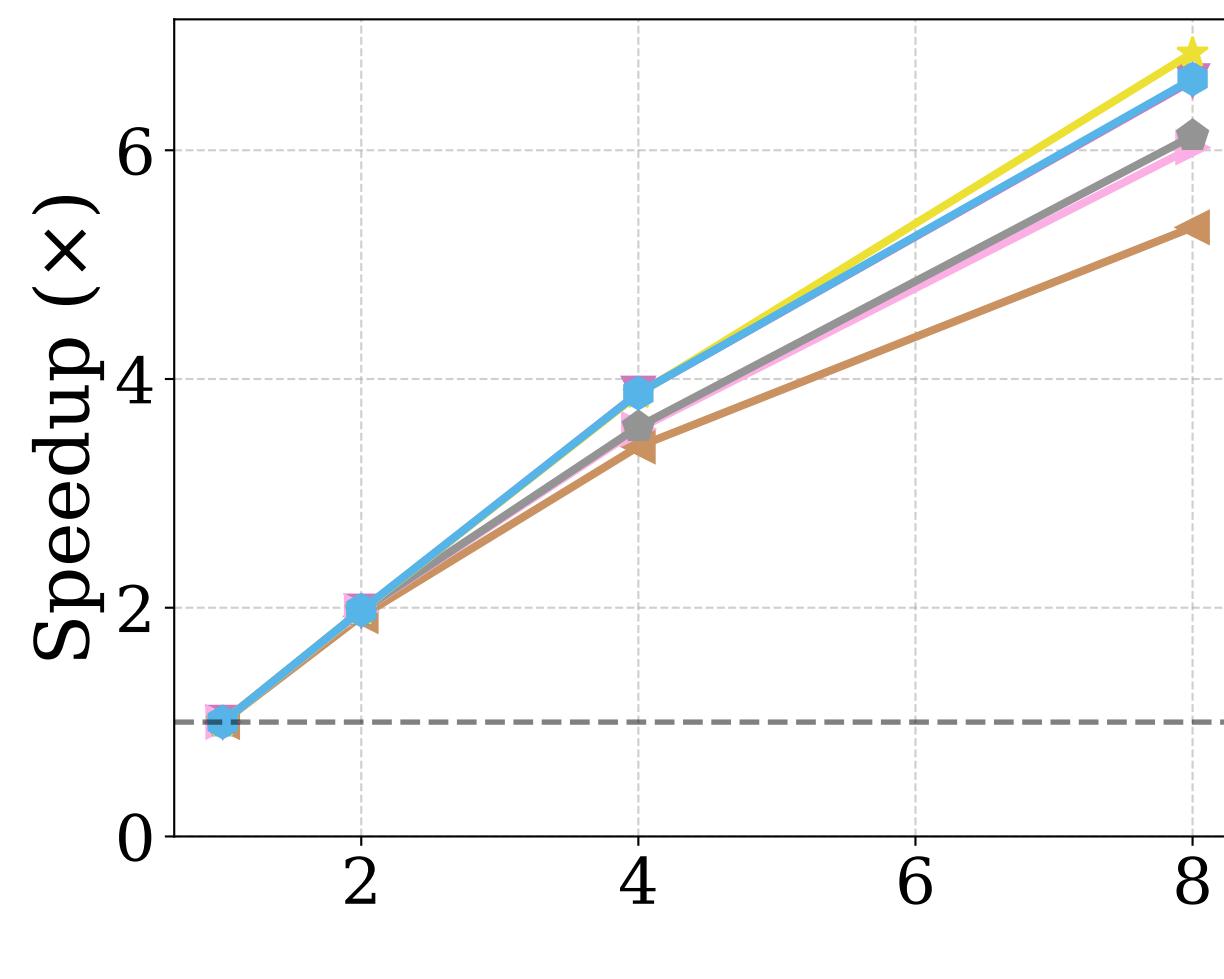
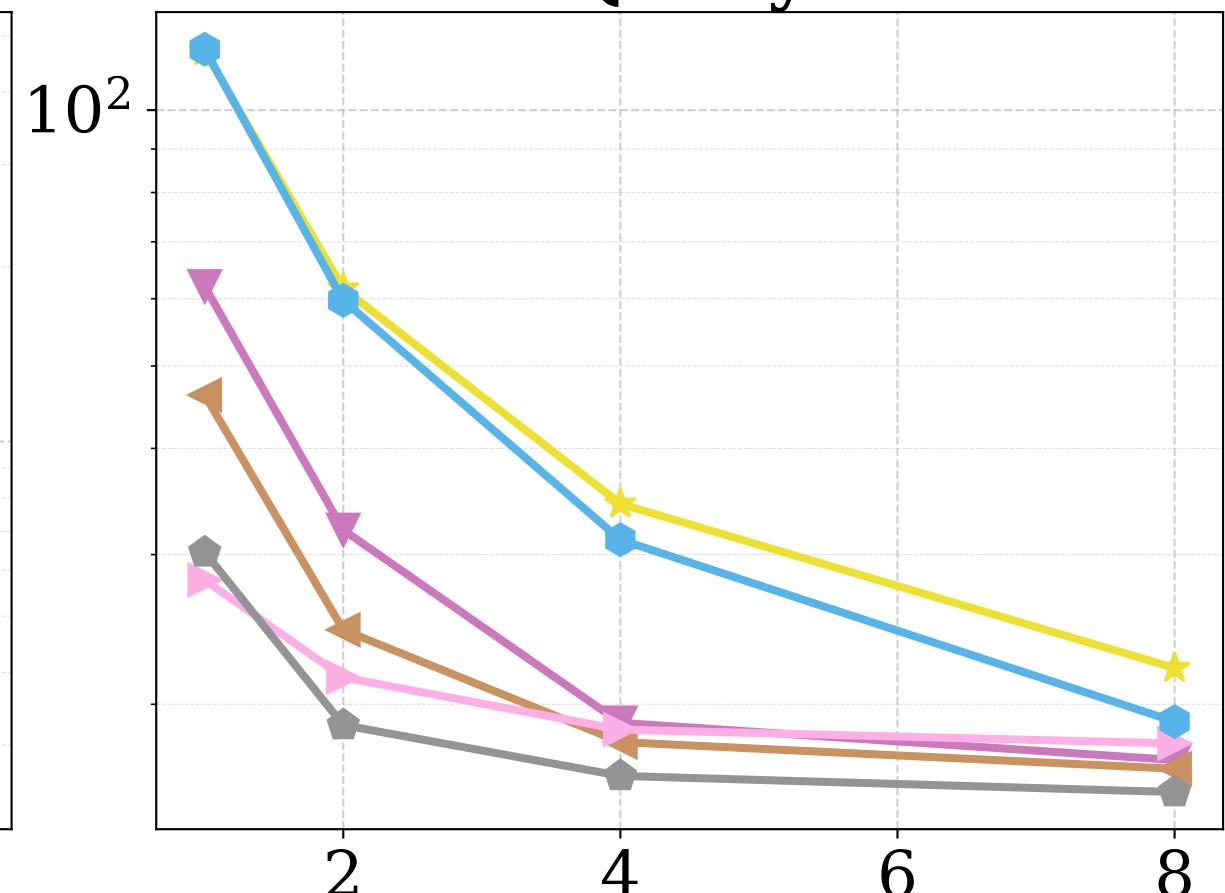
Train



Build



Query



Threads