A High Step-Down DC-DC Converter with Adequate Duty Cycle Range and High Efficiency

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This paper presents a transformerless non-isolated DC-DC converter with a high step-down voltage conversion ratio, high efficiency, and reduced current ripple. In comparison with the conventional buck converter, the proposed converter can achieve lower output voltage at a sufficiently higher duty cycle. To verify the concepts of the converter, the proposed converter topology is simulated in a PSIM environment. With a voltage conversion from 200 V to 12 V DC at 200 W, 97% efficiency was achieved.

Index terms – current ripple, dc-dc converter, high gain, non-isolated dc-dc converter, transformerless structure.

I. Introduction

The power management of many industrial applications, such as portable devices, VRM, and data centers requires reduced power loss, adequate voltage regulation, and wider voltage operation ranges. High-VCR step-down conversion is one of the key techniques to realize size- and energy-efficient power management. Conventional Buck converter is useful for low gain structures because of its simple design, low cost, and controllability, but in high VCR applications, it shows considerable disadvantages, such as low duty cycle pushed to the extreme, high power loss, and voltage stress across semiconductors [1].

To solve these problems, many different dc-dc converter topologies have been suggested. A multi-phase interleaved buck converter with a clamping capacitor [2] has a better duty cycle range and a lower current ripple. However, it increases the duty cycle only twice and is not so suitable for very high VCR. Quadratic buck converters [3] are useful to obtain a high voltage conversion ratio. Yet they suffer from high voltage stress and large inductor current ripple. Interleaved and quadratic buck converters employing coupling inductors [4] make the circuit overcomplicated affecting the duty cycle and voltage conversion ratio. Moreover, using many diodes results in higher power loss and reduced efficiency.

In this paper, a high step-down non-isolated dc-dc converter is proposed. The converter employs one input and two parallel output inductors to reduce current ripple and conduction loss. It also employs one energy-storing capacitor and one clamping capacitor, which helps extend the duty cycle. Two parallel inductors help reduce the output current ripple and inductor conduction loss, while the interleaved structure decreases the voltage stress across switches. Design techniques and the phases of operation of the proposed converter are discussed in the following sections.

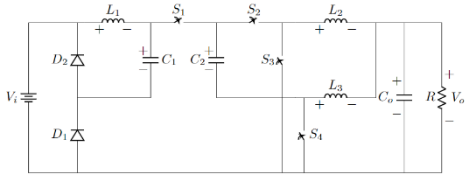

Fig.1. The topology of the proposed converter

II. Phases of operation and design procedure

The proposed dc-dc converter, shown in Fig. 1 can be considered as a combination of a quadratic buck converter (consisting of L_1C_1 filter and D_1, D_2 diodes) and an interleaved buck converter (consisting of C_2 clamping capacitor and $(L_2 \,\&\, L_3)C_o$ filter). The illustrative waveforms of the proposed converter are shown in Fig. 2

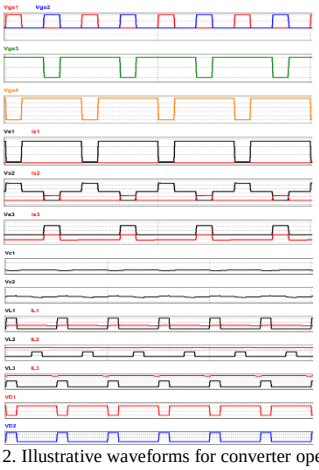

Fig. 2. Illustrative waveforms for converter operation

The converter has four phases of operation, whose respective circuits are described in Fig. 3.

Phase-1 ($t_0 < t < t_1$, $t_1 - t_0 = DT$): [*Fig. 3(a)*]

In this phase the switches, S_1 and S_3 are turned on at the time t_0, while the switches S_2 and S_4 are kept turned off. Similar to [4], the switch S_1 is connected to the inductor L_2 in series, thus it is turned on under ZCS condition. The battery charges capacitors C_1 and C_2 through the inductor L_1, along with transferring energy to the output through the inductor L_3. The second inductor L_2 also transfers its energy to the output.

$$V_{L_1} = V_{in} - V_{C_1} \quad (1)$$

$$V_{L_2} = -V_{out} \quad (2)$$

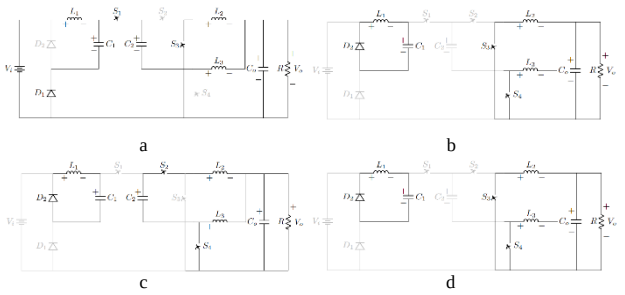

Fig. 3. The corresponding circuits of each operation phase

$$V_{L_3} = V_{C_1} - V_{C_2} - V_{out} \quad (3)$$

$$i_{L_1}(t) = i_{L_1}(t_0) + \frac{V_{in} - V_{C_1}}{L_1}, \quad i_{L_2}(t) = i_{L_2}(t_0) - \frac{V_{out}}{L_2}$$

$$i_{L_3}(t) = i_{L_3}(t_0) + \frac{V_{C_1} - V_{C_2} - V_{out}}{L_3}$$

Phase-2 ($t_1 < t < t_2, t_2 - t_1 = \frac{1-2D}{2}T$): [*Fig. 3(b)*]

The second phase starts at the time t_1, when the switch S_1 is turned off and the switch S_4 is turned on. The diode D_1 and D_2 become reverse-biased and forward-biased respectively, creating an L_1C_1 circuit in the first stage of the converter. The inductors L_2 and L_3 transfer their energies to the output.

$$V_{L_1} = -V_{C_1} \quad (4)$$

$$V_{L_2} = V_{L_3} = -V_{out} \quad (5)$$

$$i_{L_1}(t) = i_{L_1}(t_1) - \frac{V_{C_1}}{L_1}, \quad i_{L_2}(t) = i_{L_2}(t_1) - \frac{V_{out}}{L_2}$$

$$i_{L_3}(t) = i_{L_3}(t_1) - \frac{V_{out}}{L_3}$$

Phase-3 ($t_2 < t < t_3,\ t_3 - t_2 = DT$): [*Fig. 3(c)*]

The third phase starts at the time t_2, when the switch S_2 is turned on, and the switch S_3 is turned off. In this mode, the capacitor C_2 transfers its energy to the output through the inductor L_2. The inductor L_3 also gives its energy to the output.

$$V_{L_1} = -V_{C_1} \quad (6)$$

$$V_{L_2} = V_{C_2} - V_{out} \quad (7)$$

$$V_{L_3} = -V_{out} \quad (8)$$

$$i_{L_1}(t) = i_{L_1}(t_2) - \frac{V_{C_1}}{L_1}, \quad i_{L_2}(t) = i_{L_2}(t_2) + \frac{V_{C_2} - V_{out}}{L_2}$$

$$i_{L_3}(t) = i_{L_3}(t_2) - \frac{V_{out}}{L_3}$$

Phase-4($t_3 < t < t_4,\ t_4 - t_3 = \frac{1-2D}{2}T$):[*Fig. 3(d)*]

The fourth phase is identical to the second phase except for the initial values of inductor currents. Therefore, the operation does not differ.

According to the volt-second balance on the inductors, we can derive the capacitor voltages and voltage gain:

$$V_{C_1} = DV_{in},\ V_{C_2} = \frac{1}{2}DV_{in}$$

$$M = \frac{V_{out}}{V_{in}} = \frac{D^2}{2} \quad (9)$$

The values of the components for the converter design are listed in Table 1. Table 2 includes the voltage stress across semiconductor devices. At the nominal output power, 200 W, 97% efficiency (Fig. 4), and a very low 0.03% (Fig. 6) output voltage ripple are achieved. The peak efficiency of 98.9% (Fig. 5) occurs at 200 V / 20 V voltage conversion. Compared to the conventional Buck converter and [2 - 4], the proposed converter topology has better VCR over the adequate range of duty cycles.

Parameters	Specifications
Input / Output voltage	200 Vdc / 1 Vdc
Continuous load (P_{out})	200 W
Switching frequency (f_{sw})	1 MHz
Inductor (L_1)	70 μH
Inductors (L_2, L_3)	10 μH
Capacitors (C_1, C_2, C_o)	20 μF
Optimal Duty Ratio (D)	0.346
D_1, D_2 (V_F)	0.8 V

Table 1. Design specifications

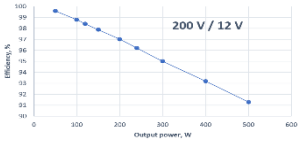

Fig. 4. Efficiency vs. Output power profile

Switching elements	Voltage stress
Switch S_1	$(1 + D/2)V_{in}$
Switch S_2	$3DV_{in}/2$
Switch S_3, S_4	$DV_{in}/2$
Diode D_1, D_2	V_{in}

Table 2. Semiconductor voltage stress

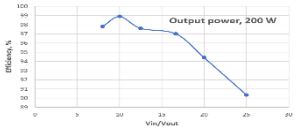

Fig. 5. Efficiency vs. voltage gain (200W)

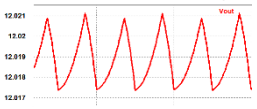

Fig. 6. Output voltage

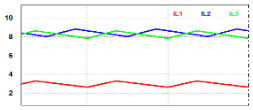

Fig. 7. Inductor currents

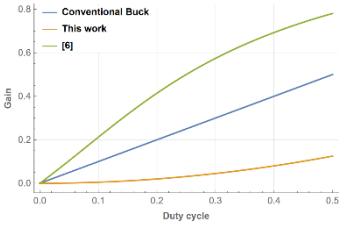

Fig. 8. The comparison of "gain vs. duty cycle" with other topologies

III. Conclusion

In this article, a high-gain non-isolated dc-dc converter topology and its operation are proposed and discussed. In terms of efficiency, voltage gain, and output voltage ripple, the converter shows a better performance compared to the conventional Buck, quadratic, and interleaved converters. The converter is tested at a 1 MHz switching frequency with 200 V / 12 V. At 200 W output power, it achieves 97% efficiency, outperforming prior works with coupled inductors with higher efficiency, better duty cycle range, and simpler design without the use of coupled inductors.

IV. Acknowledgement

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IV. References

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