BRAC UNIVERSITY

Department of Computer Science and Engineering

Examination: Quiz 4 Duration: 30 min

Semester: Summer 2025 Full Marks: 15

CSE 321: Operating Systems

Name: **ID:** **Section:**

1. During TLB search, the associative lookup time (ε) is 15ns and hit ratio (α) is 90%. For each time memory access, 100ns is needed. Calculate the effective access time, and compare it to the access time without TLB. [3]

Answer:

With TLB
0.9 * (115) + 0.1 * (215) = 125

Without TLB
100 + 100 = 200
So, with TLB, we get faster access time.

2. A process runs on a system with single-level paging. [4]
   Logical address size: 8 bits (byte-addressable)
   Page size: 32 bytes
   Main memory size: 512 bytes
   1.Determine the number of offset bits and page-number bits in the 8-bit logical address.
   2.Compute the number of pages in the process's logical space.
   3.Compute the number of frames in main memory.
   4.State the size (in bits) of a physical address in this system.

Answer:

1. Address: 8 bits, i.e. m = 8
Page size: 32 bytes or 2^5, so n = 5

Offset bits = 5 bits
Page number bits = 3 bits

2. 2^3 = 8 pages, or 2^8/2^5 = 2^3 = 8 pages

3. 512/32 = 16 frames

4. 512 = 2^9, so 9 bits for physical address

3. Use the bit split derived in Question 2 and the following Page Map Table (PMT). Frames are numbered 0–15. [8]

   For each logical address below, compute the corresponding physical address, or report a page fault if the page is invalid.

   14, 47, 98, 165, 201, 250

Page#	Frame#	Valid/Invalid
0	10	V
1	3	V
2	-	I
3	14	V
4	1	V
5	-	I
6	7	V
7	15	V

Logical Address	**Page (3-bits)**	**Offset (5-bits)**	**Frame #**	**Valid/Invalid**	**Physical Address**
14	0	14	10	Valid	334
47	1	15	3	Valid	111
98	3	2	14	Valid	450
165	5	5	—	Invalid	Page Fault
201	6	9	7	Valid	233
250	7	26	15	Valid	506