Assignment 1

Name: Md. Sabbir Akon

ID : 22301242

Section: 12

Ans to the Q.S No. 1

"Performance vs Prediction" involves improving a computers performance by anticipating future operations. This includes techniques like branch prediction on memory prefeteling where the system guesses the next instruction or data access. Accurate predictions help avoid delays, keeping the processor pipeline efficient and speeding up execution.

Ans to the Q.S No. 2

a) Amdahl's law describes how much a system's performance can improve by optimizing a specific part of it. The speedup is constrained by the fraction of the task that remains unaffected. No matter how much the optimized part improves, the unchanged portion limits the overall performance gain.

b) Amdahl's Laws connect closely with the design principle "Make the common case faster" because it highlights the importance of optimizing the most frequently used parts of a system to achieve the highest performance gains.

Ans to the Q.J No. 3

Wafen radius = 50cm

Die height = 0.1 cm

width = 0.2cm

∴ Wafen area = $\pi \times 50^2 = 7854 cm^2$

die " = $0.1 \times 0.2 = 0.02 cm^2$

∴ Dies per wafen = $\frac{7854}{0.02}$ = 392700 dies

∴ usable dies = $392700 \times \frac{65}{100} = 255255$

∴ total cost per die = 255255×5.505

= 1428151.725

∴ cost of 1570 dies = $\frac{1428151.725 \times 1570}{255255}$

= 8784.5

Adjusted total price increased to 12293.1

∴ Company selling price = 7.83 + 5 = 12.83

∴ Cost for total 1570 dies = 1570×12.83

= 20143.1

∴ Company profit = 20143.1 − 12293.1

= 7833

Ans to the Q.S No. 4

a) Total number of instructions are 18.

b)

$$\text{Average CPI} = \frac{(8\times2)+(5\times3)+(3\times4)+(2\times5)}{(8+5+3+2)}$$

$$= 2.94$$

Given,

Clock cycle duration = 3s

∴ Execution time = $18 \times 2.94 \times 3$

$= 158.76$ sec.

c)

$$\text{Clock rate} = \frac{1}{\text{clock dur.}} = \frac{1}{3} = 0.33 \text{ Hz}$$

d) I'll choose to add instruction to speed up, Here, add instruction is the most used instructim. So, if I optimized it, the system will be mone fasten.

e) CPU time = 158.76 sec

Now, $T_{improved} = \frac{158.7}{1.2} = 132.3$ sec

$T_{affected} = IC_{add} * \text{Avg CPI} \times \text{Clock dun.}$

$= 70.66$

∴ $T_{unaffected} = 158.76 - 70.66 = 80.11$.

$$\therefore T_{improved} = \frac{70.66}{n} + 88.11$$

2) $n = 1.6$

$\therefore$ Improvement factor is 1.6.

Ans to the Q.S No. 5

a) To know which type of istruction is performed and also which type of instruction format is performed, we look at the opcode field.

Ans to the QS No. 6

LD X_9, $10[X_{21}]$

Moving data from memory to registers,

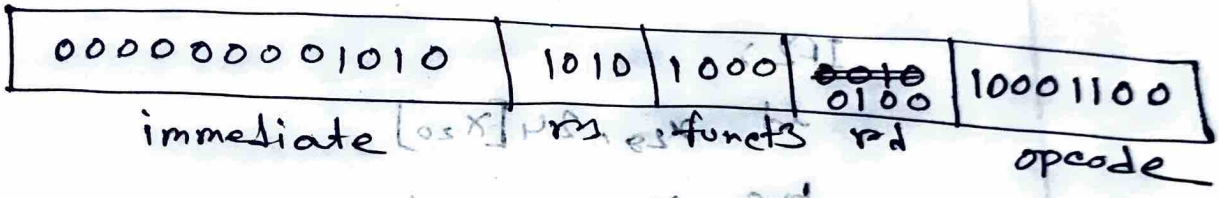
Data Size	Events
64 bits	000
32 bits	001
16 bits	010
8 bits	011

Moving data from register to memory: -

Data size	Funct3
64 bits	010
32 bits	011
16 bits	001
8 bits	000

machine code:

[I type] :



Ans to the Q.S No. 2

Program counter is a CPU register that stores the address of the next instruction to execute, ensuring sequential execution.

example:

```
addi   r1, r1, 5
addi   r2, r2, -1
beq    r2, zero, Exit
```

Ans to the Q.5 No. 8

a)

```
IF1:
    ld   x5, 24 [x20]
    ld   x6, 48 [x20]
    beq  x5, x6, else1
IF2:
    ld   x28, 24 [x20]
    bne  x0, x28, else2
    addi x20, x28, 2
    sd   x20, 24 [x20]
    beq  x0, x0, exit
else1:
    ld   x22, 48 [x20]
    slli x22, x22, 3
    sd   x22, 48 [x20]
    beq  x0, x0, exit
else2:
    ld   x23, 48 [x20]
    slli x23, x23, 4
    sd   x23, 48 [x20]
    beq  x0, x0, exit
exit:
```

b) ld x_5, 24(x_{20})

000000011000	10100	xxx	00101	xxxxxxx

ld x_6, 48(x_{20})

000000110000	10100	xxx	00110	xxxxxxx

ld x_{28}, 24(x_{20})

000000011000	10100	xxx	11100	xxxxxxx

addi x_{29}, x_{28}, 2

000000000010	11100	xxx	11101	xxxxxxx

sd x_{29}, 24(x_{20})

0000000	11101	10100	xxx	11000	xxxxxxx

ld x_{22}, 48(x_{20})

000000110000	10100	xxx	10110	xxxxxxx

slli x_{22}, x_{22}, 3

000000000011	10110	xxx	10110	xxxxxxx

sd x_{22}, 48(x_{20})

0000001	10110	10100	xxx	10000	xxxxxxx

ld x_{23}, 48(x_{20})

000000110000	10100	xxx	10111	xxxxxxx

- srli x_{23}, x_{23}, 4

sd x_{23}, 48(x_{20})