

InGaAs/InP Single-Photon Avalanche Diode With Reduced Afterpulsing and Sharp Timing Response With 30 ps Tail

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Abstract—In this paper, we present the design, fabrication, and experimental characterization of a new Single-Photon Avalanche Diode (SPAD) made in InGaAs/InP for photon-counting operations up to 1700 nm. Working in gated-mode at 225 K with 5 V excess bias, this detector shows very low afterpulsing, hence the hold-off time can be set as low as a few microseconds, thus allowing high photon-counting rates (towards 1 Mcps). The timing response has a full-width at half maximum of less than 90 ps and a full-width at 1/1000 of maximum of less than 450 ps, thanks to a very fast (30 ps) exponential tail, thus allowing extremely wide dynamic ranges in time-correlated single photon counting measurements. Furthermore, such InGaAs/InP SPAD shows good photon detection efficiency (>25% at 1550 nm and 40% at 1000 nm) at a moderately low dark count rate, below 100 kcps for a 25 μm active-area diameter detector. These good results are due to design and fabrication optimization.

Index Terms—Afterpulsing, near-infrared detector, photons counting, single-photon avalanche diode (SPAD), timing jitter.

I. INTRODUCTION

SINGLE-PHOTON detectors are employed in a wide range of applications that require high detection efficiency with single-photon sensitivity and very sharp time resolution. Different kinds of detectors for single-photon counting in the short-wave infrared (SWIR) wavelength range are available, such as photomultiplier tubes (that have wide active areas, but have low detection efficiency, require high bias voltages and are mounted in large housings) [1] or superconducting single-photon detectors (that have low dark count rate, good detection efficiency and very low timing jitter, but require bulky cooling systems) [2].

Single-Photon Avalanche Diodes (SPADs) have the distinctive advantages of solid-state detectors (small size, low bias, low power consumption and reliability) and are frequently the best choice for applications that require high detection efficiency, very good timing resolution and ease of operation [3]. InGaAs/InP SPADs are used for single-photon counting and timing in the SWIR wavelength range (up to 1700 nm) [4]–[6]. In recent years, the design and fabrication of such photodetectors have improved, thus leading

to better-performing detectors, specifically, lower dark-count rate and less afterpulsing [6]. However, afterpulsing still limits the wide deployment of InGaAs/InP SPADs in many scientific and industrial applications because it limits the maximum count rate by requiring long hold-off times (tens or even hundreds of microseconds) after each avalanche ignition. Several complex front-end electronics have been developed [7]–[10] to limit the trapping of carriers, and hence afterpulsing, as much as possible. Nevertheless InGaAs/InP growths and semiconductor processing quality is still the limiting factor for both afterpulsing and dark count rate, therefore both design and fabrication technology must be improved to reach far better performance.

In this paper, we present the performance of the InGaAs/InP SPAD that we designed and fabricated to allow high count rates and extremely sharp timing performance. Section II describes the InGaAs/InP SPAD internal structure and the main design criteria. Section III briefly details the manufacturing process. Finally, Section IV reports an analysis of the SPAD performance.

II. DEVICE STRUCTURE

InGaAs/InP SPADs are typically made in a separate absorption, grading, charge and multiplication (SAGCM) heterostructure, composed by different layers, as shown in Fig. 1. The structure, introduced for linear-mode Avalanche PhotoDiodes (APDs) [11]–[14], guarantees a sufficiently high electric field in the InP multiplication region, thus enabling avalanche multiplication, while keeping a low electric field in the InGaAs absorption region in order to avoid tunneling in that lower energy-gap layer.

While InGaAs/InP SPADs and APDs share similar layer structures, there are important differences in the design criteria: 1) the positive feedback in the avalanche process (hence comparable ionization coefficients of holes and electrons in InP) is no more a drawback for SPADs, instead it must be exploited for attaining Geiger-mode operation; 2) peripheral leakage, which significantly increases the dark current in linear mode APDs, is not multiplied (i.e. it does not trigger an avalanche process) and, therefore, it does not contribute to the SPAD dark count rate [15]; 3) SPADs are designed to operate above the breakdown voltage and at relatively low temperature (about 230 K), therefore the electric field must be tailored in those conditions and not at room temperature.

Manuscript received March 23, 2012; revised June 7, 2012; accepted July 1, 2012. Date of current version July 24, 2012.

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Digital Object Identifier 10.1109/JQE.2012.2208097

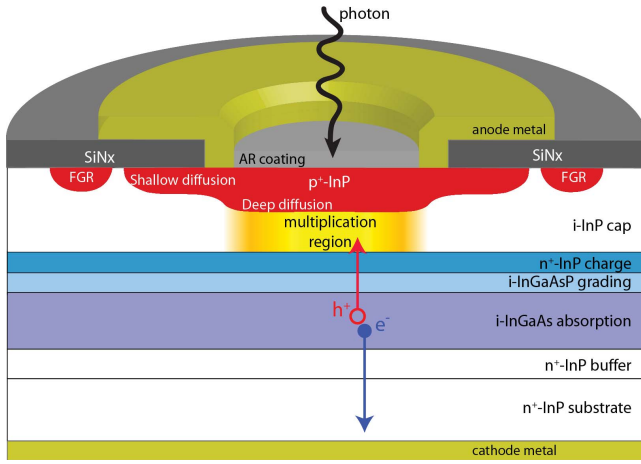


Fig. 1. Cross section of the front-illuminated InGaAs/InP SPAD.

We designed a planar front-illuminated detector with a 200 nm SiN_x anti-reflection coating layer optimized for 1550 nm (SiN_x dielectric constant is ~ 1.94 at 1550 nm) and an absorbing $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer ($E_G \sim 0.75$ eV at 295 K), whose thickness ($> 1 \mu\text{m}$) is designed to provide an absorption efficiency higher than 50% at 1550 nm. The photogenerated electron-hole pair is separated by the electric field: the hole is drifted to the InP multiplication region ($E_G \sim 1.35$ eV at 295 K, thickness $> 1 \mu\text{m}$), where it can trigger a self-sustaining avalanche process in response to a single photon. The intensity and shape of the electric field in the multiplication region are tailored to yield an avalanche triggering probability greater than 50% when the SPAD is biased at least 5 V above the breakdown voltage. Between the absorption and the multiplication regions a thin and highly doped InP charge layer allows to keep high electric field only in the multiplication region. An InGaAsP graded layer (thickness < 100 nm) avoids hole pile-up at the InGaAs - InP heterointerface, reducing transit time of photogenerated holes and hence the overall timing jitter in acquiring photon arrival times.

The confinement of the high electric field in the active area is achieved by means of a double p-type diffusion made by deep and shallow Zn diffusions [16]. The latter has a wider diameter for reducing the electric field peaking at the edge of the active area, which would lead to premature edge breakdown. In order to have a good uniformity of the electric field in the active area for achieving low timing jitter and uniform sensitivity [17], we adjusted the difference in depth and in diameter of the two Zn diffusions. In detail: 1) the depth of shallow diffusion was designed to guarantee difference of at least 10 V in the breakdown voltage between the active area and the surroundings; 2) the diameter of the shallow diffusion is designed to have a difference of less than 3% between breakdown voltage in the center and at the edge of the active area. Besides the double Zn diffusion, floating guard rings (FGR) are added in order to better control the electric field uniformity both in the center and in the periphery of the active area.

On top of the SPAD, the anode metallization is made over the shallow diffusion and acts also as a pinhole for incoming photons, with a diameter equal to the active area.

III. FABRICATION OF InGaAs/InP SPADs

The epitaxial layer structure was grown on a (100) n-doped InP wafer by metal-organic chemical vapor deposition (MOCVD). Since the electric field profile should be as flat as possible in both absorption layer and cap layer, they are intentionally left un-doped, eventually resulting in very low level n-type doping. In order to provide a very sharp transition between multiplication and absorption layers, the InP charge layer was made thin (< 100 nm) and highly doped ($> 10^{17} \text{ cm}^{-3}$).

The p-type profile defining the p-n junction results from two subsequent zinc diffusions, performed in the MOCVD reactor with different SiN_x masks. In order to achieve good uniformity in the active area, we analyzed the Zn diffusion process and we adjusted the diffusion temperature, the partial pressure of carrier gases and the diffusion times with trial and error method.

IV. MEASUREMENTS RESULTS

We characterized the $25 \mu\text{m}$ active area diameter InGaAs/InP SPAD in gated mode with a passive quenching circuit, as shown in Fig. 2. During the gate-OFF period (T_{OFF}) the device is biased 0.5 V below the breakdown voltage, whereas during the gate-ON period (T_{ON}) it is turned ON with a bias voltage of some volts above breakdown. During T_{ON} , the difference between overall bias and breakdown voltage is usually named excess bias, V_{EX} .

The main drawback of gated-mode operation is that the fast (in the nanosecond or even sub-nanosecond ranges) rising and falling edge transitions generate large capacitive transients that can couple to the output line (see Fig. 2) thus, eventually, impairing the time resolution of the acquired waveform or also limiting the ability to detect an avalanche [18]. Since the time jitter of the SPAD improves at low avalanche detection thresholds [19], we suppressed such capacitive feed-through employing a technique based on a “dummy” path, which mimics the spurious spikes, and a differential comparator, which then detects just the useful avalanche triggering, as reported in [7].

A. Primary Dark Count Rate

The primary dark count rate (DCR) in InGaAs/InP SPADs is due to thermal generation through deep-levels and electric-field assisted tunneling processes, either band-to-band or trap-assisted. Thermal generation is typically dominant at high temperatures and is stronger in InGaAs depleted region because of the lower energy-gap. Instead, tunneling is typically the main noise source at low temperatures and at high electric fields, i.e. at high excess bias [5], in the InP multiplication layer, provided the electric field in the InGaAs layer is kept low (below about 120 kV/cm).

We measured the primary DCR of several SPADs with gate-OFF periods long enough ($500 \mu\text{s}$) to completely rule out afterpulsing. We applied excess bias between 2 V and 7 V, corresponding to 3% and 10%, respectively, of the breakdown voltage, which is about 65 V at 225 K. Fig. 3 shows that primary DCR are moderately low below 225 K.

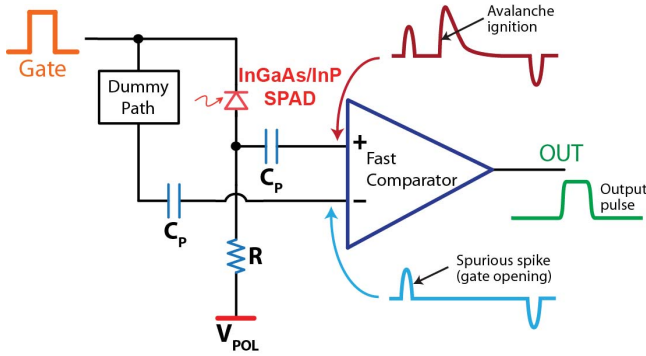


Fig. 2. Front-end circuit used to detect the avalanche signal from the InGaAs/InP SPAD operated in gated-mode.

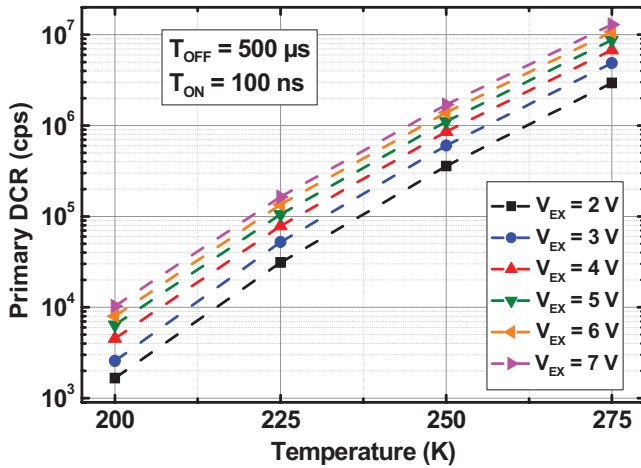


Fig. 3. Primary DCR as a function of operating temperature, at different excess bias voltages.

This temperature can be easily achieved with thermo-electric coolers mounted inside compact packages, thus paving the way to practical and cost-effective exploitation of these detectors in SWIR applications. As an example, at 5 V excess bias and 225 K, the primary DCR is about 100 kcps, while it reduces to about 6 kcps at 200 K.

The quite strong dependence of DCR on temperature and the low dependence on excess bias suggest that the dominant source of dark counts is thermal generation in the InGaAs layer, over the entire temperature range explored here. Therefore, the quality of the InGaAs in fabricated SPADs (in terms of defects and impurities concentrations) can be improved further. On the other hand, the growth conditions of InP cap layer lead to good quality (i.e. low defect and impurity concentration) of the multiplication layer, guaranteeing a small contribution to the dark counts from such high field region.

B. Afterpulsing

During each avalanche, a large number of charge carriers flow through the multiplication region. Some of these carriers get trapped by deep-levels and are then released with exponential time decays. If a carrier is de-trapped during a subsequent gate-ON period, it can trigger an avalanche, thus giving birth to an unwelcome ignition, a so-called afterpulse. A simple way to reduce afterpulsing is to keep the SPAD

OFF for a sufficiently long time after each avalanche: the drawback is a corresponding reduction of the maximum count rate, given by $1/T_{\text{OFF}}$.

Fig. 4 shows the dependence of DCR on T_{OFF} . With a gate-ON time of 20 ns, the afterpulsing is barely visible only at high excess bias ($>5\text{V}$) even when T_{OFF} is as short as $1\text{ }\mu\text{s}$ (corresponding to a maximum count rate of 1 Mcps). Such behavior is remarkably good and is much better than what reported in literature on similar detectors operated with equivalent circuits [5], [8]. As a comparison, in [5] the afterpulsing is visible at T_{OFF} shorter than $10\text{ }\mu\text{s}$ when gate-ON time is 20 ns. When increasing T_{ON} to 100 ns, afterpulsing becomes more evident as shown in Fig. 5, where DCR increases when $T_{\text{OFF}} < 10\text{ }\mu\text{s}$ and $V_{\text{EX}} > 4\text{V}$. Since the amount of carriers trapped in each avalanche does not depend on the gate-ON duration thanks to the passive quenching, the reason of such increase is the higher probability of releasing trapped carriers within the gate-ON period.

As already shown in literature [8], [9], [20], [21], afterpulsing can be reduced by limiting the number of carriers per avalanche with very fast quenching circuits. Instead, for the characterizations reported in the present work we employed a simpler circuit, like the one previously used for the measurements reported in [22] on state-of-the-art detectors: the gate pulse is applied to the cathode, the quenching is passive ($R = 47\text{ k}\Omega$) and the avalanche is read from the anode by $C_P = 8.2\text{ pF}$ connected to ground through a $50\text{ }\Omega$ resistor (integrated in the comparator). We estimated that the SPAD capacitance is about 0.7 pF and that the avalanche charge is in the range $30\text{--}40\text{ pC}$, while the charge for the measurements reported in [22] was lower than 30 pC , smaller because of lower SPAD series resistance. Therefore, despite higher avalanche charge, the SPAD here described has lower afterpulsing because of fewer deep levels in the multiplication region. Such result is due to good control of the fabrication process, i.e. the InP growth temperature and rate are optimized on the basis of some preliminary trials. We expect even better afterpulsing suppression also at longer gate-ON durations when fast quenching circuit (see [7]) are employed. Finally, approaches like sinusoidal gating can strongly reduce the avalanche charge thus lowering the afterpulsing but with very short ON duration (less than 1 ns) [23], [24].

C. Photon Detection Efficiency

For measuring the photon detection efficiency (PDE), we employed a broad-band light source, a monochromator, an integrating sphere and optical filters. As a reference, we used a calibrated power meter with an InGaAs detection head. We scanned from 800 nm to 1700 nm at 50 nm steps. Fig. 6 shows the photon detection efficiency measured at 200 K : at 1550 nm the SPAD provides a $\text{PDE} > 25\%$ at $V_{\text{EX}} = 5\text{ V}$, whereas at 1000 nm PDE reaches 40% and it is still about 2.5% at 1700 nm .

D. Timing Jitter

Timing jitter is an important SPAD parameter, which results in a spread of the measured delay time between photon

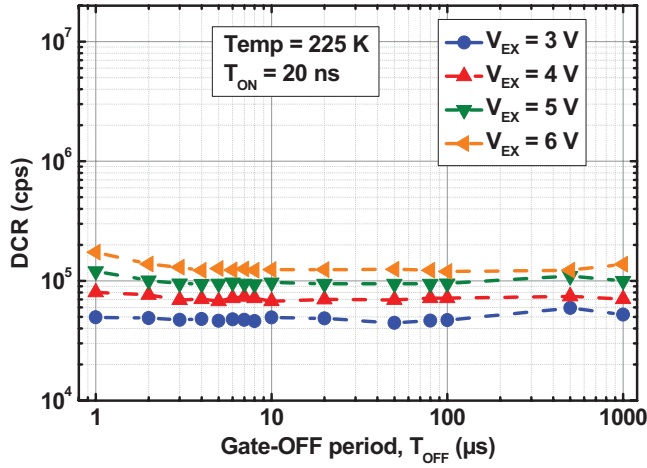


Fig. 4. Dark count rate as a function of gate-OFF period, with a gate-ON time of 20 ns. Note that afterpulsing is very low.

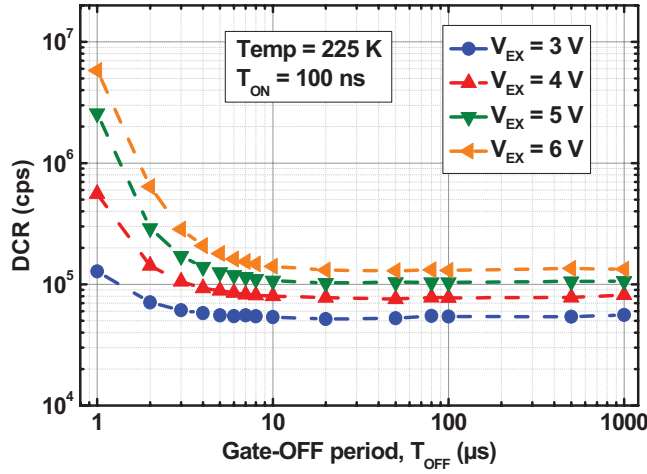


Fig. 5. Dark count rate as a function of gate-OFF period, with a gate-ON time of 100 ns. Afterpulsing (leading to DCR increase) is visible at short T_{off} ($<10 \mu\text{s}$) and high excess bias.

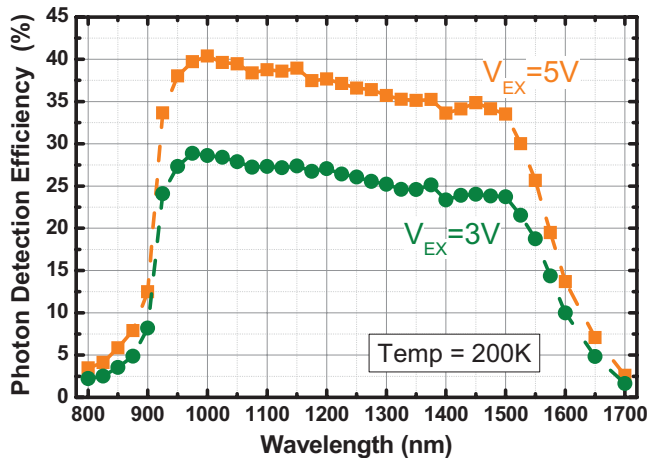


Fig. 6. Photon detection efficiency of the InGaAs/InP SPADs at different excess bias voltages and at 200 K.

absorption and avalanche current detection by means of the front-end circuitry. It is usually measured by the Full-Width at Half Maximum (FWHM) of the arrival time distribution of photons, coming from a very sharp pulsed laser excitation.

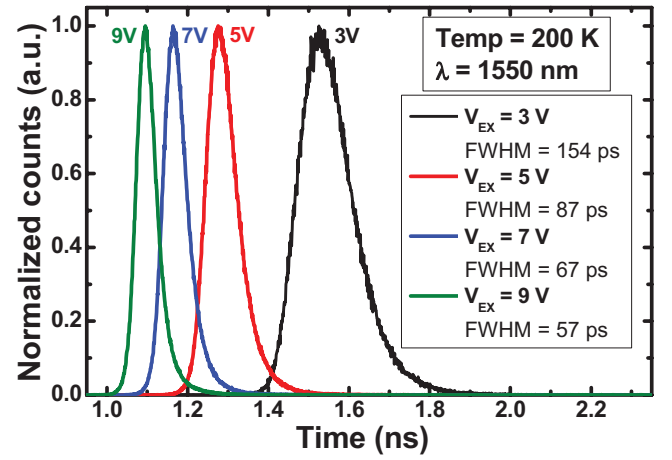


Fig. 7. Normalized timing response distributions of the InGaAs/InP SPADs at different excess bias voltages and at 200 K.

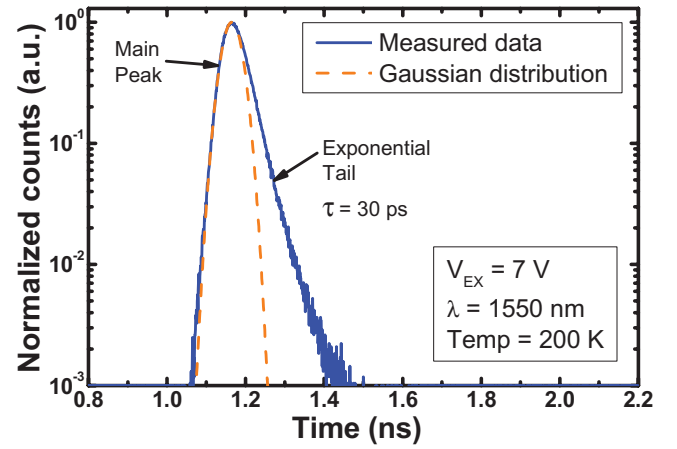


Fig. 8. Timing response distribution on a logarithmic scale, at 7 V excess bias. The response closely approaches a Gaussian distribution with standard deviation $\sigma = 25 \text{ ps}$, plus a minor exponential tail with a time constant of 30 ps.

We employed a pulsed laser at 1550 nm with a FWHM of about 20 ps. The light illuminates the entire SPAD area, including surrounding metallization. We measured the timing response at 200 K at different excess bias. As shown in Fig. 7, the time jitter is very good and decreases as the excess bias increases, from about 87 ps at 5 V excess bias and about 57 ps at 9 V. Moreover, it can be noted that even with low excess bias ($<3 \text{ V}$), the FWHM is still about 150 ps. Such values are very good when compared to what reported in literature [5], [6], [23], [24].

Furthermore, the new InGaAs/InP SPAD shows very “clean” timing response, approaching a Gaussian distribution, with neither secondary peaks nor slow “tails” [17]. As an example, Fig. 8 shows in a log scale the time response at $V_{\text{EX}} = 7 \text{ V}$: 1) the main peak response can be fit by a Gaussian distribution with standard deviation $\sigma = 25 \text{ ps}$; 2) the exponential tail is very fast, with a time-constant of about 30 ps. Such characteristics are very important in applications where optical waveforms have to be acquired with high time resolution and with very wide dynamic range. In fact, the full width at 1/1000 of the maximum is about 360 ps, very much superior to any

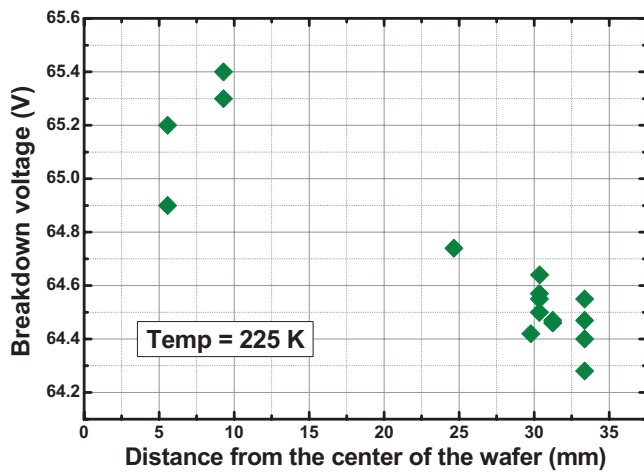


Fig. 9. Breakdown voltages of several SPADs from the same wafer, as a function of their position.

InGaAs/InP SPAD response so far reported. At 5 V excess bias the FWHM is 87 ps and the full width at 1/1000 of the maximum is about 450 ps.

E. Across-Wafer Variations

We measured nearly uniform breakdown voltage distribution of SPADs across the wafer, proving good center-to-edge uniformity of growths and diffusion processes. Fig. 9 shows the measured breakdown voltages of several SPADs from different positions in the wafer: the variation from the center to the edge is about 1.5 % (i.e. 1 V). We also crosschecked that layer thicknesses, doping levels and diffusion depths show very small variations.

V. CONCLUSION

We described the performance characterization of InGaAs/InP SPAD we designed and fabricated. This new single photon detector shows low afterpulsing, allowing the maximum count rate to reach at least 1 Mcps, better than what reported in literature on similar detectors operated in equivalent conditions (i.e. with gate-ON time of tens of nanoseconds). The new SPAD provides very good and sharp timing response, with time jitter below 90 ps (FWHM) at 5 V excess bias, and wide dynamics (three decades below the main peak the response is still narrower than 450 ps). Moreover the detection efficiency is good (higher than 25% at 1550 nm at 5 V excess bias) and dark count rate is moderately low (about 100 kcps at 225 K and less than 10 kcps at 200 K). The described performance makes it an excellent candidate for advanced single-photon counting and timing applications up to 1700 nm.

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