Instruction	Unused (2 bit) Bit 15 to 14	rD (3 bit) Bit 13 to 11	rA / M / Immediate Value (3 bit) Bit 10 to 8	Conditional (1 bit) Bit 7	Opcode (7 bit) Bit 6 to 0
XADD	XX	000 – 111	000 – 111	0 1	XXX0000
XCHG	XX	000 – 111	000 – 111	0 1	XXX0001
MUL	XX	000 – 111	000 – 111	0 1	XXX0010
DIV	XX	000 – 111	000 – 111	0 1	XXX0011
SHR	XX	000 – 111	000 – 111	0 1	XXX0100
SHL	XX	000 – 111	000 – 111	0 1	XXX0101
TEST	XX	000 – 111	000 – 111	0 1	XXX0110
TSTI	XX	000 – 111	000 – 111	0 1	XXX0111
MOV	XX	000 – 111	000 – 111	X	XXX1000
LDI	XX	000 – 111	000 – 111	X	XXX1001

LDI RAM0, 1 : 0000000110001001

LDI RAM1, 3 : 0000101110001001

LDI BX, 3 : 0000101100001001

XCHG RAM0, BX : 0000000110000001

XCHG BX, RAM0 : 0000100000000001

XADD BX, RAM0 : 0000100000000000

XADD RAM0, BX : 0000000110000000

MUL BX, RAM0 : 0000100000000010

MUL RAM0, BX : 0000000100000010