CSCE 3304 – Digital Design II

Project 1: Designing a Small Standard Cell Library

In this project you will work in a team (2 to 3 students not necessarily from the same section) to design (schematic and layout) and simulate few CMOS (**1.8V**) standard cells using the Electric VLSI and LTSpice software. The project has 2 milestones. The first one is worth 15% of the coursework while the second is worth 20% for a total of 35% of the digital design II coursework.

Preparations:

- Install Electric VLSI from: https://ftp.gnu.org/pub/gnu/electric/electricBinary-9.07.jar
- Guide to set LTspice up for use with Electric http://cmosedu.com/cmos1/ltspice/ltspice_electric.htm
- Watch videos 1 and 3 from: http://cmosedu.com/videos/electric/electric_videos.htm
- Use the design rules and technology files provided.

Procedure:

Design (layout and schematic), verify, and characterize the following cells:

1) Inverter (sizes: 1, 2, 4 and 8)
2) 3 input NAND gate (sizes: 1, 2 and 4)
3) 3 input NOR gate (sizes: 1, 2 and 4)
4) The complex function: $f(x, y, z, w) = \overline{xy + wz}$ (sizes: 1, 2 and 4)
5) The complex function: $g(x, y, z) = \overline{xy + xz + yz}$ (sizes: 1, 2 and 4)
6) The complex function: $h(x, y, z, \mathrm{w}) = \overline{xyz + (x + y + z)w}$ (sizes: 1, 2 and 4)

Rules:

- You need to select the widths of the transistors for each cell to achieve equal rise and fall times (symmetrical cell). *Hint: You will not be able to design a perfect symmetrical cell.*
- Size 1 cell has, in worst case, the same pull-up and pull-down resistances of the smallest inverter.
- Size n cell transistors have n times the widths of those of Size 1.
- For a standard cell library, every cell should have a width which is multiple of a standard unit, we call this unit "site", in our project the site width is 4λ.
- You need to obtain t_{pdr} and t_{pdf} for each cell using spice simulation. t_{pdr} and t_{pdf} should be obtained for different loads C_{inv}, $2C_{inv}$, $4C_{inv}$ and $8C_{inv}$. Also, you need to use different transition times (Here the transition time is defined as the time needed for the signal to go from 10% to 90% of its final value): 0ps, 100ps, 400ps and 800ps (In total there will be 32 simulations per cell; 16 for t_{pdr} and 16 for t_{pdf}).
- The gates layout should follow the standard cells layout guidelines mentioned in the lectures (for example, all the gates should have the same height). Also, the layout should be DRC and LVS clean. The height of the cell should be as minimum as possible. You will receive up to a **10% bonus** if you show evidence of efforts to reduce the cells height. Obviously, all the cells have to be designed correctly to receive the bonus.

Deliverables

- **Milestone 1: To be delivered through Blackboard by Wednesday May 5th, 2021 11:59 PM**
  - A PDF report containing:
    - Stick diagrams for all cells (using proper colors)
    - Your estimation for all cell heights
    - The layout of at least one size for each cell
- **Milestone 2: To be delivered through Blackboard by Tuesday May 11th, 2021 11:59 PM**
  - A single **compressed file** containing:
    - Electric VLSI library that contains the schematic and the layout for all the cells
    - Spice decks used to obtain t_{pdr} and t_{pdf}
    - A detailed **PDF** report to outline the design experience and to report the collected data. The report has to show your work to determine the cells height as well as the stick diagrams used for the layout.
  - Note: the report must indicate the work of each group member. Group members may receive different grades based on their contribution to the project.

Plagiarism is NOT tolerated and will be reported. Late submissions will be penalized by a 5% deduction for every late milestone submission (one day maximum)