

Report Asynchronous FIFO (Self Project)

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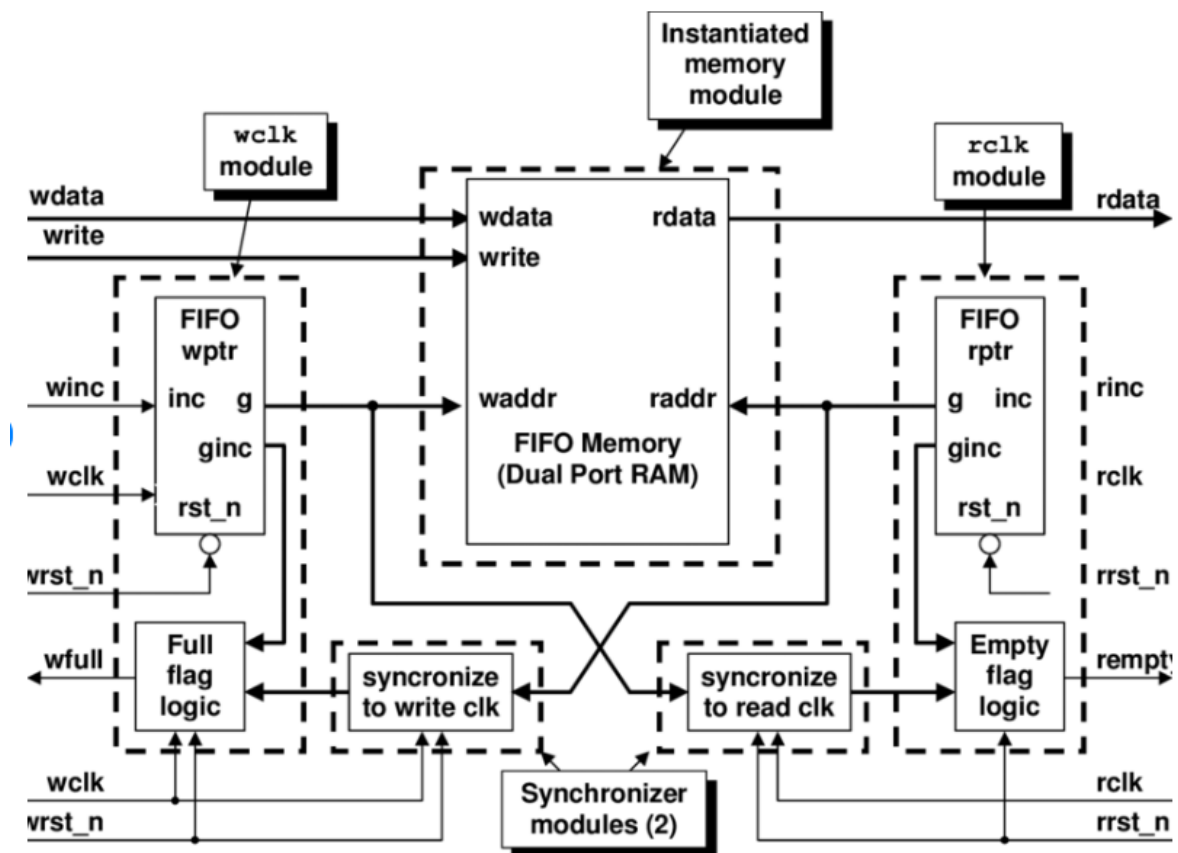
Asynchronous FIFO

In asynchronous FIFO, data read and write operations use different clock frequencies. Since write and read clocks are not synchronized, it is referred to as asynchronous FIFO. Usually, these are used in systems where data need to pass from one clock domain to another which is generally termed as 'clock domain crossing'.

Efforts to synchronize multiple signals from one clock domain to a new clock domain, ensuring the synchronization of all these signals in the new domain, has proven to be problematic. In designs, First-In-First-Out (FIFO) structures are used in designs to securely transfer multi-bit data chunks from one clock domain to other. These data chunks are inserted into a FIFO buffer memory array through control signals in one clock domain, and the removal of data chunks occurs through another port of the same FIFO buffer memory array using control signals from a different clock domain.

The challenges associated with FIFO design arise primarily from devising the FIFO pointers and identifying a dependable method for ascertaining the "full" and "empty" status of the FIFO.

Block Diagram of Asynchronous FIFO:



Asynchronous FIFO Pointers Using Gray Counters

- Gray numbers are unidistance numbers wherein just a single bit alters between consecutive counts, differentiating them from binary numbers.
- Although Gray pointers still encounter challenges with metastability when synchronized with distinct clock domains, the impact is diminished due to the single-bit alteration.
- In scenarios where one bit succumbs to metastability, it induces a count discrepancy of ± 1 , which proves more favourable when compared to the ± 8 count discrepancy in binary pointers. Given this reduced error propensity, gray counters are typically favoured for application as FIFO pointers.

Waveforms:

