

09/09/2014

UNIT-III

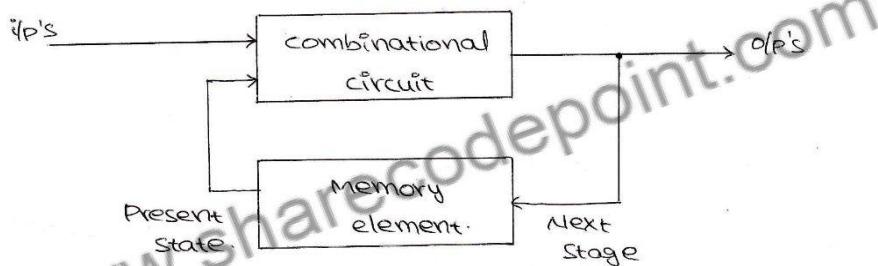
SEQUENTIAL LOGIC

(1)

Differences b/w combinational circuit and sequential circuit:

combinational circuit	sequential circuit
(i) Output depends on only present inputs.	(i) Output depends on present i/p's and past outputs.
(ii) Memory unit is not required.	(ii) Memory unit is required to store the past history of o/p's.
(iii) Faster in speed.	(iii) slower than combinational circuits
(iv) Easy to design.	(iv) compared to combinational circuits harder to design.
(v) Ex:- Encoders, Decoders, MUX, DEMUX.	(v) Ex:- Flip-flops, Registers, counters.

Block diagram of sequential circuit:-



- * One of the most fundamental sequential circuit is latch / flip-flop.
- * A latch / flip-flop is a bistable multivibrator, that can store 1 bit of binary information (either 0 or 1).
- * Because of their ability to retain a given state, these elements are useful as storage elements.

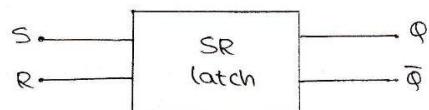
* LATCHES :-

(2)

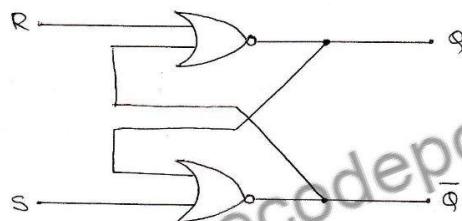
1. RS latch / SR latch / set - Reset latch / Reset - Set latch :-

- * The most fundamental type of storage element is an SR latch.
- * SR latch has two I/P's (S and R), two O/P's (Q & \bar{Q}) which are complemented to each other.
- * The SR latch can be constructed from either NAND (or) NOR gates.

Logic symbol of SR latch :-



Logic circuit of RS latch using NOR gates :-

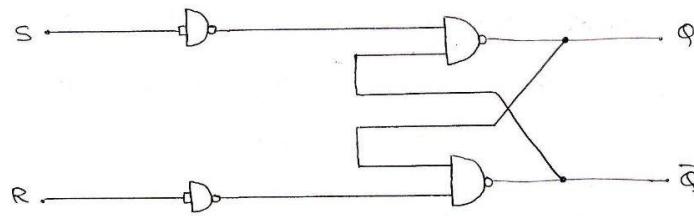


Truth table / Function table :-

I/P's	O/P			
R	S	Q_n	Q_{n+1}	State
0	0	0	0	No change
0	0	1	1	
0	1	0	1	Set
0	1	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	X	Indeter-
1	1	1	X	-minate.

Logic circuit of RS latch using NAND Gate :-

(3)



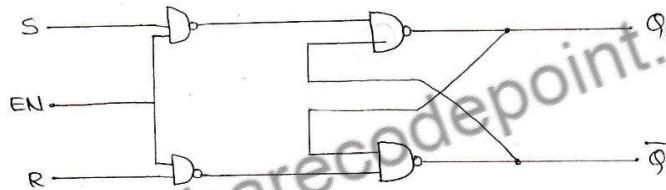
2. Gated SR latch :-

SR latch with enable I/P is known as "Gated SR latch".

Block diagram / logic symbol :-



Logic circuit :-



Truth table / Function table :-

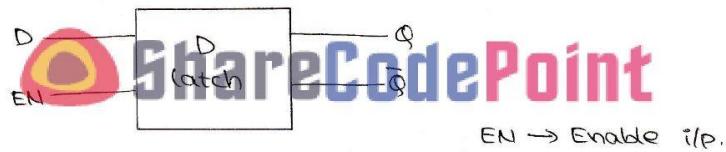
EN	I/P's			O/P Q_{ntf}	State
	R	S	Q_n		
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	1	Set
1	0	1	1	1	
1	1	0	0	0	Reset
1	1	0	1	0	
1	1	1	0	X	Indeter- -minate
1	1	1	1	X	
0	X	X	0	0	No change
0	X	X	1	1	

3. D latch / Data latch :-

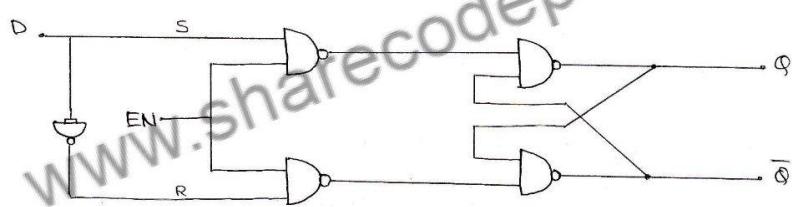
(4)

- * From the truth table of SR latch it is clear that when both i/p's are same, the o/p either doesn't change or it is invalid.
- * In many practical applications these i/p conditions are not required.
- * These i/p conditions can be avoided by making i/p's complement to each other.
- * This modified SR latch is known as "D latch".

Block diagram / logic symbol :-



logic circuit:-



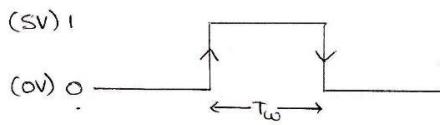
Truth table / Function table :-

i/p's		o/p		State
EN	D	Q_n	Q_{n+1}	
0	X	0	0	No change
0	X	1	1	change
1	0	0	0	Reset
1	0	1	0	
1	1	0	1	Set.
1	1	1	1	

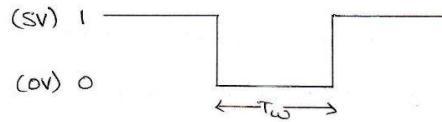
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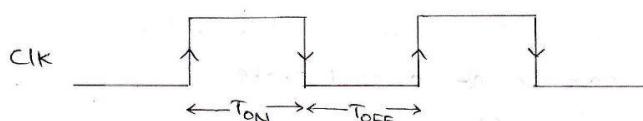
Positive pulse (0 to 1)



Negative pulse (1 to 0).

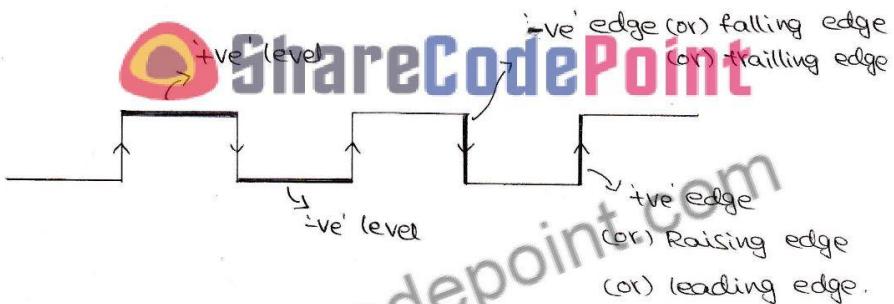


clk → clock is a periodic pulse train



Time period of clk signal $T = T_{on} + T_{off}$

frequency of clk (f) = $\frac{1}{T}$.



* Types of triggerings :-

1. Level triggering.

- (a) '+ve' level triggering
- (b) '-ve' level triggering

2. Edge triggering

- (a) '+ve' edge triggering
- (b) '-ve' edge triggering

→ '-ve' edge triggered

circuit responds to edges only
at '-ve' edges of clk signal.

* Latches uses level triggering.

* flip-flops uses edge triggering.

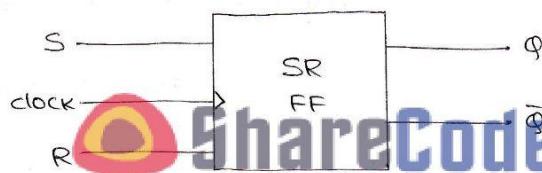
* flip-flop :-

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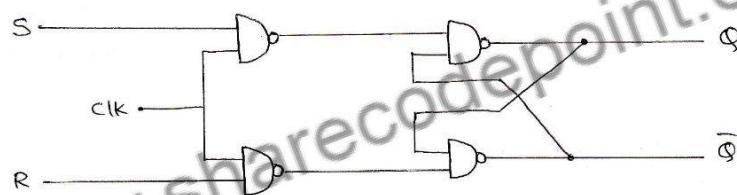
- * flip-flop is a memory element stores 1 bit of binary information.
- * flip-flop has two stable states (1 or 0).
- * state of flip-flop i.e. bit stored is indicated by Q output.
- * other names of flip-flop are 1 bit memory cell, Bistable circuit, Bistable multivibrator.
- * on power, FF can be at 0 or 1 state

1. Clocked SR flip-flop :-

(i) logic symbol of 'tve' edge triggered SR flip-flop :-



logic circuit :-



Truth table :-

i/p's			o/p	State
CLK	S	R	Q_n	Q_{n+1}
↑ (or) 1	0	0	0	No change
↑ (or) 1	0	0	1	No change
↑	0	1	0	Reset
↑	0	1	1	Set
↑	1	0	0	Set
↑	1	0	1	Set
↑	1	1	0	Indeterminate
↑	1	1	1	Indeterminate
↑	X	X	0	No change
↑	X	X	1	No change

$Q_n \rightarrow$ state of FF before applying clk pulse
 $Q_{n+1} \rightarrow$ state of FF after applying clk

characteristic table

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

characteristic equation of SR flip-flop :-

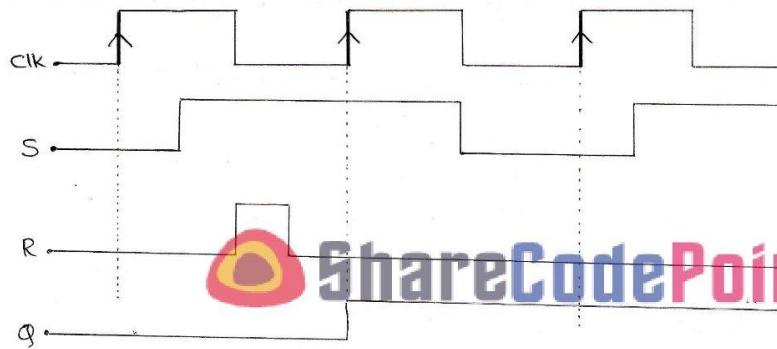
K-map for Q_{n+1}

S R _n	00	01	11	10
0	1			
1	1	1	X	X

$$\therefore Q_{n+1} = S + \bar{R}Q_n$$

characteristic equation of SR flip-flop is $Q_{n+1} = S + \bar{R}Q_n$

i/p & o/p waveforms of 'ive' edge triggered SR flip-flop:-

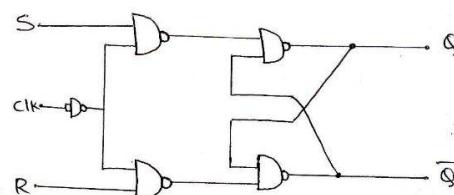


(ii) logic symbol of 've' edge triggered SR flip-flop :-



clock signal symbol
 $\overline{\text{P}}(\text{or}) \downarrow$

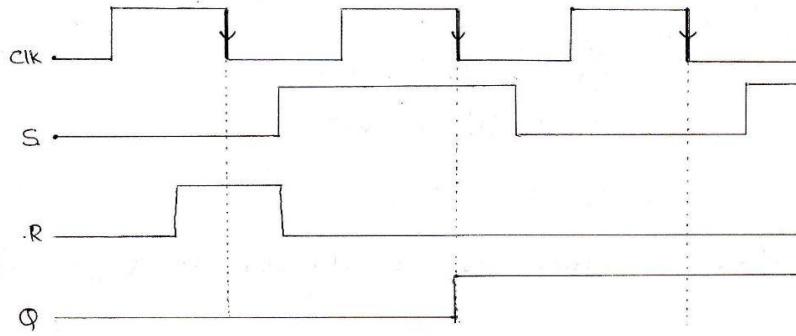
logic circuit :-



Truth table :-

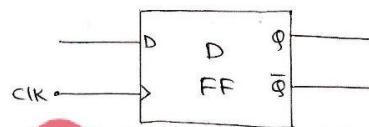
CLK	i/p's			o/p	State
	S	R	Q_n	Q_{n+1}	
$\overline{\text{P}}(\text{on}) \downarrow$	0	0	0	0	No change
$\overline{\text{P}}(\text{on}) \downarrow$	0	0	1	1	Set
$\overline{\text{P}}(\text{on}) \downarrow$	0	1	0	0	Reset
$\overline{\text{P}}(\text{on}) \downarrow$	0	1	1	0	Indeterminate
\downarrow	1	0	0	1	
\downarrow	1	0	1	1	
\downarrow	1	1	0	X	
\downarrow	1	1	1	X	
\downarrow	X	X	0	0	No change
\downarrow	X	X	1	1	

i/p & o/p waveforms of 've' edge triggered SR flip-flop :-

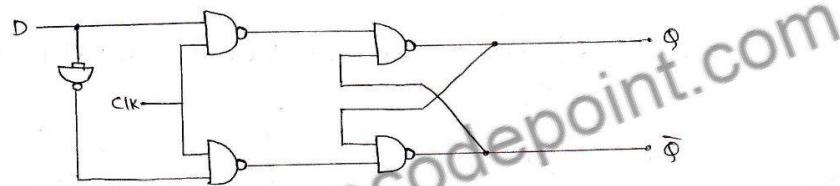


2. clocked D flip-flop :- / data flip-flop / Delay flip-flop :-

(i) logic symbol of 've' edge triggered D flip-flop :-



 ShareCodePoint
logic circuit:-



Truth table:-

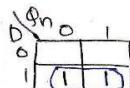
i/p's		o/p		State
CLK	D	Q_n	Q_{n+1}	
↑	0	0	0	Reset
↑	0	1	0	
↑	1	0	1	Set
↑	1	1	1	
0	x	0	0	No change
0	x	1	1	

characteristic table:-

D	Q_{n+1}
0	0
1	1

characteristic equation of D flip-flop:-

K-map for Q_{n+1}

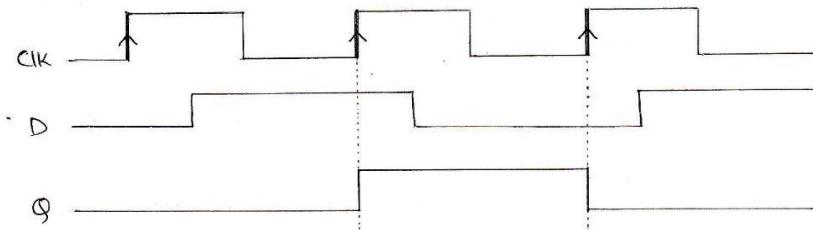


$$\therefore Q_{n+1} = D$$

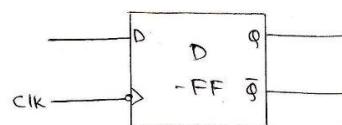
∴ characteristic equation of D flip-flop is $Q_{n+1} = D$

(9)

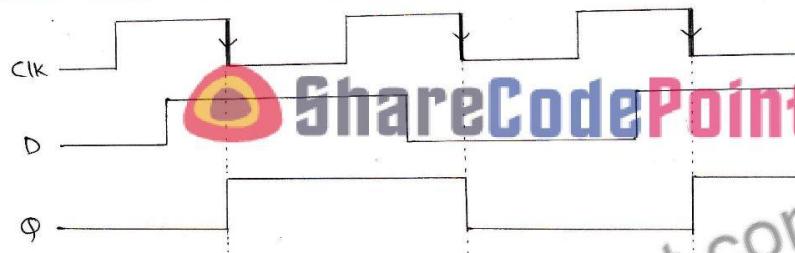
i/p & o/p waveforms of 'tve' edge triggered D flip-flop:-



(ii) logic symbol of '-ve' edge triggered D flip-flop:-



i/p & o/p waveforms of '-ve' edge triggered D flip-flop:-



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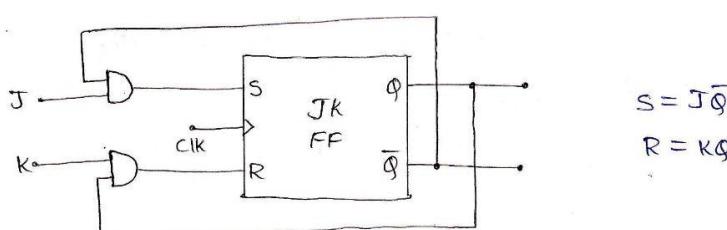
3. clocked JK flip-flop:

the uncertainty in the state of an SR FF

when $S = R = 1$ can be eliminated by converting it

into a JK flip-flop.

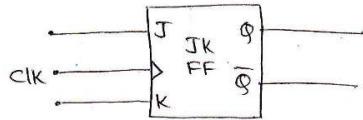
JK flip flop using SR flip-flop :-



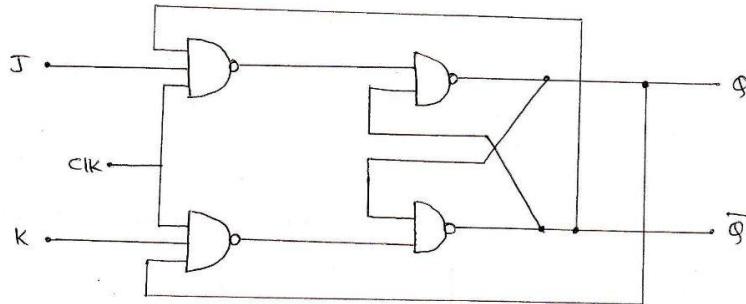
$$S = J\bar{Q}$$

$$R = KQ$$

logic symbol of JK flip-flop :-



logic circuit of JK flip-flop using NAND gates :-



Truth table :-

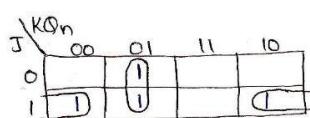
i/p's				o/p	
CLK	J	K	Q_n	Q_{n+1}	\bar{Q}_{n+1}
0	x	x	0	0	
0	x	x	1	1	
↑	0	0	0	0	
↑	0	0	1	1	
↑	0	1	0	0	
↑	0	1	1	0	
↑	1	0	0	1	
↑	1	0	1	1	
↑	1	1	0	1	
↑	1	1	1	0	

characteristic table :-

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

characteristic equation of JK flip-flop :-

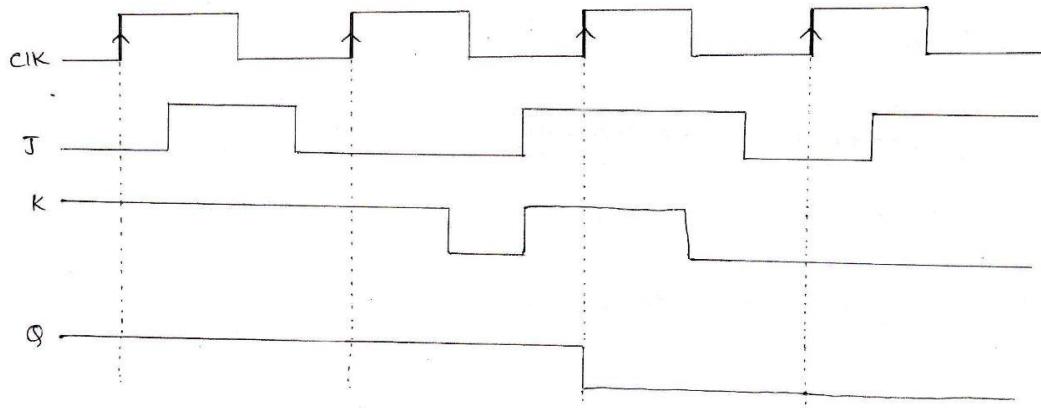
K-Map for Q_{n+1}



$$\therefore Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$$

characteristic equation of JK flip-flop is $Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

i/p & o/p waveforms of 'tve' edge triggered JK flip-flop:-



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* Race around condition :-

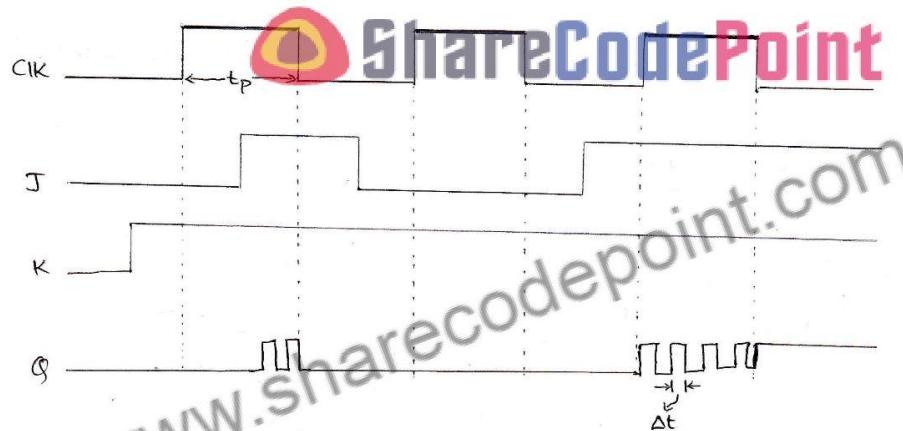


fig: tve level triggered JK FF i/p & o/p waveforms

$t_p \rightarrow$ pulse width

$\Delta t \rightarrow$ propagation delay of 2 level NAND gates

(considering JK FF using NAND gates circuit)

- * In JK flip-flop, when $J=K=1$, the o/p continuously toggles in that region (o/p changes either from 0 to 1 or from 1 to 0). which creates disturbance in ... \therefore this situation is referred to as the

Race around condition.

* There are 3 solutions for reducing race around condition.

(i) Use of edge triggering.

(ii) RAC exists when $t_p \geq \Delta t$. Thus by keeping $t_p < \Delta t$, we can avoid RAC.

(iii) Use of Master slave flip-flop configuration.

* Master - slave JK flip-flop :-

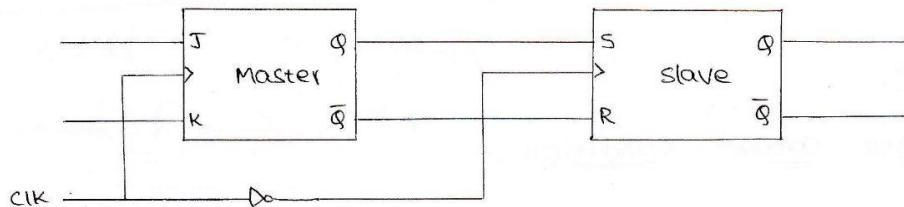


Fig: logic diagram of master - slave JK flipflop.

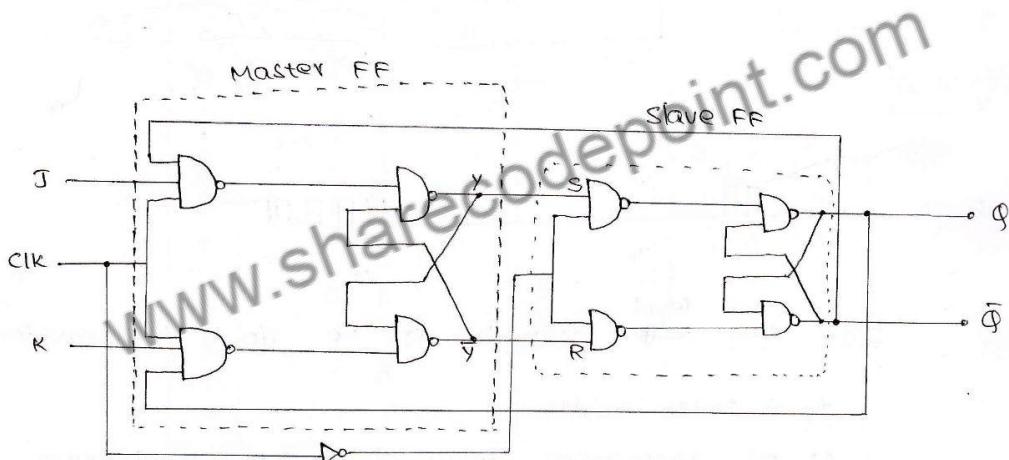


Fig: Logic circuit of master slave JK FF.

* Master slave JK flip-flop consists of clocked JK flip-flop as the master and clocked SR flip-flop as a slave.

- * the o/p of the Master flip-flop is fed as an i/p to the slave FF.
- * clock signal is connected directly to the ~~Master~~ Master flip-flop but it is connected through inverter to the slave flip-flop.

\therefore the information present at the J4 K i/p's is transmitted to the o/p of master flip flop on the 've clock pulse & it is held there until the '-ve' clock pulse occurs; After which it is allowed to pass through to the o/p of slave FF. The o/p of the slave FF is connected to the third i/p of the 3^r Master JK FF.

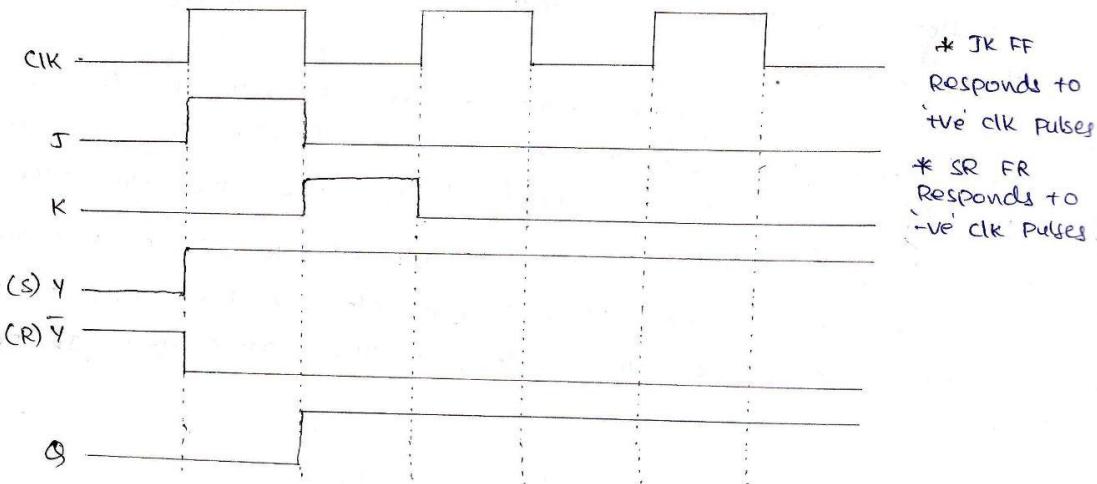
Truth table:-

CLK	J	K	Q_n	Master FF o/p Y	Slave FF o/p Q_{n+1}
\uparrow	0	0	0	0	No change
\downarrow	0	0	0	NC	0
\uparrow	0	0	0	NC	NC
\downarrow	0	0	1	No change	1
\uparrow	0	1	0	0	NC
\downarrow	0	1	0	NC	0
\uparrow	0	1	1	0	NC
\downarrow	0	1	1	NC	0
\uparrow	1	0	0	1	NC
\downarrow	1	0	0	NC	1
\uparrow	1	0	1	1	NC
\downarrow	1	0	1	NC	1
\uparrow	1	1	0	1	NC
\downarrow	1	1	0	NC	1
\uparrow	1	1	1	0	NC
\downarrow	1	1	1	NC	0

- * When $J=1$ & $K=1$ Master flip-flop toggles on 've' clock and slave then copies the o/p of master on the '-ve' clock. at this instant, feedback i/p's to the Master flip-flop are complemented but as it is '-ve' half of the clock pulse Master FF is inactive.

This prevents race around condition.

i/p & o/p waveforms of Master-slave JK FF :-



Differences b/w latch & flip-flop :-



- * A latch checks all its i/p's continuously & changes its o/p's accordingly at any time.
- * NO clock is used.
- * flip-flop samples its i/p's if changed change its o/p's only at a time as determine by a clock signal.
- * A clock is used.

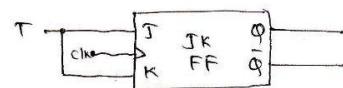
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Clocked T flip-flop / Toggle FF :-

* The T flip-flop is a modification of the JK flip-flop.

* T flip-flop is obtained from a JK flip-flop by connecting J & K inputs together.

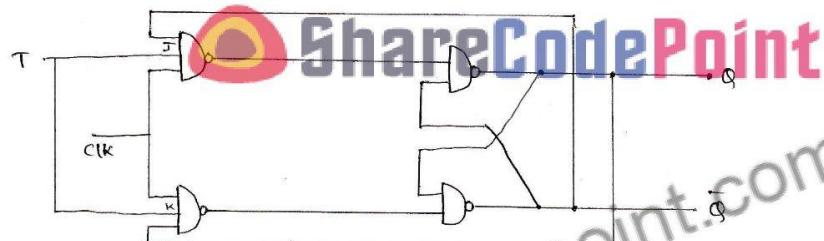
Logic diagram of T FF using JKFF :-



Logic diagram of T FF :-



Logic circuit :-



Truth table :-

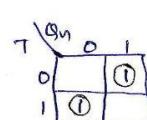
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic table :-

T	Q_{n+1}
0	Q_n
1	\bar{Q}_n

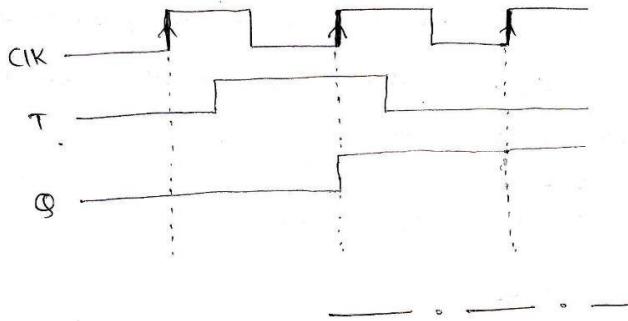
Characteristic equation of T flip flop:-

K Map for Q_{n+1}



$$\therefore Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n.$$

I/p and o/p waveforms of +ve edge triggered T-FF:-



* Flip-flop excitation tables:-

1. SR flip-flop:-

characteristic table:-

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	*

Excitation table:-

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

2. D flip-flop:-

characteristic table:-

D	Q_{n+1}
0	0
1	1

Excitation table:-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3. JK flip-flop:-

characteristic table:-

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

Excitation table:-

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

4. T - flip-flop :-

Characteristic table :-

T	Q_{n+1}
0	Q_n
1	\bar{Q}_n

Excitation table :-

Q	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Realisation of one flip-flop using other flip-flop :-

Ex:- convert SR FF to D FF.

Sol:- Excitation table for SR to D FF conversion :-

i/p	Present state		Next state		FF i/p's.	
	D	Q_n	Q_{n+1}	S	R	
0	0	0	0	0	X	
0	1	0	0	0	1	
1	0	0	1	0	0	
1	1	1	1	X	0	

K-map simplification :-

for S

D	Q_n	0	1
0	0		
1	1	(1)	X

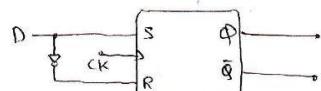
$$\therefore S = D$$

for R

D	Q_n	0	1
0	0	X	1
1	1		

$$\therefore R = \bar{D}$$

Logic diagram of DFF using SR FF :-



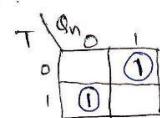
2. Convert D FF to T FF :-

Excitation table for D to T FF conversion :-

i/p	Present state	Next State	FF i/p
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

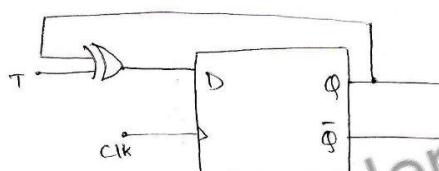
K-Map Simplification :-

for D :-



$$\therefore D = \bar{T}Q_n + T\bar{Q}_n = T \oplus Q_n$$

Logic diagram of T FF using D FF :-



3. convert SR FF to JK FF.

Excitation table for SR FF to JK FF conversion :-

i/p		Present State	Next State	FF i/p	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

K-MAP Simplification :-

for S

J _{KQn}		00	01	11	10
0	D	X		C	
1					

$$\therefore S = J\bar{Q}_n$$

for R

J _{KQn}		00	01	11	10
0	X	*	1	0	X
1					

$$\therefore R = K\bar{Q}_n$$

Logic diagram of JK flip-flop using SR FF :-

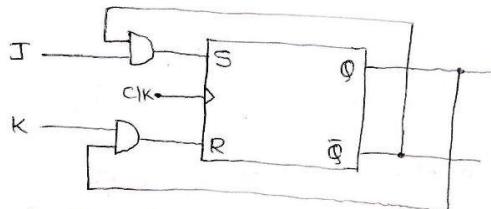


Fig:- logic diagram of JK FF using SR FF.

21/10/2014

Analysis and Design of Synchronous (or) Clocked Sequential Circuits

The synchronous or clocked sequential circuits are represented by two models.

- (i) Moore circuit (or) Moore model (or) Moore Machine
- (ii) Mealy circuit.

1. Moore circuit :-

(i) Moore circuit o/p depends only on the present state of FF's.

- (ii) I/p changes doesn't effect the o/p.
- (iii) It requires more no. of states for implementing function which is implemented using Mealy circuit.

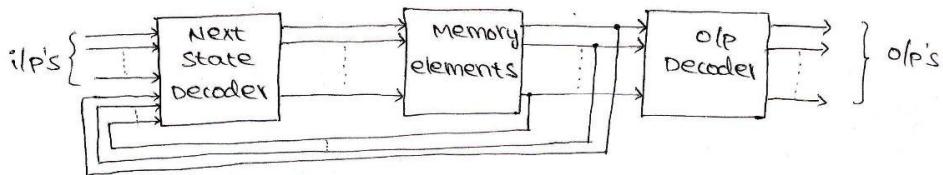


Fig:- B.D. of Moore circuit.

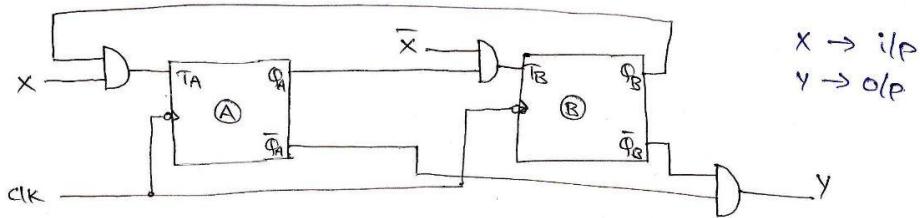


Fig:- Example of moore circuit.

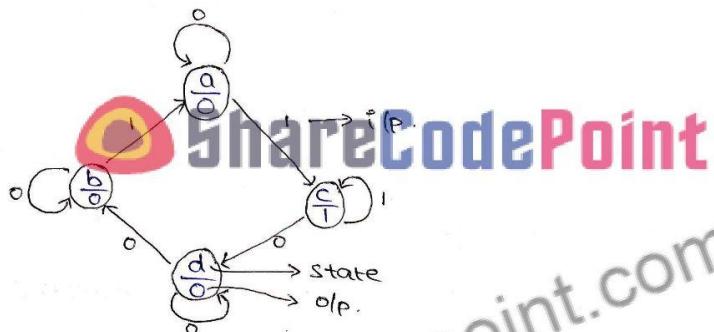


Fig:- Example state diag. for moore circuit.

2. Mealy circuit:

- (i) The o/p depends on both the present state of the FF's and on the i/p's.
- (ii) I/p changes may effect the o/p of the ckt.
- (iii) It requires less no. of states for implementing the function which is implemented using Moore circuit.

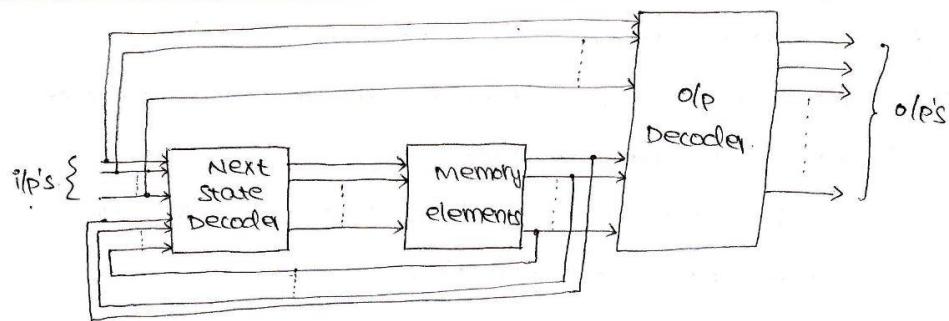


Fig:- B.D. of Mealy circuit.

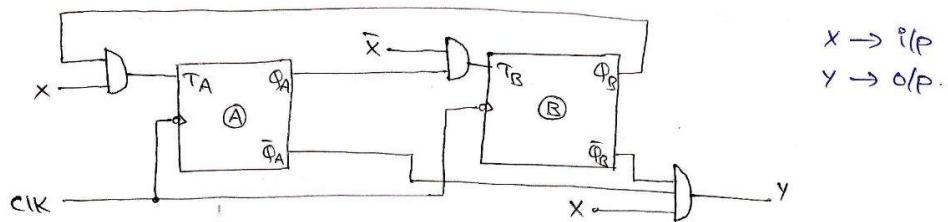


Fig:- Example of mealy circuit

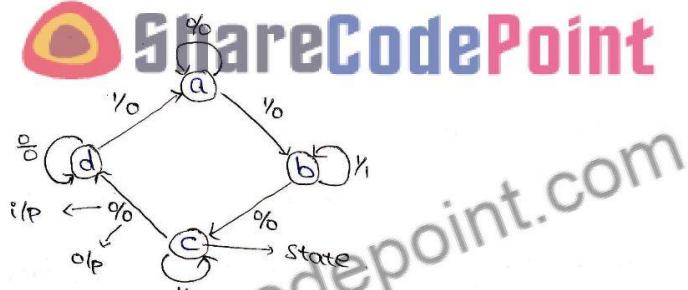


Fig:- example diag. for mealy circuit.

Steps for the design of a synchronous (or) clocked sequential circuits:-

Step 1: Obtain the state table from the given circuit information such as state diagram.

Step 2: Reduce no. of states if possible by state reduction technique.

Step 3: Assign binary values to each state in the state table.

Step 4: Determine the no. of FF's needed and

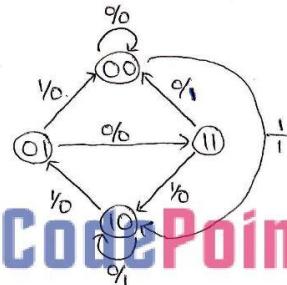
choose the type of FF to be used.

Step 5: From the state table derive the circuit excitation & o/p tables.

Step 6: Using K-map, derive the circuit o/p functions and the FF i/p functions.

Step 7: Draw the logic diagram.

Q:- A sequential circuit has 1 i/p & 1 o/p. The ckt state diagram is shown below. Design the Sequential circuit with D-FF.



Sol:- Step 1: State diagram

The given state diagram has 4 states with one i/p and one o/p. Considering $X \rightarrow \text{i/p}$ and $Y \rightarrow \text{o/p}$.

Present state Q_A Q_B	Next state		o/p (Y)	
	$X=0$	$X=1$	$X=0$	$X=1$
0 0	0 0	1 0	0	1
0 1	1 1	0 0	0	0
1 0	1 0	0 1	1	0
1 1	0 0	1 0	1	0

Step 2: State Reduction and State Assignment

Here binary values are already assigned to states and it is not possible to reduce no. of states because no two present states, next states and o/p's are same.

Step 3: Determine no. of FF's required.

Determine no. of FF's required using eq.,

$$2^n \geq N \quad n \rightarrow \text{no. of FF's.}$$

$$N \rightarrow \text{no. of states.}$$

$$\therefore n=2$$

FF's required $\rightarrow 2$
FF's using $\rightarrow D$ FF's

Step 4: Excitation table

Present state	i/p	Next state		FF i/p's		o/p	
		Q_A	Q_B	X	Q_{A+1}	Q_{B+1}	
0 0	0	0	0	0	0	0	0
0 0	1	1	0	1	0	1	1
0 1	0	1	1	1	1	0	0
0 1	1	0	0	0	0	0	0
1 0	0	0	0	1	0	1	1
1 0	1	0	1	0	1	0	0
1 1	0	0	0	0	0	1	1
1 1	1	1	0	1	0	0	0

(\because D-FF
excitation table)

Q_n	Q_{n+1}	D
0 0	0	0
0 1	1	1
1 0	0	0
1 1	1	1

Step 5: K-map simplification.

K-map simplification for FF i/p functions & sequential circuit o/p function.

<u>for D_A</u>	
Q_A	$Q_B X$
0	00 01 11 10
1	① ① ① ①

$$\therefore D_A = Q_A \oplus Q_B \oplus X$$

<u>for D_B</u>	
Q_A	$Q_B X$
0	00 01 11 10
1	① ① ① ①

$$\therefore D_B = \bar{Q}_A \bar{Q}_B \bar{X} + Q_A \bar{Q}_B \bar{X}$$

<u>for Y</u>	
Q_A	$Q_B X$
0	00 01 11 10
1	① ① ① ①

$$\therefore Y = \bar{Q}_A \bar{Q}_B X + Q_A \bar{Q}_B \bar{X}$$

Step 6: logic diagram.

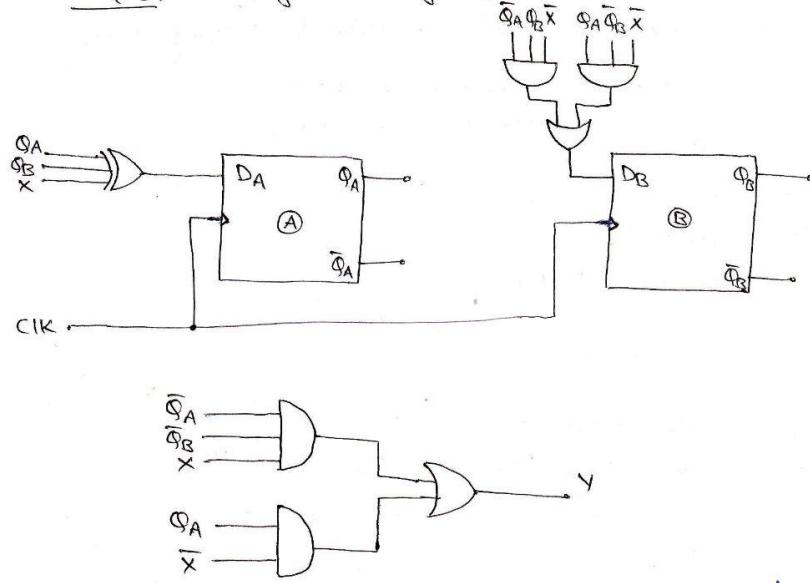
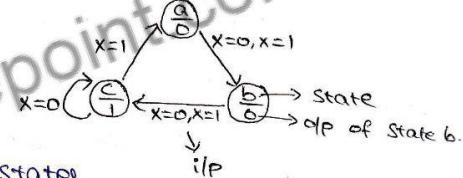


Fig: Logic diagram of mealy circuit for given sequential State diagram.

22/10/2014



Q: Realize the sequential circuit for the state diagram shown below.



Sol: Given state diag. has 3 states,
one i/p, one o/p.

considering $x \rightarrow$ i/p
 $y \rightarrow$ o/p

Step 1: State table

Present state	Next state		Output y
	$x=0$	$x=1$	
a	b	b	0
b	c	c	0
c	c	a	1

Step 2: State Reduction

there is no possibility of State Reduction since no two states, Next states & O/p's are same.

Step 3: No. of FF's Required

Determine no. of FF's required using eq.

$$2^n \geq N \quad n \rightarrow \text{no. of FF's}$$

$N \rightarrow \text{no. of states}$

$$2^n \geq 3$$

$$\therefore n=2$$

$\boxed{\begin{array}{l} \text{FF's required} = 2 \\ \text{FF's using} \rightarrow T \text{ FF's} \end{array}}$

Step 4: State Assignment

Assign Binary values to states.

$$a = 00, b = 01, c = 10$$

Step 5: Excitation table

Present state	i/p	Next state		FF i/p's		o/p
		Q_A	Q_B	T_A	T_B	
0 0	0	0	0 1	0	1	0
0 0	1	0	1 1	0	1	0
0 1	0	1	0 0	1	1	0
0 1	1	1	1 0	1	1	0
1 0	0	1	0 0	0	0	1
1 0	1	0	0 0	1	0	1

T-FF excitation table	
Q_n	Q_m
0 0	0
0 1	1
1 0	1
1 1	0

State 11 is Unused state. \therefore Treat that state as don't care.

Step 6: K-map simplification

K-Map simplification for FF's i/p functions and sequential circuit o/p function.

for T_A

Q_A	Q_B	00	01	11	10
0	X	0	1	1	1
1	X	1	X	X	X

$$\therefore T_A = Q_A X + Q_B$$

for T_B

Q_A	Q_B	00	01	11	10
0	X	0	1	1	1
1	X	1	X	X	X

$$\therefore T_B = \bar{Q}_A$$

for y

Q_A	Q_B	00	01	11	10
0	X	0	1	1	1
1	X	1	1	X	X

$$\therefore Y = Q_A$$

Step 6: LOGIC DIAGRAM

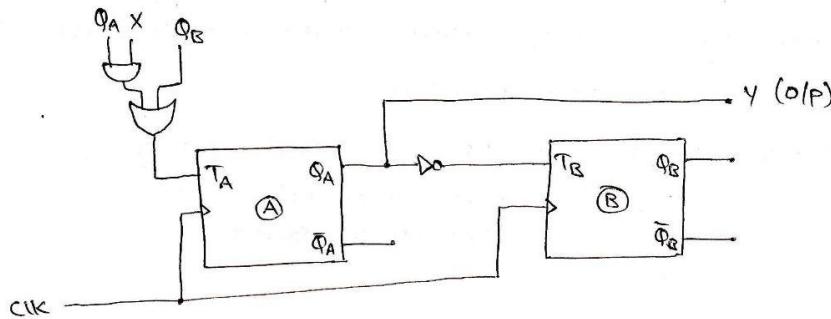


Fig:- logic diagram of moore sequential ckt
for given state diagram.

Q:- Design a clocked sequential circuit for State diagram shown below.

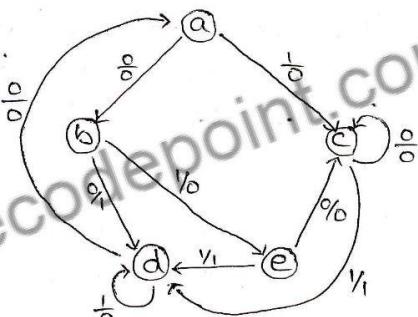


Sol:- Given state diag.

has 5 states with
one i/p and one o/p.

considering,

$x \rightarrow$ i/p
 $y \rightarrow$ o/p.



Step 1: state table

Present state	Next state		o/p (y)	
	$x=0$	$x=1$	$x=0$	$x=1$
a	b	c	0	0
b	d	e	1	0
c	d	c	0	1
d	a	d	0	0
e	c	d	0	1

c & e states next states and o/p's are same.
∴ we can cancel either c or e state. if e is cancelled then replace e with c.

Reduced State table

Present State	Next State		o/p(y)	
	$x=0$	$x=1$	$x=0$	$x=1$
a	b	c	0	0
b	d	c	1	0
c	c	d	0	1
d	a	d	0	0

Step 2: Determine no. of FF's required.

No. of FF's required to design seq. ckt can be determined by the eq.,

 ShareCodePoint

$$2^n \geq 4 \quad (\because \text{After state reduction } N=4) \\ \therefore n=2$$

∴ no. of FF's required = 2

FF's using → D-FF's.

Step 3: State Assignment

Assign Binary values to states

$$a=00, b=01, c=10, d=11$$

Step 4: Excitation table

(for procedure refer
previous problem)

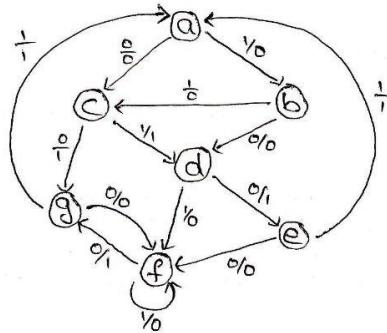
Step 5: K-map simplification

Step 6: Logic diagram

Q: Design a clocked seq. circuit for state diagram shown below.

Sol: The given state diag. has 7 states with one i/p & one o/p.

considering $X \rightarrow i/p$
 $Y \rightarrow o/p$.



Step1: State table

Present state	Next state		o/p(Y)	
	$X=0$	$X=1$	$X=0$	$X=1$
a	c	b	0	0
b	d	c	0	0
c	g/e	d	1	1
d	f	a	0	1
e	f	e	1	0
f	g/e	f	1	0
x/g	f	a	0	1

e & g states next states and o/p's are same.

\therefore we can cancel either e or g state. If 'g' is cancelled then replace g with e.

reduced state table

Present state	Next state		o/p(Y)	
	$X=0$	$X=1$	$X=0$	$X=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	f/d	1	0
e	f/d	a	0	1
x/f	e	f	1	0

d and f states next states and O/P's are same.
∴ we can cancel either d or f state. If 'f' is cancelled then replace 'f' with 'd'

final reduced state table

Present State	Next State		O/P (Y)	
	X=0	X=1	X=0	X=1
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	d	1	0
e	d	a	0	1

Step 2:



no. of FF's required = 3 ($\because 2^n \geq 5$
 $n=3$)

FF's using \rightarrow 3 FF's.

Step 3: state assignment

Assign binary values to states

$$a = 000, b = 001, c = 010, d = 011, e = 100.$$

101, 110, 111 are unused states.

∴ treat them as don't cares.

(i.e) for 101, 110, 111 states, Next states and i/p and o/p's are don't cares.

Step 4: excitation table

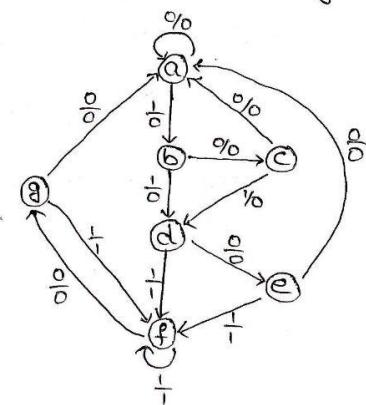
Step 5: K-map simplification

Step 6: logic diagram

25/10/2014

Q:- Obtain the reduced state table and reduced state diagram for a sequential ckt whose state diagram shown below.

Sol:- The give state diagram has 7 states, one i/p & 1 o/p.
considering,
 $x \rightarrow \text{i/p}$



Step1: State table.

Present state	Next state		o/p	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a b		0 0	
b	c d		0 0	
c	a d		0 0	
d	e f		0 1	
e	a f		0 1	
f	g e	f	0 1	
x	g	a f	0 1	

\therefore e & g states next states and o/p's are same.
 \therefore we can cancel either e or g state. If 'g' is cancelled then replace g with e.

reduced state table

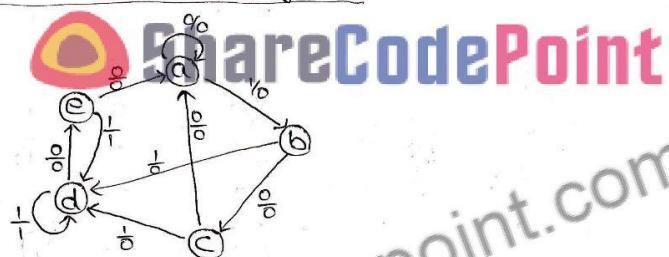
Present state	Next state		o/p	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a b		0 0	
b	c d		0 0	
c	a d		0 0	
d	e f d		0 1	
e	a f d		0 1	
x	f	(e f)	0 1	

\therefore d & f states next states and o/p's are same.
 \therefore we can cancel either d or f state. If 'f' is cancelled, then replace 'f' with 'd'.

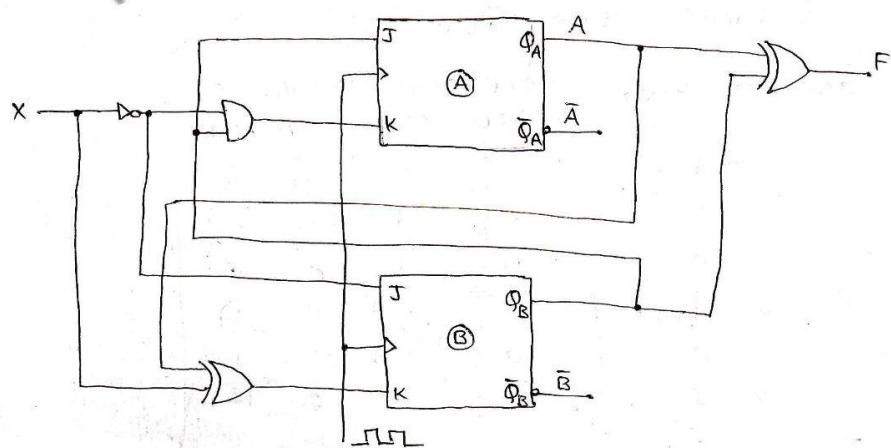
Final reduced state table

Present State	Next State		O/P	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

Reduced state diagram:



Q.:- Derive the transition table, state table & state diagram for the Moore sequential circuit given below.



Sol: Step 1: Determine the FF ilp Eq.'s & the o/p eq.'s of sequential circuit from the above seq. ckt.

FF ilp eq's

$$J_A = Q_B$$

$$K_A = \bar{X}Q_B$$

$$J_B = \bar{X}$$

$$K_B = Q_A \oplus X$$

Seq. circuit o/p

$$F = Q_A \oplus Q_B$$

Step 2: Derive the transition eq.'s.

The transition eq.'s for JK FF's can be derived from the characteristic eq. of JK FF.

char. eq. of JK FF is $Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

$$Q_{A+1} = J_A \bar{Q}_A + \bar{K}_A Q_A$$

After substituting J_A & K_A eqn's,

Above eqn. becomes,

$$\therefore Q_{A+1} = Q_B \bar{Q}_A + (\bar{X}Q_B) Q_A$$

$$Q_{B+1} = J_B \bar{Q}_B + \bar{K}_B Q_B$$

After substituting J_B & K_B eqn's,

Above eqn. becomes,

$$\therefore Q_{B+1} = \bar{X} \bar{Q}_B + (\bar{Q}_A \oplus X) Q_B$$

Step 3: Transition table.

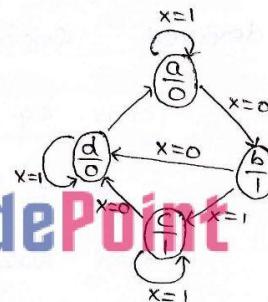
Present State Q_A Q_B	Next State $x=0$		Output F	
	Q_{A+1}	Q_{B+1}	Q_{A+1}	Q_{B+1}
0 0	0	1	0	0
0 1	1	1	1	1
1 0	1	1	1	1
1 1	0	0	1	0

Step 4: State table.

Considering $a=00$, $b=01$, $c=10$, $d=11$.

Present State	Next State $x=0$ $x=1$		O/P (F)
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0

Step 5: State diagram



$A \text{ (or) } Q_A$	
$A^+ \text{ (or) } Q_{A+}$	$\text{ (or) } A(t+1) \text{ (or) } Q_A^+$

} Different representations.

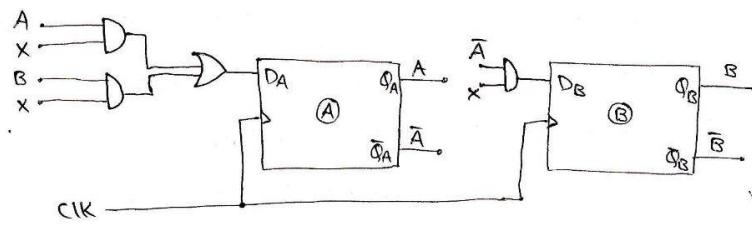
Q. :- A sequential circuit with two D-FF's A & B and i/p x & o/p y. is specified by the following Next state and o/p equations.

$$A(t+1) = Ax + Bx'$$

$$B(t+1) = A'x \quad ; \quad y = (A+B)x'$$

- (i) Draw the logic diagram of the ckt.
- (ii) Derive the State table
- (iii) Derive the State diagram.

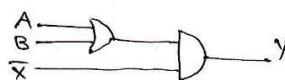
Sol: (i) logic diagram



for D-FF,
 $D/P = i/p.$

$$\therefore D_A = A(t+k)$$

$$D_B = B(t+i)$$

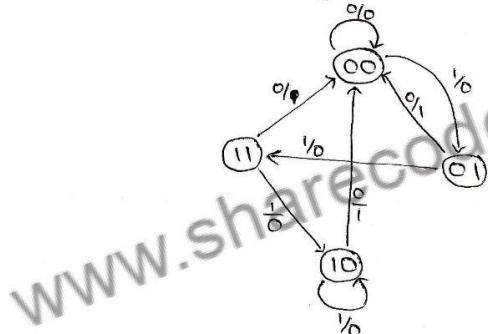


(ii) State table

Present state		Next state				$D/P(Y)$	
		$x=0$	$x=1$	$A(t+i)$	$B(t+i)$		
A	B	$A(t+i)$	$B(t+i)$	$x=0$	$x=1$		
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	0	0	0	0

(iii) state diagram

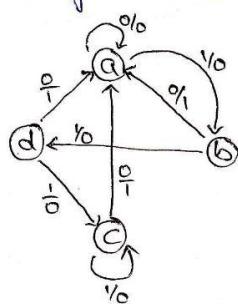
considering $a=00, b=01, c=10, d=11$



Present state	Next state		$D/P(Y)$	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	a	d	1	0
c	a	c	1	0
d	a	c	1	0

(or)

considering $a=00, b=01, c=10, d=11$



27/09/2014

UNIT-IV

1

REGISTERS AND COUNTERS

Applications of Flip-flops :-

- (i) It can be used as a memory element.
- (ii) It can be used to eliminate key debounce.
- (iii) It is used as a basic building block in sequential circuits such as counters and Registers.
- (iv) It can be used as a delay element.
- (v)

REGISTERS :-

- (i) Register is a group of flip-flops.
- (ii) n-bit Register consists of n number of flip-flops and it stores n bit binary information.

Types of shift Registers:-

1. Serial In serial Out shift register (SISO) :-

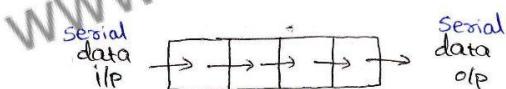


Fig: Data flow in SISO shift right register

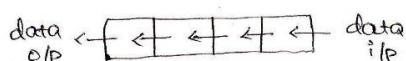


Fig: Data flow in SISO shift left register.

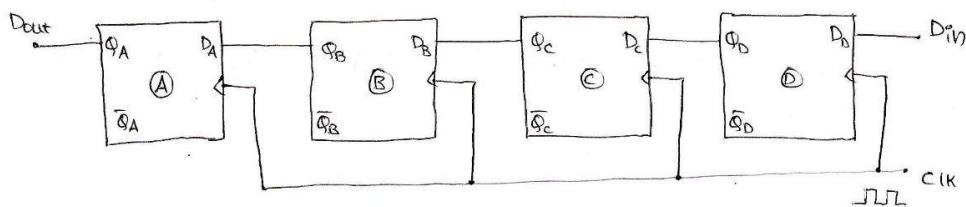


Fig: 4-bit SISO shift left register.

i/p to reg 1011

CLK	Q_A	Q_B	Q_c	Q_D	reg. o/p (D_{out})
0	0	0	0	0	
$\text{Fwd} \uparrow$	0	0	0	1	
\uparrow	0	0	1	0	
\uparrow	0	1	0	1	
\uparrow	1	0	1	1	→ i/p data stored in register.
\uparrow	0	1	1	0	
\uparrow	1	1	0	0	
\uparrow	1	0	0	0	→ all 4 data i/p bits are transferred to o/p side
\uparrow	0	0	0	0	→ reg. cleared.

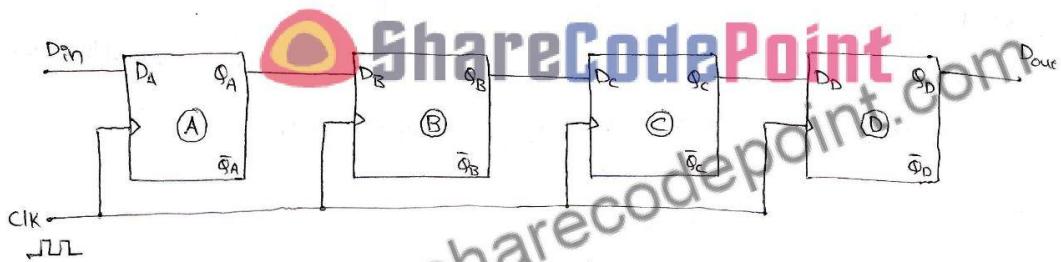


Fig:- 4-bit SISO shift right register.

2. Serial IN Parallel OUT shift Register (SIPO) :-

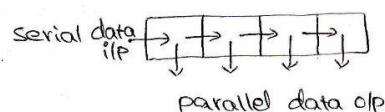


Fig:- data flow in SIPO shift right register.

In this case, data bits enters into register in serial, but o/p is taken in parallel.

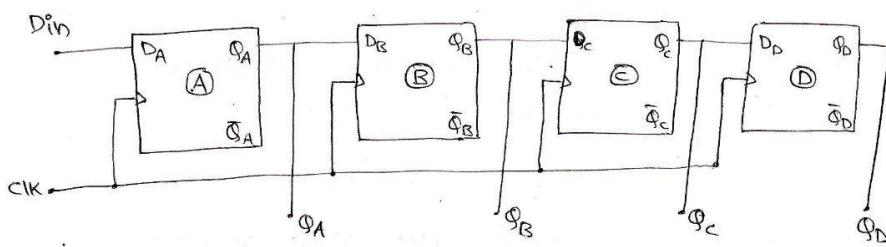


Fig: 4-bit SIPO shift right register.

D_{in} → Serial data i/p

$Q_A \ Q_B \ Q_C \ Q_D$ → 4-bit parallel data o/p.

Register with parallel load :-

- * the transfer of new information into a register is referred to as loading Register.
- * If all the bits of Register are loaded simultaneously with a common clock pulse, we say that the loading is done in parallel

3. Parallel IN parallel OUT shift register (PIPO) :-

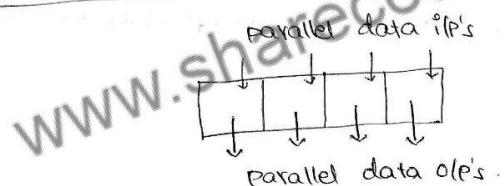


Fig: data flow in PIPO shift register.

Data bits are entered into reg in parallel.
and o/p is taken in parallel.

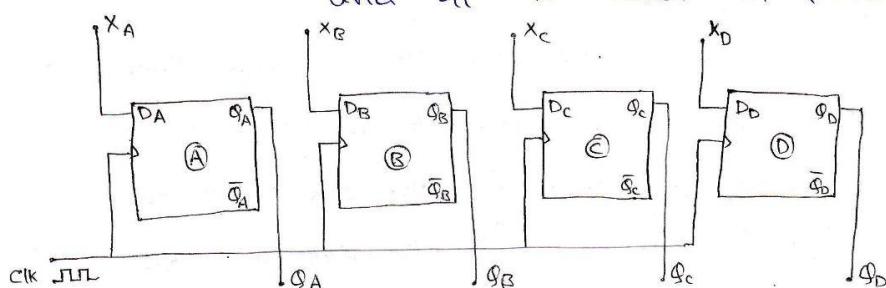


Fig: 4-bit PIPO shift register.

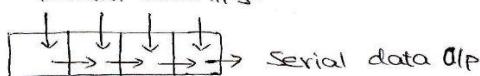
$X_A \ X_B \ X_C \ X_D$ → parallel data i/p's

$Q_A \ Q_B \ Q_C \ Q_D$ → 4-bit parallel data o/p.

07/10/2014

4. Parallel In serial Out shift Register (PISO) :-

Parallel data i/p's.



Serial data o/p

Fig: Dataflow in PISO shift right register.

I/P data entered into register parallelly but o/p is taken

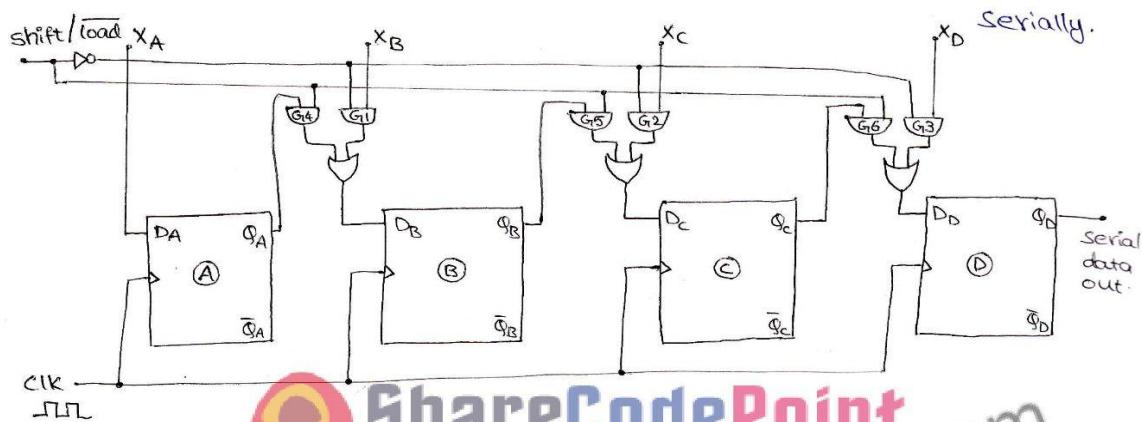


Fig: 4-bit PISO shift right register

$x_A, x_B, x_C, x_D \rightarrow$ parallel data i/p's

If shift/load = 0 then parallel data loads into reg.

when shift/load = 1, reg shifts the stored data to right

* Asynchronous (or) direct i/p's of flip-flops :-

(i) Set (or) Pre-set :-

If set i/p is high then flip-flop

o/p is '1' for any data i/p irrespective of data i/p's & clk i/p

If set is high \Rightarrow 1 \Rightarrow flip-flop will set

If set is low \Rightarrow 0 \Rightarrow flip-flop will set.

(ii) clear (or) reset:

If reset i/p is high then flip-flop o/p is '0' (for any data i/p) irrespective of clk & data i/p's

3

* Universal shift register:

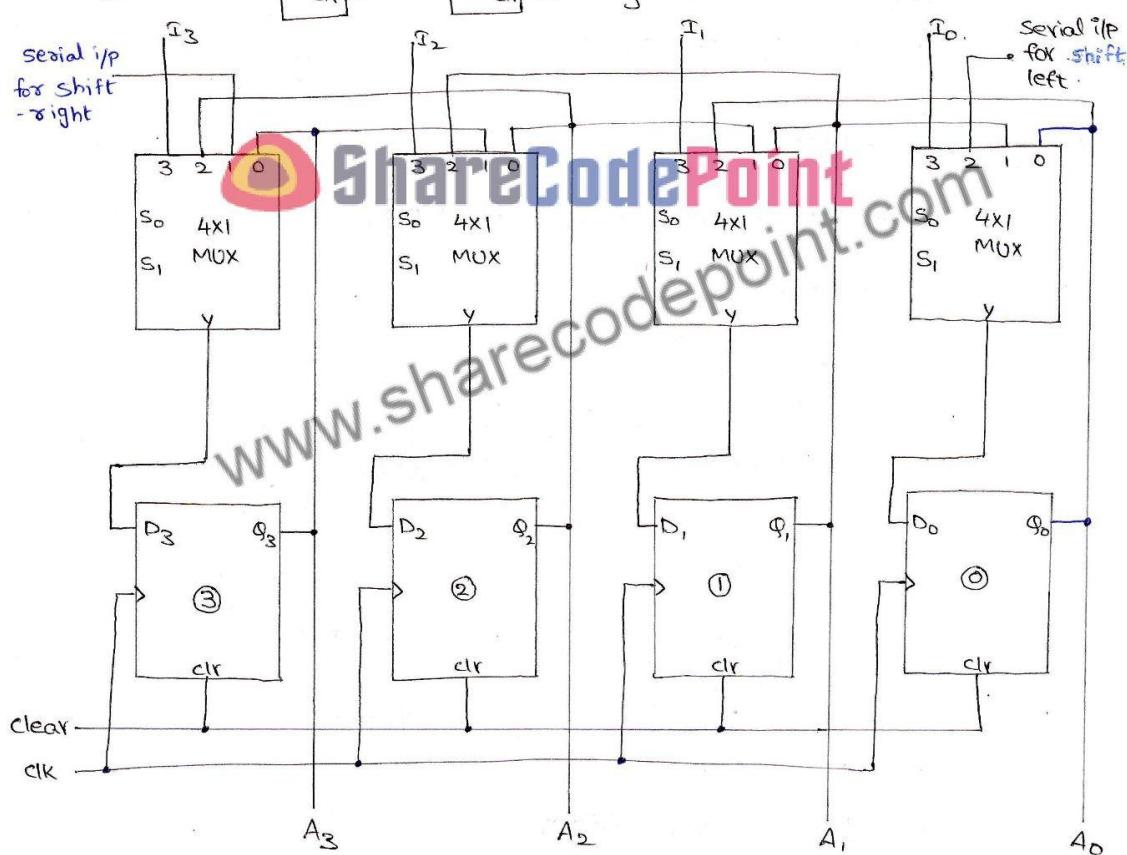
If the register has both ^{shift}_{both} (left & Right) and Parallel load capabilities, it is referred to as Universal shift register.

- acts like PISO, PIPO, SISO, SIPO
- acts like shift (right & left)
- (i.e) performs all operations.

Note:-



} both are same.



$S_0, S_1 \rightarrow$ are common selection i/p's, but not o/p's of previous MUX. For simplicity we have drawn in the above way.

Fig:- 4-bit universal shift register.

Function table :-

Mode control S ₁ S ₀	Reg. operation
0 0	NO change
0 1	shift right
1 0	shift left
1 1	parallel load.

I₃ I₂ I₁ I₀ → parallel i/p's

A₃ A₂ A₁ A₀ → parallel o/p's.

for '00' we observe all '0' connections in MUX,
gives o/p to D₁, D₂, D₃, D₀.

Similarly, for '11' we observe all '1' connections in MUX,
gives o/p to D₀, D₁, D₂, D₃.

* Serial Adder :-

It performs serial addition.

Block diagram:-

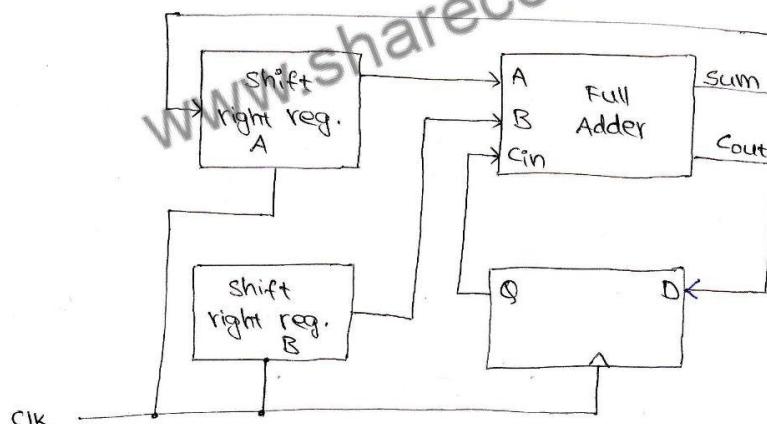


Fig.: Serial Adder

let us consider two numbers → $\begin{array}{r} 0 \\ 1 \\ 0 \\ 1 \end{array} + \begin{array}{r} 1 \\ 0 \\ 0 \\ 1 \end{array}$ → Intermediate carry
 considering A & B are 4 bit registers.
 (SISO shift right reg.)
 A reg. content is 1011.
 B reg. content is 1001.

$$\begin{array}{r}
 0 \ 1 \ 1 \\
 + 1 \ 0 \ 0 \ 1 \\
 \hline
 1 \ 0 \ 1 \ 0 \ 0
 \end{array}$$

end carry sum

serial adder performs operation.

4

$$A \leftarrow A+B$$

Arrow indicates dataflow direction.

when clk is applied Reg.'s performs shift right operation.

During shift right, LSB comes out & goes to full Adder.

and FF adds A, B, cin bits and transfers sum to A reg. & cout to D-FF.

After performing serial addition contents of

reg A \rightarrow 0100 (sum)

B \rightarrow 0000

FF D \rightarrow 1 (end carry)

Serial

Transfer :-

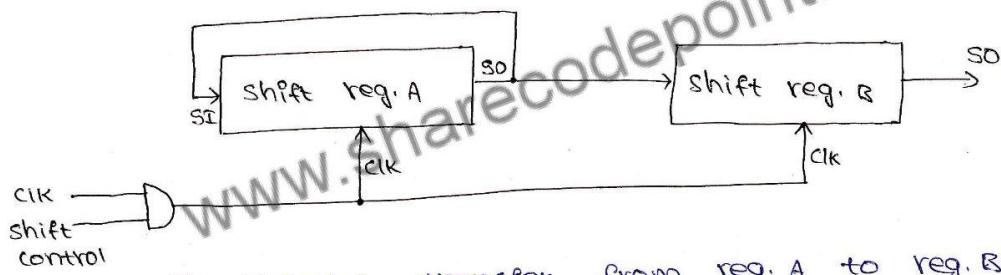


Fig:-(a) serial transfer from reg. A to reg. B.

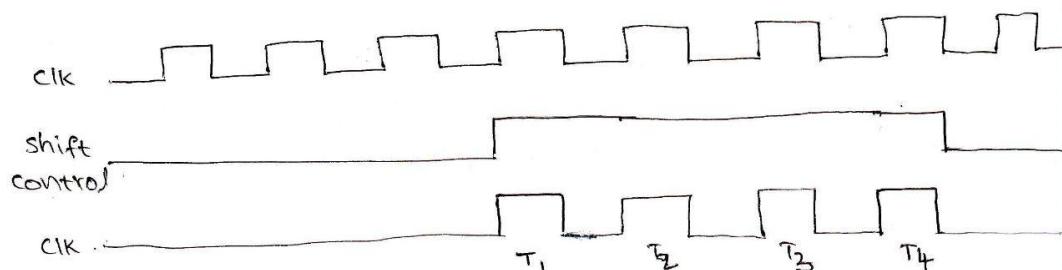


Fig:- (b) Timing diagram

considering A & B are 4-bit SISO shift right reg.'s.

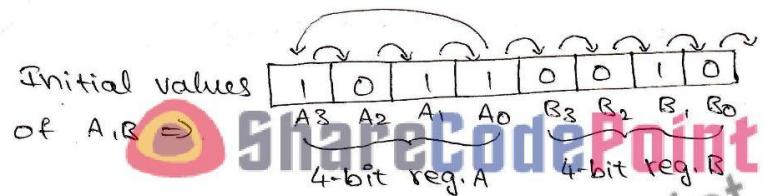
SO \rightarrow Serial out ; SI \rightarrow serial in.

The above ckt performs operation

$B \leftarrow A$ (or) $A \rightarrow B$ Arrow indicates direction of dataflow.

After performing register transfer operation $A=B$

Fig (a) performs shift operation only when shift control is high because reg.'s receives clk i/p only when shift control = 1.



serial transfer

Timing pulse	shift reg. A	shift reg. B
Initial value of reg.	1011	0010
After T_1	1101	1001
T_2	1110	1100
T_3	0111	0110
T_4	1011	1011

After T_4 , both A & B reg.'s content is same.

(i.e) $A=B$.

COUNTERS:-

A counter is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived.

(or)

A counter is essentially a register that goes through a predetermined sequence of binary states.

* counters are available in two categories.

1. Asynchronous counters.
2. Synchronous counters.

Asynchronous counters	Synchronous counters
<ol style="list-style-type: none">1. In this type of counter, flip-flops are connected in such a way that o/p of 1st FF drives the clk for the next FF.2. All the FF are not clocked simultaneously.3. logic circuit is very simple even for more number of states4. Main drawback of these counters is their low speed as the clk is propagated through no. of FF before it reaches last FF.	<ol style="list-style-type: none">1. In this type, there is no connection b/w o/p of 1st FF and clk i/p of the next FF.2. All the FF are clocked simultaneously.3. Design involves complex logic circuits as no. of states increases.4. As the clk is simultaneously given to all FF's there is no problem of propagation delay. Hence they are high speed counters.

Asynchronous (or) Ripple (or) serial counters (or) Non-synchronous counter:

1. 3-bit Asynchronous Up counter :-

An upcounter is a counter which counts in the upward direction. (i.e) 0, 1, 2, 3, ..., n.

state diagram:-

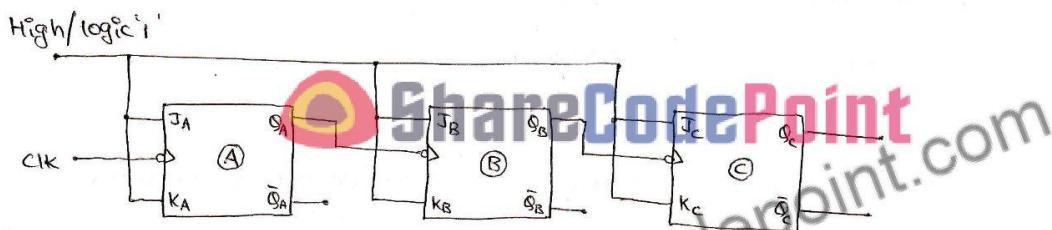
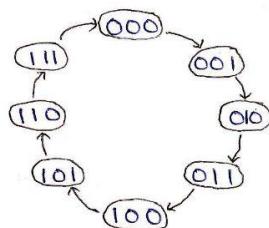
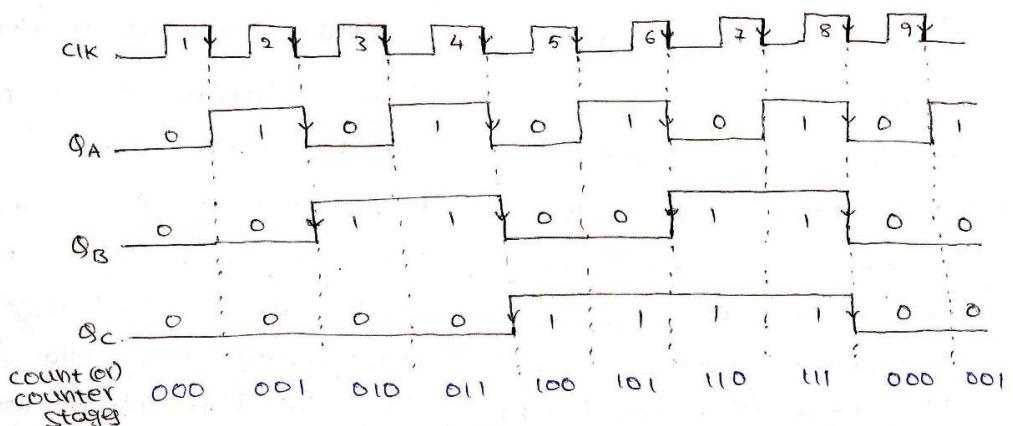


Fig.: 3-bit ripple up counter

using -ve edge triggered JK FF's.

counter o/p \rightarrow $Q_c \ Q_b \ Q_a$
MSB LSB

O/P waveforms



* The number of states through which the counter passes before returning to the starting state is called the Modulus of the counter.

(or)

The Mod number of a counter is the total no. of states it sequences through in each complete cycle.

* Since a 3-bit counter has 8 states it is called a Mod-8 (or) Modulus-8 counter. (or) Modulo-8 counter.

3-bit Ripple up counter using T-FF's:

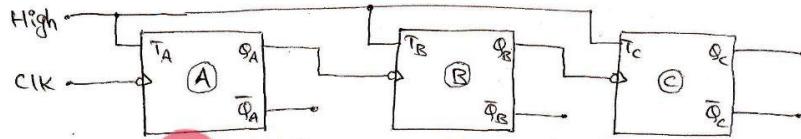


Fig:- 3-bit Asynchronous up counter using
'tve' edge triggered T-FF's.

counter o/p \rightarrow $Q_c \quad Q_b \quad Q_a$
MSB LSB.

Note:- For designing ripple up counter using 'tve' edge triggered FF's connect 't' o/p's to CLK i/p's of next flip-flops.

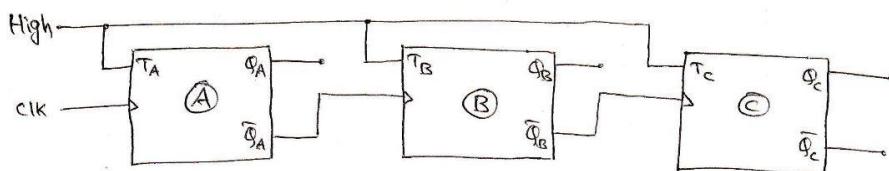


Fig:- 3-bit Ripple up counter using 'tve' edge triggered T-FF's.

Counter o/p \rightarrow $Q_c \quad Q_b \quad Q_a$
MSB LSB.

2. 3-bit Asynchronous down counter :-

Down counter counts in downward direction. (i.e) $n, n-1, n-2, \dots, 2, 1, 0$.

State diagram :-

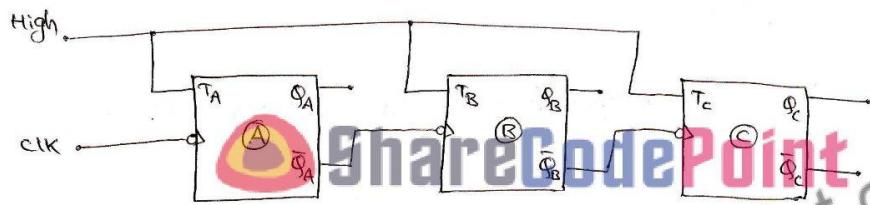
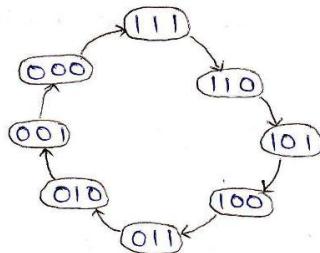
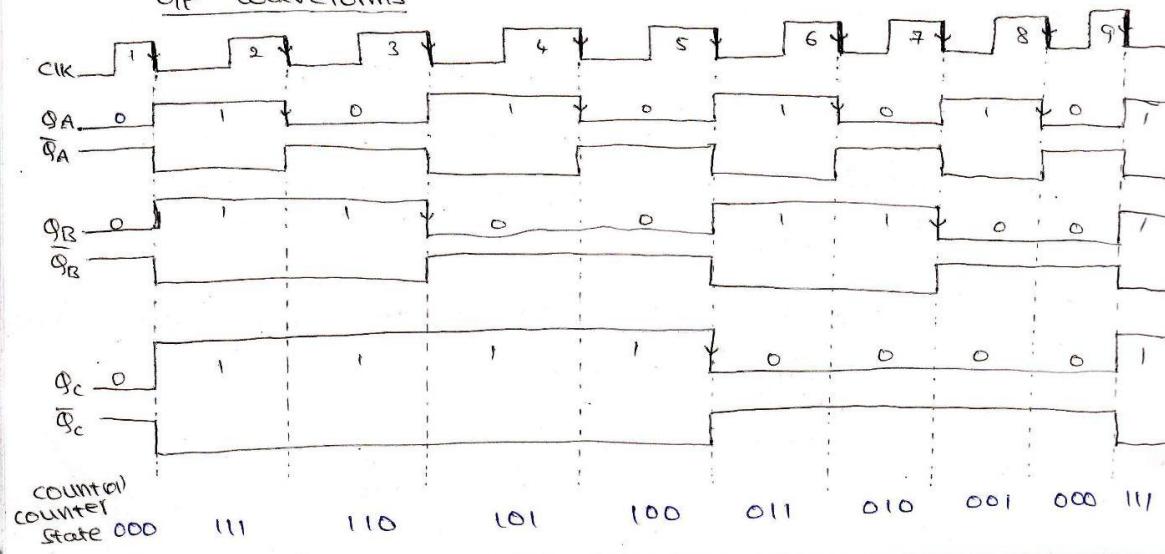


Fig.: 3-bit ripple down counter using -ve edge triggered T-FF's.

counter o/p $\rightarrow Q_c \ Q_b \ Q_a$
MSB LSB

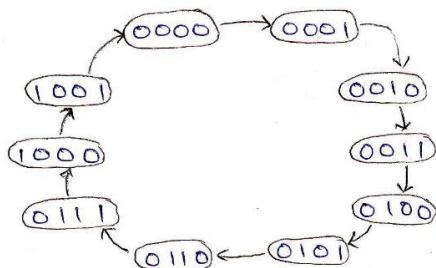
O/P waveforms



3. Asynchronous Mod-10 counter (or) Decade counter (or) 7

BCD counter :-

state diagram :-



for NAND gate

draw bubbles
for clrs i/p

for AND gate
Don't draw bubbles

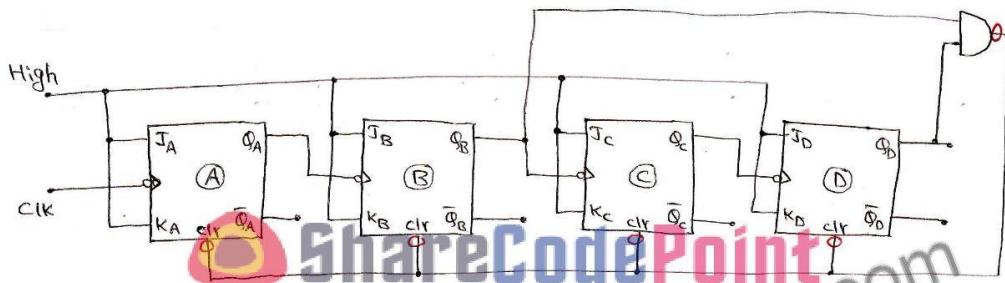


Fig: MOD-10 ripple counter.

counter o/p \rightarrow $Q_D \ Q_C \ Q_B \ Q_A$
MSB LSB

* When counter o/p is 1010, o/p of And gate becomes 1. Since o/p of And gate is connected to reset (or) clear i/p's of FF's, counter enters into 0000 state after 1010 state.

Truth table:-

CLK	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0

CLK	Q_D	Q_C	Q_B	Q_A
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0
11	0	0	0	1
12	0	0	1	0
13	0	0	1	1
14	0	1	0	0

4. Asynchronous Mod-12 counter :-

State diagram :-

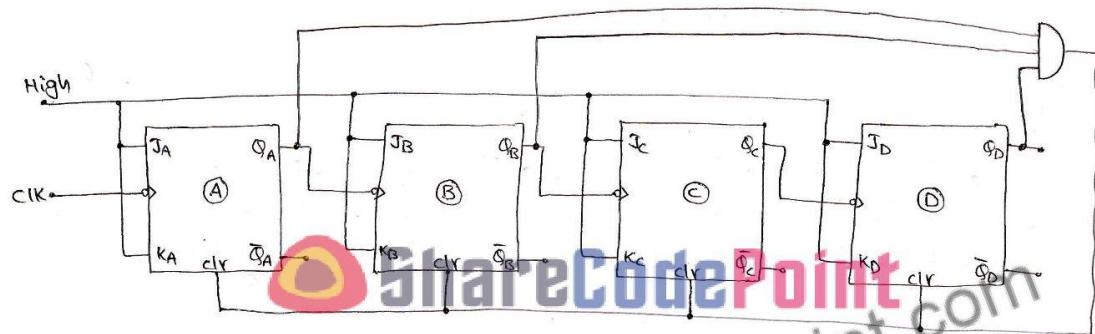
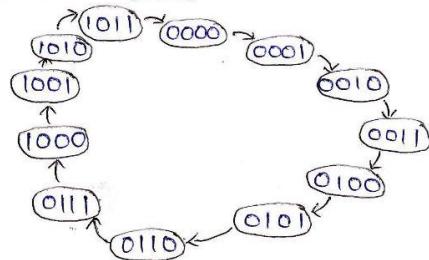


Fig:- MOD-12 ripple counter

counter o/p $\rightarrow Q_D \bar{Q}_C \bar{Q}_B \bar{Q}_A$
MSB LSB

* When counter o/p is $1011^{Q_0 Q_1 Q_2 Q_3}$, o/p of And gate becomes 1. Since o/p of And gate is connected to reset (or) clear i/p's of FF's, counter enters into 0000 state after 1011 state.

Truth table:-

CLK	Q_0	Q_1	Q_2	Q_3	Q_A
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0

CLK	Q_D	Q_C	Q_B	Q_A
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	0	0	0	0
13	0	0	0	1
14	0	0	1	0
15	0	0	1	1
16	0	1	0	0
17	0	1	0	1

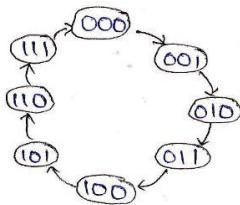
14/10/2014

Synchronous (or) Parallel counters :-

8

1. 3-bit synchronous Binary up counter (or) Mod-8 sync. counter:-

State diagram:-



Logic diagram:-

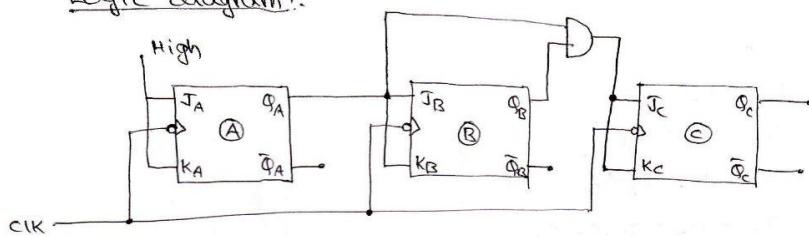


Fig:- MOD-8 Sync. counter
FF i/p's

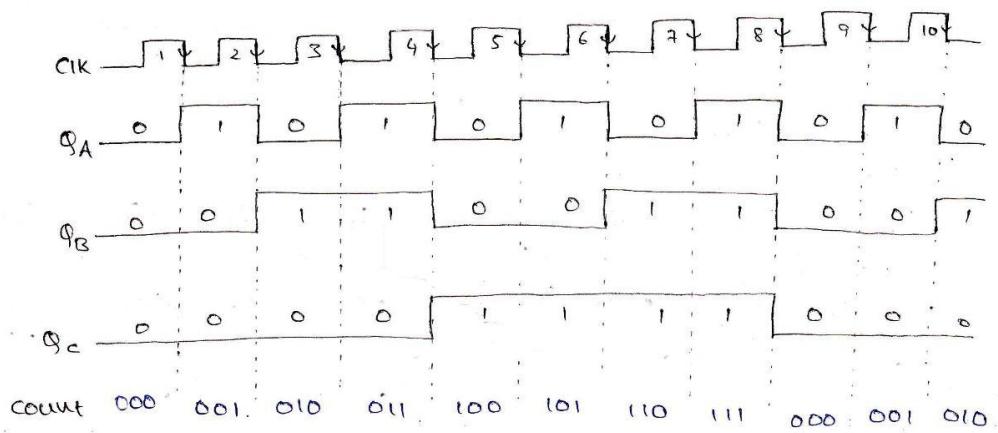
$$J_A = K_A = 1$$

$$J_B = K_B = Q_A$$

$$J_C = K_C = Q_A \cdot Q_B$$

counter o/p $\rightarrow Q_C \ Q_B \ Q_A$
MSB LSB

Output waveforms:-



2. 4-bit Synchronous Binary Up counter (or) MOD-16 counter:

Block diagram:

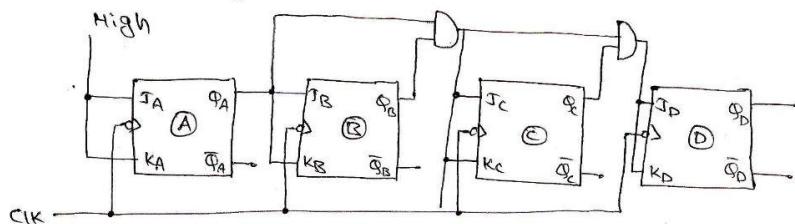


Fig: MOD-16 Binary up counter.

FF i/p's

$$J_A = K_A = 1$$

$$J_B = K_B = Q_A$$

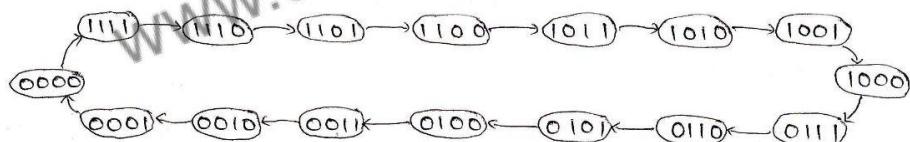
$$J_C = K_C = Q_A \cdot Q_B$$

$$J_D = K_D = Q_A \cdot Q_B \cdot Q_C$$

Counter  ShareCodePoint.com

3. 4-bit Synchronous Down counter (or) MOD-16 Down counter:-

State diagram:



Logic diagram:

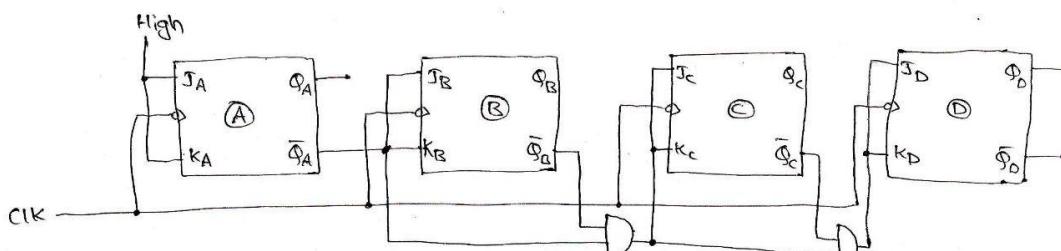


Fig: MOD-16 Down counter

FF i/p's

91

$$J_A = K_A = 1$$

$$J_B = K_B = \bar{Q}_A$$

$$J_C = K_C = \bar{Q}_A \bar{Q}_B$$

$$J_D = K_D = \bar{Q}_A \bar{Q}_B \bar{Q}_C$$

counter o/p $\rightarrow Q_D \quad Q_C \quad Q_B \quad Q_A$
MSB LSB

Truth table (or) Function table :-

CLK	counter o/p			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1

CLK	counter o/p			
	Q_D	Q_C	Q_B	Q_A
10	0	1	1	0
11	0	1	0	1
12	0	0	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0
17	1	1	1	1
18	1	1	1	0
19	1	1	0	1

* Design of Synchronous counters :-

Q. Design synchronous MOD-5 counter using JK flip-flops.

Sol:- Note:- If counter type is not mentioned then design up counter.

Step 1:- Determine number of flip-flops.

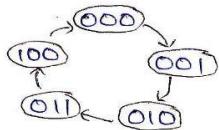
The no. of FF's required to design MOD-5 synchronous up counter can be determine by the equation, $2^n \geq N$ where $n \rightarrow$ no. of FF's $N \rightarrow$ MOD no.

The possible value of 'n' which satisfies the above equation is 3.

thus MOD-5 counter uses 3 FF's.

Step 2:- Flip-flop type - JK FF.

Step 3 :- State diagram



Step 4 :- Excitation table

Present Stage			Next Stage			FF i/p's					
Q_C	Q_B	Q_A	Q_{Ct1}	Q_{Bt1}	Q_{At1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

\therefore JK FF
Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 5 :- K-map simplification

for J_C			
$Q_C \backslash Q_B Q_A$	00	01	11
0	0	1	1
1	X	X	X

$$\therefore J_C = Q_B Q_A$$

for J_B			
$Q_C \backslash Q_B Q_A$	00	01	11
0	0	1	1
1	X	X	X

$$\therefore J_B = Q_A$$

for J_A			
$Q_C \backslash Q_B Q_A$	00	01	11
0	1	X	1
1	X	X	X

$$\therefore J_A = \bar{Q}_C$$

for K_C			
$Q_C \backslash Q_B Q_A$	00	01	11
0	X	X	X
1	X	X	X

$$\therefore K_C = 1$$

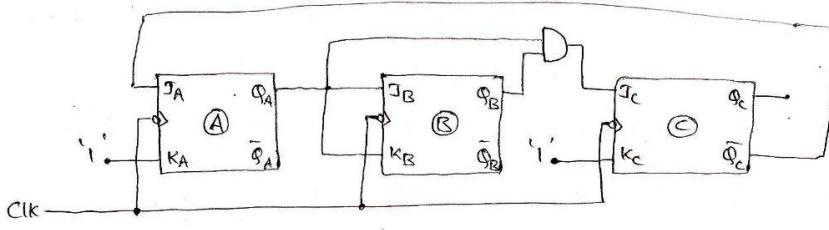
for K_B			
$Q_C \backslash Q_B Q_A$	00	01	11
0	X	X	1
1	X	X	X

$$\therefore K_B = Q_A$$

for K_A			
$Q_C \backslash Q_B Q_A$	00	01	11
0	X	1	1
1	X	X	X

$$\therefore K_A = 1$$

Step 6 :- Logic diagram



15/10/2014

Q. Design MOD-10 synchronous up counter using T-Flip-flops.

10

(Decade counter / BCD counter / MOD-10 counter).

Sol: Step 1: Determine no. of FF's required.

$$2^n \geq N \quad \text{where } N \rightarrow \text{Mod No.}$$

$$n \rightarrow \text{no. of FF's.}$$

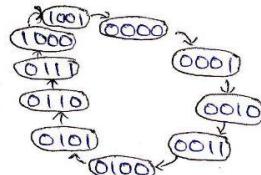
$$2^n \geq 10$$

$$n = 4$$

$$\therefore \text{No. of FF's required} = 4$$

FF TYPE \rightarrow T-FF

Step 2: State diagram



Step 3:

Excitation table

Present Stage $Q_0\ Q_1\ Q_2\ Q_3$	Next Stage $Q_{0+1}\ Q_{1+1}\ Q_{2+1}\ Q_{3+1}$	FF i/p's			
		T_D	T_C	T_B	T_A
0 0 0 0	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1
0 0 0 1	0 0 1 0	0 0 1 0	0 0 1 0	0 0 1 1	0 0 1 1
0 0 1 0	0 0 1 1	0 0 1 1	0 0 1 1	0 0 0 1	0 0 0 1
0 0 1 1	0 1 0 0	0 1 0 0	0 1 1 1	0 1 1 1	0 1 1 1
0 1 0 0	0 1 0 1	0 1 0 1	0 0 0 1	0 0 0 1	0 0 0 1
0 1 0 1	0 1 1 0	0 1 1 0	0 0 0 1	0 0 1 1	0 0 1 1
0 1 1 0	0 1 1 1	0 1 1 1	0 0 0 1	0 0 0 1	0 0 0 1
0 1 1 1	1 0 0 0	1 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1
1 0 0 0	1 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1
1 0 0 1	0 0 0 0	1 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1
1 0 1 0	X X X X	X X X X	X X X X	X X X X	X X X X
1 0 1 1	X X X X	X X X X	X X X X	X X X X	X X X X
1 1 0 0	X X X X	X X X X	X X X X	X X X X	X X X X
1 1 0 1	X X X X	X X X X	X X X X	X X X X	X X X X
1 1 1 0	X X X X	X X X X	X X X X	X X X X	X X X X
1 1 1 1	X X X X	X X X X	X X X X	X X X X	X X X X

\therefore T-FF excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4 : K-Map Simplification

for T_D

		$\bar{Q}_D \bar{Q}_C$	$\bar{Q}_B \bar{Q}_A$		
		00	01	11	10
		00		1	X
		01		X	X
		11	X	X	X
		10	1	X	X

$$\therefore T_D = Q_D \bar{Q}_A + Q_C \bar{Q}_B \bar{Q}_A$$

for T_C

		$\bar{Q}_D \bar{Q}_C$	$\bar{Q}_B \bar{Q}_A$		
		00	01	11	10
		00		1	X
		01		1	X
		11	X	X	X
		10		X	X

$$\therefore T_C = \bar{Q}_B \bar{Q}_A$$

for T_B

		$\bar{Q}_D \bar{Q}_C$	$\bar{Q}_B \bar{Q}_A$		
		00	01	11	10
		00		1	1
		01	1	1	
		11	X	X	X
		10		X	X

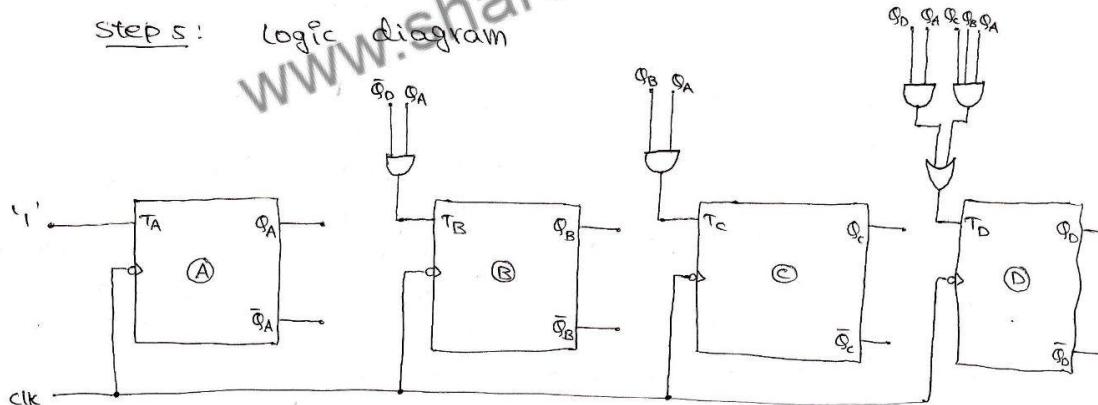
$$\therefore T_B = \bar{Q}_D \bar{Q}_A$$

for T_A

		$\bar{Q}_D \bar{Q}_C$	$\bar{Q}_B \bar{Q}_A$		
		00	01	11	10
		00	1	1	1
		01	1	1	1
		11	X	X	X
		10	1	X	X

$$\therefore T_A = 1$$

Step 5 : logic diagram



counter o/p $\rightarrow Q_D \ Q_C \ Q_B \ Q_A$
MSB LSB

Counter with unused states :-

Q. Design a modulo-5 counter to count the sequence 0, 1, 3, 7, 6. Design should include circuitry to ensure that if we end up in an unwanted state, the next clock pulse will reset the counter to $Q_2, Q_1, Q_0 = 000$. Use T-flipflops.

Sol:- Step 1: no. of FF's required to design MOD-5 counter can be determined by equation,

$$2^n \geq N \quad \text{where } n \rightarrow \text{no. of FF's.}$$

$$N \rightarrow \text{MOD no.}$$

$$\therefore 2^n \geq 5$$

$$\therefore n=3$$

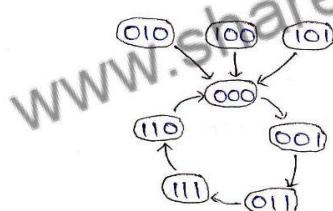
∴ no. of FF's required $\rightarrow 3$

FF's using \rightarrow T FF's.

Step 2: State diagram

used states $\rightarrow 0, 1, 3, 7, 6$

unused states $\rightarrow 2, 4, 5$



(\because for unused states next stage is 000)

Step 3: Excitation table

Present State Q_2, Q_1, Q_0	Next State $Q_{2+1}, Q_{1+1}, Q_{0+1}$ (or) Q_2^+, Q_1^+, Q_0^+	FF i/p's		
		T_2	T_1	T_0
0 0 0	0 0 1	0	0	1
0 0 1	0 1 1	0	1	0
0 1 0	0 0 0	0	1	0
0 1 1	1 1 1	1	0	0
1 0 0	0 0 0	1	0	0
1 0 1	0 0 0	1	0	1
1 1 0	0 0 0	1	1	0
1 1 1	1 1 0	0	0	1

\therefore T-FF excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4: K-map simplification

for T_2

		Q ₂ Q ₁	00	01	11	10
		0	0	0	1	0
		1	1	1	0	C

$$\therefore T_2 = Q_2 Q_1 + Q_2 \bar{Q}_0 + \bar{Q}_2 Q_1 \bar{Q}_0$$

for T_1

		Q ₂ Q ₁	00	01	11	10
		0	0	1	0	1
		1	1	0	1	1

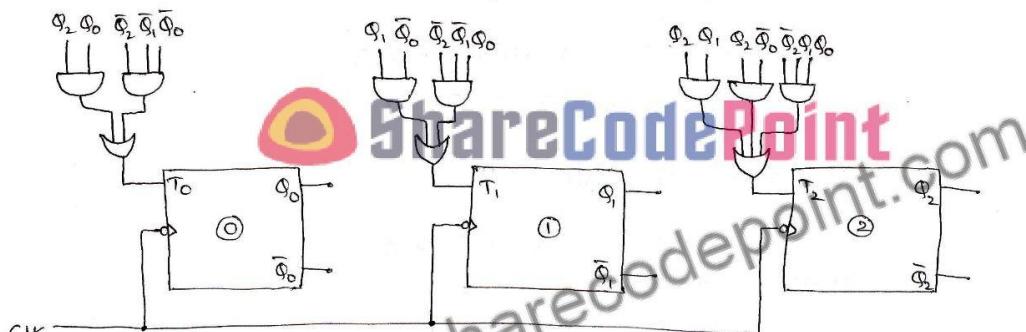
$$\therefore T_1 = Q_1 \bar{Q}_0 + \bar{Q}_2 \bar{Q}_1 \bar{Q}_0$$

for T_0

		Q ₂ Q ₁	00	01	11	10
		0	1	0	0	0
		1	0	1	1	1

$$\therefore T_0 = \bar{Q}_2 \bar{Q}_1 \bar{Q}_0 + Q_2 Q_0$$

Step 5: Logic diagram



counter output $\rightarrow Q_2 \ Q_1 \ Q_0$
MSB LSB

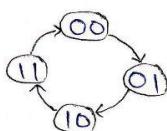
Q. Design a synchronous counter with states 0, 1, 2, 3,

0, 1, Using JK FF's.

Sol: Counter states are 0, 1, 2, 3, 0, 1, ...

\therefore It is MOD-4 counter.

State diagram:-



Q. Design synchronous counter using JK FF. to count 12
the following sequence.

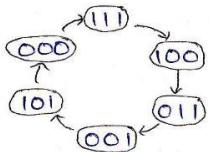
7, 4, 3, 1, 5, 0, 7, -----

Sol: Total no. of states \rightarrow 6

\therefore It is MOD-6 counter.

Used states \rightarrow 7, 4, 3, 1, 5, 0.

State diagram:-



Unused states \rightarrow 2, 6.

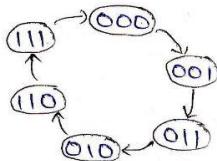
Treat unused states as don't cares.

Q. Design a synchronous gray code MOD-6 up counter.

Sol:

	Binary	Gray
0	0 0 0	0 0 0
1	0 0 1	0 0 1
2	0 1 0	0 1 1
3	0 1 1	0 1 0
4	1 0 0	1 1 0
5	1 0 1	1 1 1

State diagram:-



Unused states are 4, 5.

\therefore treat them as don't cares.

* Synchronous up/down counter (or) Multimode counter (or)

Bidirectional counter :-

Q. Design 3-bit synchronous up/down counter.

Sol: → The counter which is capable of progressing in either direction (i.e) in ascending order (incrementing order) (or) descending order (decreasing order) through a certain counting sequence is known as up/down counter.

→ Usually, up/down operation of the counter is controlled by up/down (M) signal.

→ When $M=1$, the counter goes through up sequence ($0, 1, 2, \dots, n$).

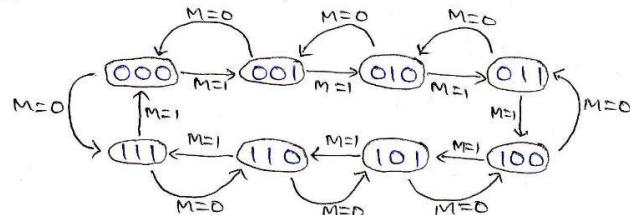
→ When $M=0$, the counter goes through down sequence ($n, n-1, \dots, 2, 1, 0$).

Step 1:

No. of FF's required $\rightarrow 3$ (\because it is 3-bit counter)

FF's using \rightarrow T FF's.

Step 2: State diagram



Step 3: Excitation table

(13)

control i/p UP/down (M)		present state			Next stage $Q_{A+1}, Q_{B+1}, Q_{A+1}$			FF i/p's		
		Q_A	Q_B	Q_C	T_c	T_B	T_A	Q_A	Q_B	Q_C
Down	0	0	0	0	1	1	1	1	1	1
	0	0	0	1	0	0	0	0	0	1
	0	0	1	0	0	0	1	0	1	1
	0	0	1	1	0	1	0	0	0	1
	0	1	0	0	0	1	1	1	1	1
	0	1	0	1	1	0	0	0	0	1
	0	1	1	0	1	0	1	0	1	1
	0	1	1	1	1	1	0	0	0	1
UP	1	0	0	0	0	0	1	0	0	1
	1	0	0	1	0	1	0	0	1	1
	1	0	1	0	0	1	1	0	0	1
	1	0	1	1	1	0	0	1	1	1
	1	1	0	0	1	0	1	0	0	1
	1	1	0	1	1	1	0	0	1	1
	1	1	1	0	0	0	1	0	0	1
	1	1	1	1	0	0	0	1	0	1

$\therefore T\text{-FF}$
excitable
table

Q_n	Q_{n+1}	T
00	0	0
01	1	
10	1	1
11	0	0

Step 4: K-map simplification

		$Q_B Q_A$	00	01	11	10
		$M Q_C$	00	01	11	10
<u>for T_c</u>	<u>for T_B</u>	00	1			
		01	1			
<u>for T_c</u>	<u>for T_B</u>	11		1		
		10		1	1	

$$\begin{aligned}\therefore T_c &= \bar{M} \bar{Q}_B \bar{Q}_A + M \bar{Q}_B Q_A \\ &= M \bar{Q}_B \oplus Q_A\end{aligned}$$

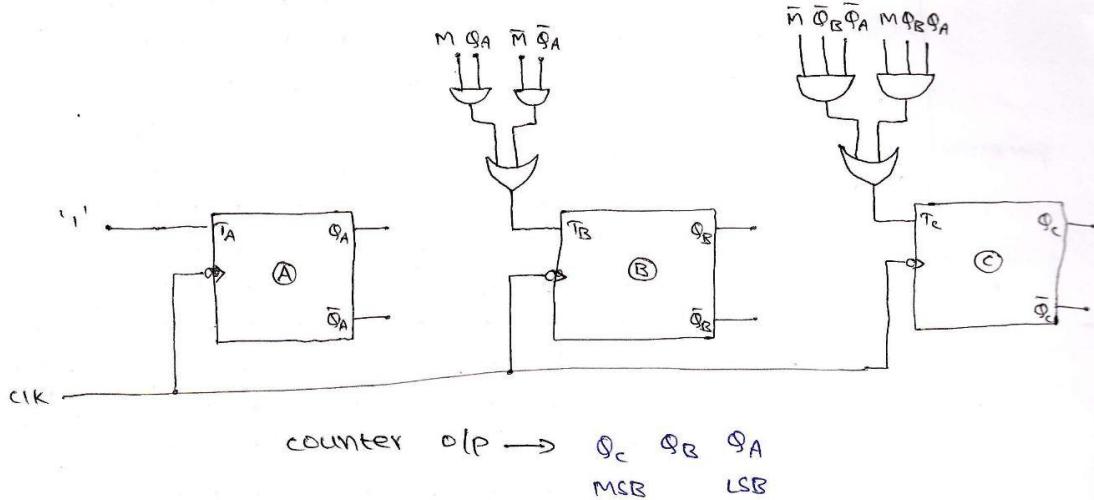
		$Q_B Q_A$	00	01	11	10
		$M Q_C$	00	01	11	10
<u>for T_c</u>	<u>for T_B</u>	00	1			
		01	1			

$$\begin{aligned}\therefore T_B &= \bar{M} \bar{Q}_A + M Q_A \\ &= M \bar{Q}_A\end{aligned}$$

		$Q_B Q_A$	00	01	11	10
		$M Q_C$	00	01	11	10
<u>for T_A</u>	<u>for T_B</u>	00	1	1	1	1
		01	1	1	1	1

$$\therefore T_A = 1$$

logic diagram :-



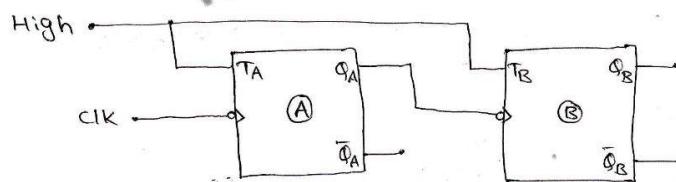
16/10/2014

* Frequency dividers :-

2-bit Asynchronous counter (or) MOD-4 counter (or)

Divide - by - 4 counter :-

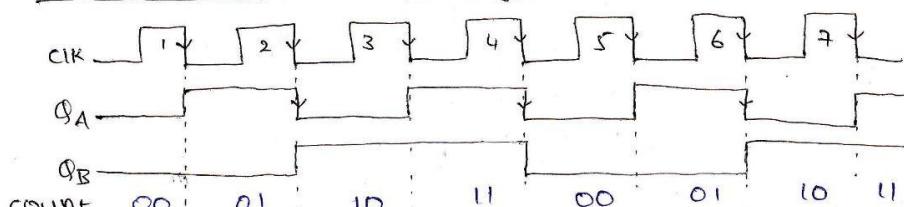
logic diagram:-



counter o/p \rightarrow $Q_b \ Q_a$
MSB LSB

fig:- 2-bit ripple counter.

O/P waveform (or) Timing diag. of 2-bit ripple counter:-



* From the timing diagram it is clear that the frequency of Q_A is one half of the frequency of clk signal, Q_B is one half of Q_A and Q is one fourth of the clk frequency.

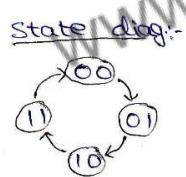
* If the clk frequency is 1000 Hz, then $Q_A = 500$ Hz & $Q_B = 250$ Hz. Hence the 2-bit ripple counter is also called as divide-by-4 counter.

Note:- Each FF acts as a divide by 2 ($\div 2$) frequency divider. (i.e) Each FF divides the incoming clk signal frequency by 2.

3-bit counter \rightarrow	MOD-8 counter \rightarrow	Divide-by-8 counter
4-bit counter \rightarrow	MOD-16 counter \rightarrow	Divide-by-16 counter
MOD-5 counter \rightarrow	Divide-by-5 counter	
MOD-6 counter \rightarrow	Divide-by-6 counter	

State table :-

The state table represents the state diagram in tabular form.



State table :-

Present State	Next State
0 0	0 1
0 1	1 0
1 0	1 1
1 1	0 0

* Lock out condition :-

In a counter if the next state of some unused state is again an unused state and if by chance the counter happen to find itself in the unused states and never arrived at a used state then the counter is said to be in the "lockout condition".

The circuit that goes in lockout condition is called "bushless circuit"

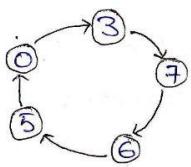


Fig: a) Desired sequence

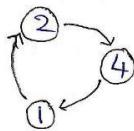


Fig: b) Unused states forming lockout.

To avoid lockout condition, the unused states are introduced in front of the used states.

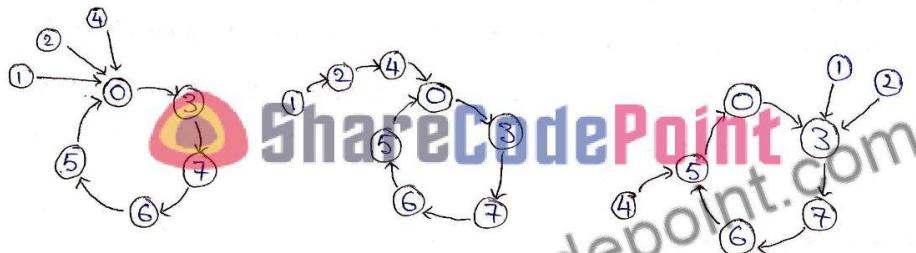
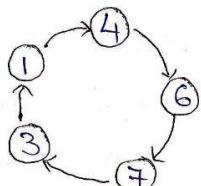


Fig: state diagrams for removing lockout.

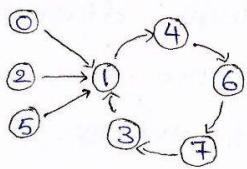
Q: Design a synchronous counter for the following sequence. $4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4 \dots$
Avoid lockout condition use JK type of design.

Sol: state diagram:-



Used states $\rightarrow 1, 3, 4, 6, 7$

Unused states $\rightarrow 0, 2, 5$



(or)

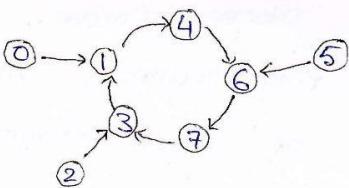


Fig: state diagrams for Avoiding lockout condition.

* Shift Register counters :-

A shift Register counter is basically a shift register with the serial o/p connected back to the serial i/p to produce special sequences. These devices are classified as counters because they exhibit a special sequence of states.

Two of the most common types of shift Register counters are

(i) Ring counter

(ii) Johnson counter

1. Ring counter :-

A Ring counter is a circular shift register with only 1 FF being set at any particular time, all others are cleared.

The single bit is shifted from one FF to the next to produce the sequence of timing signals.

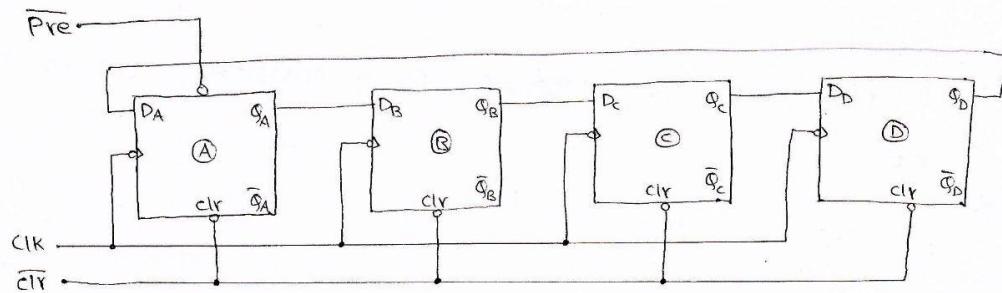


Fig.: 4-bit ring counter.

clr → clear (or)
Reset i/p
Pre → Set (or)
clock i/p

The above figure shows the logic diagram of 4-bit ring counter. As shown in the fig., the Q output of each stage is connected through the D input of the next stage and the output of the last stage is fed back to the D₀ of first stage. The CLR & PRE inputs are used to make the o/p of first stage to 1 and remaining o/p's to zeros.

(i.e) $Q_A Q_B Q_C Q_D = 1000$.

Truth table:-

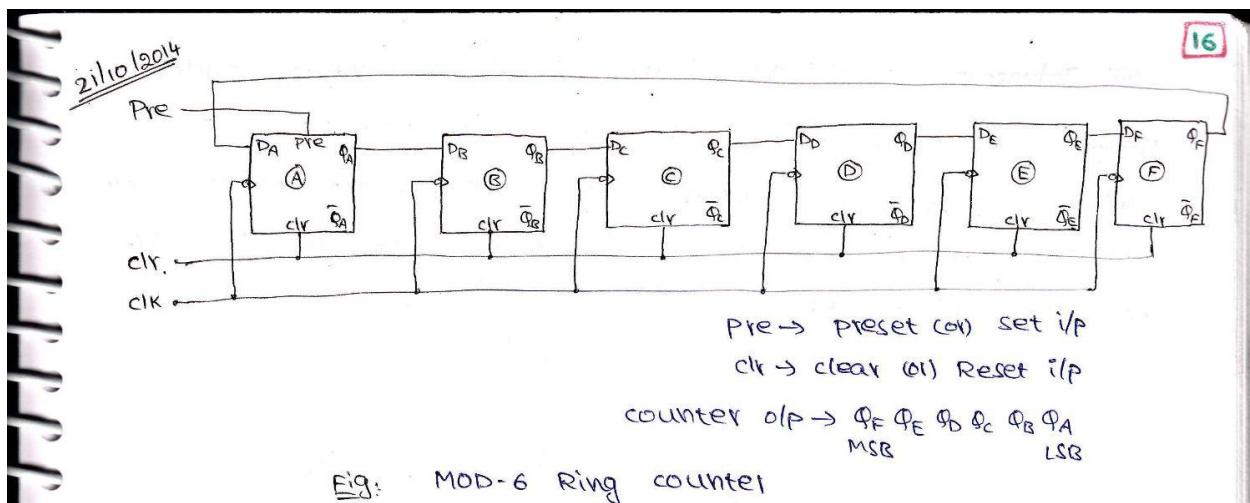
CLK	Q _A	Q _B	Q _C	Q _D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0

Since the 4-bit ring count has 4 distinct states, it is also known as a MOD-4 counter.

Note:- A MOD-N ring counter will require 'N' no. of flip-flops connected together to circulate a single data bit providing 'N' different o/p states.

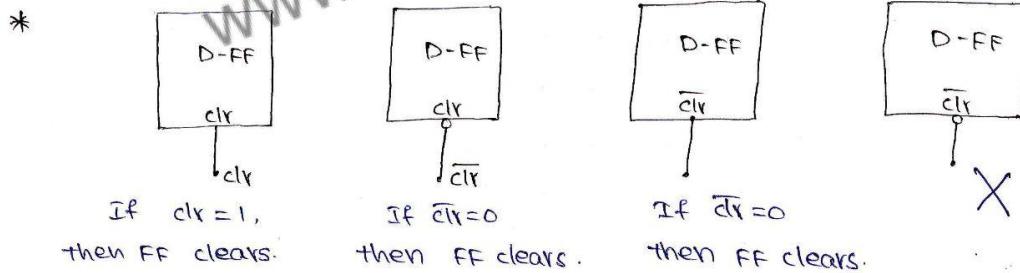
Q:- Implement a MOD-6 Ring counter using suitable FF's.

Sol:-



Truth table:-

clk	Q _A	Q _B	Q _C	Q _D	Q _E	Q _F
0	1	0	0	0	0	0
1	0	1	0	0	0	0
2	0	0	1	0	0	0
3	0	0	0	1	0	0
4	0	0	0	0	1	0
5	0	0	0	0	0	1
6	1	0	0	0	0	0

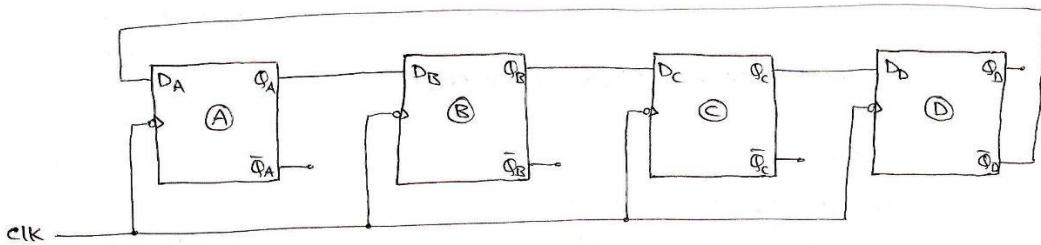


* Johnson counter (or) Twisted ring counter (or) switch tile ring counter :-

- (i) the 'n' bit ring counter circulates a single bit among the FF's to provide 'n' different states.
- (ii) The no. of states can be doubled if the shift register is connected as a switch tile counter.

(iii) Johnson counters have basic counting cycles of length 2^n , where 'n' is the no. of FF's.

(iv). In Johnson counter, the compliment of the o/p of the last FF is connected back to the i/p of the first FF.



counter o/p $\rightarrow Q_0 Q_1 Q_2 Q_3$

MSB LSB

Fig: 4-bit Johnson ring counter.

Truth table (on state sequence)

CLK	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

