

**END TERM EXAMINATION**

THIRD SEMESTER [B.TECH.] JANUARY-FEBRUARY 2023

Paper Code: AIDS/AIML/IOT-205

Subject: Digital Logic Design

Time: 3 Hours

Maximum Marks: 75

**Note:** Attempt five questions in all including Q. No. 1 which is compulsory. Select one question from each unit. Assume missing data, if any.

**Q1** (a) Convert the followings:- (3)

(i)  $(225.225)_{10}$  to (...) $_2$  (ii)  $(2AC5.D)_{16}$  to (...) $_10$

(iii)  $(CAFÉ)_{16}$  to (...) $_8$

(b) Minimize the following Boolean expressions:- (3)

(i)  $\underline{AB + A\bar{C} + A\bar{B}C(AB + C)}$

(ii)  $\underline{AB + \bar{A}\bar{B}C + A(B + AB)}$

(iii)  $\underline{AB + \bar{C} + (\bar{A} + B + C)}$

(c) Explain the implicants, Prime implicants and Essential Prime implicants with suitable examples. (3)

(d) Illustrate the design procedure used to design the combinational circuits. (3)

(e) Compare between combinational and Sequential circuits. (3)

**UNIT-I**

**Q2** (a) Discuss the common features between the different number systems and also perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. (7.5)

(i)  $101011 - 111000$  (ii)  $1110 - 110010$  (iii)  $11010 - 1101$

(b) State and prove Absorption and Consensus Laws in Boolean algebra. (7.5)

**OR**

**Q3** (a) Explain the error detection and error correction codes. A 7-bit Hamming code is received as 0101101. Find the correct code? (7.5)

(b) Express the function  $Y = A + \bar{B}C$  in

(i) Canonical SOP form (ii) Canonical POS form (7.5)

**UNIT-II**

**Q4** (a) Solve the logical expression  $Y = ABCD + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + AB$  on a 4-variable K-map and obtain the simplified expression from the map. (7.5)

(b) Using K-map method, simplify the following Boolean function and obtain (i) minimal SOP and (ii) minimal POS expressions : (7.5)

$$Y = \Sigma m(0,2,3,6,7) + \Sigma d(8,10,11,15)$$

**OR**

**Q5** (a) Realize (a)  $Y = A + B\bar{C}\bar{D}$  using NAND gates. (7.5)

(b)  $Y = (A + C)(A + \bar{D})(A + B + \bar{C})$  using NOR gates.

(b) Obtain the minimal sum of products expression for the following function and implement the same using universal gates. (7.5)

$$F(A, B, C, D) = \Sigma(0,2,3,5,7,8,13) + \Sigma d(1,6,12)$$

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UNIT-III

- Q6.** (a) Design the following using logic gates and truth tables:-  
 (i) 3 to 8 decoder      (ii) Octal to binary encoder.  
 (b) Discuss the 2-bit magnitude comparator with suitable expression and digital circuit.

(17.5)

logical

(7.5)

OR

- Q7 (a) Implement the following Boolean function  $F(A,B,C,D)$   
 $m(2,5,8,9,10,14,15)$  by using:  
(i) 8x1 Mux      (ii) 4x1 Mux  
(b) List the differences among ROM, PROM, EPROM and EEPROM

$$= \Sigma$$

(7.5)

15

UNIT-IV

- Q8** (a) Describe the race-around problem in J-K FF. With the help of suitable logic diagram explain how it is eliminated in Master-Slave J-K FF. (7.5)  
 (b) What is a shift register? Explain the working of a serial in- serial out register with logic diagram and waveforms. (7.5)

OR

- Q9** (a) Draw the circuit diagram of 4-bit ring counter using D flip flops and explain its operation with the help of waveforms. (7.5)  
(b) Discuss the following:- (7.5)  
    (i) Programmable Logic Array (PLA)  
    (ii) Programmable Array Logic (PAL)

(7.5)

(7.5)

Total No. of Pages: 2

Student Name: Kanishk .....

Enrollment No: 23 .....

### Mid-Term Examination – November 2022

Programme: B.Tech (AI&DS), (AI&ML), (IIoT)

Semester: Third Semester (Sep. 2022 – Jan. 2023)

Paper Code: AIDS205/AIML205/IOT205

Paper Name: Digital Logic Design

Time: 1½Hrs.

Maximum Marks: 30

Note:

- Question No. 1 is compulsory.
- Attempt any two questions from the remaining questions.
- Some questions have internal choice also.
- All questions carry equal marks.

Q. No.	Question 1	Marks	CO	BL
1(a)	Convert the hexadecimal number 3BD into an equivalent octal number.	[1]	CO1	3
1(b)	Find the two's complement of the number 11001011 without inverting and adding one. Also write the process followed to find the same.	[1]	CO1	3
1(c)	Analyze the function performed by an AND gate with schematic "bubbles" on its inputs.	[1]	CO2	4
1(d)	Convert the Gray code number (11010) to decimal number.	[1]	CO2	3
1(e)	Illustrate with the help of an example, the difference between prime implicant and essential prime implicant.	[1]	CO3	3
1(f)	Evaluate according to Idempotent Law if $X+X = X/2X/0/1$ . (Choose one Correct Option).	[1]	CO2	5
1(g)	Evaluate the expression $Y=AB+BC+AC$ and identify the correct operation POS/SOP/NOR/EX-OR/AND. (Choose one correct option).	[1]	CO3	5
1(h)	'Parity check technique can be employed successfully to detect and correct errors in transmitted codes.' Analyze and justify whether this statement is true or false.  OR 'Excess 3 is weighted code and is a modified form of BCD code' Analyze and justify whether this statement is true or false.	[1]	CO1	4
1(i)	Using K-Map, simplify $xy + x'y + x'y'$ .	[1]	CO3	3
1(j)	Find the Complement of the expression $A'B + CD$ .	[1]	CO1	3
Question 2				
2(a)	Using basic Boolean theorem prove: $(x+y)(x+z)=x+yz$	[3]	CO2	3

2(b)	First obtain the truth table of the following function and then implement the simplified function with the appropriate logic gates. $F = xy + y'z + x'y + x'z$	[4]	CO2	3																
2(c)	Hamming code is useful for both detection and correction of error present in the received data. Explain how? If we get the Hamming code as $b_7b_6b_5b_4b_3b_2b_1 = 1001011$ . Find the error position when the code received is $b_7b_6b_5b_4b_3b_2b_1 = 1001111$ .	[3]	CO2	4																
OR																				
	Draw and analyze switch equivalent circuits of NAND, NOT and X-OR.																			
<b>Question 3</b>																				
3(a)	Obtain the simplified expressions in (i) sum of products and (ii) product of sums of the following function: $F = x'z' + y'z' + yz' + xyz$	[3]	CO3	3																
3(b)	Simplify the following equation by K-Map and build the equivalent digital circuit $F(x,y,z) = \sum m(0,2,4) + \sum d(1,3,5,6,7)$	[4]	CO3	6																
OR																				
	You are given two X-OR gates. First design a buffer using these two gates and then design an inverter.																			
3(c)	<p style="text-align: center;">A</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>d</td><td></td><td></td><td>d</td></tr> <tr> <td></td><td>1</td><td>1</td><td></td></tr> <tr> <td></td><td>1</td><td>1</td><td>d</td></tr> <tr> <td>1</td><td></td><td></td><td>1</td></tr> </table> <p style="text-align: center;">B</p> <p>Find out the reduced SOP expression that can be obtained from the above K-map</p>	d			d		1	1			1	1	d	1			1	[3]	CO3	3
d			d																	
	1	1																		
	1	1	d																	
1			1																	
<b>Question 4</b>																				
4(a)	Design a 2-input AND Gate using 2-input NOR Gate. Give the expression to demonstrate the Absorption law of Boolean algebra.	[3]	CO2	6																
4(b)	What do you understand by the term logic families? What is the importance of Fan out?	[4]	CO1	2																
4 (c)	Given a function $F(x,y,z) = \sum (1,3,5,7)$ (i) Obtain the min term representation of the above function F (ii) Obtain the max term representation of the above function F	[3]	CO3	3																

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**CLASS TEST****B. TECH PROGRAMMES**

Third Semester, January 2023

**Paper Code: AIDS205/AIML205****Subject: Digital Logic Design****Time: 1 ½ Hrs.****Max. Marks: 30****Note: Attempt Q.No.1 which is compulsory and any two questions from remaining.**

<b>Q. No.</b>	<b>Question</b>	<b>Max. Marks</b>	<b>CO</b>										
1(a)	Any combinational circuit can be designed using only (i) AND gates (ii) OR gates (iii) NOR gates (iv) XOR gates. Choose the correct option.	[1]	CO5										
1(b)	Choose the correct option: (i) Shift registers (ii) Counters (iii) Multiplexers (iv) Flip-Flops are an example of combinational circuit.	[1]	CO4										
1(c)	Identify the gate from the truth table.	[1]	CO4										
	<table border="1"> <thead> <tr> <th><b>Input</b></th><th><b>Output</b></th></tr> </thead> <tbody> <tr> <td>A 0</td><td>Y 1</td></tr> <tr> <td>0</td><td>0</td></tr> <tr> <td>1</td><td>0</td></tr> <tr> <td>1</td><td>1</td></tr> </tbody> </table>	<b>Input</b>	<b>Output</b>	A 0	Y 1	0	0	1	0	1	1		
<b>Input</b>	<b>Output</b>												
A 0	Y 1												
0	0												
1	0												
1	1												
1(d)	In a 1-to-4 DEMUX, how many select lines are required?	[1]	CO5										
1(e)	Counter is based on (i) Combinational logic (ii) Sequential logic (iii) Both (iv) Random Logic. Choose the correct option.	[1]	CO4										
1(f)	When the binary numbers $A = 1100$ and $B = 1001$ are applied to the inputs of a comparator, the output levels are obtained as $A > B = 1$ , $A < B = 0$ , $A = B = 0$ . True or False?	[1]	CO4										
1(g)	A shift register in which the output of the last flip-flop connected to the input of the first flip-flop is (i) Ripple Counter (ii) BCD Counter (iii) Ring Counter (iv) Parallel Counter. Choose the correct option.	[1]	CO5										
1(h)	The number of bits needed to address 4K memory is	[1]	CO4										
1(i)	RAM/ROM is a volatile memory and RAM/ROM is a non-volatile memory. Choose the correct option accordingly.	[1]	CO4										
1(j)	Half-adder is also known as	[1]	CO4										
<b>Question 2</b>													
2(a)	Differentiate combinational vs sequential logic.	[3]	CO4										
2(b)	Realize half-adder with minimum number of input NAND gates.	[4]	CO5										
2(c)	Draw the logic circuit of SR flip flop using T flip flop.	[3]	CO5										
<b>Question 3</b>													
3(a)	Differentiate between synchronous and asynchronous sequential circuits.	[3]	CO4										
3(b)	What are the differences between latch and flip flop. Define race around condition.	[4]	CO4										
3(c)	Implement the following expression using 8x1 MUX: $F(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 12, 14)$	[3]	CO5										
<b>Question 4</b>													
4(a)	How a Ring counter will be converted into a Johnson's counter?	[3]	CO5										
4(b)	Explain the operation of magnitude comparator.	[4]	CO4										
4(c)	What is the difference between PAL and PLA?	[3]	CO4										

Total No. of Pages:

Student Name: KASAK .....

Enrollment No: ... 02715611922 .....

### Mid-Term Examination – November 2023

Programme: B.Tech (AI & DS), (AI&ML),IIoT

Semester: Third Semester (Sep23-Jan24)

Paper Code: AIDS205/AIML205/IOT205

Paper Name: Digital Logic Design

Time: 1½Hrs.

Maximum Marks: 30

Note:

- Question No. 1 is compulsory.
- Attempt any two questions from the remaining questions.
- Some questions have internal choice also.
- All questions carry equal marks.
- Only scientific calculator is allowed.

	Question 1	Marks	CO
1(a)	Convert the following decimal number into Octal number $(66.38)_{10}$	[ 1 ]	CO1
1(b)	Find the grey code for the following binary number 11001100	[ 1 ]	CO1
1(c)	Analyze the function performed by “AND” gate with schematic “bubbles” on its inputs	[ 1 ]	CO2
1(d)	Simplify by using Boolean Algebra $Y(A, B, C) = \sum m(0, 1, 2, 3, 4, 5, 6, 7)$	[ 1 ]	CO3
1(e)	Explain the characteristics of digital logic families (Any two) i. Figure of Merit ii. Fan out iii. Noise Immunity	[ 2 ]	CO1
1(f)	What are the essential prime implicants? How are they different from prime implicants?	[ 2 ]	CO3
1(g)	Implement XOR gate with minimum number of NAND gates	[ 2 ]	CO1
	Question 2		
2(a)	A transmitter uses a single error correcting code for the message using even parity. The message received at the receiving end is 1110101. Check & correct the error by using Hamming code.	[ 4 ]	CO1

2(b)	Simplify the function $F(A,B,C,D) = D(A+C)(A'+BD') + ACD$	[ 3 ]	CO2
2(c)	Express the Boolean function in sum of minterms $F(x,y,z) = (x+y)(x+z') + (y+z')$	[ 3 ]	CO3

### Question 3

3(a)	Find the essential prime implicants by QM method. $F(A,B,C,D) = \sum m(0,2,4,8,10,14) + d(1,3,5,15)$	[ 7 ]	CO3
3(b)	Obtain the minimal expression by using K map & implement by using NOR gate $F(A,B,C,D) = \pi M(1,3,5,9,13) . d(0,2,7,14)$	[ 3 ]	CO2

### Question 4

4(a)	Minimize the following Boolean function by using K maps $Y(A,B,C,D,E) = \sum m(0,1,5,6,9,13,14,17,21,22,25,29)$	[ 5 ]	CO3
4(b)	Find the Boolean function for the equation using K maps $Y(A,B,C,D) = (A+B+C')(A'+C+D')$	[ 3 ]	CO3
4 (c)	Obtain the Canonical form by using Boolean Algebra $F(x,y,z) = [(x+y') + (y+z')]' + yz$	[ 2 ]	CO2

(Please write your Enrolment No. immediately)

Enrolment No. 02715611922

## CLASS TEST

### B. TECH PROGRAMMES (UNDER THE AEGUS OF USICT)

Third Semester, January, 2024

Paper Code: AIDS 205/AIML 205

Subject: Digital Logic Design

Time: 1 Hrs.

Max. Marks: 30

Note: Attempt Q.No.1 which is compulsory and any two questions from remaining.

Q.1 (a)	Write main two differences among EPROM and EEPROM	[5]	CO5
(b)	What is Race Around Condition in JK Flip Flop. Name a technique to avoid this condition.	[5]	CO4
Q.2 (a)	Discuss the 2-bit magnitude comparator with suitable logical expression and digital circuit diagram.	[5]	CO4
Q.2 (b)	Illustrate the design procedure used to design Synchronous counters.	[5]	CO5
Q.3 (a)	Explain the working operation of 4-bit Twisted Ring Counter using D flip flops with the help of waveforms.	[10]	CO5
OR			
Q.3 (b)	Explain the working of a parallel-in serial-out register with logic diagram and waveforms.	[10]	CO5
Q.4 (a)	Implement the following Boolean Function by using 8:1 MUX $F(A, B, C, D) = \sum m(2, 5, 8, 9, 10, 14, 15)$	[10]	CO4
OR			
Q.4 (b)	Implement the following Boolean Function by using two 4:1 MUX $F(A, B, C, D) = \sum m(2, 5, 8, 9, 10, 14, 15)$	[10]	CO4