# Vidya Jyothi Institute of Technology (Autonomous)

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(Aziz Nagar, C.B.Post, Hyderabad -500075)

R18

**Subject Code:A23405**

B.Tech. II Year I Semester Regular Examination, November-2019

**Subject Name: Digital Logic Design** **BRANCH:CSE&IT**

**Time: 3 Hours** **Max. Marks:75**

**Note:** This question paper contains two ***Parts A and B.***

***Part A*** is compulsory which carries 25 Marks. Answer all the questions.

***Part B*** consists of 5 questions. Answer all the questions.

**Bloom's Level:**

| | | | | | |
|---|---|---|---|---|---|
| Remember | L1 | Apply | L3 | Evaluate | L5 |
| Understand | L2 | Analyze | L4 | Create | L6 |

| | **PART - A** | **Bloom's Level** | **25 Marks** |
|---|---|---|---|
| | **ANSWER ALL THE QUESTIONS** | | |
| 1 | Convert $(49056)_{10}$ to Binary Number System? | L3 | 3M |
| 2 | Find 1's and 2's complement of 010100. | L3 | 2M |
| 3 | Write Demorgan's principles. | L1 | 3M |
| 4 | What is a K-map? What are its advantages and disadvantages? | L2 | 2M |
| 5 | Draw Half Adder circuit? | L3 | 3M |
| 6 | Write any two differences between combinational and sequential circuits? | L2 | 2M |
| 7 | Define the differences among a Latch and FlipFlop? | L1 | 2M |
| 8 | Write the Excitation table for D flip-flop. | L3 | 3M |
| 9 | Explain about associative memory. | L2 | 3M |
| 10 | What are different types of ROMs? | L1 | 2M |
| | **PART - B** | **Bloom's Level** | **50 Marks** |
| | **ANSWER ALL THE QUESTIONS** | | |
| 11.i.a) | Convert the following octal numbers to hexadecimal A) 2035 B) 6054.263 | L3 | 5M |
| b) | Design a 7-bit Hamming code with 1100 for even parity. | L4 | 5M |
| | **[OR]** | | |
| ii.a) | Convert the following numbers with the given radix to decimal and then to binary A) $5654_8$ B) $1199_{16}$ | L4 | 5M |
| b) | Perform the following decimal additions in the 8421 code. A) 25+13 B) 679+536 | L3 | 5M |
| 12.i.a) | Convert the function into standard sop form F(A,B,C)= AB+BC+CA. | L3 | 7M |
| b) | Write any five Boolean algebra laws? | L1 | 3M |
| | **[OR]** | | |
| ii.a) | Reduce the function using k-map $F(A,B,C)=\sum m(0,2,4,6,8,13)+d(1,3,5)$. | L3 | 5M |
| b) | Draw the logic diagram of a 2 line to 4 line decoder. | L2 | 5M |
| 13.i.a) | Design BCD to Excess-3 code conveter. | L4 | 7M |
| b) | Draw the logic diagram of a 4 line to 2line encoder. | L4 | 3M |
| | **[OR]** | | |
| ii.a) | Design 8*1 multiplexer. | L4 | 5M |
| b) | Explain Full- subtractor along with truth table and logic diagram. | L2 | 5M |
| 14.i.a) | Write the main steps in the synthesis of synchronous sequential circuits. | L2 | 5M |
| b) | Design 3-bit Asynchronous counter. | L4 | 5M |
| | **[OR]** | | |
| ii.a) | Design a 4bit Ripple counter. | L4 | 5M |
| b) | Explain different types of shift register. | L2 | 5M |
| 15.i.a) | What is Auxillary Memory? What is its principal advantage? | L1 | 5M |
| b) | Draw the block diagram of cache memory. Explain briefly. | L2 | 5M |
| | **[OR]** | | |
| ii.a) | Explain different types of Memories. | L2 | 5M |
| b) | Write a short note on hit and miss ratio. | L1 | 5M |

***VJIT(A)***