Team Members:

1. Name- ***Akshat Toolaj Sinha***, Entry Number- ***2020CSB1068***
2. Name- ***Pranavkumar Mallela***, Entry Number- ***2020CSB1112***

Project Ideas

1. **Space-Ship Game( With an actual Hardware component ( if allowed ) )**
    - *Overall Objective :* To fabricate a 1D arcade spaceship game, in which:
        - The user has to defeat as many enemies as possible before depleting its health, while dodging enemy fire and obstacles.
    - *Implementation type :* FPGA (Verilog)
    - *Functionality :*
        - Motion of user: In 1D (to move left and right)
        - Motion of enemy: In 1D (towards the user)
        - Firing: (by user and enemy): Lasers of the user and the enemy will move at same speed (pixel/s). Colliding lasers do not have any effect on each other.
        - Measure of health: enemy is defeated after one hit; user has finite health
        - Obstacles: (user gets double the damage as done by enemy fire;enemy is defeated after one hit)
        - First aid: Similar to obstacles, but increases the user's health. It does not affect enemies.
        - Score: User's score = number of enemies defeated
        - High score saver: stores the highest score achieved by the user till then
        - High score notification: Buzzer rings when a new high score is achieved.
        - The game does not support audio.
        - Display: On an LCD screen.

2. **Taylor Series Generator**
    - *Overall Objective :* To generate the Taylor series of some select functions (trigonometric functions, exponential functions) around a given point x0 until 8-10 terms.
    - *Implementation type :* RTL/ Verilog
    - *Functionality :*
        - Factorial finder: Will be used to compute the factorial of a given positive integer.
        - Differentiation finder: Will find the nth derivative of a given function, at a given point x0. (1<=n<=10)
        - Finding the value of (x-x0)^k
3. **Random Number Generator**
    - *Overall Objective:* To create a Random number generator that can be used in cryptography.
    - Implementation type: RTL/ Verilog
    - Functionality:
        - We will be explaining some Random number generators Algorithms like

        - Blum Blum Shub
        - XorShift
        - Multiply with carry
        - Linear Feedback shift register
    - We will be implementing only one of them depending upon their difficulty level and our current knowledge of the course
    - We will be mainly taking references from http://ethesis.nitrkl.ac.in/1960/1/final_prj.pdf and additional references from other internet resources.
    - We will see if it is to be done on FPGA or not

4. **Image processing: (Image resizing)**
    - *Overall Objective :* To resize an image from a given size to the required size.
    - *Implementation type :* RTL / Verilog + FPGA
    - *Functionality :*
        - *Inputs:* Take an image as a hexadecimal file and read its pixel values in RGB( 0-255), and the required output size of the image
        - Image Resizer: resize the input image to output size
        - Output: Output is the final resized image.
        - Algorithm and procedure to perform resizing will be decided after more research.